

## Wafer-scale uniformity of Dolan-bridge and bridgeless Manhattan-style Josephson junctions for superconducting quantum processors

Muthusubramanian, N.; Finkel, M.; Duivesteyn, W.J.; Zachariadis, C.; van der Meer, S.L.M.; Veen, H.M.; Beekman, M.W.; Stavenga, T.; Bruno, A.; DiCarlo, L.

**DOI**

[10.1088/2058-9565/ad199c](https://doi.org/10.1088/2058-9565/ad199c)

**Publication date**

2024

**Document Version**

Final published version

**Published in**

Quantum Science and Technology

**Citation (APA)**

Muthusubramanian, N., Finkel, M., Duivesteyn, W. J., Zachariadis, C., van der Meer, S. L. M., Veen, H. M., Beekman, M. W., Stavenga, T., Bruno, A., & DiCarlo, L. (2024). Wafer-scale uniformity of Dolan-bridge and bridgeless Manhattan-style Josephson junctions for superconducting quantum processors. *Quantum Science and Technology*, 9(2), Article 025006. <https://doi.org/10.1088/2058-9565/ad199c>

**Important note**

To cite this publication, please use the final published version (if applicable).  
Please check the document version above.

**Copyright**

Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

**Takedown policy**

Please contact us and provide details if you believe this document breaches copyrights.  
We will remove access to the work immediately and investigate your claim.

PAPER • OPEN ACCESS


## Wafer-scale uniformity of Dolan-bridge and bridgeless Manhattan-style Josephson junctions for superconducting quantum processors

To cite this article: Nandini Muthusubramanian *et al* 2024 *Quantum Sci. Technol.* **9** 025006

View the [article online](#) for updates and enhancements.

You may also like

- [Security of quantum key distribution with imperfect phase randomisation](#)  
Guillermo Currás-Lorenzo, Shlok Nahar, Norbert Lütkenhaus et al.
- [Computing electronic correlation energies using linear depth quantum circuits](#)  
Chong Hian Chee, Adrian M Mak, Daniel Leykam et al.
- [Experimentally ruling out joint reality based on operational completeness](#)  
Qiuxin Zhang, Yu Xiang, Xiaoting Gao et al.

 **kiutra**

Easy-to-use and Helium-3 free  
cryogenics solutions

LEARN MORE

# Quantum Science and Technology



## PAPER

### OPEN ACCESS

RECEIVED  
7 May 2023

REVISED  
2 October 2023

ACCEPTED FOR PUBLICATION  
28 December 2023

PUBLISHED  
2 February 2024

Original Content from this work may be used under the terms of the [Creative Commons Attribution 4.0 licence](#).

Any further distribution of this work must maintain attribution to the author(s) and the title of the work, journal citation and DOI.



## Wafer-scale uniformity of Dolan-bridge and bridgeless Manhattan-style Josephson junctions for superconducting quantum processors

Nandini Muthusubramanian<sup>1,2,4</sup> , Matvey Finkel<sup>1,2</sup>, Pim Duivestijn<sup>1,2,4</sup>, Christos Zachariadis<sup>1,2,5</sup>, Sean L M van der Meer<sup>1,2</sup>, Hendrik M Veen<sup>1,2</sup>, Marc W Beekman<sup>1,3</sup>, Thijs Stavenga<sup>1,2,5</sup>, Alessandro Bruno<sup>1,2,5</sup> and Leonardo DiCarlo<sup>1,2,\*</sup>

<sup>1</sup> QuTech, Delft University of Technology, PO Box 5046, 2600 GA Delft, The Netherlands

<sup>2</sup> Kavli Institute of Nanoscience, Delft University of Technology, PO Box 5046, 2600 GA Delft, The Netherlands

<sup>3</sup> Netherlands Organisation for Applied Scientific Research (TNO), PO Box 155, 2600 AD Delft, The Netherlands

<sup>4</sup> Present address: QphoX B.V., Elektronicaweg 10, 2628 XG Delft, The Netherlands.

<sup>5</sup> Present address: Quantware B.V., Elektronicaweg 10, 2628 XG Delft, The Netherlands.

\* Author to whom any correspondence should be addressed.

E-mail: [L.DiCarlo@tudelft.nl](mailto:L.DiCarlo@tudelft.nl)

**Keywords:** transmon, scalability, through-silicon vias, frequency targeting, Dolan-bridge junction, Manhattan-style junction

Supplementary material for this article is available [online](#)

### Abstract

We investigate die-level and wafer-scale uniformity of Dolan-bridge and bridgeless Manhattan-style Josephson junctions, using multiple substrates with and without through-silicon vias (TSVs). Dolan junctions fabricated on planar substrates have the highest yield and lowest room-temperature conductance spread, equivalent to  $\sim 100$  MHz in transmon frequency. In TSV-integrated substrates, Dolan junctions suffer most in both yield and disorder, making Manhattan junctions preferable. Manhattan junctions show pronounced conductance decrease from wafer center to edge, which we qualitatively capture using a geometric model of spatially-dependent resist shadowing during junction electrode evaporation. Analysis of actual junction overlap areas using scanning electron micrographs supports the model, and further points to a remnant spatial dependence possibly due to contact resistance.

## 1. Introduction

Monolithic superconducting quantum processors (SQPs) have scaled to enable key demonstrations of quantum-computational advantage [1] and milestone demonstrations of quantum error correction [2–4] on the road to fault-tolerant quantum computing. Sustaining this scaling requires a multi-faceted fabrication approach simultaneously meeting yield, frequency, coherence, and coupling requirements of circuit elements, as well as the routing of control lines needed for gate and measurement operations. The latter motivates the active development of 3D integration strategies such as flip-chip [5–7] to avoid overcrowding of circuit elements and vertical routing [8–10] of input and output lines to circumvent the scaling limitations associated with lateral wirebonding. Through-silicon vias (TSVs) are needed in some vertical routing approaches [11–14], and especially for suppression of resonance modes arising from the increased size of SQPs and their packaging.

TSVs further aggravate the targeting of superconducting qubit frequencies, which already bottlenecks the yield of operable devices even on planar substrates [15]. Poor qubit frequency targeting is a primary cause of crosstalk induced by microwave drives [2] and can limit gate speeds. It also increases residual ZZ coupling in processors with always-on qubit-qubit coupling [2, 3, 16], making gate fidelity and leakage dependent on the state of spectator qubits [17]. Laser annealing of qubit Josephson junctions (JJs) [15, 18–21] is an established method for selective qubit frequency trimming without intrinsic effect on qubit coherence. Currently, laser annealing allows a monotonic decrease with  $\sim 300$  MHz range and  $\sim 15$  MHz imprecision (defined as the

standard deviation of frequency targeting error post-annealing) [21]. To safely rely on laser annealing for post-fabrication trimming, fabrication itself must achieve an imprecision several times lower than the tuning range, e.g.  $\sim 50$  MHz.

The main limit to qubit frequency targeting is variability in the fabrication of Al-AlO<sub>x</sub>-Al JJs, which most commonly relies on double-angle shadow evaporation with intermediate *in-situ* oxidation. Two main variables affecting the Josephson coupling energy ( $E_J$ ) are the overlap area between the two Al electrodes and the tunnel barrier thickness. The two most popular JJ fabrication variants differ only in the shadowing mechanism: Dolan-bridge [22] junctions use a suspended resist bridge whereas Manhattan-style [23] junctions do not. Since Dolan JJs are more sensitive to resist-height variation by design, Manhattan JJs may be preferable particularly on substrates with TSVs that compromise the uniformity of spin-coated resist. Previous works have shown a reduction in wafer-scale variation of Manhattan JJs [24, 25]. On the other hand, recent reports [26–28] indicate that geometric effects cause pronounced center-to-edge variation in Manhattan JJs, affecting their uniformity at wafer scale.

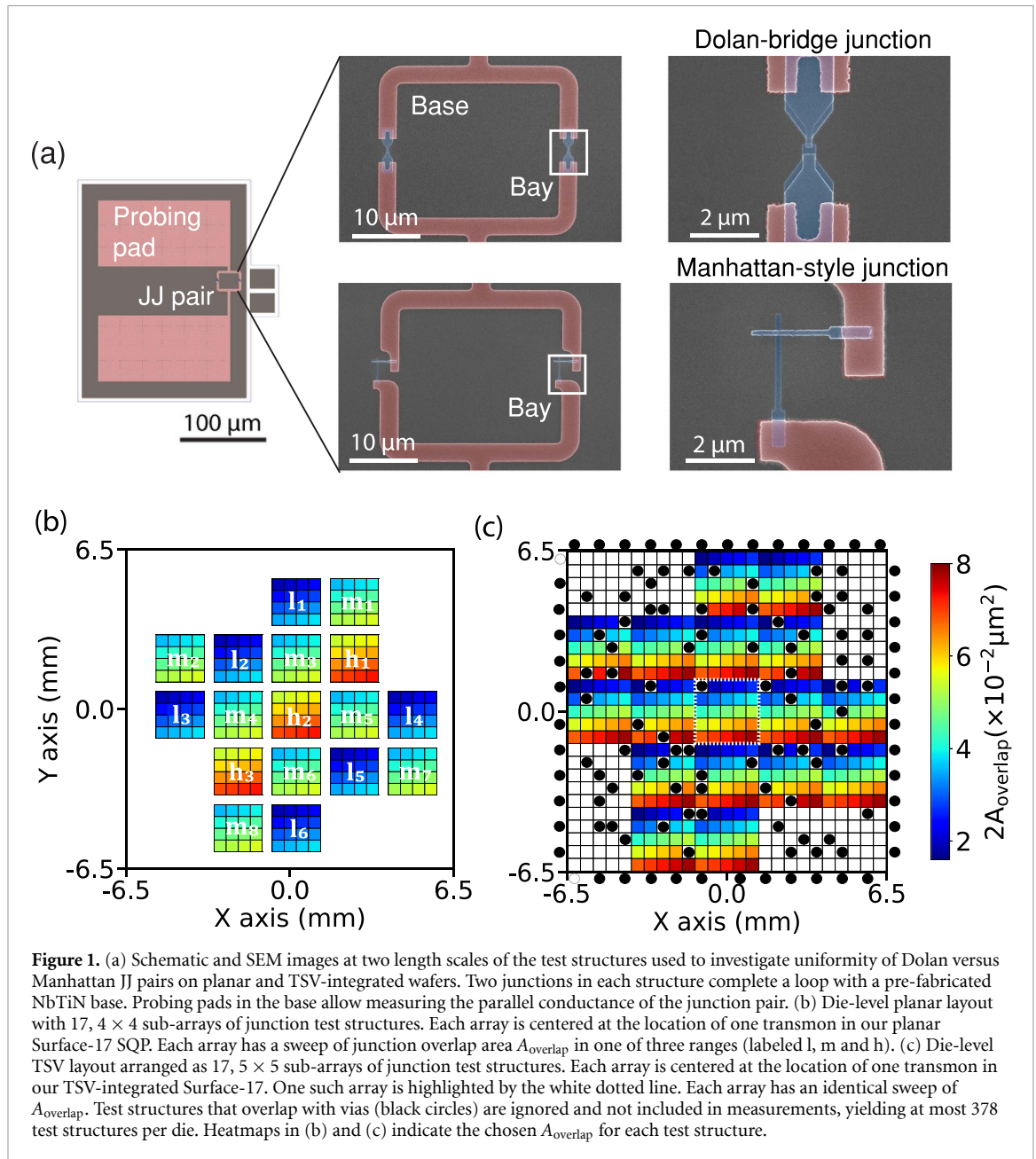
In this work, we present an experimental investigation comparing the uniformity of Dolan versus Manhattan JJs at both die- and wafer-scale on planar substrates with and without TSVs. We benchmark uniformity using room-temperature (RT) conductance ( $G$ ) measurements, extracting the conductance coefficient of variation (CV) and residual standard deviation (RSD) of predicted transmon frequency. A wafer-center-to-edge variation is again observed particularly in Manhattan junctions, which we attribute to a geometric shadowing effect during electrode evaporation. Scanning electron microscopy (SEM) of many junctions supports the model, and further points to remnant spatial dependence possibly due to contact resistance. Our findings indicate that for our current fabrication processes, Dolan JJs perform best for planar substrates, while the opposite holds for TSV-integrated substrates. We identify several paths for further required improvement.

## 2. Design of experiments

We investigate uniformity of Dolan and Manhattan JJs using six 100 mm diameter Si wafers. (Sections S1 and S2 of the Supplementary Information provide detailed descriptions of the fabrication processes used.) Three of these wafers, labeled Planar 17Q (quantity one) and TSV 17Q (quantity two), are used to obtain and compare metrics for both junction variants in fully planar substrates and TSV-integrated ones. Each wafer contains thousands of test structures, each consisting of two nominally identical JJs connecting in parallel to pre-fabricated NbTiN probing pads (200 nm thick, defined by sputtering and etching). These test structures mimic the two-junction transmon with NbTiN capacitor plates used in our standard SQPs (figure 1(a)).

In the Planar 17Q wafer, a  $13 \times 13$  mm die-level layout mimicking our planar 17-qubit SQP (Surface-17 [11, 21, 29]) is copy-pasted into two  $2 \times 4$  arrays. The top half of the wafer has test-structure arrays for Dolan-bridge JJs, while the bottom half has test-structure arrays for Manhattan-style JJs. At the location of each transmon of the SQP, we place a sub-array of  $4 \times 4$  test structures. Within each sub-array (figure 1(b)), the designed single-junction overlap area ( $A_{\text{overlap}}$ ) is finely stepped within one of three ranges, labeled low (l), mid (m) and high (h), mimicking the choice of three qubit-frequency groups in our SQPs [11, 16, 21, 29]. For Dolan-bridge JJs, we change  $A_{\text{overlap}}$  by varying the width  $W_t$  of the top electrode and keeping the width of the bottom electrode  $W_b = 3W_t$ . For Manhattan-style JJs, we instead vary  $W_b$  and fix  $W_t = 160$  nm. In total, the wafer contains 2176 test structures of each JJ variant. We first fabricate only the Manhattan JJs on the bottom half of the wafer and perform all conductance measurements on them. We subsequently fabricate and measure all Dolan JJs on the top half of the wafer. Each TSV 17Q wafer contains test structures of only one JJ variant. In each wafer, the die-level layout (copy-pasted into one  $2 \times 4$  array) has TSVs placed at the same locations as a variant of Surface-17 with TSVs (figure 1(b)). The density ( $\sim 1.7\%$  area coverage) and position of TSVs is chosen to push the lowest-frequency spurious modes of the SQP in its sample holder to  $\gtrsim 15$  GHz (as per finite-element simulation). At the location of each transmon in the SQP, we place a  $5 \times 5$  sub-array of test structures. In this case, all sub-arrays are identical. Importantly, test structures overlapping with TSVs, although fabricated, are ignored and not included in conductance measurements. This yields at most 378 viable test structures per die and thus 3024 per wafer.

Three additional wafers, labeled Planar  $35 \times 35$ , are used to test the geometric resist-shadowing model and to investigate further sources of spatial non-uniformity in Manhattan JJs. Each wafer (figure 5) has a  $35 \times 35$  array of nominally identical test structures ( $W_b = W_t = 200$  nm). In the first wafer, like in the 17Q wafers, the test structures have symmetric JJ pairs with NbTiN probing pads. In the second, they have symmetric JJ pairs with TiN probing pads (160 nm thick, pre-defined by atomic layer deposition (ALD) and etching). In the third, they have single JJs with Al probing pads evaporated simultaneously with the JJ electrodes.



### 3. Measurements and analysis

All  $G$  measurements are acquired by the 2-point method using a home-built transimpedance amplifier with gain  $10^5 \Omega$ . A low input voltage (10 mV) is applied across the junctions to minimize the possibility of causing failure to open or short circuit. With one exception noted below, measurements on all planar wafers are performed using a manual probe station located inside our cleanroom, which is temperature controlled to  $20 \pm 1^\circ\text{C}$ . During manual measurements, the intensity from a light-emitting diode source is set to the lowest possible visibility ( $< 500\text{lx}$ ), limiting the contribution from substrate conductance to  $< 1 \mu\text{S}$ , as determined from  $G$  measurements on test structures both without JJs and with JJs known to have failed to open circuit. Measurements on the TSV 17Q wafers as well as on the Planar  $35 \times 35$  TiN wafer are performed using a home-built automated probe station, also located inside the cleanroom, whose measurements are performed fully in the dark. To quantify series resistance from the probe contact and external cabling, we compared 2- and 4-point  $G$  measurements taken with the automated probe station, finding a best-fit value of  $\sim 18 \Omega$ . The series resistance of NbTiN probing pads is found to vary from  $200 \Omega$  at wafer center to  $330 \Omega$  at wafer edge by fabricating test structures with bays short-circuited directly in the base layer. This variation is attributed to the radial dependence of the thickness of the sputtered NbTiN films (resistivity

$\rho = 100 \mu\Omega\text{-cm}$ ). Reported  $G$  values are raw, i.e. as obtained from 2-point measurement without correction for series resistance, substrate conductance, nor a  $4 \mu\text{S}$  offset from the transimpedance amplifier.

The range of  $G$  is  $40 - 350 \mu\text{S}$ . Values  $< 20 \mu\text{S}$  and  $> 500 \mu\text{S}$  are filtered out as they mostly correspond to open and shorted junctions, respectively. To systematically detect and filter out data containing an open junction in a pair, a two-part linear regression analysis of conductance versus  $A_{\text{overlap}}$  is implemented within each die in the Planar and TSV 17Q wafers. Values below 70% of the initial best fit are filtered out (figures S3 and S4). For the Planar  $35 \times 35$  wafers containing nominally identical test structures throughout, conductance values below 70% of the mean are filtered out.

To quantify non-uniformity at both die and wafer scale, we use the conductance CV as a function of  $A_{\text{overlap}}$  and the RSD of predicted qubit frequency. Die-(wafer-) level conductance CV is calculated using all the test structures with identical  $A_{\text{overlap}}$  across the die (wafer) when calculating the mean  $\mu_G$  and standard deviation  $\sigma_G$ . The spatial variation of junction conductance is visualized using heatmaps of conductance normalized by  $\mu_G$  of all test structures with identical  $A_{\text{overlap}}$ . The predicted transmon qubit transition frequency ( $f_{01}$ ) is calculated from  $G$  using

$$f_{01} = \sqrt{8f_c f_j} - f_c,$$

where  $f_c = E_c/h = 270 \text{ MHz}$  with  $E_c$  the designed transmon charging energy,  $f_j = E_j/h$ , and  $f_j = MG$  [30–32]. Here,  $M = 134 \text{ GHz/mS}$  is an experimentally determined constant obtained by comparing  $G$  measured immediately prior to cooldown to the  $E_j$  extracted for transmons across many of our SQPs. ( $E_j$  is extracted from spectroscopy data obtained during cryogenic characterization.) Die-level frequency RSD is calculated from the residuals of the second fit. Wafer-level RSD is calculated similarly, but the residuals are obtained by performing a single fit on the combined filtered  $G$  data from all dies.

To test the geometric resist-shadowing model, SEM images of JJs from different coordinates on all Planar  $35 \times 35$  wafers are acquired at  $10^5 \times$  magnification. A total of 34 (35) JJ pairs are imaged for the NbTiN (TiN) wafer, and 36 single JJs for the Al wafer. Imaging is performed only after conductance measurements are completed. The actual deposited junction widths ( $W'_b, W'_t$ ) and overlap area ( $A'_{\text{overlap}}$ ) are extracted using home-made image analysis software (based on the OpenCV package) with the work flow presented in figure S8. The presence of other sources of spatial non-uniformity is evidenced from the spatial dependence of effective JJ conductivity calculated as  $G/\Sigma A'_{\text{overlap}}$ .

## 4. Results

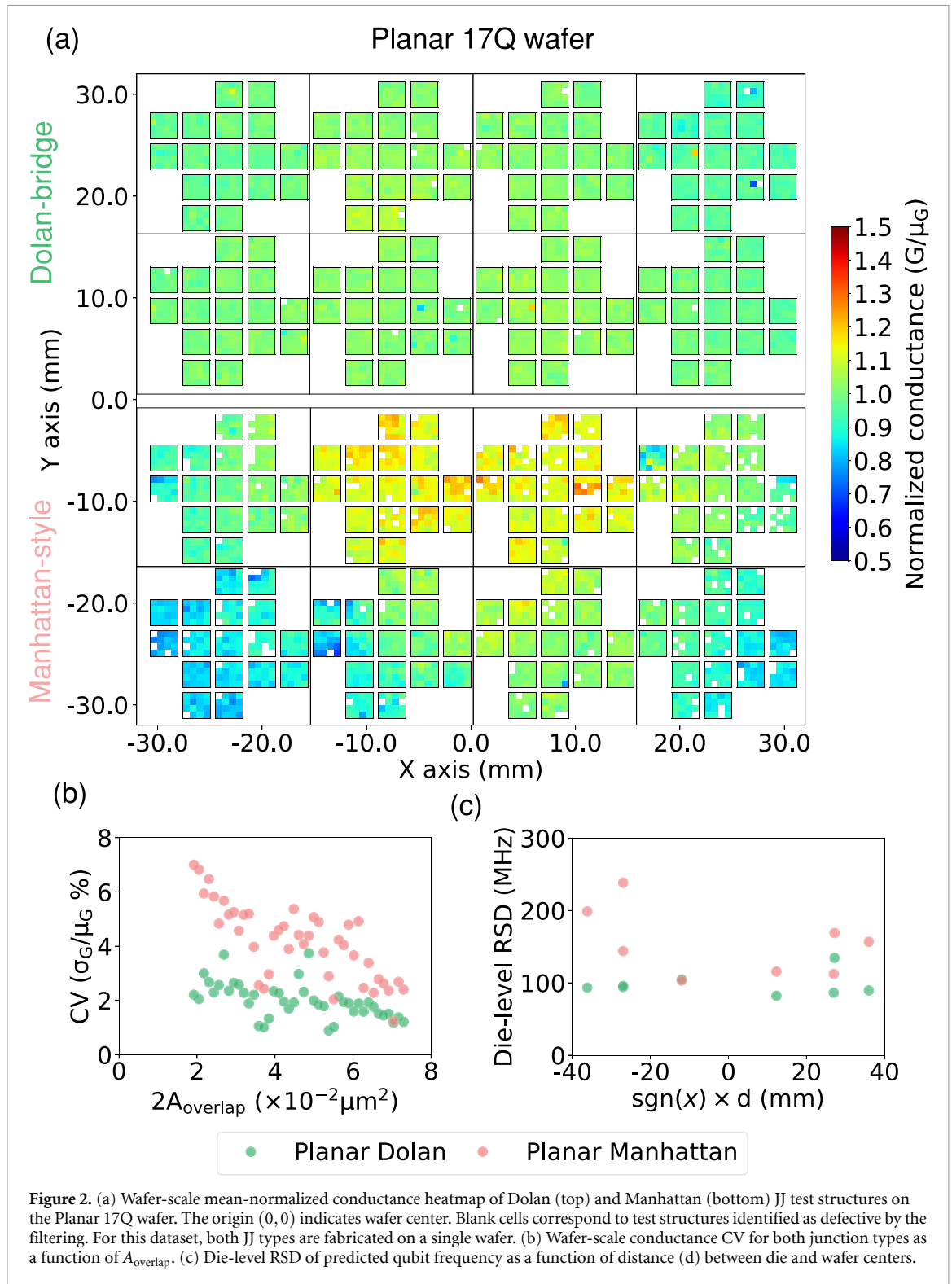
A total of 2176 (3024) test structures are fabricated per JJ variant for the Planar and TSV 17Q datasets. A zoomed-out view (figure 2) of the planar dataset shows that the spatial variation of normalized conductance for Dolan JJs is significantly lower than for Manhattan JJs. For the latter, there is a clear systematic decrease from center to edge, making it unsurprising that the wafer-scale conductance CV is higher for Manhattan over all  $A_{\text{overlap}}$ . The general decrease observed in the conductance CV with increasing  $A_{\text{overlap}}$  is in line with previous works [33, 34]. At die level, the spread of Dolan JJs is also lowest, with  $\sim 100 \text{ MHz}$  frequency RSD uniform across the wafer. For Manhattan JJs, the frequency RSD increases away from wafer center, indicating that the spatial variation is relevant even at die level.

Turning over to the TSV dataset (figure 3), we can again discern an underlying center-to-edge dependence for Manhattan JJs. However, this trend is masked by a significant increase in disorder. The disorder is much stronger for Dolan JJs, evident both at wafer scale and die level. Interestingly, the CV for Dolan does not display any clear dependence on  $A_{\text{overlap}}$ , suggesting that resist-height variations dominate the spread. Measurements of resist-height variations caused by TSVs and evidence of the impact of such variations on junction electrode and overlap geometries are shown in figure S2.

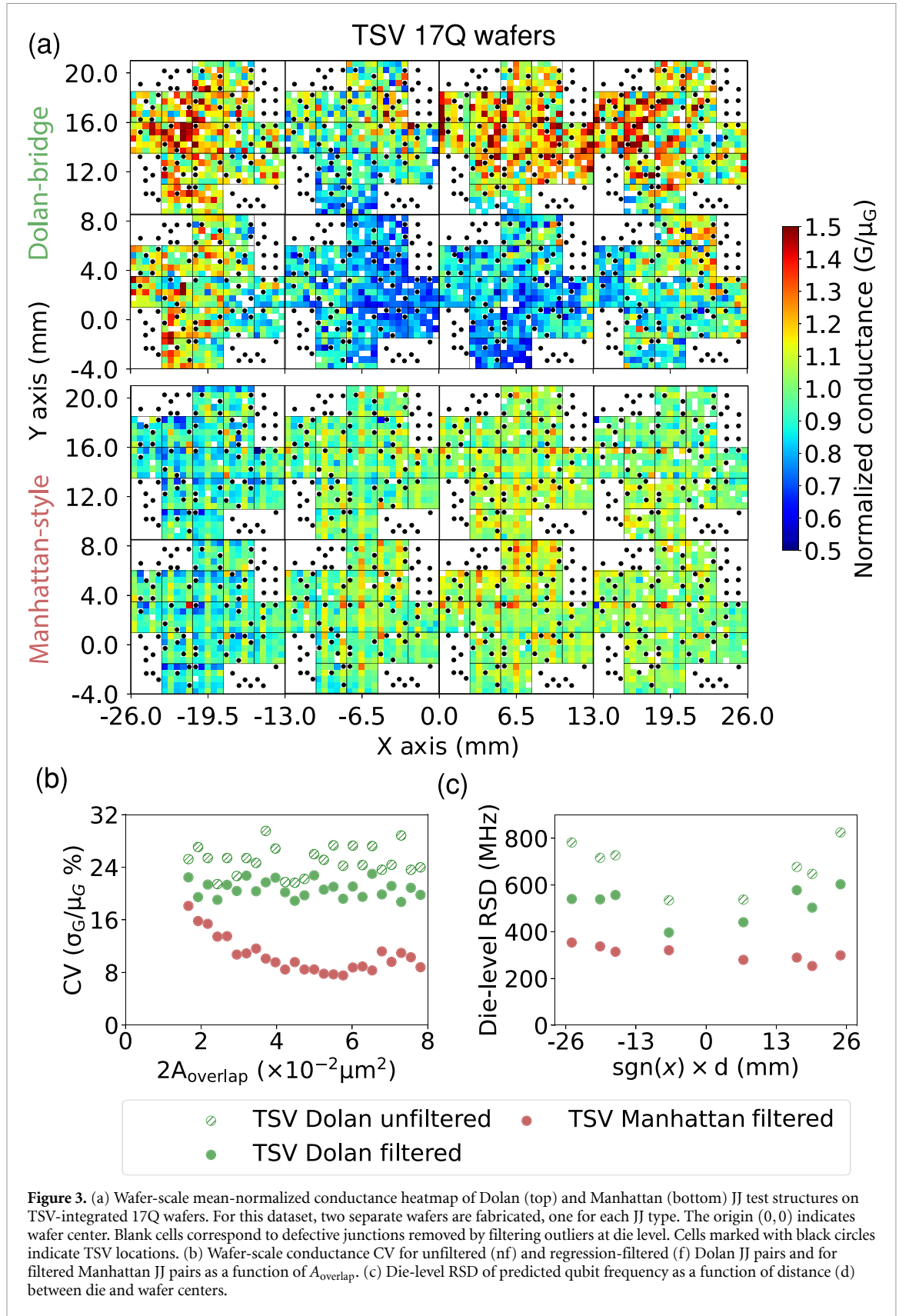
Note that the CV and RSD for Dolan are calculated both with and without applying regression filters. This is necessary because the high disorder makes the regression filter unable to reject only defective junctions. Even with the artificial improvement of Dolan CV and RSD that may arise from removing non-defective junctions, a strong conclusion holds: with TSVs, Manhattan JJs systematically outperform Dolan JJs. Nonetheless, with  $> 300 \text{ MHz}$  RSD at die level, even Manhattan JJs fall very short of frequency targeting objectives in the presence of TSVs. However, there is room for optimism as this investigation is best interpreted as a worst-case scenario for actual TSV-integrated SQPs. In our test, we place many junction pairs per transmon location of Surface-17. Therefore, in a real Surface-17, transmon JJ pairs would on average be  $500 \mu\text{m}$  away from TSVs. Furthermore, the footprint of TSVs could be further optimized following [12].

### 4.1. Geometric resist-shadowing model

The essence of the geometric model is a spatial dependence of junction electrode widths arising from oblique incidence of the Al flux during evaporation. Specifically, the width of vertical electrodes (both electrodes for



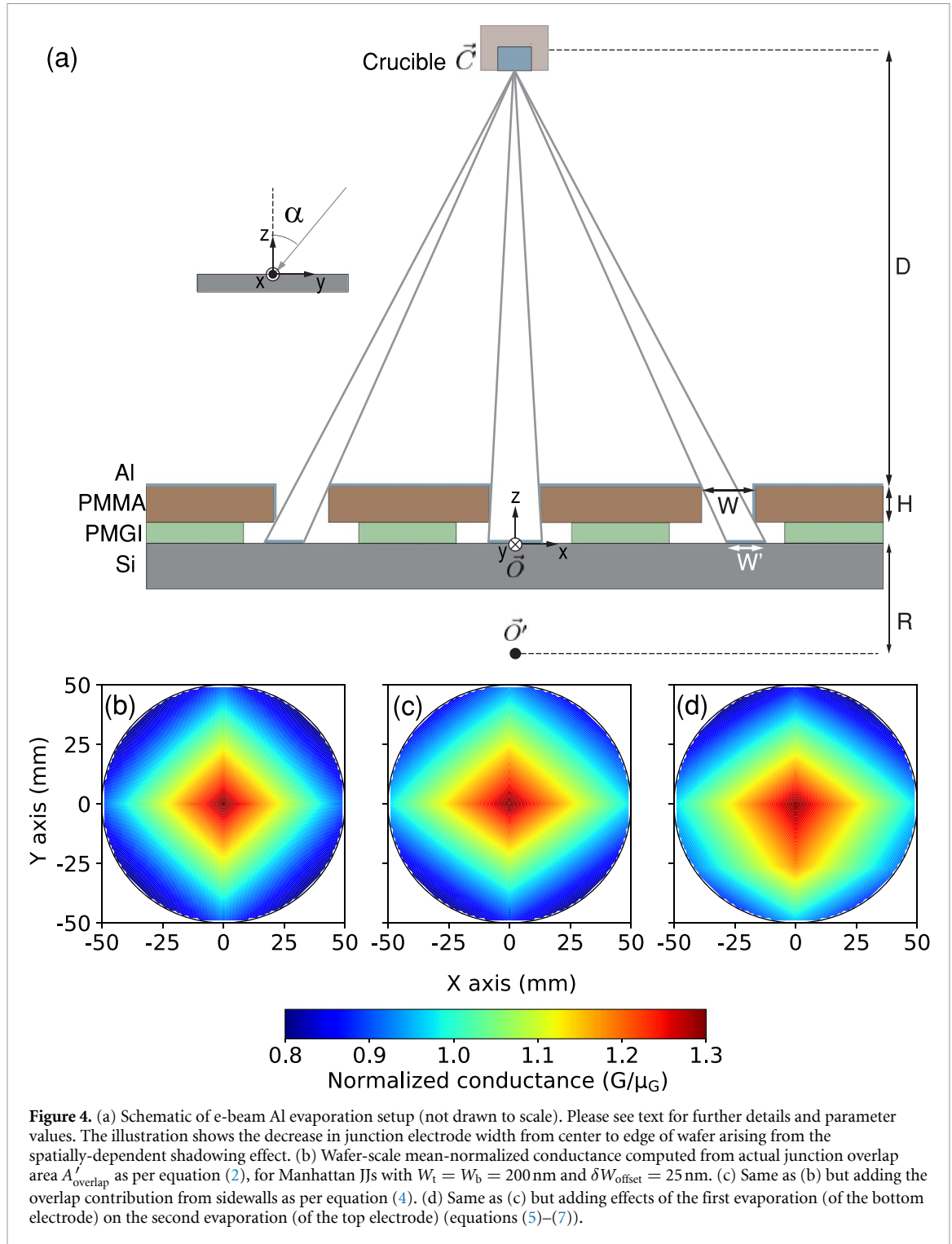
Dolan JJs, bottom electrode for Manhattan JJs) depends on the  $x$  coordinate, while that of horizontal electrodes (top electrode for Manhattan) depends on the  $y$  coordinate. Key parameters of the model are the thickness of the top resist  $H = 600$  nm (which acts as the shadow mask), the wafer tilt  $\alpha = 35^\circ$  during Al evaporations, and the physical configuration of the electron-beam (e-beam) evaporator (Plassys MEB550S). These last parameters include the distance  $D' = 650$  mm between the crucible at  $\vec{C}$  and the pivot point  $\vec{O}'$  of the sample holder, and the distance  $R = 62.5$  mm between  $\vec{O}'$  and center  $\vec{O}$  of the exposed wafer surface (see schematic in figure 4(a)). This results in a distance  $D = D' \cos(\alpha) - R$  between  $\vec{C}$  and the plane defined by



this surface [35]. In a cartesian coordinate system with origin at  $\vec{O}$  and  $\vec{r} = (x, y, 0)$  lying on this plane,  $\vec{C} = (0, D' \sin(\alpha), D)$ . Evaporation under these conditions deposits electrodes extending along the  $y$  axis. An electrode of this orientation with  $x$  coordinate has actual width

$$W'(x) \approx W + \delta W_{\text{offset}} - |x| \frac{H}{D}, \quad (1)$$





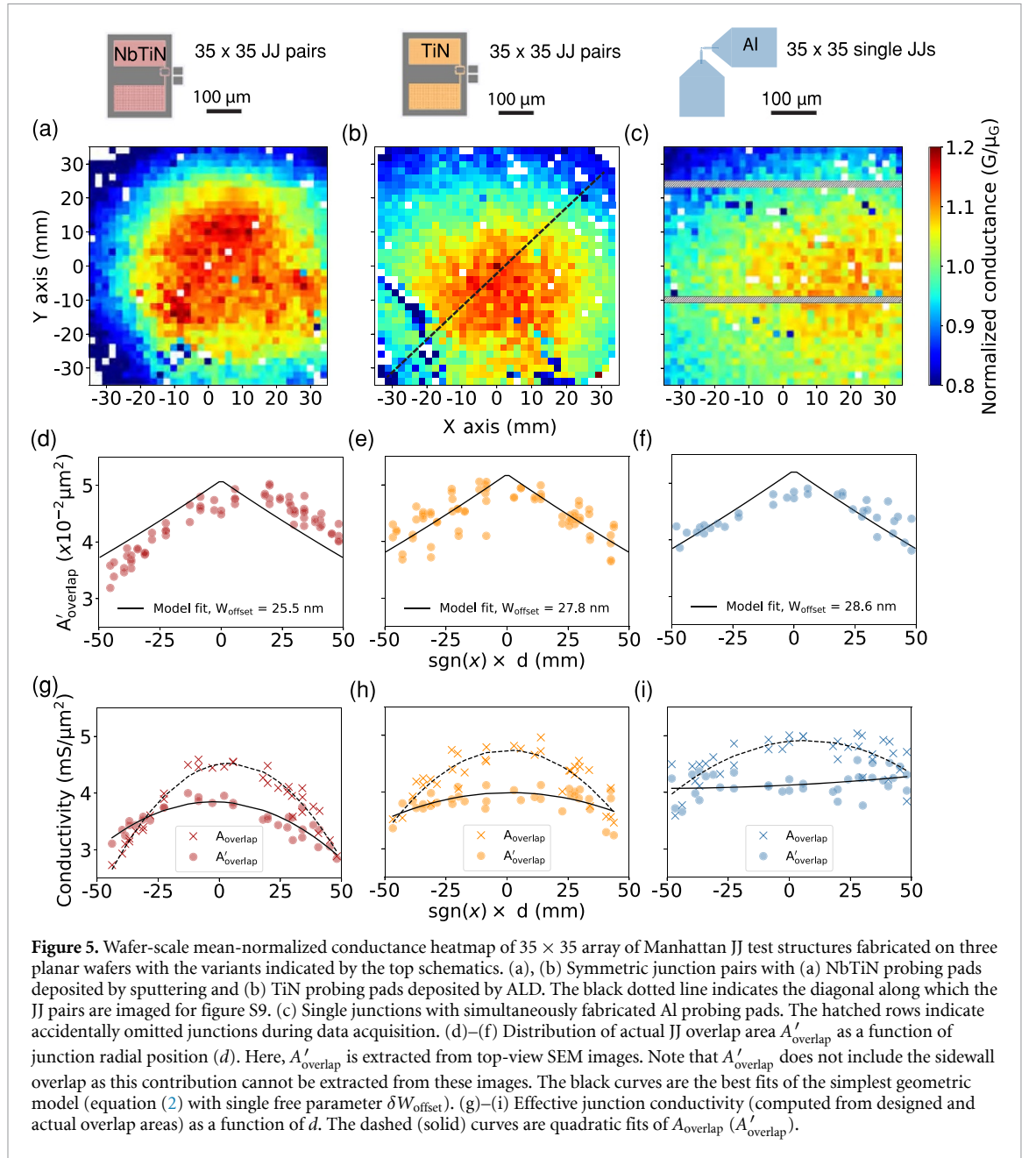
where  $\delta W_{\text{offset}}$  is a constant widening from over-exposure and development of the e-beam resist. Including these modifications to the width of both electrodes, the actual overlap becomes

$$A'_{\text{overlap}}(\vec{r}) = W'_b(x) W'_t(y). \quad (2)$$

Figure 4(b) shows the spatial dependence of  $A'_{\text{overlap}}$  for Manhattan JJs with  $W_b = W_t = 200$  nm and  $\delta W_{\text{offset}} = 25$  nm on a 100-mm diameter wafer.

We can further expand the model by approximating the contribution of sidewalls to  $A'_{\text{overlap}}$ . The spatially-dependent actual bottom electrode thickness is

$$T'_b(\vec{r}) = T_b \frac{(D' - R)^2 D}{|\vec{r} - \vec{C}|^3}, \quad (3)$$



where  $T_b = 35 \text{ nm}$  is the calibrated thickness at  $\vec{O}$  under normal incidence ( $\alpha = 0$ ). Approximating the sidewalls as vertical,

$$A'_{\text{overlap}}(\vec{r}) = (W'_b(x) + 2T'_b(\vec{r})) W'_t(y), \quad (4)$$

The modified spatial dependence is shown in figure 4(c). Note that we do not model the effect of shadowing by the bottom electrode during evaporation of the top electrode, which most likely reduces the overlap at the eastern sidewall (evident in figure S9).

Finally, we can model some predictable effects of the first evaporation (for the bottom electrode) on the top electrode. The first evaporation deposits an Al layer above the top resist, effectively increasing its height by  $\delta H(\vec{r})$  (also given by the right-hand side of equation (3)). More importantly, it also deposits a lip on the southern resist edge for the top electrode (see figure S1), with width  $W_{\text{lip}}$  and height  $H_{\text{lip}}$ :

$$W_{\text{lip}}(\vec{r}) = -T_b \frac{(D' - R)^2 (D' \sin(\alpha) - y)}{|\vec{r} - \vec{C}|^3}, \quad (5)$$

$$H_{\text{lip}}(\vec{r}) = \frac{DW_t}{D' \sin(\alpha) - y}. \quad (6)$$

**Table 1.** Summary of metrics obtained for Dolan and Manhattan JJ test structures on all wafers used throughout this study. The 17Q yield reported is that calculated for a Surface-17 SQP using the per-junction-pair yield of the Planar and TSV 17Q wafers. We note that the yield of actual planar Surface-17 SQPs with Manhattan-style JJs is roughly 50%, higher than that calculated from the Planar 17Q wafer. The die-level frequency RSD is the average across the eight dies in the 17Q wafers. For the  $35 \times 35$  Planar wafers, the die-level frequency RSD is calculated from the average of sixteen  $6 \times 6$  arrays of test structures within the inner  $50 \times 50 \text{ mm}^2$  area of the wafers.

Summary of results					
Junction type	Substrate	Yield (%)	Conductance CV wafer scale (%)	Frequency RSD wafer scale (MHz)	Frequency RSD die level (MHz)
Dolan-bridge	Planar 17Q NbTiN	2160/2176 = 99.2 17Q yield = 87.2	0.8–3.7	140	98
	TSV 17Q NbTiN	2958/3024 = 97.8 17Q yield = 68.5 <sup>a</sup> 2770/3024 = 91.6 17Q yield = 22.5 <sup>b</sup>	21.6–29.5 18.5–22.5	800 666	681 <sup>a</sup> 520 <sup>b</sup>
Manhattan-style	Planar 17Q NbTiN	2006/2176 = 92.2 17Q yield = 25.1	1.2–7	317	155
	TSV 17Q NbTiN	2867/3024 = 94.8 17Q yield = 40.3	7.5–18	342	306
	Planar $35 \times 35$ NbTiN	1176/1225 = 96.0	11.3	549	182
	Planar $35 \times 35$ TiN	1161/1225 = 94.8	8.9	446	172
	Planar $35 \times 35$ Al	1121/1155 = 97.0 <sup>c</sup>	6.8	251	119

<sup>a</sup> Without regression filtering.

<sup>b</sup> With regression filtering.

<sup>c</sup> Two rows were accidentally omitted during data acquisition.

The shadowing effect of these features makes

$$W'_t(\vec{r}) \approx W_t + \delta W_{\text{offset}} - \begin{cases} W_{\text{lip}}(\vec{r}) + H'(\vec{r}) \frac{|y|}{D}, & \text{for } y \geq 0, \\ \max\left(H'(\vec{r}) \frac{|y|}{D}, W_{\text{lip}}(\vec{r}) + H'_{\text{lip}}(\vec{r}) \frac{|y|}{D}\right), & \text{for } y < 0, \end{cases} \quad (7)$$

where  $H'(\vec{r}) = H + \delta H(\vec{r})$  and  $H'_{\text{lip}}(\vec{r}) = H_{\text{lip}}(\vec{r}) + \delta H(\vec{r})$ . Including all modeled effects leads to  $A'_{\text{overlap}}(\vec{r})$  as shown in figure 4(d).

The geometric model predicts that junction conductivity erroneously computed as  $G/\Sigma A_{\text{overlap}}$  will show a center-to-edge decrease. Experimental results for the three Planar  $35 \times 35$  wafers clearly show this trend (figures 5(g)–(i)). In turn, the model predicts that conductivity computed as  $G/\Sigma A'_{\text{overlap}}$  will be flat. Due to the inaccuracy of approximating  $A'_{\text{overlap}}$  using top-view SEM images, a slight center-to-edge increase could even be observed. Conductivity computed as  $G/\Sigma A'_{\text{overlap}}$  is very uniform for the all-Al wafer, but not for the wafers with NbTiN and TiN probing pads. In these, the conductivity is very similar ( $\sim 4 \text{ mS } \mu\text{m}^{-2}$ ) at wafer center, but decreases noticeably away from it. These observations suggest that series resistance from the contact region (nominally  $32.4 \times 10^{-2} \mu\text{m}^2$ ) between Al electrodes and the NbTiN or TiN bays is small at wafer center but increases significantly away from center. While the contact region area is also impacted by the geometric shadowing effect, fractionally the effect is much less significant than for the JJ overlap areas, and cannot explain the observation. Using circuit analysis, we can calculate the net contact series resistance per junction required to match the observed reduction in conductivity computed from  $A'_{\text{overlap}}$  at wafer edge. We find  $\sim 2.3 \text{ k}\Omega$  for NbTiN pads and  $\sim 900 \Omega$  for TiN pads.

It remains important for future research to directly measure the magnitude and spatial dependence of this contact resistance, and to reduce both using bandaging layers [33, 36].

## 5. Conclusions

Table 1 summarizes the findings of our investigation of Dolan and Manhattan JJs on planar and TSV-integrated substrates, spanning yield, conductance CV and frequency RSD at wafer level, as well as average die-level RSD. For planar substrates, Dolan JJs perform best in all categories. In TSV-integrated substrates, Dolan JJs show a marked increase in disorder and decrease in yield, most likely due to their higher susceptibility to resist-height variation. Manhattan JJs are thus the preferred choice for TSV-integrated substrates, but their uniformity must be further improved. First, we must pre-compensate the spatial variation of junction overlap area that arises from the shadowing effect captured by the geometric model. For

the Manhattan-JJ resist stack used, the model predicts a narrowing of electrode widths by  $\sim 60$  nm from wafer center to edge (see figure S7). The resolution of our e-beam lithography system in 100 kV write mode is 5 nm, and thus it is possible in principle to pre-compensate the spatial variation in  $A'_{\text{overlap}}$ . Next, the magnitude and strong spatial dependence of contact resistance between the Al electrodes and the NbTiN bays, only inferred from our data, should be quantified, understood, and hopefully diminished using bandaging layers. These improvements will allow to quantify the intrinsic disorder of Manhattan JJs and approach the  $\sim 50$  MHz target that will secure SQP yield by post-fabrication trimming using laser annealing.

### Data availability statement

The data that support the findings of this study are openly available at the following URL/DOI: [http://github.com/DiCarloLab-Delft/Wafer\\_Scale\\_Fab\\_Data](http://github.com/DiCarloLab-Delft/Wafer_Scale_Fab_Data).

### Acknowledgments

We thank Bas van Asten for experimental assistance and David Michalak for valuable discussions. This research is supported by Intel Corporation and by the Office of the Director of National Intelligence (ODNI), Intelligence Advanced Research Projects Activity (IARPA), via the U.S. Army Research Office Grant No. W911NF-16-1-0071. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of the ODNI, IARPA, or the U.S. Government.

### Additional information

The data shown in all figures of the main text and Supplementary Information are available at [http://github.com/DiCarloLab-Delft/Wafer\\_Scale\\_Fab\\_Data](http://github.com/DiCarloLab-Delft/Wafer_Scale_Fab_Data). Correspondence and requests for additional materials should be addressed to L.D.C. (l.dicarlo@tudelft.nl).

### ORCID iD

Nandini Muthusubramanian  <https://orcid.org/0000-0003-0332-0280>

### References

- [1] Arute F *et al* 2019 Quantum supremacy using a programmable superconducting processor *Nature* **574** 505–10
- [2] Krinner S *et al* 2022 Realizing repeated quantum error correction in a distance-three surface code *Nature* **605** 669–74
- [3] Chen E H, Yoder T J, Kim Y, Sundaresan N, Srinivasan S, Li M, Córcoles A D, Cross A W and Takita M 2022 Calibrated decoders for experimental quantum error correction *Phys. Rev. Lett.* **128** 110504
- [4] Acharya R *et al* 2022 Suppressing quantum errors by scaling a surface code logical qubit (arXiv:2207.06431)
- [5] Foxen B *et al* 2017 Qubit compatible superconducting interconnects *Quantum Sci. Technol.* **3** 014005
- [6] Rosenberg D *et al* 2017 3D integrated superconducting qubits *npj Quantum Inf.* **3** 1–4
- [7] Kosen S *et al* 2022 Building blocks of a flip-chip integrated superconducting quantum processor *Quantum Sci. Technol.* **7** 035018
- [8] Béjanin J H *et al* 2016 Three-dimensional wiring for extensible quantum computing: the quantum socket *Phys. Rev. Appl.* **6** 044010
- [9] Bronn N T, Adiga V P, Olivadese S B, Wu X, Chow J M and Pappas D P 2018 High coherence plane breaking packaging for superconducting qubits *Quantum Sci. Technol.* **3** 024007
- [10] Spring P A *et al* 2022 High coherence and low cross-talk in a tileable 3D integrated superconducting circuit architecture *Sci. Adv.* **8** eabl6698
- [11] Versluis R, Poletto S, Khammassi N, Tarasinski B, Haider N, Michalak D J, Bruno A, Bertels K and DiCarlo L 2017 Scalable quantum circuit and control for a superconducting surface code *Phys. Rev. Appl.* **8** 034021
- [12] Yost D W *et al* 2020 Solid-state qubits integrated with superconducting through-silicon vias *npj Quantum Inf.* **6** 1–7
- [13] Alfaro-Barrantes J A, Mastrangeli M, Thoen D J, Visser S, Bueno J, Baselmans J J A and Sarro P M 2020 Superconducting high-aspect ratio through-silicon vias with DC-sputtered Al for quantum 3D integration *IEEE Electron Device Lett.* **41** 1114–7
- [14] Grigoras K *et al* 2022 Qubit-compatible substrates with superconducting through-silicon vias *IEEE Trans. Quantum Eng.* **3** 1–10
- [15] Hertzberg J B *et al* 2021 Laser-annealing Josephson junctions for yielding scaled-up superconducting quantum processors *npj Quantum Inf.* **7** 1–8
- [16] Marques J F *et al* 2022 Logical-qubit operations in an error-detecting surface code *Nat. Phys.* **18** 80–86
- [17] Krinner S, Lazar S, Remm A, Andersen C K, Lacroix N, Norris G J, Hellings C, Gabureac M, Eichler C and Wallraff A 2020 Benchmarking coherent errors in controlled-phase gates due to spectator qubits *Phys. Rev. Appl.* **14** 024042
- [18] Muthusubramanian N, Bruno A, Tarasinski B M, Fognini A, Hagen R and DiCarlo L 2019 Local trimming of transmon qubit frequency by laser annealing of Josephson junctions *Bull. Am. Phys. Soc.* B29–015
- [19] Zhang E J *et al* 2022 High-performance superconducting quantum processors via laser annealing of transmon qubits *Sci. Adv.* **8** eabi6690
- [20] Kim H *et al* 2022 Effects of laser-annealing on fixed-frequency superconducting qubits *App. Phys. Lett.* **121** 142601
- [21] Vallés-Sanclemente S *et al* 2023 Post-fabrication frequency trimming of coplanar-waveguide resonators in circuit QED quantum processors *App. Phys. Lett.* **123** 034004
- [22] Dolan G J 1977 Offset masks for lift-off photoprocessing *App. Phys. Lett.* **31** 337

- [23] Potts A, Routley P R, Parker G J, Baumberg J J and de Groot P A J 2001 Novel fabrication methods for submicrometer Josephson junction qubits *J. Mater. Sci. Mater.* **12** 289–93
- [24] Kreikebaum J M, O'Brien K P, Morvan A and Siddiqi I 2020 Improving wafer-scale Josephson junction resistance variation in superconducting quantum coherent circuits *Supercond. Sci. Technol.* **33** 06LT02
- [25] Osman A, Fernández-Pendás J, Warren C, Kosen S, Scigliuzzo M, Kockum A F, Tancredi G, Fadavi Roudsari A, and Bylander J 2023 Mitigation of frequency collisions in superconducting quantum processors (arXiv:2303.04663)
- [26] Muthusubramanian N, Duivesteyn W, Zachariadis C, Finkel M, Bruno A and DiCarlo L 2021 Fabrication parameters for frequency targeting in scalable superconducting quantum processors *Proc. APS March Meeting* vol 66 pp V30–002
- [27] Kreikebaum J M, Chen L, Morvan A, Ville J, O'Brien K and Siddiqi I 2021 Highly uniform submicron junction arrays for quantum information processing *Proc. APS March Meeting* vol 66 pp V30–003
- [28] Takahashi T, Kouma N, Doi Y, Sato S, Tamate S and Nakamura Y 2022 Uniformity improvement of Josephson-junction resistance by considering sidewall deposition during shadow evaporation for large-scale integration of qubits *J. Appl. Phys.* **62** SC1002
- [29] Marques J F *et al* 2023 All-microwave leakage reduction units for quantum error correction with superconducting transmon qubits *Phys. Rev. Lett.* **130** 250602
- [30] Ambegaokar V and Baratoff A 1963 Tunneling between superconductors *Phys. Rev. Lett.* **10** 486–9
- [31] Tinkham M 2004 *Introduction to Superconductivity* 2nd edn (Dover Publications)
- [32] Koch J, Yu T M, Gambetta J, Houck A A, Schuster D I, Majer J, Blais A, Devoret M H, Girvin S M and Schoelkopf R J 2007 Charge-insensitive qubit design derived from the Cooper-pair box *Phys. Rev. A* **76** 042319
- [33] Osman A, Simon J, Bengtsson A, Kosen S, Krantz P, Lozano D P, Scigliuzzo M, Delsing P, Bylander J and Fadavi Roudsari A 2021 Simplified Josephson-junction fabrication process for reproducibly high-performance superconducting qubits *Appl. Phys. Lett.* **118** 064002
- [34] Verjauw J *et al* 2022 Path toward manufacturable superconducting qubits with relaxation times exceeding 0.1 ms *npj Quantum Inf.* **8** 93
- [35] Bonnin L, Piot A, Isac N and Bosseboeuf A 2020 Deposition and patterning of electrodes on the vertical sidewalls of deep trenches *J. Micromech. Microeng.* **30** 105014
- [36] Nersisyan A *et al* 2019 Manufacturing low dissipation superconducting quantum processors *Int. Electron Devices Meeting (IEDM)*