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Feng, Xiangdong ; Luo, Yuxuan; Cai, Tianyi ; Xuan, Yangfan ; Zhang, Yunshan; Shen, Yili ; Yang, Changgui; Xiao, Qijing ; Du, Sijun ; Zhao, Bo

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A 72-Channel Resistive-and-Capacitive Sensor-Interface Chip With Noise-Orthogonalizing and Pad-Sharing Techniques

Xiangdong Feng, *Graduate Student Member, IEEE*, Yuxuan Luo, *Senior Member, IEEE*, Tianyi Cai, Yangfan Xuan, Yunshan Zhang, *Student Member, IEEE*, Yili Shen, Changgui Yang, *Student Member, IEEE*, Qijing Xiao, *Student Member, IEEE*, Sijun Du, *Senior Member, IEEE*, and Bo Zhao, *Senior Member, IEEE*

***Abstract*— The growing trend of the Internet of Things (IoT) involves trillions of sensors in various applications. An extensive array of parameters need to be gathered concurrently with high-precision, low-cost, and low-power sensor nodes, such as resistive (R) and capacitive (C) sensors. Single-chip channel fusion can be an effective solution, while it is challenging to suppress the noise and integrate massive I/O pads. However, conventional oversampling noise-shaping methods increase power consumption, which fails to meet the demand of long-term monitoring applications. In addition, existing R/C sensor-interface chips require a pair of I/O pads for each sensor, where the pad frame dominates the overall chip area in massive-channel integration. In this work, we demonstrate a 72-channel R&C sensor-interface chip for proximity-and-temperature sensing. A noise-orthogonalizing technique is proposed to eliminate the quantization noise at the signal frequencies, achieving an energy efficiency of 19.1 pJ/step/channel. Moreover, a pad-sharing technique is proposed to reduce the number of I/O pads by half, enabling 72 sensors to be read by 36 pairs of I/O pads. The chip is fabricated by 65-nm CMOS technology, and measurement results show resolutions of 286 Ω and 162 fF, respectively. The power consumption and die area are reduced to 0.74 μW/Channel and 0.038 mm^2/Channel, respectively.**

***Index Terms*— Low power, multichannel sensing, noise-orthogonalizing, pad-sharing, sensor interface.**

I. Introduction

THE recent surge in the Internet of Things (IoT) sensors requires the integration of a large number of channels on a single chip, where noise reduction and massive I/O integration present the two main design challenges. In typical applications such as environmental monitoring, trillions of battery-powered resistive (R) or capacitive (C) sensors are distributed in the target area to simultaneously detect a myriad of parameters such as temperature, pressure, humidity, and proximity [1], [2], [3], [4], [5], [6], [7], [8]. In these cases, the sensor nodes should be power-efficient and low-cost, necessitating the integration of numerous channels on a single R&C sensing chip. However, increasing the number of channels leads to a significant increment in power consumption and chip area, particularly in the I/O pad frame, which contradicts the goal of cost-effective and energy-efficient IoT deployment.

Noise-shaping methods based on oversampling have been widely adopted in conventional multichannel sensing chips, but the high sampling frequency increases the power consumption. For example, the time-domain noise-shaping technique in [2] necessitated a sampling frequency of 2 MHz, resulting in 15.6-μW power consumption. As the fusion of multiple channels reduced the available dynamic range of each channel, a high-resolution noise-shaping analog-to-digital converter (ADC) was desired in [9] and [10], leading to 1.534-mW power consumption [10]. The oversampling SAR ADCs can also achieve low power consumption and moderate resolution, whereas noise-shaping ADCs can trade speed for resolution. For sensor-interface chips, noise shaping is widely adopted to realize high precision. However, conventional noise-shaping methods still suffer from signal-to-noise-ratio (SNR) degradation due to the impact of quantization noise [see Fig. 1 (top-right)].

The integration of massive I/O pads presents another design challenge in multichannel sensor-interface chips. In conventional multiplexing methods for R&C sensors, each R or C sensor necessitates a pair of I/O pads [6], resulting in the pad frame dominating the overall die area of a massive-channel sensor-interface chip [see Fig. 1 (top-left)]. This leads to significant costs in the chip fabrication process. For example, a 32-channel R&C sensor-interface chip [4] measured a die area of 4.5 mm^2, and an eight-channel electrical impedance tomography chip [11] occupied a die area of 4.84 mm^2.

To address the issues of noise and pad frame, a 72-channel R&C sensor-interface chip is demonstrated for proximity and

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Xiangdong Feng and Bo Zhao are with the Institute of VLSI Design, Zhejiang University, Hangzhou 310027, China, and also with the Nanhu Brain-Computer Interface Institute, Hangzhou 311100, China (e-mail: zhaobo@zju.edu.cn).

Yuxuan Luo, Tianyi Cai, Yangfan Xuan, Yili Shen, Changgui Yang, and Qijing Xiao are with the Institute of VLSI Design, Zhejiang University, Hangzhou 310027, China.

Yunshan Zhang is with Microaiot, Ltd., Hangzhou 310013, China.

Sijun Du is with the Department of Microelectronics, Delft University of Technology, 2628 Delft, The Netherlands.

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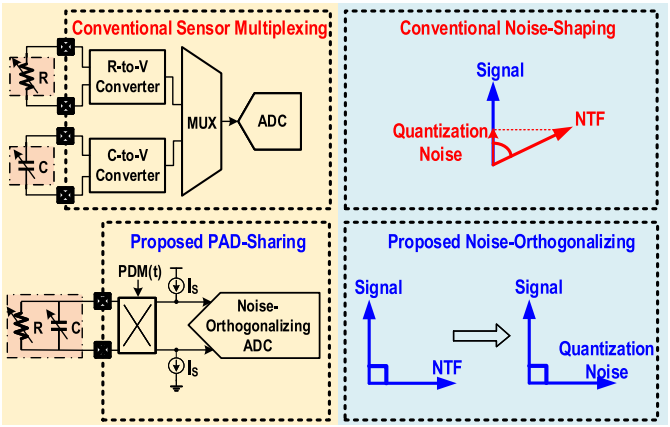

Fig. 1. Conventional R/C sensor-interface methods and proposed techniques.

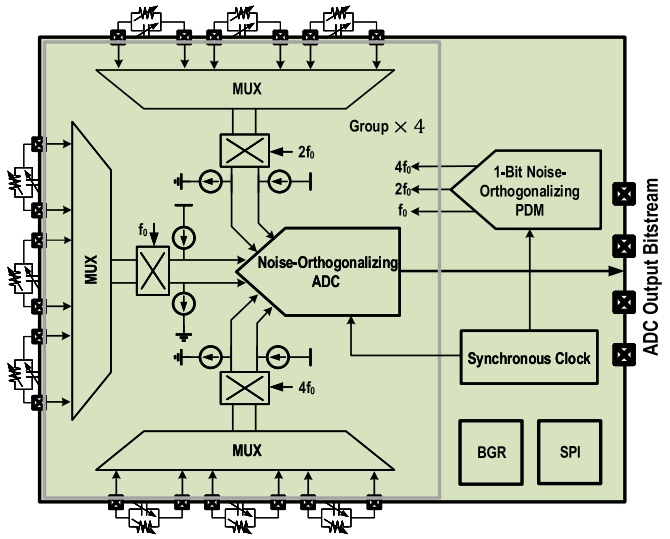

Fig. 2. System architecture of the proposed 72-channel R&C sensor-interface chip.

temperature sensing, where the chip area and power consumption are reduced to 0.038 mm^2/channel and 0.74 μW/channel, respectively (first introduced in [12]). Two techniques are proposed to surmount the design challenges in conventional works [see Fig. 1 (bottom)]: 1) a noise-orthogonalizing technique is proposed to strip the quantization noise at the frequencies of stimulated sensing signals, achieving energy efficiency of 19.1 pJ/step per channel and 2) a pad-sharing technique is proposed to cut down the number of I/O pads by half, enabling 72 sensors to be read by 36 pairs of I/O pads.

The rest of this article is organized as follows. Section II describes the system structure and proposed techniques. The detailed circuit designs are described in Section III. Section IV shows the experimental results and prototype demonstration. Finally, Section V concludes the work.

II. System Architecture and Proposed Techniques

The system architecture of the proposed 72-channel R&C sensor-interface chip is illustrated in Fig. 2. The chip includes four groups of sensor-interface units, a 1-bit noise-orthogonalizing pulse density modulator (PDM), a bandgap reference (BGR), and a serial peripheral interface (SPI). Each group is composed of three subgroups, and each pair of I/O pads is connected to a parallel combination of an R sensor and a C sensor, which can be simultaneously read out by the synchronous 1-bit noise-orthogonalizing PDM and ADC. The clock of ADC is synchronized with the PDM stimulation, and then the first bit of the ADC output matches the initial phase of the stimulation waveform in the time domain, which helps to obtain both amplitude and phase of the R&C sensors in parallel. In each subgroup, three R&C sensor pairs share six I/O pads and a multiplexer (MUX). Subsequently, the outputs of three R&C sensor subgroups are multiplied by f_0, $2f_0$, and $4f_0$ and then merged into the input of the 1-bit noise-orthogonalizing ADC. As a result, a single ADC can process the nine R&C sensor pairs, corresponding to 18 R&C sensors. In this way, the sensor-interface chip can handle 72 R&C sensors with 72 I/O pads, reducing the number of I/O pads by half compared to the conventional structures.

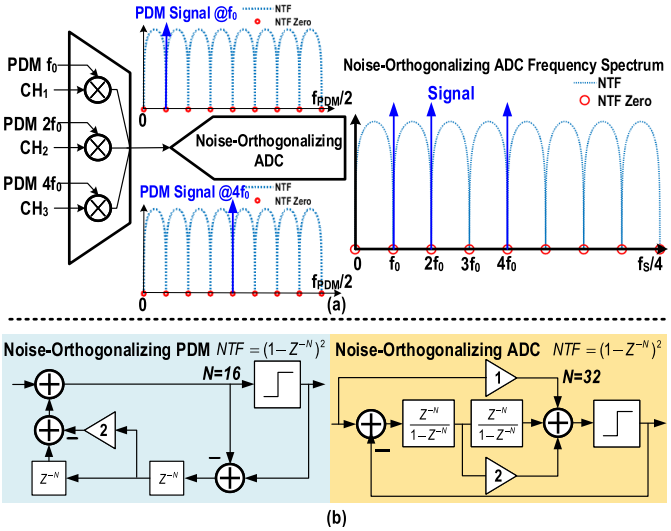

Fig. 3. Proposed noise-orthogonalizing technique. (a) Signal spectrums. (b) NTFs of PDM and ADC.

A. Noise-Orthogonalizing Technique

To improve the SNR of each sensing chain, a noise-orthogonalizing technique is proposed to protect the sensing signals from noise, as shown in Fig. 3. The stimulation signal and noise transfer function (NTF) are designed to be orthogonal with each other. Both the NTFs of the stimulating PDM and detecting ADC are designed to be $(1-z^{-N})^2$, which presents N uniformly distributed zeros in the frequency range of $0-f_S$. Then, the stimulation frequencies are set to f_0, $2f_0$, and $4f_0$ at the zero points of NTF. In this way, both the wide-band truncation noise of PDM and the quantization noise of ADC present notches at the signal frequencies. The nonlinearity of the integrator and the inherent nonlinearity of the 1-bit quantizer introduce third-harmonic distortion, which will lead to crosstalk at $3f_0$ frequency. Therefore, the $3f_0$ frequency is skipped to avoid the crosstalk.

The stimulation and detection chain employs a 1-bit second-order error-feedback (EF) PDM and a 1-bit Silva-Steensgaard

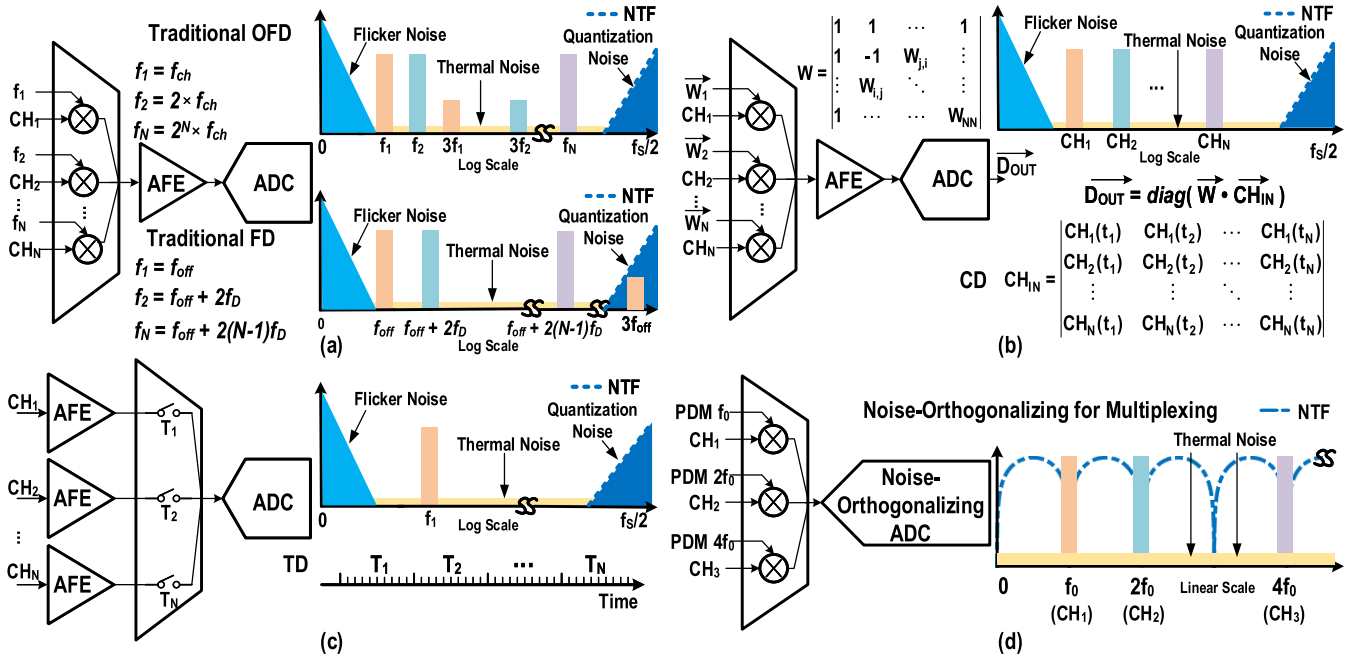

Fig. 4. Signal and noise of multiplexing structures. (a) OFD and FD. (b) CD. (c) TD. (d) Noise-orthogonalizing.

ADC to realize a high linearity, as shown in Fig. 3(b). The parameter N is set to 16 and 32 for PDM and ADC, respectively, forming an antialiasing filtering characteristic, which will be described in Section II-C. Thus, the relationship between ADC sampling rate (f_S), the PDM clock frequency (f_{PDM}), and f_0 can be expressed by $f_S = 32f_0$ and $f_{\text{PDM}} = 16f_0$. Then, the second-order noise shaping provides 40-dB/decade rejection toward the zero-point frequencies. Multiplied by the stimulation frequencies (f_0, $2f_0$, and $4f_0$), the sensor signals are merged into the input of noise-orthogonalizing ADC to realize the R&C-to-digital conversion. Therefore, the proposed noise-orthogonalizing technique can improve the sensing SNR in a power-efficient and area-efficient way. The basic function of the proposed noise-orthogonalizing ADC is similar to that of an N-path-transformed bandpass noise-shaping ADC. However, the PDM and ADC are codesigned and share the same NTF in the proposed structure, which ensures that the signal is located at the zeros of NTF throughout the entire signal chain, eliminating the impact of quantization noise. In the traditional bandpass noise-shaping ADCs, the signal is distributed across the passband, where part of the signal will still be affected by quantization noise. If the sensor signals contain a non-dc component with a specific frequency (e.g., f_1), the signal at the ADC will be located at $i \cdot f_0 \pm f_1, i = 1, 2, 4$. In this case, the quantization noise can be suppressed partly instead of fully eliminated.

To mitigate the impact of flicker noise, the proposed technique utilizes PDM modulation to upconvert sensor signals, as shown in Fig. 4(d). The precision of conventional noise-shaping methods with a high-pass NTF will be affected by the flicker noise, especially in sensor-interface applications operating at low frequencies. For example, the continuous-time $\Delta\Sigma$ ADC in [13] exhibited evident flicker noise spanning from dc to 10 kHz in the spectrum. Although chopping is widely used to mitigate the impact of flicker noise, it introduces noise folding in sensor interfaces with $\Delta\Sigma$ ADCs. The noise folding occurs when the shaped quantization noise is folded back into the signal band, resulting in performance degradation [13], [14]. In another classical work focusing on humidity sensors [15], auto-zeroing technology was adopted to reduce flicker noise, but the measured spectrum still exhibited flicker noise from dc to 800 Hz. In this work, the noise-orthogonalizing PDM signals are employed to upconvert low-frequency sensor signals, effectively avoiding the impact of flicker noise, as shown in Fig. 4(d). The selection of the fundamental carrier frequency (f_0) involves a tradeoff between flicker noise and power consumption. A higher f_0 results in lower flicker noise but also increases power consumption. Therefore, $f_0 = 2.5$ kHz is selected to balance the power consumption and flicker noise.

In comparison to conventional oversampling noise-shaping methods, the proposed noise-orthogonalizing technique can realize the same signal-to-quantization-noise ratio (SQNR) with a lower sampling frequency. As analyzed in the Appendix, the SQNR of the proposed noise-orthogonalizing system is

$$\text{SQNR} = \frac{15M^5}{2\pi^4 N^4}. \tag{1}$$

For conventional oversampling noise-shaping methods with high-pass NTF in Figs. 1 and 4, the relationship between SQNR and oversampling ratio (OSR) [16] is

$$\text{SQNR} = \frac{15(\text{OSR})^5}{2\pi^4}. \tag{2}$$

If the conventional noise-shaping with high-pass NTF targets at the same SQNR as the proposed noise-orthogonalizing

TABLE I
COMPARISON OF MULTIPLEXING SCHEMES WITH THE NORMALIZED SQNR

Multiplexing	Required Total Signal Bandwidth	ADC Sampling Frequency
OFD	10.02kHz	2.505MHz
FD	2.72kHz	0.68MHz
CD	5.02kHz	1.255MHz
TD	7.56kHz	1.89MHz
Proposed	0.12kHz	0.08MHz

technique, the OSR is required to be

$$\text{OSR} = \frac{M}{\sqrt[5]{N^4}}. \tag{3}$$

The ADC sampling frequency is $f_S = 80$ kHz, as $f_0 = 2.5$ kHz is selected. The single-sideband bandwidth is $f_B = 20$ Hz, which is adopted to process the non-dc sensor signals. Based on the design parameters and (1), the normalized SQNR is 93.7 dB. To realize the same SQNR as the proposed technique, conventional oversampling noise-shaping methods need an OSR of 125 according to the definition in [17], which will result in a much higher sampling frequency. In comparison, the multiple pass bands allow the proposed system to achieve a lower overall sampling frequency, as shown in Table I.

As the noise-orthogonalizing ADC can process multiple channels simultaneously, we compare it with conventional noise-shaping methods with multiplexing. In traditional orthogonal frequency-division (OFD) multiplexing, N input signals are modulated onto N orthogonal chopping frequencies [see Fig. 4(a) (top)]. For frequency-division (FD) multiplexing, the carrier frequencies of the N channels are set with equal intervals, and a frequency offset is introduced in each carrier to avoid the impact of the third harmonic of the fundamental carrier [see Fig. 4(a) (bottom)]. Code-division (CD) multiplexing employs orthogonal codewords, enabling a higher spectrum efficiency for a large number of channels [see Fig. 4(b)]. Time-division (TD) multiplexing is a straightforward technique to process the input signals in different time slots [see Fig. 4(c)].

The specific sampling frequency of the proposed technique is compared with conventional noise-shaping techniques employing various multiplexing techniques (OFD, FD, CD, and TD), which are shown in Fig. 4 and summarized in Table I. To ensure a fair comparison among the multiplexing methods, it is assumed that all the methods are implemented under identical conditions, including the number of channels (three channels), the single-channel bandwidth ($2f_B = 40$ Hz), and the fundamental carrier frequency ($f_0 = 2.5$ kHz). Table I provides the required total signal bandwidths for OFD, FD, CD, and TD, which are 10.02, 2.72, 5.02, and 7.56 kHz, respectively. Based on the spectrum shown in Fig. 4, the bandwidths for OFD, FD, CD, and TD are calculated by $4f_0 + f_B$, $f_0 + 5f_D$ ($f_D = 50$ Hz), $2f_0 + f_B$, and $3(f_0 + f_B)$, respectively. The sampling frequency of OFD, FD, CD, and TD is 2.505, 0.68, 1.255, and 1.89 MHz, respectively. It can be seen that the proposed noise-orthogonalizing technique shows the lowest sampling frequency at the same SQNR. The lower sampling frequency in the proposed noise-orthogonalizing technique helps to reduce power consumption.

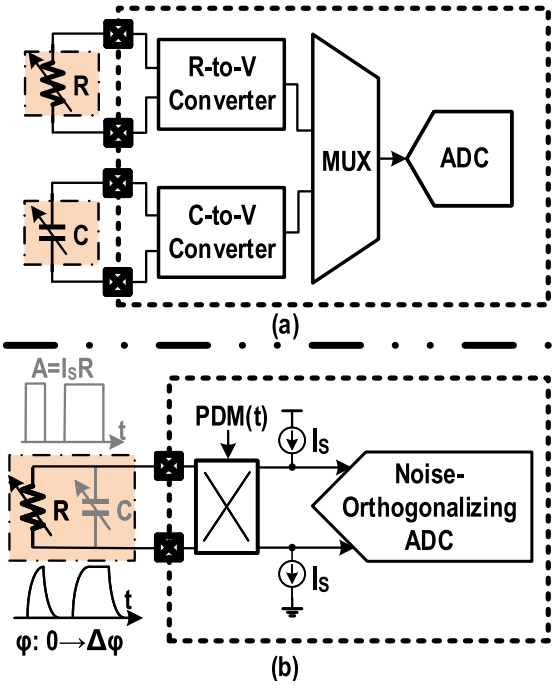

Fig. 5. (a) Conventional separated R sensor interface and C sensor interface. (b) Proposed pad-sharing R&C sensor interface.

B. Pad-Sharing Technique

The pad-sharing technique reduces the number of I/O pads by 1/2, which benefits from simultaneously sensing R and C. In conventional MUX-based R&C sensing, each R or C sensor necessitates a pair of I/O pads [6], as given in Fig. 5(a), leading to a large pad frame in massive-channel integration. The proposed pad-sharing technique connects an R sensor and a C sensor in parallel, which is stimulated and read simultaneously, as shown in Fig. 5(b). Both the amplitude and phase of the PDM stimulation signal are shifted by the R&C network, which can be analyzed by the digital part to resolve the R&C values. Denoting the impedance of RC parallel combination by $Z == \text{real}(Z) + j \cdot \text{imag}(Z)$, we can have

$$\text{real}(Z(j\omega)) + j \cdot \text{imag}(Z(j\omega)) = \frac{R}{1 + j\omega RC}. \tag{4}$$

Then, the values of R and C can be expressed by

$$R = \frac{\text{real}(Z(j\omega))^2 + \text{imag}(Z(j\omega))^2}{\text{real}(Z(j\omega))} \tag{5}$$

$$C = \frac{-\text{imag}(Z(j\omega))}{(\text{real}(Z(j\omega))^2 + \text{imag}(Z(j\omega))^2)\omega} \tag{6}$$

where the value of $Z(j\omega)$ can be determined through the spectrum analysis at frequency bins of f_0, $2f_0$, and $4f_0$. The

parasitic capacitance in the R sensor and parasitic resistance in the C sensor will impact the measurement results. However, the commonly used R sensor ranges from 100 Ω to 2 MΩ, while the parasitic resistance in parallel presents a very high value. For example, the capacitive humidity sensor in [15] exhibited a shunt parasitic resistance of ≥1 GΩ, which can be neglected in parallel connection with the R sensor. For the R sensor, its parasitic capacitance remains constant at the pF level, and it can be eliminated as a baseline during digital processing. However, this parasitic capacitance degrades the dynamic range, resulting in a slight reduction in the effective number of bits (ENOB). The ADC clock synchronizes the PDM stimulation signal, facilitating the acquisition of both R and C values. The power consumption of digital post-processing modules is about 5.3 μW, including the discrete Fourier transform (DFT) circuit, squaring circuit, adders, and dividers. The DFT circuit adopts the architecture proposed in [18], which acts as a decimation filter. The total inductance of the bonding wire and printed circuit board (PCB) trace amounts to approximately 15 nH. At an operating frequency of 80 kHz, the total impedance is 6 mΩ. Compared to the 100-kΩ baseline impedance of the thermistor, the 6-mΩ parasitic impedance can be negligible. As the PDM and ADC use a synchronous clock, the frequency sweeping and impedance spectroscopy can be obtained by scanning the clock frequency.

C. Antialiasing Consideration

The harmonic components of the PDM stimulation signal should be rejected by an antialiasing filter, as depicted in Fig. 6(a). In conventional sensing chains, an antialiasing filter is typically placed at the input of ADC [1], [9], [10], which enlarges the die area and power consumption.

In this work, the proposed sensing structure presents an intrinsic antialiasing character, eliminating the need for an additional filter. As illustrated in Fig. 6(b), the parallel combination of the R sensor and C sensor forms a low-pass filter that suppresses the high-frequency harmonics. In addition, the PDM signal is generated through the convolution of a digital code word and a zero-order holding signal in the time domain, which results in a Sinc-envelope frequency response in [see Fig. 6(c)], indicating the secondary low-pass filter. At an ADC sampling frequency of f_S, the three high-frequency harmonics ($f_S - f_0$, $f_S - 2f_0$, and $f_S - 4f_0$) can be suppressed by the low-pass responses of both RC-sensor and the Sinc-envelope function. In this way, the proposed sensing circuits provide an intrinsic antialiasing performance without requiring a separate filter. The PDM Sinc envelope can suppress the $f_S - f_0$ harmonic by 30 dB by setting $N = 32$, as shown in Fig. 6(c).

According to the experimental results, the antialiasing functionality remains effective when sensor multiplexing is implemented. Although the multiplexing process modulates the control signal on the sensor signal, the resulting frequency change is smaller than the spectrum resolution and can be disregarded. As a result, the multiplexing induces little impact on the filtering behavior and spectrum.

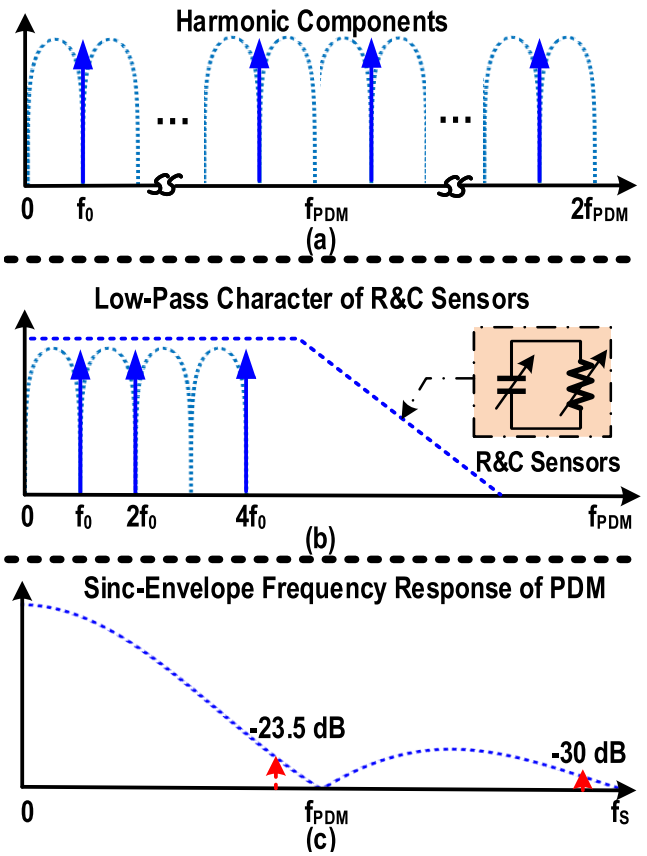

Fig. 6. Intrinsic antialiasing characteristics of the proposed sensor-interface circuits. (a) Harmonic components induced by PDM. (b) Low-pass filtering of pad-sharing R&C sensor. (c) Sinc-envelop low-pass frequency response induced by PDM.

III. Circuit Designs

A. Single-Bit Noise-Orthogonalizing PDM

Fig. 7(a) details the circuit of noise-orthogonalizing PDM. The PDM consists of three 12-bit pseudo-sine lookup tables (LUTs) for f_0, $2f_0$, and $4f_0$, respectively, as well as three second-order digital EF $\Delta\Sigma$ modulators [NTF $= (1 - z^{-N})^2$] and a 15-bit pseudorandom binary sequence (PRBS) generator. As the phase accumulator sends rotational counter values to the amplitude-mapped memory, the LUTs output 12-bit integer data of sinusoidal waveform. The phase of f_0 is not shifted, while both the phases corresponding to $2f_0$ and $4f_0$ are delayed by 90°. Then, the $\Delta\Sigma$ modulator shapes the stimulation signal into a single-bit stream, where the spurs are reduced by the dithering of the PRBS generator. The LUTs and digital circuitry are implemented on-chip, as shown in the die micrograph.

The dynamic range is enlarged to combine the signals in three channels, as shown in Fig. 7(b) and (c). Merging the sensing signals multiplied by f_0, $2f_0$, and $4f_0$ into a single ADC can potentially reduce the dynamic range of each channel. In this work, the phase relationship of the three channels is controlled to increase the dynamic range. As the PDM signal is filtered by the R&C sensors and the Sinc function, the input signal of ADC can be approximated to be a sinusoidal waveform to evaluate the dynamic range.

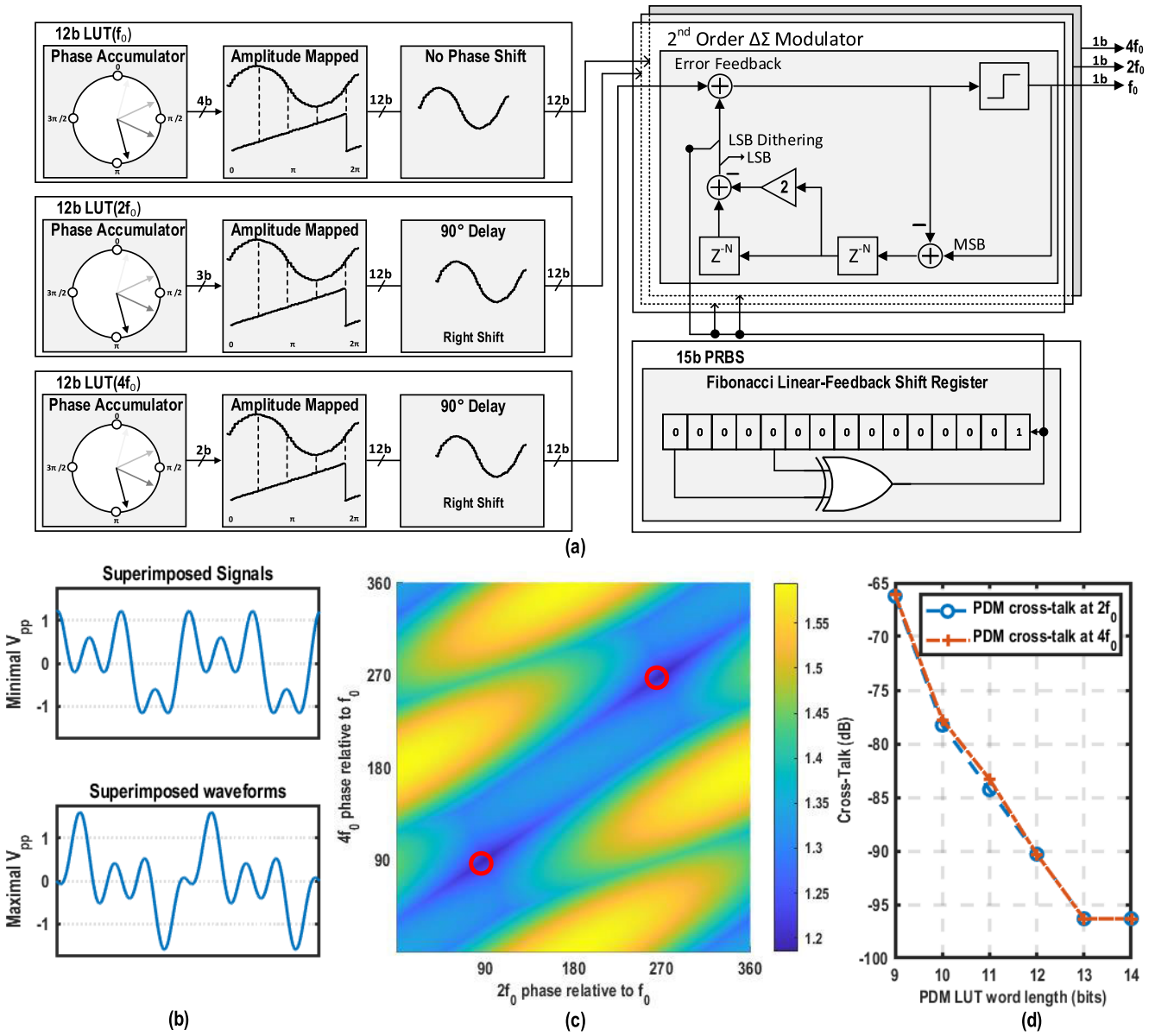

Fig. 7. Noise-orthogonalizing PDM. (a) Signal flow and block diagram. (b) Time-domain waveforms of merged signals with minimum V_{pp} and maximum V_{pp} values. (c) Merged signal amplitude versus phase scanning. (d) Crosstalk versus PDM LUT word length.

In traditional FD, CD, and OFD multiplexing structures, the amplitude of each channel is reduced by a factor of N when N channels are combined [19]. For instance, in the case of an ADC with $V_{PP} = 1.2$-V input dynamic range and three multiplexed channels, the maximum V_{PP} of each channel would be 0.4 V. In this work, the relationship between V_{PP} and the phase is illustrated in Fig. 7(b) and (c), where all the three sinusoidal waveforms ($V_{PP} = 0.6$ V) at f_0, $2f_0$, and $4f_0$ are summed. As the relative phases of $2f_0$ and $4f_0$ to f_0 are 90° or 270°, respectively, the sum of the three amplitudes is 1.2 V, which does not exceed the ADC's input dynamic range. In this way, the phase-shifting operation helps to increase V_{PP} of each channel in the noise-orthogonalizing ADC to 0.6 V, which is 1.5 times that achieved by FD, CD, or OFD multiplexing methods. In TD multiplexing, V_{PP} in a single channel can reach 1.2 V, which doubles that of a single channel in the noise-orthogonalizing technique. However, the TD structure requires a much higher sampling frequency. In Table I, the TD with noise-shaping necessitates a sampling frequency that is 23.6 times of the proposed technique. Therefore, the proposed technique still offers an advantage even when the maximum V_{PP} is only half of that in the TD multiplexing.

The system-level crosstalk is determined by the maximum value between PDM crosstalk and ADC crosstalk. The main reason for PDM crosstalk is that the harmonics of f_0 cause interference to the signals at $2f_0$ and $4f_0$, which is primarily determined by the word length of the LUT in PDM. The PDM crosstalk is simulated in Fig. 7(d), where the crosstalk reaches the valley as the LUT word length ranges between 9 and 13 bits. The PRBS generator determines the down limit of crosstalk beyond 13 bits. Therefore, the word length of LUT is set to 12 bits.

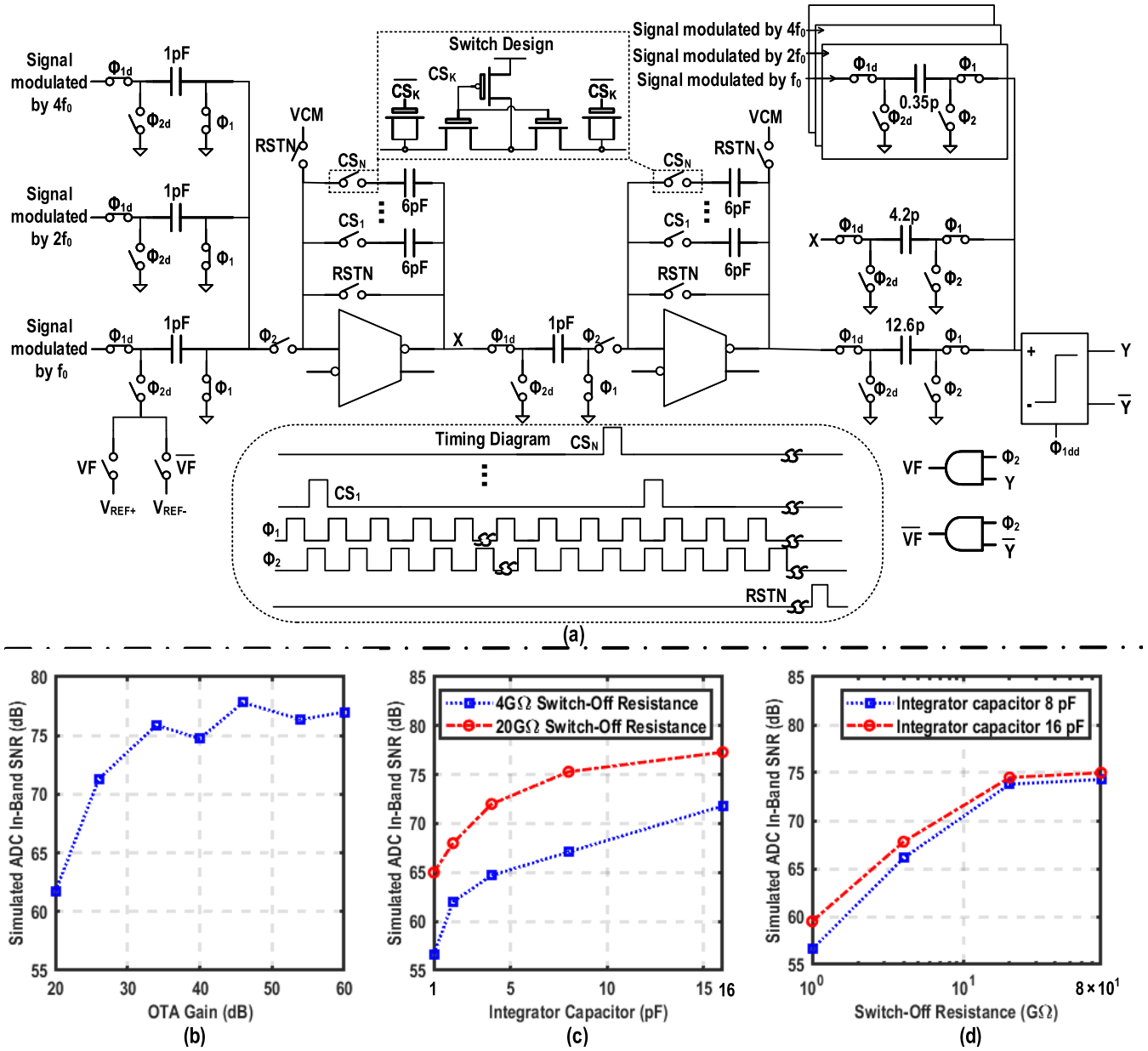

Fig. 8. Noise-orthogonalizing ADC. (a) Schematic and timing diagram. (b) Simulated ADC in-band SNR versus OTA gain. (c) Simulated ADC in-band SNR versus integrator capacitor. (d) Simulated ADC in-band SNR versus switch-off resistance.

B. Single-Bit Noise-Orthogonalizing ADC

Fig. 8 shows the schematic of the noise-orthogonalizing ADC, which employs the low-power cascade-of-integrators-with-feed-forward (CIFF) topology [20], [21]. To process the input three-channel signals simultaneously, three sampling circuits and three feed-forward circuits are included in the ADC, while the single feedback digital-to-analog converter (DAC) results in lower power consumption. The single integral capacitor in the integrator of conventional $\Delta\Sigma$ ADC is replaced by N parallel integral capacitors, and the N-path parallel integral capacitors are turning on sequentially, as shown in the timing diagram of Fig. 8(a). To reduce the impact of clock feedthrough and charge injection, two dummy NMOS transistors are added to the two terminals of each switch. In this way, the integrator of conventional $\Delta\Sigma$ ADC

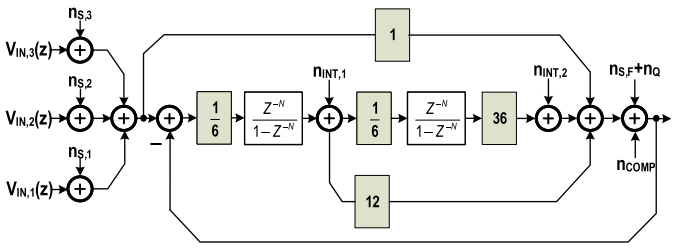

Fig. 9. Noise model of noise-orthogonalizing ADC.

$[z^{-1}/(1-z^{-1})]$ is changed into $z^{-N}/(1-z^{-N})$ to realize the noise-orthogonalizing function of $(1-z^{-N})^2$.

The nonideal factors limit the in-band SNR, which should be considered in circuit designs. As the NTF zeros are

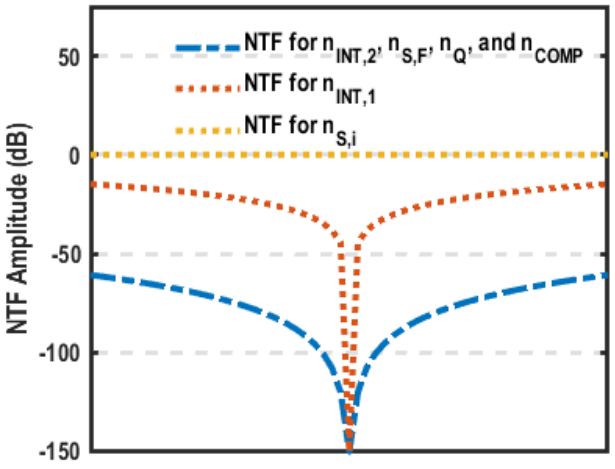

Fig. 10. Zoomed-in diagram of NTF in the signal band.

TABLE II
NTFs FOR VARIOUS NOISE SOURCES IN THE PROPOSED NOISE-ORTHOGONALIZING ADC

Noise Type	NTF
Sampling ($N_{S,i}$)	1
1^{st}-integrator ($N_{INT,1}$)	$6(2-z^{-N})(1-z^{-N})$
2^{nd}-integrator ($N_{INT,2}$)	$(1-z^{-N})^2$
Feedforward switch ($N_{S,F}$)	$(1-z^{-N})^2$
Comparator (N_{COMP})	$(1-z^{-N})^2$
Quantization (N_Q)	$(1-z^{-N})^2$

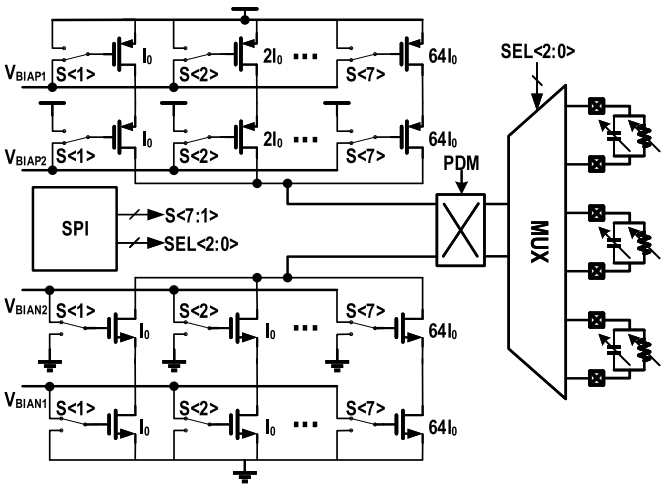

Fig. 11. Schematic of programmable excitation current source.

employed to mitigate quantization noise, the nonideal factors can lead to deviations in the NTF zeros, which degrade the SNR. The simulation results in Fig. 8(b) present the relationship between in-band SNR and operational transconductance

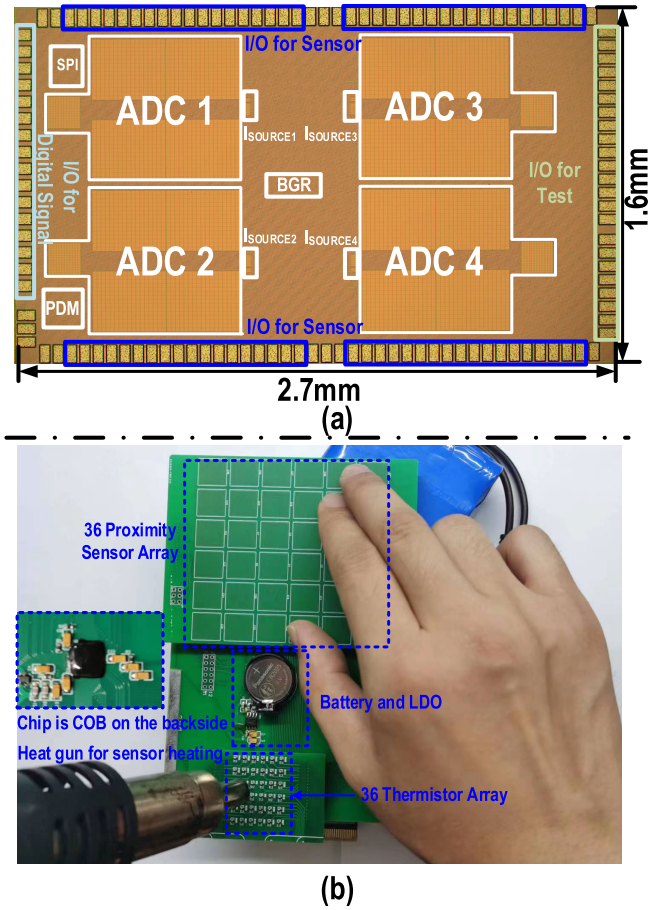

Fig. 12. (a) Die micrograph. (b) Measurement setup.

amplifier (OTA) gain, where the in-band SNR becomes saturated at 75 dB when the OTA gain exceeds 34 dB. In this design, a single-stage class-A OTA with local positive feedback [20] is used to realize a gain higher than 48.5 dB across all process, voltage, and temperature (PVT) corners, resulting in little impact on SNR. The swing of the integrator is reduced to minimize the distortion, so the coefficient of the first-stage integrator is set to 1/6, which is determined by the ratio of the sampling capacitor (1 pF) over the integrating capacitor (6 pF). There is a tradeoff in sizing the sampling capacitor. If the sampling capacitor is too small, both the kT/C noise and the integrator's leakage will degrade the SNR, as illustrated in Fig. 8(c). Conversely, if the sampling capacitor is too large, the size of the integrating capacitors should also be increased, leading to SNR degradation due to low slew rate and settling issue of the integrator. As a result, a 1-pF sampling capacitor is adopted to optimize the SNR. According to the simulation in Fig. 8(d), a higher switch-off impedance of MOSFET switches can improve the in-band SNR. Therefore, a T-switch [22] based on thick-gate MOSFET is utilized to realize a switch-off impedance above 22.07 GΩ.

Thermal noise is generally one of the main design challenges. As shown in Fig. 9, the noise sources in the ADC consist of various components, including the thermal noise of the sampling switch ($N_{S,i}$), the output thermal noise of the two integrators ($N_{\mathrm{INT},1}$ and $N_{\mathrm{INT},2}$), feedforward switch thermal

TABLE III
PERFORMANCE COMPARISON

	[2]	[3]	[4]	[6]	[7]	[8]	This Work
Sensor Type	R&C	R&C	R&C	R&C	C	C	R&C
Num. of Sensors	2	2	32	3	1	1	72
Application	RH & Temp.	RH & Temp.	Prox.	Acc., Temp. & pH	RH	IoT	Prox. and Temp.
Process	180nm	180nm	130nm	65nm	110nm	22nm	65nm
Core Area	0.72mm^2	0.175mm^2	1.19mm^2	0.084mm^2	0.46mm^2	N/A	3.09mm^2
Area/Ch.	0.36mm^2	0.088mm^2	0.04mm^2	0.03mm^2	0.46mm^2	N/A	0.038mm^2
Supply Voltage	1.5 2V	1V	N/A	0.6V	1.2V	1.1V	1.2V
Total Power	15.6μW	140μW	70μW	1.34μW	3.19μW	4.71μW	53μW
Power/Ch.	7.8μW	70μW	2.2μW	0.447μW	3.19μW	4.71μW	0.74μW
C Range	N/A	5.4 pF$^{(a)}$	100 pF	7.85pF	3.15pF	5.16pF	1 nF
C ENOB	8.22$^{(b)}$	14$^{(a)}$	11.3	9.05	14	11.5	10.5
C Resolution	N/A	114aF	13.75fF	4.26fF	17.9aF	37.12aF	162fF
R Range	N/A	15 k$\Omega^{(a)}$	249 kΩ	30.2kΩ	N/A	N/A	910 kΩ
R ENOB	8.22$^{(b)}$	13.8$^{(a)}$	11.4	7.1	N/A	N/A	10.13
R Resolution	N/A	0.37Ω	32.5Ω	63.7Ω	N/A	N/A	286Ω
Conversion Time$^{(c)}$	2ms	5.86ms	32ms	80μs	1.01ms	5μs	37.5ms
Energy Effi/Ch.$^{(d)}$ (pJ/step)	52.3	28.8	27.84	0.224	0.094	0.0079	19.1
Sensor/Pad	N/A	2/3	16/17	0.5	N/A	N/A	1

(a) The sensing resolution corresponds to the R&C range. (b) Calculated from paper data.
(c) Conversion Time=1/(2·BW$_{CH}$), BW$_{CH}$ is the single channel bandwidth.
(d) Energy Effi/Ch.=(Power/Ch.·Conversion Time)/(2^{ENOB}).

noise ($N_{S,F}$), comparator noise (N_{COMP}), and quantization noise (N_Q). In the noise model, the noise sources $N_{\text{INT},2}$, $N_{S,F}$, and N_{COMP} located at the same position as N_Q and then go through second-order noise-orthogonalizing in the proposed ADC. Consequently, all the four noise sources are suppressed by the noise-orthogonalizing technique in Fig. 10 and Table II. The output noise of the first-stage integrator only undergoes first-order noise-orthogonalizing while the thermal noise of the sampling switch cannot be shaped and directly affects the SNR of ADC.

C. Sensor Modulation and Current Source

Fig. 11 details the design of the current source and sensor modulation circuit. The chopper modulator is connected to a 7-bit current DAC and an R&C sensor pair, with an analog MUX to select different sensor pairs. The modulation signal is provided by the PDM signal (e.g., f_0). The cascade current mirror structure is adopted to enhance the output impedance of the current source. A 7-bit current DAC is employed to adapt to different sensor impedances. The standard current unit is replicated to maintain a good linearity, where transistor matching is considered during the layout design. To ensure an adequate voltage headroom, the current can be tuned via the SPI.

IV. EXPERIMENTAL RESULTS

The chip is fabricated by a 65-nm CMOS process, and the die micrograph is shown in Fig. 12(a). The core circuits take a die area of 3.09 mm^2. Based on the chip, a PCB prototype with 36 temperature sensors (thermistor) and 36 proximity sensors is designed. As shown in Fig. 12(b), the chip is mounted on the backside of the PCB. The data output by the chip is then collected and processed by an FPGA. A heating gun is used to demonstrate the response of temperature sensors, and the proximity sensors are tested by touching the pixel array with fingers. The nominal values for the thermistor and proximity sensor are 100 kΩ and 40 pF, respectively. The thermistor presents a $B_{25/85}$ value of 4100 K, and its resistance ranges from 50 to 100 kΩ versus heating. In addition, the capacitance of the proximity sensor is increased by the finger touch, resulting in a total capacitance range of 40–80 pF.

A. Electrical Measurements

Fig. 13 shows the measured spectrums of the noise-orthogonalizing PDM and ADC. It can be seen

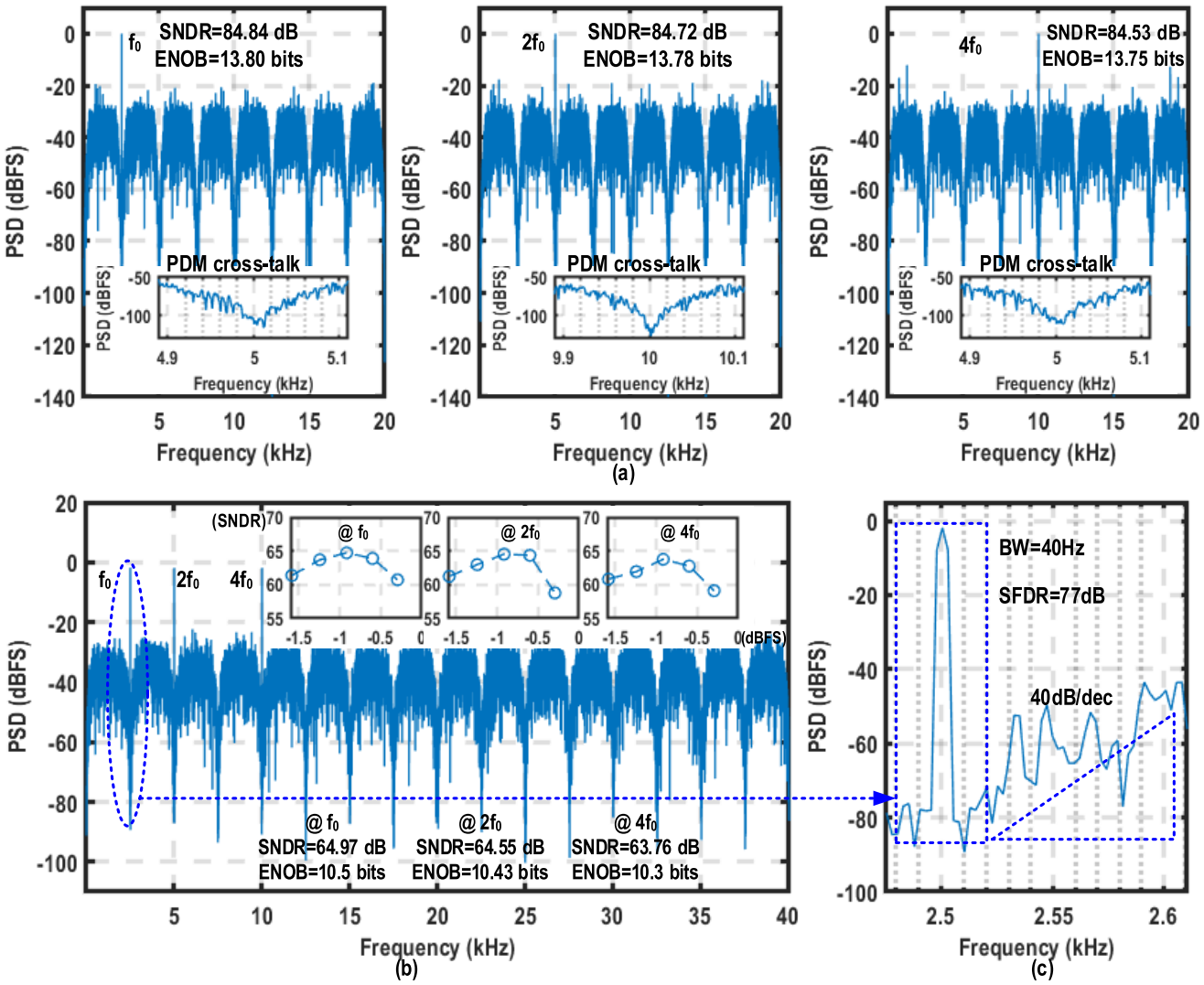

Fig. 13. PDM and ADC measurement results (32 768 point FFT). (a) PDM spectrums at f_0, $2f_0$, and $4f_0$. (b) ADC spectrum. (c) Zoomed-in ADC spectrum.

that the stimulation frequency components (f_0, $2f_0$, and $4f_0$) are located at the zero points of the PDM NTF. The stimulated signals of R and C sensors are merged and then quantized by the noise-orthogonalizing ADC, which has the same NTF zeros as the PDM NTF. The power spectral density (PSD) of noise decreases in a second-order way toward the stimulation frequencies. For a signal bandwidth of 40 Hz, the measured signal-to-noise-and-distortion ratio (SNDR) of PDM at f_0, $2f_0$, and $4f_0$ is 84.84, 84.72, and 84.53 dB, where the measured SNDR of ADC is 64.97, 64.55, and 63.76 dB, respectively. The PDM spectrum is obtained through the bit-stream pattern collected by data sampling of FPGA. Due to the all-digital implementation, the PDM is immune to nonideal factors, resulting in a PDM SNR close to the theoretical value. In comparison, the analog circuit implementation of the ADC is susceptible to various nonideal factors and thermal noise, which limits the system SNR. As the proposed noise-orthogonalizing technique uses single-bit ADC instead of a multibit quantizer, a high spurious-free dynamic range (SFDR) of 77 dB is achieved in the measurement. Our ADC performs an automatic resetting after each period of 32 768 sampling cycles, limiting the maximum number of sampling points to 32 768. As a result, the values of SNDR, ENOB, and SFDR are obtained by 16 FFT points.

The linearity measurement of R&C sensing is conducted in multiple chip samples. As shown in Fig. 14(a) and (b), the measurement of five samples demonstrates that the proposed chip can support R sensors up to 910 kΩ and C sensors up to 1 nF. In addition, the chip achieves $R^2 \geq 0.9994$ and $R^2 \geq 0.998$ for $R \leq 430$ kΩ and $C \leq 1$ nF sensors. The linearity of R sensing decreases when the resistor under test exceeds 430 kΩ, which is caused by the limited output resistance of the current source. This output resistance also results in the ENOB reduction of R compared to that of C. Gain/offset calibration is performed for different chips, adapting to the variations in the actual excitation current. All R and C results are measured when the R and C devices are connected simultaneously. The reduction in signal amplitude induced by the parallel connection of R&C can be compensated by the

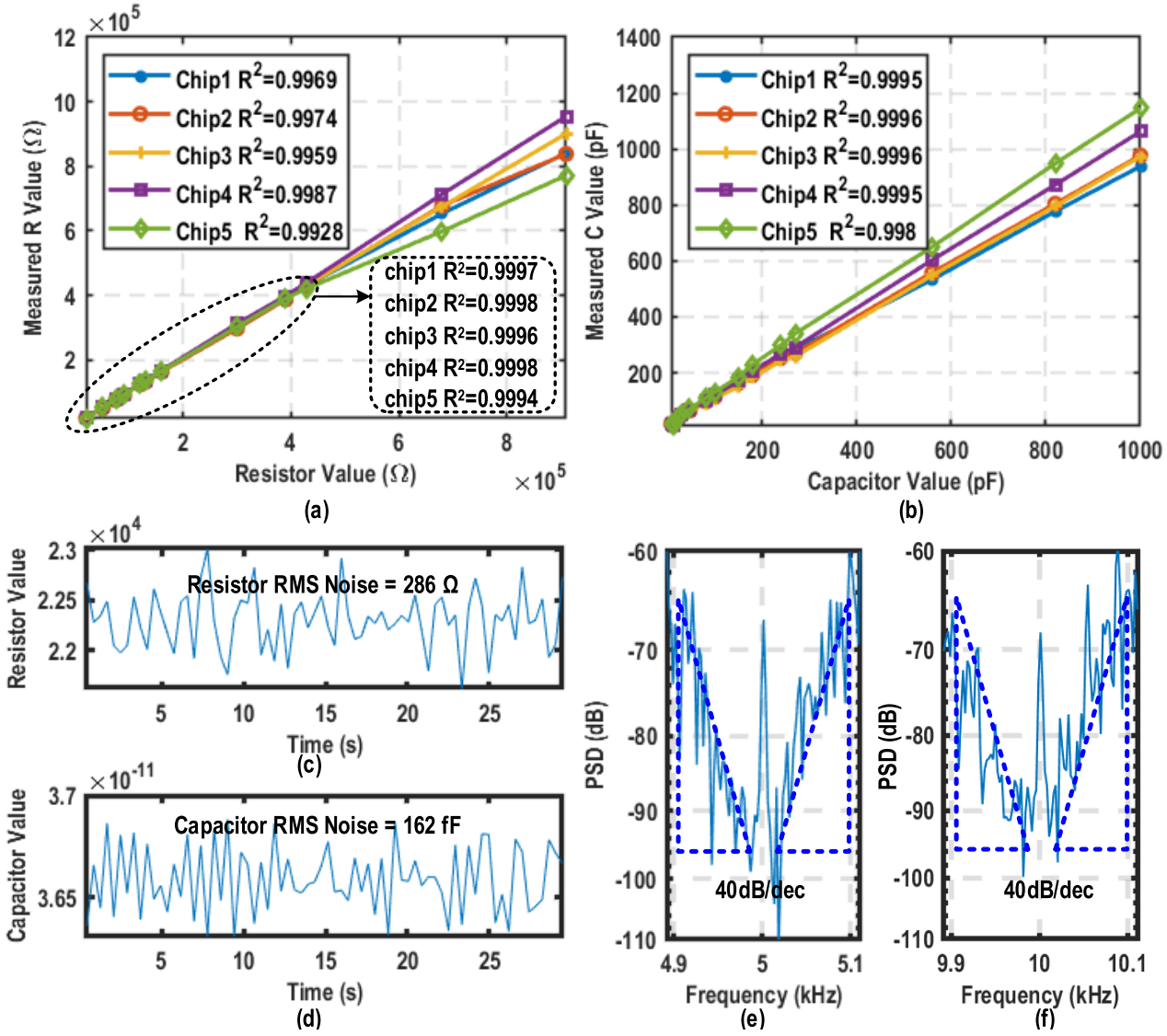

Fig. 14. Measurement results of (a) resistor sensing, (b) capacitor sensing, (c) resistor rms noise, (d) capacitor rms noise, (e) ADC crosstalk at $2f_0$, and (f) ADC crosstalk at $4f_0$.

programmable excitation current. The current setting for the maximal resistance and capacitance is 1 μA, which can be programmed through SPI based on the sensor impedance, with the maximal value of 12.7 μA. The parasitic capacitance of the R sensor can be calibrated as the baseline. The measured root-mean-square (rms) noise for R and C is 286 Ω and 162 fF, respectively, as given in Fig. 14(c) and (d). The measured PDM crosstalk remains below −90 dB as shown in Fig. 13. When the stimulation frequency is set to f_0, the measured ADC crosstalk at $2f_0$ and $4f_0$ is as low as −66.7 and −68.1 dB, respectively [see Fig. 14(e) and (f)]. As a result, the system-level crosstalk is primarily limited by the performance of the ADC.

B. Sensor-Array Demonstration

The performance of the temperature sensor array and proximity sensor array is demonstrated in Fig. 15. Without heating or finger touching, the R and C units in the pixel arrays are nearly identical, as shown in Fig. 15(a) and (b). As the pixel array composed of negative-temperature-coefficient (NTC) thermistor units is heated, part of the R units is changed in Fig. 15(c). In addition, the proximity sensor array can also reflect the finger-touching region, as shown in Fig. 15(d). In this way, the temperature sensor array can be used in bio-impedance imaging applications [23], [24], and the proximity sensor array can work as a touchscreen [25].

In Table III, the experimental results are summarized and compared with the state-of-the-art sensor-interface chips. It shows that: 1) the proposed noise-orthogonalizing technique reduces the power and conversion energy to 0.74 μW/Channel and 19.1 pJ/step and 2) the proposed pad-sharing technique cuts the pad number by 1/2, resulting in the high density of 0.038 mm^2/Channel and the maximal channel number of 72. The proposed noise-orthogonalizing technique realizes a small chip area per channel and provides a new design concept for ADCs.

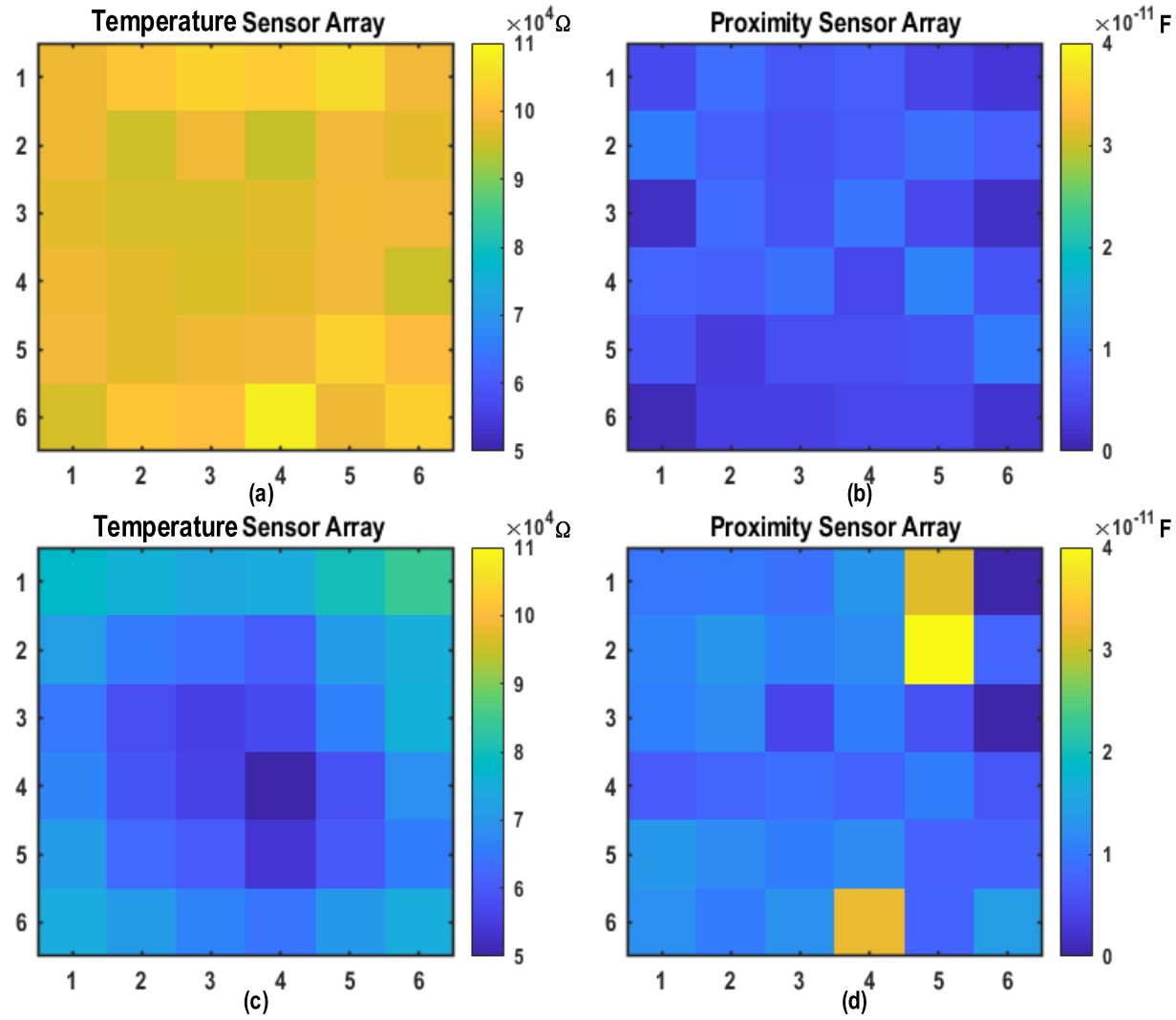

Fig. 15. Prototype demonstration. (a) Temperature sensor array (no heating). (b) Proximity sensor array (no touching). (c) Temperature sensor array (heating in the middle part). (d) Proximity sensor array (finger touching on three pixels).

V. Conclusion

In various IoT applications, long-term monitoring of multiple parameters (such as temperature, pressure, humidity, and proximity) requires a large amount of low-power R&C sensors integrated with numerous channels. Conventional multichannel structures of sensor-interface chips suffer from power-hungry noise-shaping and multiplexing circuits as well as a large pad frame. In this work, a 53-μW 72-channel R&C sensor-interface chip prototype is demonstrated for proximity and temperature sensing. The proposed techniques have addressed the issues presented in conventional multichannel sensor-interface chips: 1) the noise-orthogonalizing technique enables the chip to achieve the lowest power (0.74 μW/Channel) and 2) the pad-sharing technique reduces the chip area to 0.038 mm^2/Channel, offering one of the smallest designs in the state of the arts.

Appendix

At an ADC sampling frequency of f_S, the SQNR can be derived as below

$$\mathrm{NTF} = (1 - z^{-N})^2 \tag{7}$$

$$|\mathrm{NTF}| = 4\left(\sin\left(\frac{f \cdot N \cdot \pi}{f_S}\right)\right)^2. \tag{8}$$

The quantization noise in each sideband f_B (IBQN) can be expressed by

$$\begin{aligned}\mathrm{IBQN} &= \frac{\Delta^2}{12 f_S} \cdot \int_{i\cdot f_0 - f_B}^{i\cdot f_0 + f_B} |\mathrm{NTF}|^2 \, df \\ &= \frac{4\Delta^2}{3 f_S} \cdot \int_{i\cdot f_0 - f_B}^{i\cdot f_0 + f_B} \left(\sin\left(\frac{f \cdot N \cdot \pi}{f_S}\right)\right)^4 df, \quad i = 1, 2, 4.\end{aligned} \tag{9}$$

Due to the relationship of

$$f_0 \cdot N = f_S \;\&\; f_B \ll f_0 \tag{10}$$

we can have

$$\begin{aligned}\mathrm{IBQN} &\approx \frac{4\Delta^2}{3 f_S} \cdot \int_{-f_B}^{f_B} \left(\frac{f \cdot \pi}{f_0}\right)^4 df \\ &= \frac{\pi^4 \cdot N^4 \cdot \Delta^2}{60 \cdot M^5}\end{aligned} \tag{11}$$

where

$$M = \frac{f_S}{2f_B}. \tag{12}$$

As the signal power is $\Delta^2/8$, the SQNR of proposed noise-orthogonalizing system is

$$\text{SQNR} = \frac{15M^5}{2\pi^4 N^4}. \tag{13}$$

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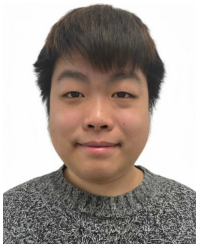
Xiangdong Feng (Graduate Student Member, IEEE) received the B.S. degree in electronic science and technology from Zhejiang University, Hangzhou, China, in 2020, where he is currently pursuing the Ph.D. degree in electronic science and technology with the School of Micro-Nano Electronics.

His research interests include analog/mixed-signal IC design and biomedical.

Yuxuan Luo (Senior Member, IEEE) received the B.Eng. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2014, and the Ph.D. degree from the National University of Singapore, Singapore, in 2018.

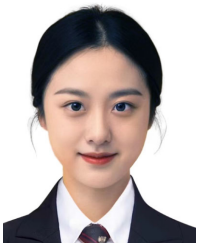
From 2018 to 2020, he was a Research Fellow with the National University of Singapore. He is currently a Faculty Member with the School of Micro-Nanoelectronics, Zhejiang University, Hangzhou, China. His current research interests include sensing circuits and systems.

Dr. Luo serves as a Technical Program Committee Member of the IEEE International Conference on Integrated Circuits, Technologies, and Applications (ICTA), a Sub-Track Chair for the 2022 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), and a Guest Editor for *Frontiers in Nanotechnology*. He was a recipient of the 2018 Institution of Engineers, Singapore (IES) Prestigious Engineering Award.



Tianyi Cai received the B.S. degree in electronic science and technology from Zhejiang University, Hangzhou, China, in 2021, where he is currently pursuing the Ph.D. degree in electronic science and technology with the School of Micro-Nano Electronics.

His current research interests include analog and mixed-signal CMOS integrated circuits and sensor interface circuit design.



Yangfan Xuan received the B.S. degree in microelectronic science and technology from Zhejiang University, Hangzhou, China, in 2021, where she is currently pursuing the M.Sc. degree in integrated circuit engineering.

Her current research interests include analog/mixed-signal IC design, biomedical sensor interface, and wireless power/data transmission circuit design for implantable medical devices.

Yunshan Zhang (Student Member, IEEE) received the B.S. degree in measurement and control technology and instruments from the Anhui University of Technology University, Ma'anshan, China, in 2017, and the Ph.D. degree in electronic science and technology from Zhejiang University, Hangzhou, China, in 2023.

Her research interests include analog/mixed-signal IC design and wireless power/data transmission circuit design for biomedical applications.

Yili Shen received the B.Eng. degree in microelectronic science and technology from Zhejiang University, Hangzhou, China, in 2021, where he is currently pursuing the Ph.D. degree in electronic science and technology.

His current research interests include analog/mixed-signal IC design, biomedical sensor interface, and wireless power/data transmission circuit design for implantable medical devices.

Changgui Yang (Student Member, IEEE) received the B.S. degree from the College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou, China, in 2019, where he is currently pursuing the Ph.D. degree in electronic science and technology.

His current research interests include analog/mixed-signal IC design, biomedical sensor interface, and wireless power/data transmission circuit design for implantable medical devices.

Qijing Xiao (Student Member, IEEE) received the B.S. degree in communication engineering from the Wuhan University of Technology, Wuhan, China, in 2021. He is currently pursuing the master's degree in electronic science and technology with Zhejiang University, Hangzhou, China.

His research interests include IoT radios, analog IC design, and wireless power/data transmission circuit design.

Sijun Du (Senior Member, IEEE) received the B.Eng. degree (Hons.) in electrical engineering from University Pierre and Marie Curie (UPMC), Paris, France, in 2011, the M.Sc. degree (Hons.) in electrical and electronics engineering from the Imperial College London, London, U.K., in 2012, and the Ph.D. degree in electrical engineering from the University of Cambridge, Cambridge, U.K., in January 2018.

He was with the Laboratoire d'Informatique de Paris 6 (LIP6), University Pierre and Marie Curie, and then an IC Engineer in Shanghai, China, from 2012 to 2014. He was a Summer Engineer Intern at Qualcomm Technology Inc., San Diego, CA, USA, in 2016. He was a Visiting Scholar at the Department of Microelectronics, Fudan University, Shanghai, in 2018. He was a Post-Doctoral Researcher at the Berkeley Wireless Research Center (BWRC), Department of Electrical Engineering and Computer Sciences (EECS), University of California at Berkeley, Berkeley, CA, USA, from 2018 to 2020. In 2020, he joined the Department of Microelectronics, Delft University of Technology (TU Delft), Delft, The Netherlands, where he is currently an Assistant Professor. His current research interests include energy-efficient integrated circuits and systems, including power management integrated circuits (PMIC), energy harvesting, wireless power transfer, and dc/dc converters used in the Internet-of-Things (IoT) wireless sensors, wearable electronics, biomedical devices, and microrobots.

Bo Zhao (Senior Member, IEEE) received the Ph.D. degree from the Department of Electronic Engineering, Tsinghua University, Beijing, China, in 2011.

He was a Research Fellow with the National University of Singapore, Singapore, from 2013 to 2015. From 2015 to 2018, he was an Assistant Project Scientist with the Berkeley Wireless Research Center (BWRC), Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA, USA. Since 2018, he has been a Professor with the Institute of VLSI Design, Zhejiang University, Hangzhou, China. He has authored or coauthored more than 60 articles and book chapters. He holds more than 30 Chinese patents. His research interests include IoT radios, wireless power transfer, and wearable/implantable radios.

Dr. Zhao serves as a Committee Member of the IEEE/C/SM. He was a recipient of the 2017 IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS Darlington Best Paper Award and the Design Contest Award of the 2013 IEEE International Symposium on Low Power Electronics and Design. He was the Publication Chair for the 2016 IEEE Biomedical Circuits and Systems Conference. In 2022, he was elected to be the Chair-Elect of the Biomedical and Life Science Circuits and Systems Society. He serves as an Associate Editor for the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS.