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Original articles

A virtual bus parallel differential power processing configuration for photovoltaic applications

Afshin Nazer*, Patrizio Manganiello, Olindo Isabella

Delft University of Technology, Delft, Netherlands

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Abstract

Photovoltaic (PV) systems are often exposed to mismatch caused by partial shading, different mounting angles, dust accumulation, cell degradation, and so on. This paper proposes a novel parallel differential power processing (P-DPP) configuration to minimize mismatch-related losses among PV strings. The proposed configuration, called *PV to Virtual Bus P-DPP*, uses a virtual bus as an input for all P-DPP converters. Since the virtual bus voltage can be selected lower than the DC Bus voltage, components' voltage rating can be reduced. An essential feature of the proposed configuration is the ability of the converters to generate both positive and negative output voltage. Therefore, a bidirectional flyback converter connected to a bridgeless converter is proposed as the P-DPP converter. To find the MPP of each PV string, the Perturb and Observe (P&O) algorithm is implemented. Moreover, a proportional–integral feedback controller controls the virtual bus voltage through the central converter. The benefits of the proposed configuration are discussed, and the operation of the proposed structure is further verified through simulations with the software PLECS.

Keywords: Distributed Maximum Power Point Tracking; Differential Power Processing; Mismatch losses; Partial shading; Photovoltaic systems

1. Introduction

PV systems are conventionally installed as a centralized solution (Fig. 1(a)). In this scenario, a number of PV strings – each made of many series-connected PV modules – are parallel-connected and then hooked up to a central inverter [6]. Due to the series connection, the same current must pass through all the PV modules of a PV string. Moreover, all PV strings must work at the same voltage owing to their parallel connection. Thus, when the PV array is subject to non-uniform operating conditions, e.g. due to partial shading of some PV modules, it is not possible to make all PV modules operate at their maximum power point (MPP), and mismatch losses arise, reducing the PV system's energy yield. Alternative PV system configurations called Distributed Maximum Power Point Tracking (DMPPT) techniques have been proposed to reduce mismatch losses and maximize the overall energy yield. DMPPT techniques with different levels of granularity have been presented. From multi-string inverters [21], in which PV strings are controlled separately (Fig. 1(b)), to module-level DMPPT solutions such as Microinverters [2,10] (Fig. 1(c)), cascade inverters (Fig. 1(d)) [26], parallel and series DC–DC converters (Fig. 1(e)

* Corresponding author.
E-mail addresses: A.Nazer@tudelft.nl (A. Nazer), P.Manganiello@tudelft.nl (P. Manganiello), O.Isabella@tudelft.nl (O. Isabella).

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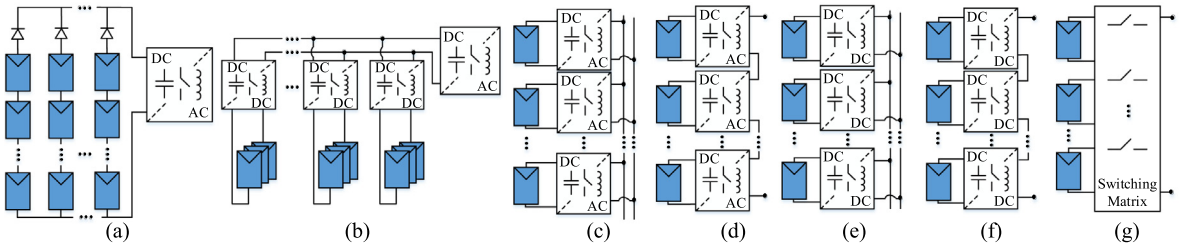

Fig. 1. PV system using: (a) Central inverter, (b) Multi-string inverter, (c) Microinverters, (d) Cascade inverters, (e) DC parallel optimizers, (f) DC series optimizer, and (g) PV reconfiguration.

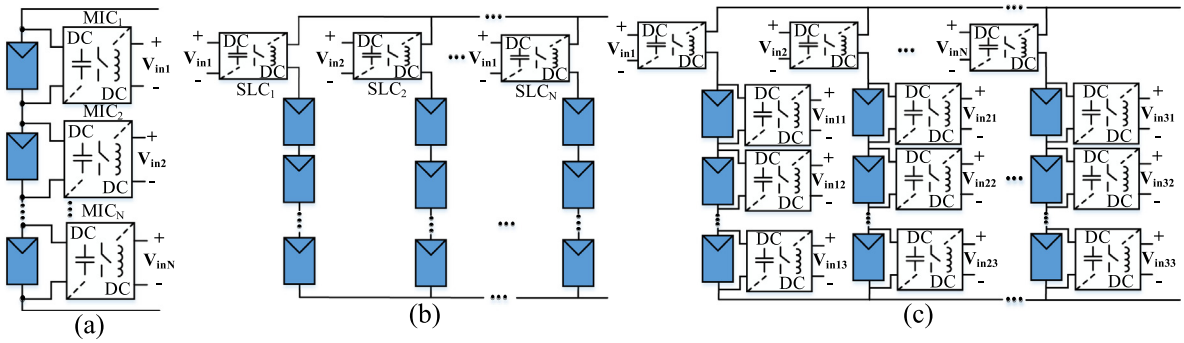

Fig. 2. PV systems using different differential power processing approaches: (a) series DPP, (b) parallel DPP, and (c) series–parallel DPP.

and (f), respectively) [1,14], reconfigurable PV modules (Fig. 1(g)) [3], and Differential Power Processing (DPP) (Fig. 2) [7,9,11–13,15–17,22,24,25,27].

Among these approaches, DPP has the advantage of only processing part of the power generated by PV modules, while the remaining part (ideally the majority) is directly delivered to the output. Thus, compared to the other solutions that process the full power, higher system efficiency is achieved even when the conversion efficiency of DPP converters is lower than that of Full Power Processing converters [23]. DPP configurations can be divided into three categories: series DPP (S-DPP) [7,22,25], parallel DPP (P-DPP) [9,11–13,24,27], and series–parallel DPP (SP-DPP) [15–17].

As shown in Fig. 2(a), S-DPP converters are usually applied as submodule/module integrated converters (SMIC/MIC) to inject or eject the required differential current between PV modules and PV string current. S-DPP architectures are categorized into: PV to PV (PV2PV) [25], PV to Bus (PV2B) [7], and PV to Virtual Bus (PV2VB) [22]. Although they remove mismatch losses among PV modules, it is not feasible to connect PV strings in parallel to achieve higher power [16]. On the other hand, P-DPP configurations as string level converters (SLC), shown in Fig. 2(b) provide the required differential voltage between PV strings and a common bus to eliminate mismatch losses among parallel-connected PV strings. P-DPP converters need lower components rating compared to conventional string inverters, reducing the cost of the system [27]. Therefore, they have the potential to replace multi-string structures for high-power applications. However, for applications in which module level DMPPT is required, P-DPP configurations are unable to remove mismatch losses among PV modules. To solve this problem, SP-DPP architectures (Fig. 2(c)) can be employed that are able to mitigate mismatch losses among both PV strings *and* PV modules with high conversion efficiency [15–17]. Note that SLCs refer to P-DPP converters in the rest of this paper.

This paper focuses on P-DPP configurations which can be an independent PV system or a part of an SP-DPP PV system. In this respect, PV2B solutions have been proposed in the literature so far [9,11–13,24,27]. One important challenge when designing PV2B P-DPP converters as SLCs is the high voltage step-up ratio from the Bus to the PV side. Moreover, the DC Bus-side switches of the P-DPP converters need to withstand high voltage stress, increasing the power loss and cost. To solve these problems, this paper introduces a novel PV2VB structure for P-DPP. It allows reducing components voltage rating and eliminates the need for high voltage gain at the expense of using

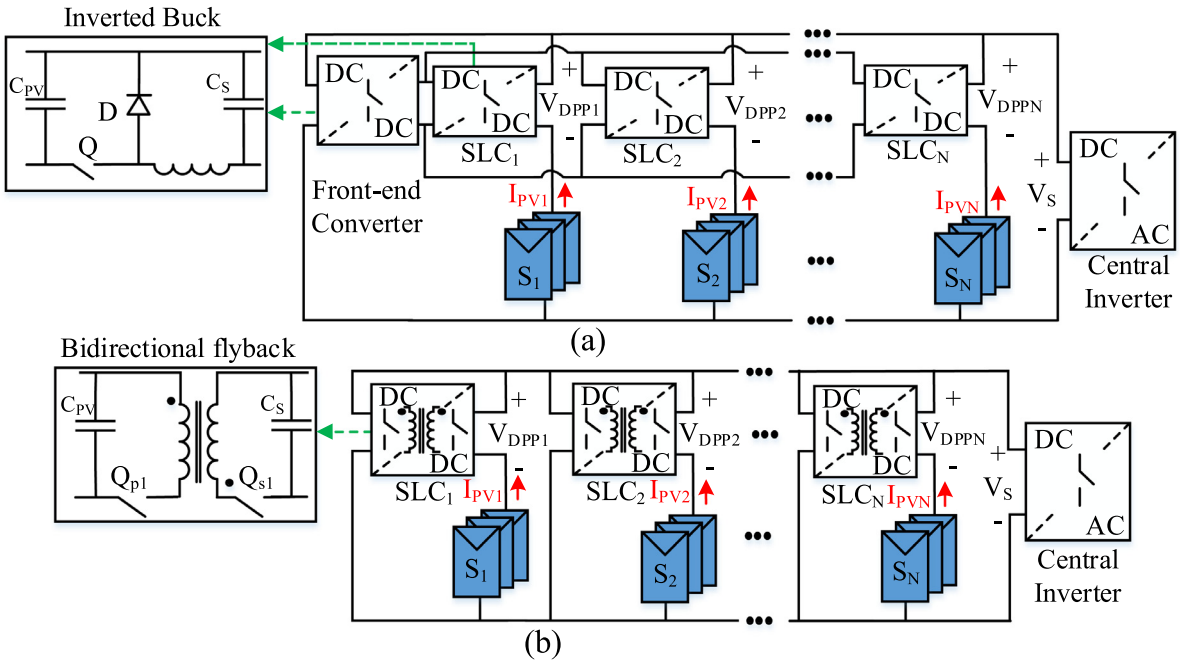

Fig. 3. PV2B P-DPP configurations. (a) With front-end converter (b) Direct connection approach.

high capacitance capacitors at the Virtual Bus. These capacitors are crucial to enable transfer of energy among PV strings.

The rest of the paper is organized as follows: Sections 2 and 3 describe PV2B and the proposed PV2VB P-DPP configurations and their mathematical model in steady state, respectively. The operation of the proposed configuration, including central and DPP converters, is discussed in detail in Section 4. Finally, simulation results are reported in Section 5 to demonstrate the feasibility of the proposed configuration. A conclusion section ends the paper.

2. PV2B P-DPP configuration analysis

In PV2B configurations, such as the ones shown in Fig. 3, the output voltage of the jth P-DPP converter (v_{DPPj}) can be expressed as:

$$v_{DPPj} = v_S - v_{PVj} \tag{2.1}$$

where v_S, and v_{PVj} represent common DC bus and jth PV string voltage, respectively. Furthermore, the input of each P-DPP converter is connected to the DC Bus (Fig. 3); therefore, the relationship between the common DC bus voltage and the output voltage of the jth P-DPP converter is

$$v_{DPPj} = k_j \times v_S \tag{2.2}$$

where k_j is the voltage gain of the jth P-DPP converter.

There are two main categories for the PV2B P-DPP configuration [9,11–13,24,27]: connection with a front-end converter (Fig. 3(a)), and direct connection (Fig. 3(b)). The front-end converter aims to step down the DC Bus voltage so that the SLCs require a smaller conversion ratio. This configuration allows using highly efficient and small-size buck converters. However, the front-end converter must process the power processed by all SLCs, which decrease the overall system's efficiency. In the direct connection approach, the SLCs are directly connected to the DC Bus. This configuration does not allow to use all converter topologies as SLCs. For instance, if an inverted buck is used, the current through the components is equal to the PV string current, and the voltage they must

tolerate is equal to the DC Bus voltage. Thus, it will be processing full power. A suitable SLC's topology for this configuration is the flyback converter, whose primary side will operate under PV string current and differential voltage, while the secondary side operates at DC link voltage and differential current. Besides, flyback converter in direct connection configuration allows to avoid extremely low duty cycles by leveraging the transformer's turn ratio. When direct connection is considered and flyback converters are used, the converter voltage gain (K_j) in steady-state is

$$K_j = \frac{n_2}{n_1} \times \frac{D_j}{1 - D_j} \tag{2.3}$$

where D_j is duty cycle of the jth DPP converter, and $\frac{n_2}{n_1}$ represents the transformer's turn ratio.

By combining (2.1)–(2.3), V_{DPPj} is obtained as

$$V_{DPPj} = \frac{K_j}{1 - K_j} \times V_{PVj} \tag{2.4}$$

In Eq. (2.4) and in the rest of the manuscript, capital letters are used to indicate the DC component of the variables. The system in steady-state can be described in a matrix form as:

$$\begin{bmatrix} \frac{1-K_1}{K_1} & 0 & \dots & 0 & 0 \\ 0 & \frac{1-K_2}{K_2} & \dots & 0 & 0 \\ \vdots & \vdots & \dots & \vdots & \vdots \\ 0 & 0 & \dots & \frac{1-K_{(N-1)}}{K_{(N-1)}} & 0 \\ 0 & 0 & \dots & 0 & \frac{1-K_N}{K_N} \end{bmatrix} \begin{bmatrix} V_{DPP1} \\ V_{DPP2} \\ \vdots \\ V_{DPP(N-1)} \\ V_{DPPN} \end{bmatrix} = \begin{bmatrix} V_{PV1} \\ V_{PV2} \\ \vdots \\ V_{PV(N-1)} \\ V_{PVN} \end{bmatrix} \tag{2.5}$$

With the final goal of maximizing the power extracted from each PV string, the output voltage of each P-DPP converter (V_{DPPj}) and the DC bus voltage (V_S) are considered as control actuators, whereas PV string voltage (V_{PVj}) represents the control objectives. Consequently, there are N control objectives and N + 1 control actuators so each PV string can be operated at its MPP by setting appropriate duty cycle for the N P-DPP converters. The extra degree of freedom stemming from the central converter helps to minimize power losses by adjusting V_S. It is worth to mention that, to the best of the authors' knowledge, only converters generating positive output voltage have been proposed for PV2B P-DPP so far [8,11–13,24,27]. However, if they only generate positive output voltage, the DC bus voltage must always be higher than the highest PV strings voltage. Ideally, the DC bus voltage should be equal to the highest actual MPP string voltage. This assumption allows minimization of the processed power, but it may be difficult to realize since some P-DPP converters must work at extremely low duty ratio under this assumption. To overcome this issue, DC Bus voltage must be increased, but the processed power will dramatically increase [11]. Hence, despite the extra degree of freedom, power processing optimization will not be exploited at its best due to the lack of appropriate P-DPP converters. Together with the other advantages mentioned in the introduction, this is an additional reason to study PV2VB P-DPP as an alternative to conventional PV2B P-DPP.

3. Proposed PV2VB P-DPP configuration

As shown in Fig. 4, in PV2VB P-DPP configurations, the P-DPP converters input is connected to a common isolated DC bus, called Virtual Bus. While strong PV strings, which are the strings that produce more power, inject energy to the Virtual Bus through the converters, weak PV strings draw energy from it.

The relationship between the output voltage (v_{DPPj}) of the jth P-DPP converter and the Virtual Bus voltage (v_{VB}) is

$$v_{DPPj} = k_j \times v_{VB} \tag{3.1}$$

where k_j is the voltage gain of the jth P-DPP converter.

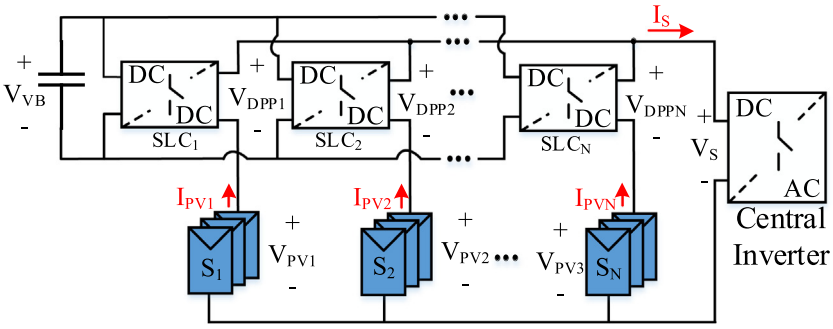

Fig. 4. Proposed PV2VB P-DPP configuration.

The output voltage of the jth P-DPP converter can be also expressed as:

$$v_{DPPj} = v_S - v_{PVj} \tag{3.2}$$

where v_{PVj} and v_S are the jth PV string's voltage and the DC bus voltage, respectively.

For proper operation, a power balance is needed at the Virtual Bus to avoid fluctuation of Virtual Bus voltage. Therefore, in addition to finding the MPP of all PV strings, the Virtual Bus power must be controlled. In (3.3), the instantaneous power relationship for the PV2VB structure is presented. For simplicity, the converter efficiency is not considered in the equation:

$$p_{VB} = p_{IN} - p_{OUT} = C_{VB} \times v_{VB} \times \frac{dv_{VB}}{dt} \tag{3.3}$$

where C_{VB} is Virtual Bus capacitance, p_{VB} is its power, p_{IN} the power generated by PV strings calculated as:

$$p_{IN} = \sum_{j=1}^{N} v_{PVj} \times i_{PVj} \tag{3.4}$$

and p_{OUT} is the system's output power:

$$p_{OUT} = v_S \times i_S, \qquad i_S = \sum_{j=1}^{N} i_{PVj} \tag{3.5}$$

where, i_S and v_S represent the DC Bus current and voltage, respectively. By substituting (3.4) and (3.5) in (3.3), Eq. (3.6) is derived:

$$p_{VB} = \sum_{j=1}^{N} v_{PVj} \times i_{PVj} - v_S \times i_S = C_{VB} \times v_{VB} \times \frac{dv_{VB}}{dt} \tag{3.6}$$

From Eq. (3.6) it can be seen that, if virtual bus power (p_{VB}) is positive, then $\frac{dv_{VB}}{dt}$ will be positive, which means the virtual bus voltage is being increased, and vice versa. It may seem that there are many actuators to control virtual bus power. However, PV strings voltages are controlled by P-DPP converters, their currents (i_{PVj}) depend on their voltages and their corresponding I–V curve, and DC Bus current (i_S) equals the sum of the PV strings' currents. Hence, the only variable that can be used to control virtual bus power and thus virtual bus voltage (v_{VB}) is the DC Bus voltage (v_S).

By substituting (3.2) into (3.6), in steady state we have:

$$P_{VB} = \sum_{j=1}^{N} V_{DPPj} \times I_{PVj} = 0 \tag{3.7}$$

It is concluded from (3.7) that to have constant Virtual Bus voltage in steady-state, the Virtual Bus average power (P_{VB}) must be zero. To achieve this, since I_{PVj} is always positive, the output voltage of some of the P-DPPs must be negative while it must be positive for other P-DPPs.

The system in steady-state can be described in matrix form as:

$$\begin{bmatrix} 1 & 0 & \dots & 0 & 0 & -1 \\ 0 & 1 & \dots & 0 & 0 & -1 \\ \vdots & \vdots & \dots & \vdots & \vdots & \vdots \\ 0 & 0 & \dots & 1 & 0 & -1 \\ 0 & 0 & \dots & 0 & 1 & -1 \\ I_{PV1} & I_{PV2} & \dots & I_{PV(N-1)} & I_{PVN} & 0 \end{bmatrix} \begin{bmatrix} V_{DPP1} \\ V_{DPP2} \\ \vdots \\ V_{DPP(N-1)} \\ V_{DPPN} \\ V_S \end{bmatrix} = \begin{bmatrix} V_{PV1} \\ V_{PV2} \\ \vdots \\ V_{PV(N-1)} \\ V_{PVN} \\ P_{VB} = 0 \end{bmatrix} \tag{3.8}$$

In PV2VB P-DPP, the output voltage of each P-DPP converter (V_{DPPi}) and the DC bus voltage (V_S) are considered as control actuators. On the other hand, PV string voltage (V_{PVi}), and Virtual Bus power (P_{VB}) are the control objectives. Consequently, there are $N+1$ control objectives and $N+1$ control actuators, so that it is possible to make each PV string work at its MPP while controlling the Virtual Bus.

From control perspective, the proposed structure loses the extra degree of freedom which PV2B P-DPP has. However, since the configuration allows designer to define the voltage of virtual bus, it provides an extra degree of freedom to optimize cost, losses, and ratings of the P-DPP converters. High Virtual Bus voltage reduces both the required Virtual Bus capacitance, because the maximum allowable voltage ripple is increased [10], and the conduction losses of the DPP converters by reducing their current. However, high Virtual Bus voltage requires semiconductor devices with higher blocking voltage, which imposes extra costs and switching losses. The development of methodologies for the optimization of the virtual bus voltage represents future work and it is out of the scope of this paper.

4. Operation analysis of PV2VB

4.1. Central inverter

In a PV2VB P-DPP system, the DC–DC stage of the central inverter sets the DC bus voltage such that the virtual bus voltage is constant. In steady-state, (3.6) can be rewritten as below:

$$P_{VB} = V_S \times \sum_{j=1}^{N} I_{PVj} - \sum_{j=1}^{N} V_{PVj} \times I_{PVj} = 0 \tag{4.1}$$

Then:

$$V_S^* = \frac{\sum_{j=1}^{N} V_{PVj} \times I_{PVj}}{\sum_{j=1}^{N} I_{PVj}} = \frac{\sum_{j=1}^{N} V_{PVj} \times I_{PVj}}{I_S} \tag{4.2}$$

Eq. (4.2) allows the calculation of the specific DC bus voltage that makes the average power of Virtual Bus equal to zero, thus keeping constant the virtual bus voltage. This voltage is called the balancing DC Bus voltage (V_S^*). Considering Eq. (3.6), the following equation describing the instantaneous rate of change of virtual bus voltage as a function of bus voltage is obtained:

$$\frac{dv_{VB}}{dt} = \frac{\sum_{j=1}^{N} v_{PVj} \times i_{PVj}}{C_{VB} \times v_{VB}} \times \left(1 - \frac{v_S}{V_S^*}\right) \tag{4.3}$$

As demonstrated in Eq. (4.3), to increase the virtual bus voltage, the actual DC bus voltage must be lower than the balancing DC bus voltage. Equally, when the DC bus voltage is higher than V_S^*, the virtual bus voltage will decrease. For the DC–DC stage of central inverter, different topologies can be selected. As shown in Fig. 5, here a conventional boost converter is chosen as the DC–DC stage of central inverter, and the virtual bus is controlled by using proportional–integral (PI) feedback control.

4.2. P-DPP converters as SLCs

As explained in the previous section, P-DPP converters must be able to generate both positive and negative output voltage, and therefore to work in both I and IV quadrants of the V–I curve. Besides, the virtual bus is capacitive, so

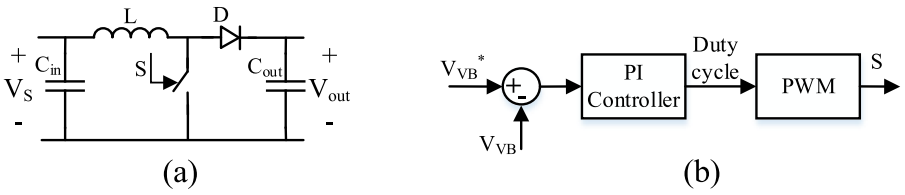

Fig. 5. DC–DC stage of the central inverter (a) Topology (b) Block diagram of the controller.

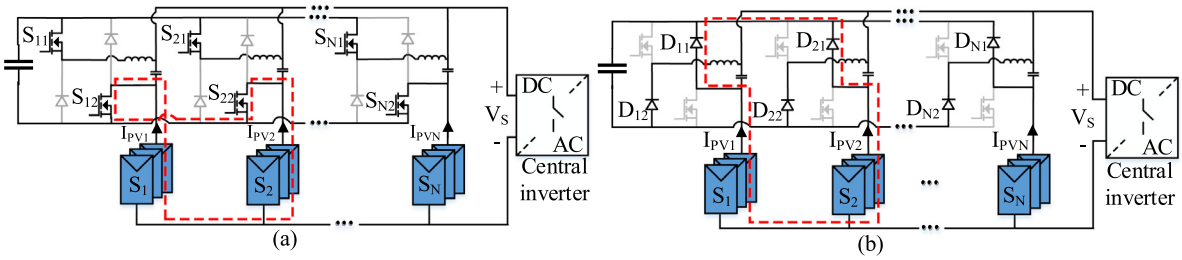

Fig. 6. PV2VB P-DPP configuration using non-isolated P-DPP converters. (a) Operation with all switches ON, and (b) operation with all switches OFF.

P-DPP converters must be voltage-source converters. Another critical requirement of P-DPP converters is isolation; otherwise, the configuration does not work properly. For instance, as shown in Fig. 6, if non-isolated bridgeless converters are used as P-DPP converters and the switches (Fig. 6(a)) or the diodes (Fig. 6(b)) of two P-DPP converters are ON at the same time, which will repeatedly happen, PV strings are then in parallel. Therefore, independent control of PV strings' voltage is unfeasible and DMPPT cannot be performed. In summary, the P-DPP converters in PV2VB P-DPP configuration must have the following characteristics: (i) being voltage-source converters, (ii) being able to work in both I and IV quadrants, (iii) being isolated. Fig. 7 shows the proposed two-stage P-DPP converter. The first stage is a Bidirectional Flyback Converter (BFC) with unit turn ratio (see Fig. 8), whereas the second stage is a Bridgeless Converter (BLC) (see Fig. 9).

The aim of BFC's control strategy is to keep the virtual bus voltage and BLCs input voltage identical [4]. Hence, a fixed duty cycle is used to control the switches in BFC. The relationship among the duty cycle (D_{BFC}), the input voltage (V_{VB}), and output voltage (V_B) of the Flyback is [4]:

$$V_{VB} = V_B \times \frac{D_{BFC}}{1 - D_{BFC}} \tag{4.4}$$

Furthermore, the inputs of all BFCs are connected in parallel. Then Eq. (4.3) can be written as follows [4]:

$$V_{VB} = V_{B1} \times \frac{D_{BFC}}{1 - D_{BFC}} = V_{B2} \times \frac{D_{BFC}}{1 - D_{BFC}} = \cdots = V_{BN} \times \frac{D_{BFC}}{1 - D_{BFC}} \tag{4.5}$$

where V_{Bj} is the input voltage of the jth BLC. Provided that D_{BFC} is equal to 0.5, all BLCs operate at the same input voltage, equal to the Virtual Bus voltage in the steady-state [4]:

$$V_{VB} = V_{B1} = V_{B2} = \cdots = V_{BN} \tag{4.6}$$

As revealed in Fig. 8, the power is transferred in both direction by the BFC converters. To transfer the energy from the Virtual Bus to BLCs input, the primary switch (Q_p) is controlled by conventional Constant Frequency Pulse-Width Modulation (CF-PWM). Meanwhile, the secondary switch Q_s is continuously off, and its built-in diode works as the Flyback diode. If the energy transfer direction is reversed, the operation of the converters is completely symmetrical. In this work, a simple and robust open-loop control is applied with no communication or sensing between PV strings, as done in [4].

Fig. 9 shows the second part of the P-DPP converter, which is the BLC. It can generate both negative and positive output voltage, which is necessary for the PV2VB structure to work properly. In this converter, switches are controlled by conventional CF-PWM, and the duty cycle D_B is given by P&O algorithm [18]. To calculate

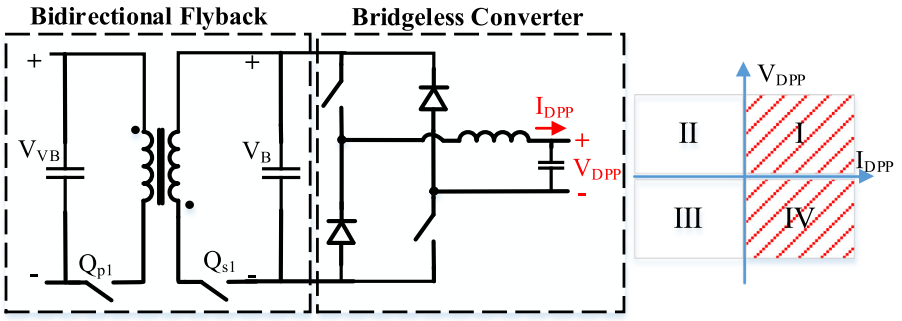

Fig. 7. Proposed two-stage P-DPP converter for PV2VB P-DPP configuration.

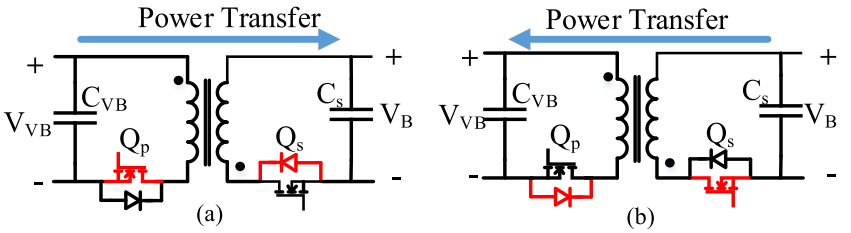

Fig. 8. BFC as the first stage of proposed P-DPP converter: Power Transfer (a) from the Virtual Bus to the PV string, and (b) from the PV string to the Virtual Bus.

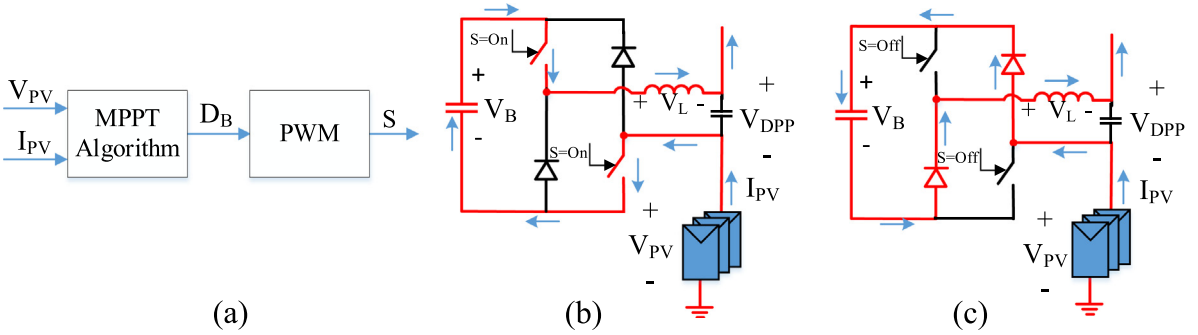

Fig. 9. BLC converter as the second stage of proposed P-DPP converter. (a) Controller block diagram, (b) operation during the on-state, and (c) operation during the off-state.

the relationship between the input and output voltage of the BLC, the volt-second balance can be applied to the inductor:

$$\int_0^{T_{sw}} V_L dt = 0 \Rightarrow (V_B - V_{DPP}) \cdot D_B \cdot T_{sw} + (-V_B - V_{DPP}) \cdot (1 - D_B) \cdot T_{sw} = 0 \tag{4.7}$$

that becomes:

$$V_{DPP} = (2 \cdot D_B - 1) \times V_B \tag{4.8}$$

where V_L, V_{DPP}, V_B, D_B and T_{SW} represent the inductor voltage, BLC output voltage, BLC input voltage, BLC duty cycle, and switching period, respectively.

As shown in Fig. 9, while the switches are on, the polarity of the voltage before the LC output filter is the same as the input voltage, and the BLC input capacitor is being discharged. On the other hand, when the switches are off the BLC inverts the input voltage, and its capacitor is being charged. To transfer average power from the input to

Table 1
Test cases for a PV system made of four strings, each consisting of nine series-connected PV modules. Numbers from 1 to 9 indicate PV modules in each string.

Case	PV string #1									PV string #2									PV string #3									PV string #4								
	1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9
I																																				
II																																				
III																																				

$1000\ \frac{w}{m^2}$; $750\ \frac{w}{m^2}$; $500\ \frac{w}{m^2}$; $100\ \frac{w}{m^2}$

the output, BLC duty cycle must be bigger than 0.5($D_{BLC} > 0.5$); otherwise, the average power direction is from the output to the input.

With respect to (4.2), DC Bus voltage must be set to a certain value, always between the highest PV string voltage and lowest PV string voltage to make the Virtual Bus voltage constant. The more irradiance a PV string receives, the higher its voltage, so the strong PV strings have higher voltage than the weaker ones, hence higher than the DC bus voltage. Therefore, their corresponding BLCs work at a duty cycle lower than 0.5, so they charge their capacitors. Similarly, the BLCs connected to the weaker PV strings discharge their capacitors.

4.3. Components

Unlike PV2VB, an important advantage of PV2B configurations is that they allow to use unidirectional converters in their structures. Therefore, compared to the unidirectional Flyback converter used for PV2B configuration, the number of components of PV2VB DPP converters is higher to enable bidirectionality. However, it does not mean that they are more costly. For instance, low blocking voltage semiconductors can be employed in PV2VB so not only does it help to reduce the cost of switches, but it also enables designers to use MOSFETs instead of IGBTs. MOSFETs work at higher frequency in comparison with IGBTs, which reduces the volume and cost of passive elements. Eventually, the PV2VB P-DPP structure eliminates the low duty ratio imposing higher eddy current loss in the core in PV2B P-DPP [20].

5. Simulation results

To investigate and verify both the PV2VB P-DPP PV system performance and its ability to properly control virtual bus voltage, dynamic simulations are set up in PLECS. In the simulation, four PV strings, consisting of nine series-connected PV modules, connected to four P-DPP converters switching at 100 kHz are considered. To simulate the PV strings, the model suggested by [5] is used for the PV arrays, and the open circuit voltage and short circuit current of each PV module are 91.5 V and 6.45 A [19], respectively. Besides, P&O algorithm having 0.005 duty cycle step size and 1 ms perturbation period is applied, and the sample time of PI controller of central converter is set to 5 ms. The capacitance and voltage of the Virtual Bus are set to 4 mF and 300 V, respectively.

Two shading scenarios are considered. The simulated irradiance conditions are summarized in Table 1. In the first scenario, the simulation run as follows. At first, all PV strings are working under uniform conditions (Case I in Table 1), which means all of them are receiving full illumination $\left(1000\ \frac{\mathrm{W}}{\mathrm{m}^2}\right)$. After 1 s, the irradiance conditions change from Case I to Case II. Namely, PV modules belonging to the PV string #1 receive different irradiance such that some of them are bypassed, leading to a higher difference between DC bus voltage and PV strings voltage. The other PV strings, PV string #2, PV string #3, and PV string #4, receive $750\ \frac{\mathrm{W}}{\mathrm{m}^2}$, $500\ \frac{\mathrm{W}}{\mathrm{m}^2}$, and $1000\ \frac{\mathrm{W}}{\mathrm{m}^2}$ irradiance, respectively. Figs. 10 and 11 show a comparison of the PV strings current and voltage with their actual MPP counterparts. All PV strings work at MPP both before and after applying partial shading. This demonstrates that the P&O MPPT algorithm implemented on P-DPP converters operates properly.

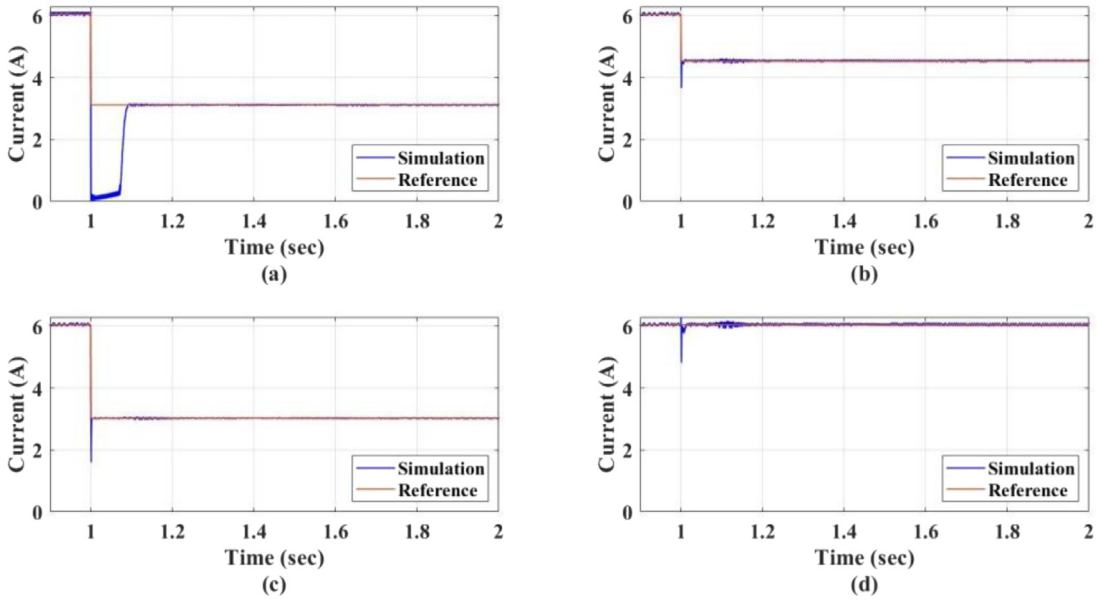

Fig. 10. PV string current, Case I → Case II: PV (a) string #1, (b) string #2, (c) string #3, and (d) string #4.

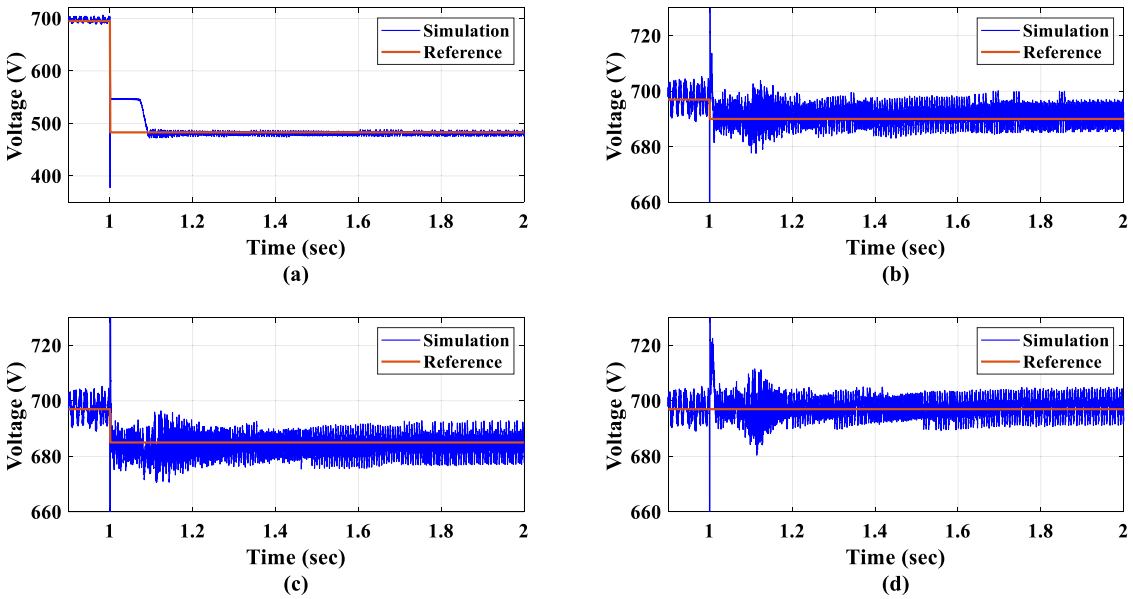

Fig. 11. PV string voltage, Case I → Case II: PV (a) string #1, (b) string #2, (c) string #3, and (d) string #4.

Fig. 12 shows the DC bus voltage and the virtual bus voltage before and after applying partial shading. As it is discussed in the previous sections, the central converter operates to set an appropriate constant voltage for the DC Bus. The reference for the DC Bus voltage in Fig. 12(a) is calculated using (4.2). Fig. 12(b) confirms that, owing to the operation of the PI controller, the virtual bus voltage reaches its steady-state in less than 1 s after partial shading.

In the second scenario, at second 2.5, the irradiance conditions change from Case II to Case III. Namely, PV modules belonging to the PV string #1 again receive uniform irradiance, whereas the irradiance of PV string #2, PV string #3, and PV string #4, remains 750 $\frac{\text{W}}{\text{m}^2}$, 500 $\frac{\text{W}}{\text{m}^2}$, and 1000 $\frac{\text{W}}{\text{m}^2}$, respectively. As shown in Figs. 13 and 14,

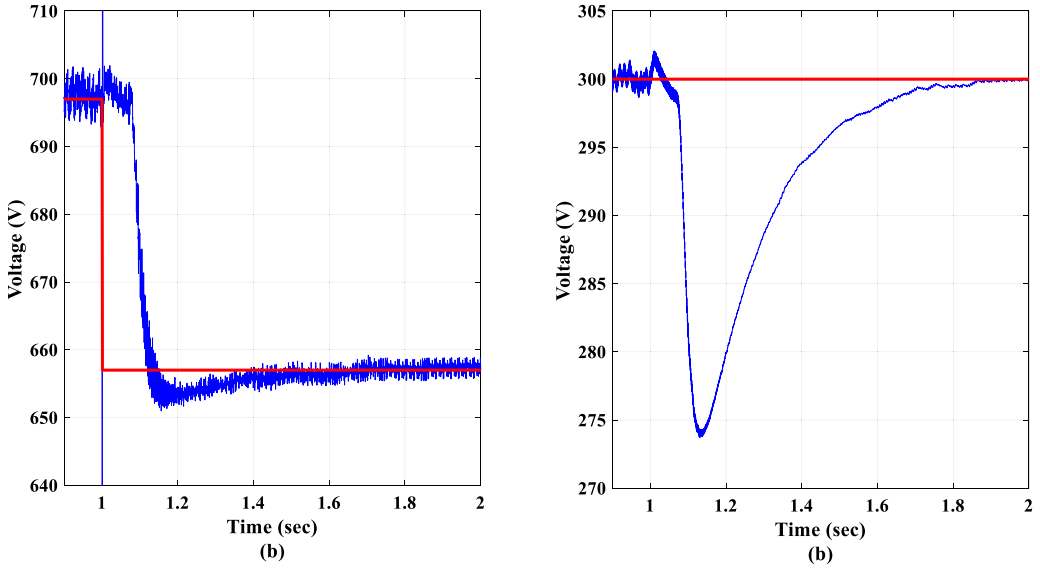

Fig. 12. Dynamic performance of central controller, Case I → Case II: (a) DC Bus voltage, and (b) Virtual Bus voltage.

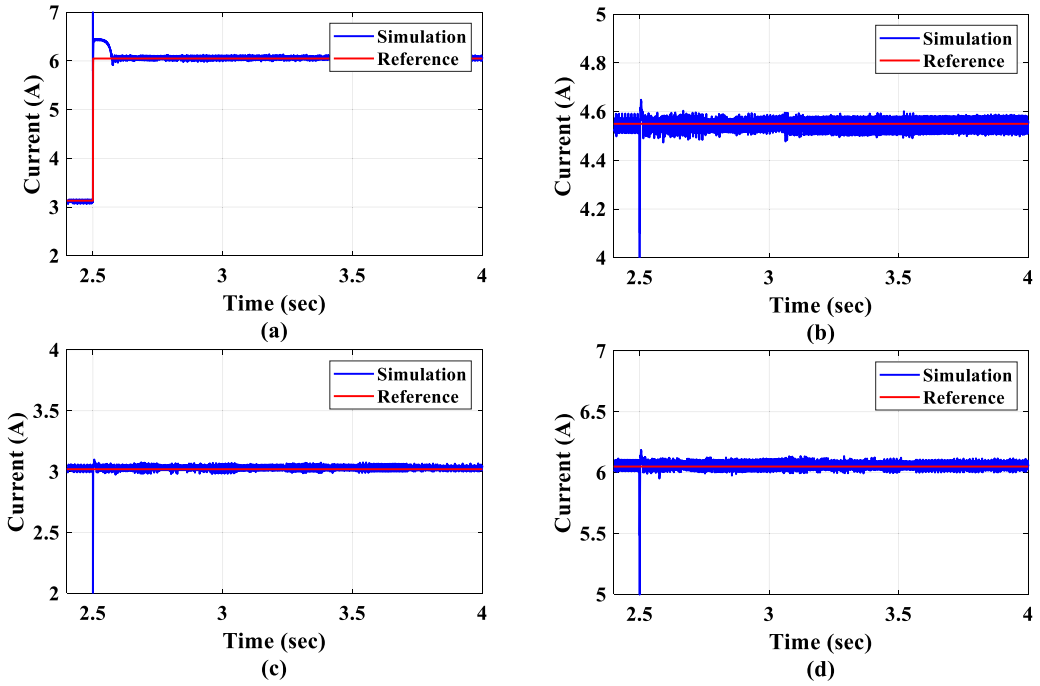

Fig. 13. PV string current, Case II → Case III: PV (a) string #1, (b) string #2, (c) string #3, and (d) string #4.

P-DPP converters make all PV strings work at their new MPP. Moreover, Fig. 15 shows that the virtual bus voltage reaches its steady-state after the perturbation within 1.5 s, and the PI controller adapts the DC voltage to maintain a fixed virtual bus voltage.

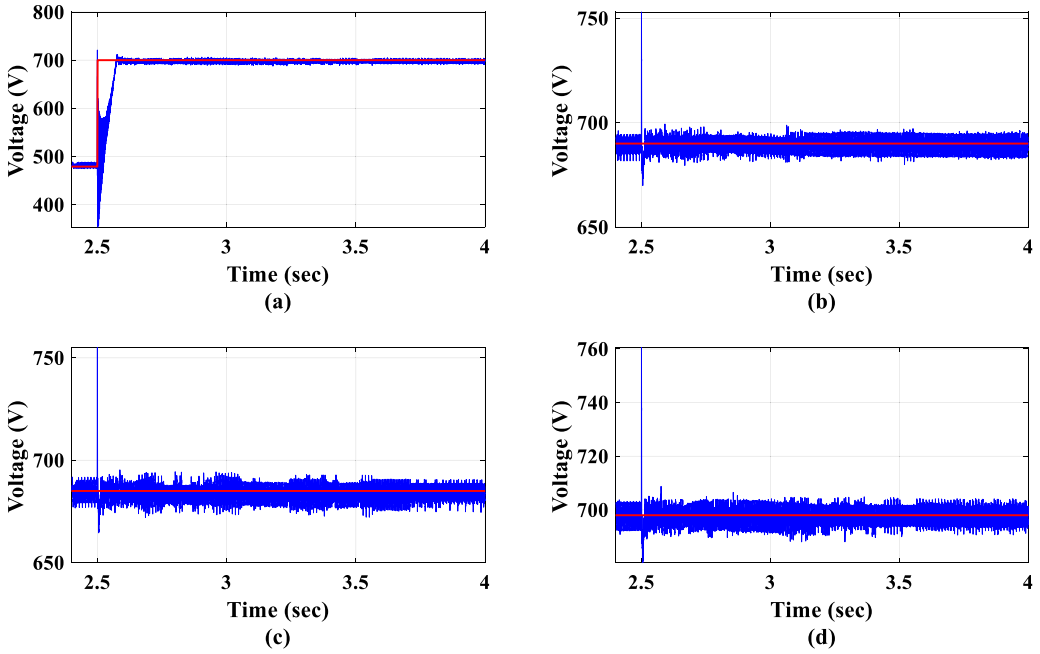

Fig. 14. PV string voltage, Case II → Case III: PV (a) string #1, (b) string #2, (c) string #3, and (d) string #4.

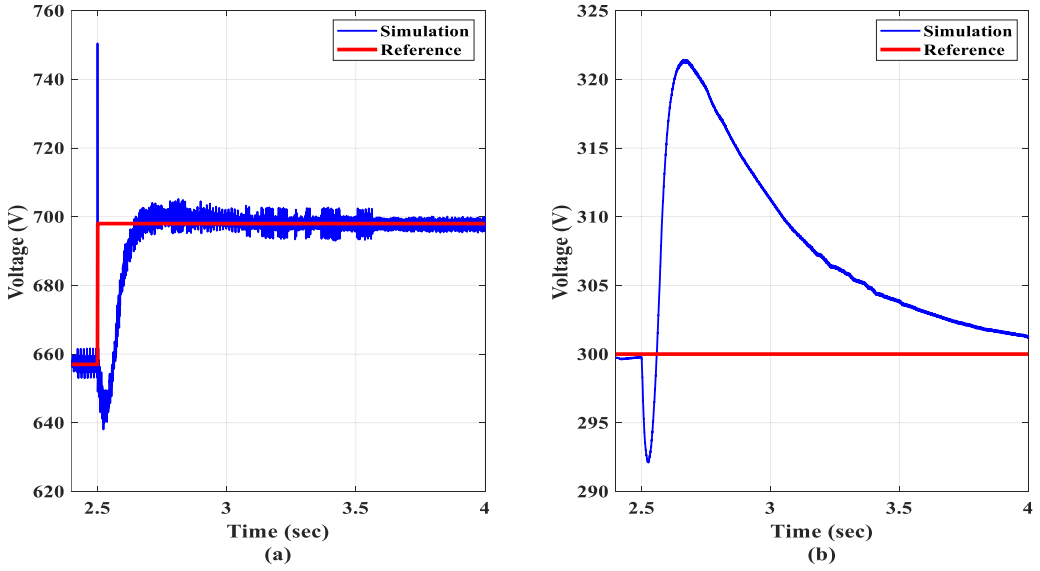

Fig. 15. Dynamic performance of central controller, Case II → Case III: (a) DC Bus, and (b) Virtual Bus voltage.

6. Conclusion

This paper proposes a PV2VB P-DPP PV system to mitigate mismatch losses among PV strings. By mathematical modeling, it is demonstrated that the configuration needs bidirectional converters which generate both positive and negative output voltage. This is obtained by means of a BFC connected to a BLC. In comparison with conventional PV2B P-DPP, the proposed P-DPP configuration allows for the employment of components with lower voltage ratings and may reduce the volume of passive components. The operation of the proposed configuration has been confirmed through dynamic simulations. In the simulation, a P&O algorithm with 1 ms perturbation period is

considered for local DPP converters to maximize the PV strings output power in a fast inner loop. Moreover, a central converter with 5 ms sampling time regulates the Virtual Bus voltage. The simulation results prove that, after each perturbation, all PV strings reach the new MPP in less than 100 ms whereas the virtual bus transient is extinguished within 1.5 s. Future work will focus on the dynamic modeling of the proposed configuration and its experimental validation.

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