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8-bit Dynamic Element Matching based Feedback Controller Applied to an Instrumentation Amplifier

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Abstract. The instrumentation amplifier, which incorporates Dynamic Element Matching (DEM) and a resistive network, utilizes a digital controller to reduce gain error by means of averaging. This paper assesses the feasibility of combining, within a general-purpose microcontroller, the appealing DEM, i.e., very accurate resistive ratios ranging between 1 and 15, with the associated versatile and scalable interrupt-aware digital controller. Given a mixed-signal system, a hybrid evaluation environment has been developed to perform relevant test-benches for assessing the systems performance, i.e., DEM controller, muxes, OpAmps, with respect to relevant metrics for integrated digital and mixed-signal circuits, i.e., energy, delay, footprint, precision. When implementing our design in a commercial 180nm technology, the gain precision of a typical amplifier is improved by more than 1800 times, with the error converging to as low as 10s of ppm, for Gaussian mismatch distribution between -1% and 1% with the cost of DEM digital circuitry which adds about 30000 μm^2 of chip area and will consume 194 μA.

Key-words: Dynamic Element Matching; digital controller; gain error; instrumentation amplifier; mismatch.

1. Introduction

Data acquisition often encounters numerous challenges, including noise interference, the necessity for instrument calibration, and the inevitable degradation of instrument accuracy over time. Therefore, it is required to improve the data acquisition process through techniques such

as filtering, increase of resolution and sample rate [1]. A widely adopted method in sensor interfacing for improved resolution involves amplifying the sensor's analog signal prior to sampling it with an analog-to-digital converter, thereby fully utilizing the converter's dynamic range [1]. However, precise amplification is a delicate matter due to offset, frequency response, discrepancies among passive components, and aging effects [2].

The studies reported in [3] and [4] have employed Dynamic Element Matching (DEM) to reduce the gain error in an instrumentation amplifier. However, their fixed gain limits the systems flexibility, requiring additional compensation from the read-out circuit. The objective of this work is to introduce versatility in gain options by incorporating a smart digital control circuit, thereby creating a programmable gain instrumentation amplifier.

Currently, the semiconductor industry has evolved to a stage where compact and cost-effective microcontrollers are equipped with numerous analog and digital peripherals, making them part of common applications such as analog signal conditioning, sensor interfacing, and the Internet of Things (IoT). Modern 8-bit microcontrollers are now integrated with multiple operational amplifiers, comparators, and self-calibrating data converters [5], [6]. Economical yet sturdy designs, utilizing a concise and efficient instruction set, necessitates less time for firmware development, thereby contributing to an overall reduction in costs.

The all-in-one integration of an accurate instrumentation amplifier, together with an analog-to-digital converter, computational capabilities, and robust communication protocols within a single chip, will position microcontrollers as a competitive low-cost solution for data acquisition, sensing, and control of complex systems [7].

This paper considers a low-cost microcontroller equipped with two operational amplifiers and an analog-to-digital converter. The primary function of this system is to store the amplified sensor output signal. A software application that can calculate the mean value from multiple measurements will be considered. The result will be transmitted through a communication protocol to a host machine. Furthermore, the outcome can also enhance the performance of other integrated subsystems, such as the microcontroller's peripherals.

To minimize voltage gain error, this work builds upon [8] and assess the feasibility of combining, within a general-purpose low-cost 8-bit microcontroller, the appealing DEM, i.e., very accurate resistive ratios ranging between 1 and 15, with the associated versatile and scalable interrupt-aware digital controller. Given the complexity of this mixed-signal system, a pure analog simulation of the entire system would require extensive hardware platforms together with a large number of simulation licenses. To assess the practical implication of our proposed DEM algorithm-based system, a hybrid analog-digital evaluation environment has been developed to perform relevant test-benches for assessing the systems performance, i.e., DEM controller, muxes, OpAmps, with respect to relevant metrics for integrated digital and mixed-signal circuits, i.e., energy, delay, footprint, precision. The design of the suggested digital controller adheres to the structure of a stand-alone peripheral for a standard RISC microcontroller architecture. It features an 8-bit data bus and a 4-bit address bus, necessary for addressing the 16 8-bit registers required for the operation and control of the resistive network.

Furthermore, this paper examines the potential implications of using a configurable architecture for the chain controller, as opposed to the single, fixed configuration for the controller as outlined in references [3] and [4]. Key performance indicators considered in our assessment included the digital circuit area, speed, and power consumption. Statistical simulations have indicated that, when using the proposed DEM circuit, a progressive reduction of gain error from 1.85% to 10s of ppm when considering a Gaussian distribution of resistor mismatch ranging

between -1% and 1% is obtained.

The rest of the paper is organized as follows: Section 2 gives the present the background of this work, the theory on which the proposed system functions and related work. Section 3 details the proposed digital controller implementation from a system standpoint. Finally, Section 4 presents the system implementation, the proposed simulation platform required for evaluating the system's main parameters, along with an overview of the entire behavior of the proposed amplifier.

2. Background

This section starts with analyzing the topology of the 2-opamp-based Instrumentation Amplifier (InAmp), including its key parameters and associated error sources. Subsequently, the impact of the DEM algorithm on a resistive network described in [8] is summarized. The section is concluded by evaluating the potential for incorporating the complete solution within a microcontroller.

2.1. The instrumentation amplifier and sources of gain error

The chosen design for this study is a simplified 2-opamp differential instrumentation amplifier topology. This design follows the architectural recommendations outlined in [3] and [4]. There are several factors that impact voltage gain, including the offset of the operational amplifier, the finite open-loop gain, and the disparity among passive components. To enhance the precision of such InAmp, techniques such as chopping, and laser trimming have been developed [1]. However, these methods become less effective over time due to the aging effects on resistor values. To overcome the limitations of the previously mentioned methods, the dynamic element matching technique (DEM) is analyzed for the case of the instrumentation amplifier. This technique principle is based on the schematic presented in Fig. 1. The objective is to interchange all passive components in all available combinations following the DEM algorithm. By doing so, the average of all InAmp gain results would accurately match the targeted gain value. By dynamically managing the total resistance within the amplifiers' feedback, RF, the values procured at each stage can be averaged. This method will mitigate the error between the computed and the mean value.

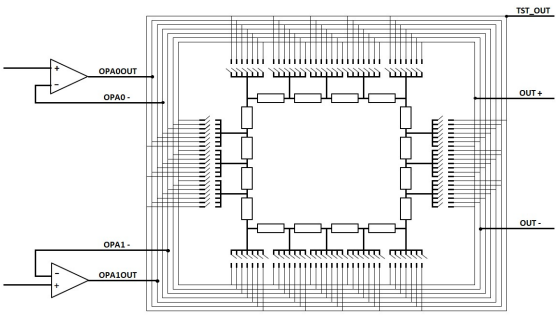

Fig. 1. The Dynamic Element Matching Instrumentation Amplifier

As indicated, every resistor value can be computed using (1), where Ra is the average value of all resistors inside the feedback of the amplifier. The gain error Δ is induced by resistor mismatch using the following relation provided in [3]:

$$R_i = R_a(1 + \epsilon_i) \tag{1}$$

and is defined in terms of

$$\Delta = \frac{1}{N}\sum_{i=1}^{N}\epsilon_i + \frac{2}{N\,(N-1)}\sum_{i=1}^{N/2}\epsilon_i\epsilon_{i+N/2} \tag{2}$$

In (2), the second term on the right-hand side is calculated by considering a single resistive chain element connected as load. The main contributor to the gain error, especially when the system is generating high gain values, is the first term.

To incorporate this averaging technique within a data acquisition system, the DEM technique requires signal oversampling at a rate that corresponds to the sum of all chain resistors. For instance, if the scenario implies using 16 resistors, the sampling frequency must be up-scaled 16 times to gather the 16 voltage values, compute their average, and produce the result. The data converter utilized in the aforementioned scenario, should feature high resolution to capture the maximum amount of data prior to averaging.

The resistive network depicted in Fig. 1 includes the necessary switches for altering resistor positions within the chain, as well as two operational amplifiers. Implementing the resistive network digital control given in [3] and [4] is straightforward and maintains the network's configuration. The decoder incorporates a 4-bit counter and does not feature gain control capability

2.2. Considerations for integrating the DEM controller into a microcontroller

The requirement for integrating DEM controller into a microcontroller is to act as a standalone peripheral. This allows independent operation from the rest of the system, thereby minimizing the CPU interaction with the DEM peripheral by using pseudo-parallel execution. The aforementioned technique enables the microcontroller core to focus on other tasks or enter sleep mode to minimize power usage. The digital controller should interact with the CPU using a dedicated data bus, which can support both read and write operations, for the dedicated registers that govern the resistive network's behavior.

Considering that InAmps are explicitly engineered for data acquisition systems, it is also essential to enable the system to link the amplifier's output to an ADC as well as to a general-purpose analog test bus. The latter ensures the system's optimal testability.

3. Proposed DEM Digital Controller

This section presents the proposed DEM digital controller concept, in relation to a standard 8-bit RISC microcontroller architecture and outlines the programming process for the DEM-based amplifier. When implementing an instrumentation amplifier as an all-in-one system, by integrating the operational amplifiers and resistor ladders into a microcontroller [5] and [6], gain error would be strongly influenced by the mismatch of internal resistors. The following concept

attempts to replace these resistors with a novel chain of resistors that can implement the rotational dynamic element matching technique.

3.1. System level integration of the digital controller

To address the lack of versatility mentioned in the previous section, this paper is proposing a new digital controller for the resistive network that implements a versatile configuration scheme with gain settings ranging from 1 to 15.

Analog switches reconfiguration is used in order to create various resistor arrangements within the amplifier's feedback. The resistive network is structured in a sequential manner, with a set of 7 switches placed between each pair of resistors. Each switch provides the capability to connect the network's node to either the inverting input, the output pins of the two operational amplifiers, or the differential output pins of the entire system. To ensure optimal design testability, an extra switch will be added to connect each network node to an analog test bus, as depicted in Fig. 1. The aforementioned structure is well suited for integration in a microcontroller.

Fig. 2 illustrates the 16x7-bit registers along with their 112-bit output bus, while Fig. 3 showcases the rotation of switch bank configurations. To minimize the real-estate within a microcontroller integration, a network of 16 resistors will be implemented, requiring 16 switch banks, cumulating 112 switches in total. To change each resistor position inside the network during every clock cycle, a default set of positions is required. Thus, a set of 16 registers that can each store 8 bits of data has been implemented. The first two registers will store control signals, flags, and multiplexer selections: i) for the clock controller that determines the rate at which resistors cycle through their positions, ii) for the interrupt requests, and iii) for enabling and disabling the rotation of the chain or even load a new configuration.

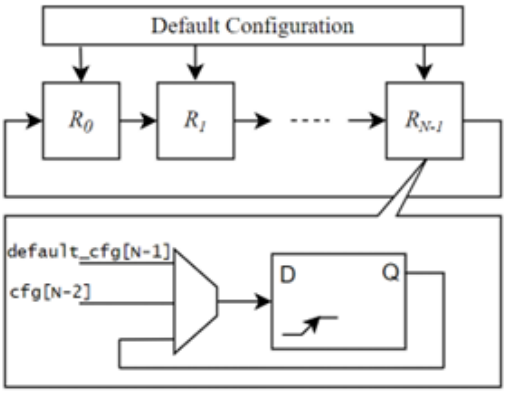

Fig. 2. DEM System Implementation

The remaining 14 registers are designated to hold the default configuration of the chain, marking the default resistor positions during reset. The 14x8-bit registers' stored values are then concatenated in a 112-bit bus and de-concatenated to create 16x7-bit registers that serve as default configuration for each switch bank.

Within each clock cycle, every bank of registers provides the option to either adopt the configuration of the preceding bank or revert to the default configuration; this decision is made through a priority encoder.

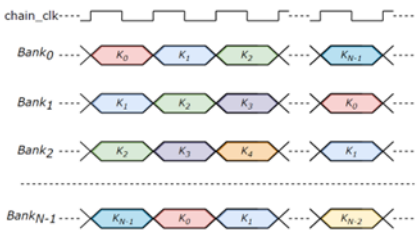

Fig. 3. Rotation of switch bank configurations

3.2. Interrupt controller for a DEM-based system

Fig. 4 provides a top-level overview of the digital controller. The register set is connected via a 4-bit address bus and an 8-bit data bus. The updated interrupt controller implementation is presented in Fig. 5. Interrupts are generated by a top-level dedicated logic based on the values in the designated bit field of Control Register 1.

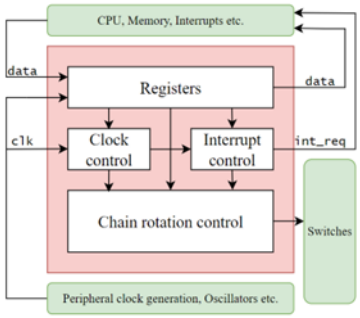

Fig. 4. Top level of digital controller

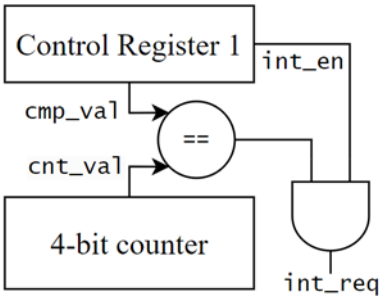

Fig. 5. Interrupt generation logic

The interrupt system works as follows: when the application configures the Control Register 1 to enable the interrupts, this event will be recorded in a read-only bit of the very same register as an interrupt flag. This interrupt flag is then sent to the CPU at the hardware level, prompting

the execution of the desired code sequence. As for how the interrupt is generated, a cycle counter is used to keep track of the state of the resistive network rotation. In the Control 1 Register there is a bit field which stores the number of the rotation steps that will trigger the interrupt. Since this implementation features 16 resistors in the network, there are at most 16 steps in a complete rotation of the system, therefore the cycle counter is only 4 bits wide. The interrupt manager is always active when the digital controller is enabled, but its interrupt flag is gated with the interrupt enable bit field of the Control 1 Register.

3.3. Programming the amplifier

Configuring each bank of switches provides the highest achievable gain of the system equal to the number of resistors inside the network minus 1, i.e., a gain of 15x. The lowest preset value is obtained by configuring the two amplifiers as voltage followers, giving a gain of 1. The internal bus width of the DEM controller is designed to match the 8-bit microcontrollers data bus, thus following the stand-alone peripheral prerequisites for an 8-bit microcontroller. Registers write access is done sequentially, by selecting the corresponding address on the address bus and raising a write operation flag. The 16 resistors chain, each with a bank of 7 CMOS switches, has been designed inside a separate analog design environment, while for the 2 operational amplifiers, a typical compact Verilog-A model was utilized. The resistor layout configuration is stored in 14x8-bit registers starting with address 2, while the control registers are stored at addresses 0 and 1. The 112 configuration bits will configure the 16x7-bit registers that provide direct control over the switch banks.

4. Implementation and Results

This section presents the implementation of the proposed digital controller architecture described in the previous section. Additionally, this section describes the simulation framework and the test-benches for evaluating the system's performance, i.e., DEM controller, muxes, OpAmps, with respect to relevant metrics for integrated digital and mixed-signal circuits, i.e., energy, delay, footprint, precision. Moreover, this section includes the comparison of the results reported in this paper against non-DEM general purpose InAmp.

4.1. The switch-controlled network

The design of the 112 switches, which manage the connections between resistors, operational amplifiers, and input/output ports, was accomplished through two distinct approaches. Initially, the switches were designed as simple transmission gates to minimize chip area, offering a cost-effective solution. Subsequently, a T-switch topology was employed, necessitating two transmission gates and a pull-down NMOS transistor. This approach improved kick-back noise immunity due to its superior isolation when disabled, it also increased the switch area by about 2x to maintain an equivalent impedance.

Upcoming simulation results presented in the subsections below demonstrate that the active transmission gates generate noise into the disabled ones when cycling through the network, hence generating voltage spikes on the output signal. However, providing good control over the timing of the acquisition process of the A/D converter by sampling the signal after the DEM network switching has occurred, the voltage spikes get filtered, hence yielding accurate conversion results.

4.2. Simulation framework

Fig. 6 depicts the simulation framework for the proposed DEM-based system. This framework incorporates a hybrid Cadence-Matlab environment. On one hand, the DEM algorithm is implemented and evaluated through thousand iterations in Matlab by developing statistical models for the feedback resistors. On the other hand, leveraging identical design and simulation parameters, the DEM-based digital controller, along with the network of switches and resistors, was designed and validated within Cadence Virtuoso simulation suite. The validation process covers the following steps: i) firstly, the functionality of the digital controller is validated at both the RTL and the gate level, which involves the generation of a unique set of test patterns for each digital simulation, ii) secondly, these test patterns are applied to the matrix of switches and resistors within an analog simulation environment, iii) thirdly, the InAmps output is monitored and, when settled, for each DEM algorithm iteration, is sampled and stored for future processing, and iv) finally, upon simulations completion, the error produced by the statistical model in Matlab is compared with the one resulted from the system designed in Cadence Virtuoso to assess the implemented system's performance.

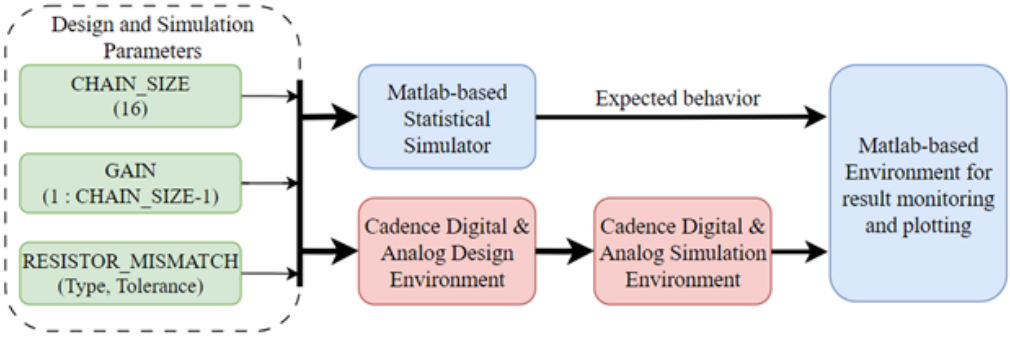

Fig. 6. Simulation environment block diagram

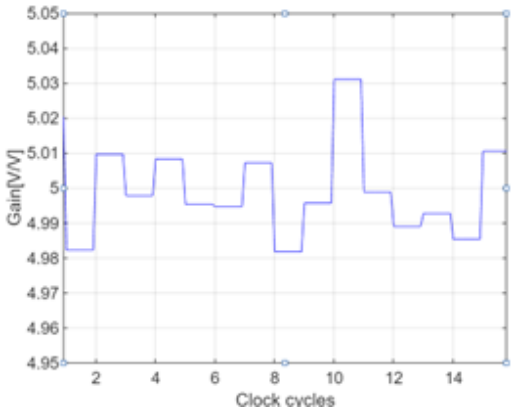

Fig. 7. Gain variation over 16 clock cycles

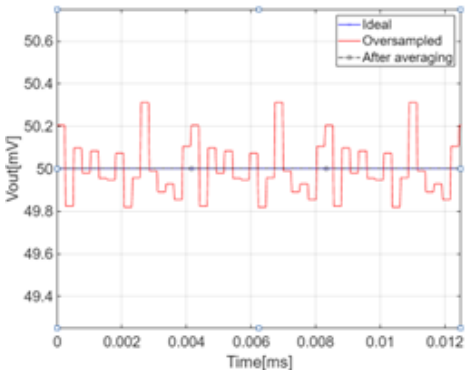

Fig. 8. Periodic gain variations - transient

4.3. The digital controller

The simulation framework presented above was used to generate digital controllers area and power consumption reports depicted in Table 1 when configuring the system for a gain of 5. These results originate from the synthesis report that yielded the highest power consumption, 194 μA at 16 MHz for a supply of 1.98 V. Each OPAMP features rail-to-rail operation, push-pull output stage, 1 MHz bandwidth and an open-loop gain of 118 dB, using a 3.3 V single-supply. The total additional area required for the DEM digital circuitry is 30199.366 μm^2.

Table 1. Power report for the proposed digital controller

Module	**Power report**				
	Instances	***Leakage***	***Internal***	***Net***	***Switching***
Clock controller	1	61.475	66916.614	8069.052	74985.666
Switch bank controller	16	22.646	2997.250	216.207	3213.460
Total	17	618.461	349130.509	34855.509	383985.868

Note: All power values are in nW.

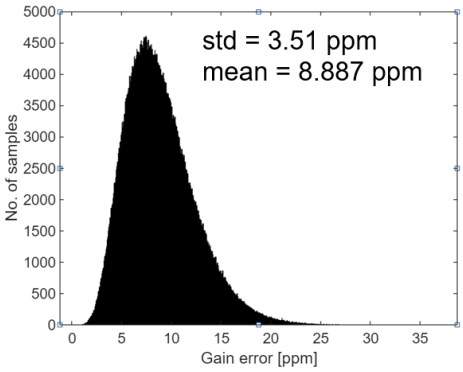

Fig. 9. Gain error for normal distributed mismatch

The test setup required amplifying a 10mV DC signal. The resistor network will cycle through 16 possible gain values. Fig. 7 shows the amplifier gain variation at each step in the DEM algorithm when considering the mismatch of resistors values to be between -1% and +1%. In Fig. 7 and Fig. 8, the output of the amplifier is also depicted within a transient simulation for a single random statistical simulation run. Upon ending a cycle, the average value of the previous 16 cycles in computed and compared to the desired gain, getting an absolute error of 5 μV. Hence, the gain precision of the amplifier is improved by up to more than 1800 times. To show the convergence of this averaging algorithm, Fig. 9 and Fig. 10 present the histogram of the results of 1 million statistical simulations performed in Matlab, where the mismatch between resistors values with respect to their nominal value is between -1% and $+1\%$. The results depicted in Fig. 7-10 demonstrate that cycling through multiple resistor combinations and averaging these results will yield a gain error reduction from up to 1.85% to as low as a few tenths of ppm for either a normal or a uniform distribution.

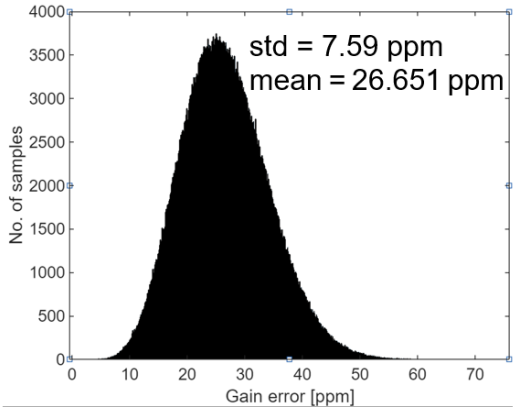

Fig. 10. Gain error for uniform distributed mismatch

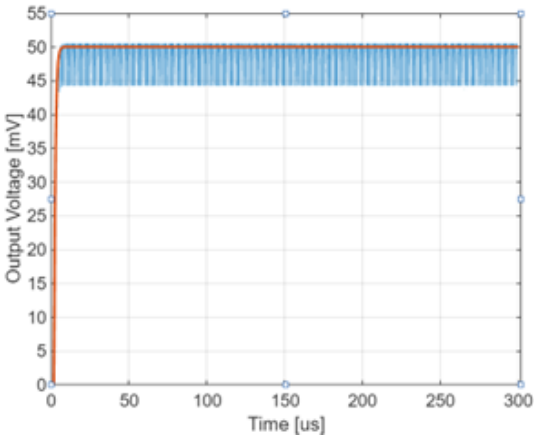

Fig. 11. Raw voltage output in blue, averaged output in orange

By pairing this controller with two operational amplifiers such as the ones found in micro-

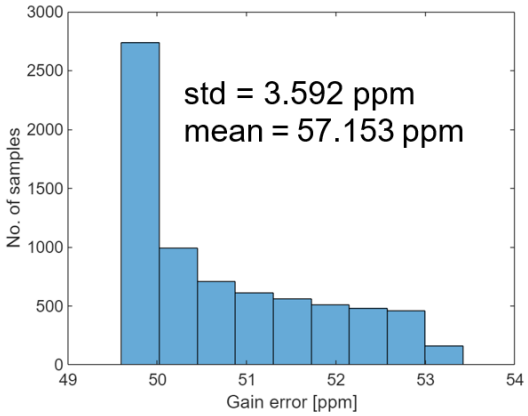

Fig. 12. Histogram of measured average gain error

controllers described in [5] and [6], it would be created an instrumentation amplifier with a gain error as low as 10 ppm in comparison with the current instrumentation amplifier configuration already available, that has a gain error in the range of several percentage.

The digital controller has been interfaced with a pair of operational amplifiers and evaluated through SPICE simulation together with a resistor network and an array of switches. Subsequently, the simulation involved iterating over all switch configurations to attain a 5x gain for an input signal of $10\ mV\ DC$, resulting in an output voltage of $50\ mV\ DC$. The simulation results, along with a histogram depicting the measurement data, are presented in Fig. 11 and Fig. 12.

5. Conclusions

This paper evaluated the feasibility of combining, within a general-purpose microcontroller, the appealing DEM, i.e., very accurate resistive ratios ranging between 1 and 15, with the associated versatile and scalable interrupt-aware digital controller. Given a mixed-signal system, a hybrid evaluation environment has been implemented to perform relevant test-benches for assessing the systems performance, i.e., DEM controller, muxes, OpAmps, with respect to relevant metrics for integrated digital and mixed-signal circuits, i.e., energy, delay, footprint, precision. When implementing our design in a commercial 180nm technology, the gain precision of a typical amplifier is improved by more than 1800 times, with the error converging to as low as 10s of ppm, for Gaussian mismatch distribution between -1% and 1% with the cost of DEM digital circuitry which adds about 30000 μm^2 of chip area and will consume 194 μA.

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