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High-Efficiency Bridgeless Resonant Converter for Street LED Lighting Application

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ABSTRACT A novel single-stage LED driver for street lighting application is proposed in this article which combines a totem-pole boost PFC and a non-isolated LCCL resonant network. The converter offers several benefits, including: appropriate total harmonic distortion (THD) level and high power factor (PF) of the input current; reduced conduction losses and suppressed electromagnetic interference (EMI) thanks to its bridgeless structure; zero-voltage switching (ZVS) for the main switches and zero-current switching (ZCS) for rectifier diodes across the entire input voltage range and load conditions; a constant output current to an LED string load due to the LCCL network characteristic at the resonant frequency; and fixed-frequency operation via the main switches duty cycle for regulating the output current. The paper provides a detailed explanation of the proposed driver operating modes and theoretical analysis, as well as a comprehensive analysis of the impact of parameters on DC-link voltage level and main switches voltage stress. A design procedure is also presented. Experimental verification is demonstrated through a 100W prototype circuit operating at 200 kHz.

INDEX TERMS LED driver, LEDs application, resonant converter, power converters, soft switching.

I. INTRODUCTION

Nowadays high frequency AC-DC converters are widely employed in on-board power module, laptop and PC charger, and LED lighting application to meet the international grid standards such as IEEE519, IEC/EN61000-3-2 and IEC/EN61000-3-12 [1], [2], [3], [4].

In LED driver application, there are two well-known AC-DC structures [5]. Two-stage LED drivers can provide an excellent output current regulation and long life-span due to utilizing non-electrolytic capacitors [6], [7], [8]. The independent front-end PFC stage only improves the power factor of the input current, while the second stage is responsible for regulating the LED current independently. But due to cascaded structure and multistate power processing, the system efficiency is reduced, and the component count is increased. The single-stage AC-DC converter for LED drivers, consist of two integrated operating stages for simultaneously ensuring suitable LED current, maintaining a high power factor (PF) and low total harmonic distortion (THD) input current, reducing component count and providing higher efficiency than the two-stage topologies. In recent studies, integrating a front-end PFC stage and a resonant converter is very popular scheme for AC-DC application [9], [10], [11], [12], [13], [14], [15], [16]. Among the various single-stage topologies, Boost-LLC structure is widely developed and investigated due to its simple structure and high efficiency [9], [11], [12], [13], [14], [15]. In this structure, the PFC boost converter is usually designed in Discontinuous Conduction Mode (DCM) and the input inductor can reduce the required line filter size. Also, in order to eliminate the bridge rectifier conduction losses and improve the converter efficiency, bridgeless (BL) boost converter named totem pole boost converter can be adopted [17], [18]. The major advantage of the totem pole boost converter is much smaller common-mode noise than that of the basic bridgeless boost PFC rectifier. However, due to step-up characteristic of the boost topology, the DC-Link voltage can be almost twice the input voltage peak value, resulting in large voltage stresses on the semiconductor devices, requiring large

volumes for DC-Link capacitor, and complicates the post-regulator stage design [19]. The major LLC stage advantage is achieving zero-voltage switching (ZVS) for the primary side switches and zero-current switching (ZCS) for the secondary side rectifier diodes when the LLC resonant network input impedance is inductive [20]. However, Pulse Frequency Modulation (PFM) with a fixed operating duty cycle of the main switches is typically used for regulating the output voltage/current which negatively impacts the DC-Link voltage variation and increases the voltage stress of the semiconductor devices especially for universal line voltage of 110-220 V_{RMS} [14]. Also, the secondary side rectifier diodes lose ZCS operation when the switching frequency becomes higher than the series resonant frequency. Furthermore, the LLC converter is responsible for providing a constant current (CC) for the LED load and employing tight current feedback is essential since a minor variation of the output voltage leads to much larger LED current variations [5], [21], [22]. Also, due to the voltage gain characteristic of the LLC resonant network, wide switching frequency range is required for regulating the LED current at the desired value [12], [23].

In order to reduce the amplitude of the DC-link voltage, a step-up/down converter can be adopted for input PFC stage. Using a buck-boost or fly-back based font-end stage provides a very low input current THD with simple structure, while, due to the pulsating input current intolerable EMI effects is the main drawback, and a large input passive filter is inevitable. Employing SEPIC converter can reduce the input current ripple and has an inherent input current filtering capability. However, the passive components count is increased [15].

In [12], [14] a single-stage resonant LED driver based on interleaved bridgeless buck-boost PFC converter and an CLCL network is presented to replace the conventional boost-LLC structure with a high efficiency. The proposed topology is designed to provide constant output voltage for LED load and the switching frequency variation range is reduced than the conventional LLC converter.

In this paper, a single-stage LED driver is presented by combining a totem-pole boost converter and an isolated LCCL resonant converter suitable for street lighting application. Due to using totem-pole boost structure at the input side, the input current is shaped with an appropriate THD level and high PF. Also, the conduction losses of the bridge rectifier diodes are eliminated which improves the efficiency. The proposed LCCL resonant network provides ZVS condition for the main switches and ZCS condition for rectifier diodes, while delivers constant output current at the operating frequency equal to the resonant frequency. The proposed single-stage converter can operate within a wide input and output voltage variation ranges, and a well-regulated output current is provided by adjusting the duty cycle of the main switches.

II. PROPOSED CONVERTER AND OPERATING PRINCIPLES

The circuit diagram of the proposed single-stage LED driver is depicted in Fig. 1. The proposed topology is composed of a totem-pole boost PFC converter at the input stage combined

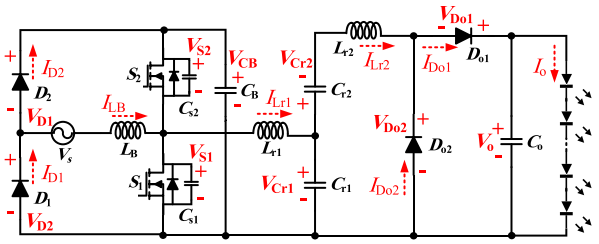

FIGURE 1. Circuit diagram of the proposed single-stage LED driver.

with a LCCL resonant converter to provide constant output current to a LED string. In this structure, D_1, D_2, L_B, S_1, and S_2 are the totem pole boost converter components and S_1, S_2, L_{r1}, L_{r2}, C_{r1}, C_{r1}, D_{o1} and D_{o2} are the LCCL resonant converter components. During the positive half line cycle, switch S_1 along with D_1 and the body diode of S_2 are activated and similarly, switch S_2 along with D_2 and the body diode of S_1 operate in the negative half-line cycle. Therefore, the gating signals of S_1 and S_2 can be applied complementary with a small dead time just as the conventional totem pole boost converter. To simplify the analysis, semiconductor devices are assumed ideal, but the switches output capacitors (C_{s1} and C_{s2}) are considered for accurate investigation. The input voltage source along with the required input LC input filter are modeled as V_s and the switching frequency f_s is much higher than the AC line frequency f_L. As a result, V_s is assumed constant during a switching cycle. The converter operating modes over a complete switching period at steady state are explained. Since the operating modes in the positive and the negative half line cycles are identical, only the operation in the positive half-line cycle is analyzed which is divided into eight intervals. The converter key waveforms and the equivalent circuit of each interval is illustrated in Figs. 2 and 3, respectively.

Interval 1 [t_0–t_1]: During this mode, S_1 and D_1 are conducting, and L_B is being charged through the input source. Also, at t_0, I_{Lr2} has reached zero and D_{o2} starts conducting. Hence, the resonant network input and output are short circuited and its elements L_{r1}, C_{r1} and C_{r2} are discharging while, the output current is fed via C_o. This interval ends when S_1 is turned off at t_1.

Interval 2 [t_1–t_2]: When S_1 is turned off, I_{Lr1} starts charging and discharging C_{s1} and C_{s2}, respectively. After C_{s2} is fully discharged, S_2 body diode starts conducting.

Interval 3 [t_2–t_3]: At t_2, S_2 is turned on under ZVS condition, and V_{CB}-V_s is applied across L_B which decreases I_{LB} linearly. Also, V_{CB} is applied to the resonant input and through a resonance, L_{r1}, L_{r2} and C_{r1} charge and C_{r2} discharges. At t_3 the S_2 current direction is reversed and this mode.

Interval 4 [t_3–t_4]: At t_3, I_{Lr1} becomes positive, D_1 and D_{o2} continue conducting and C_o supplies the output current. At t_4, I_{LB} and I_{Lr1} reach zero which turn off D_1 and D_{o2} under ZCS condition and this mode ends.

Interval 5 [t_4–t_5]: At beginning of this interval, D_{o1} turns on, and V_{CB} is applied to the resonant network. During this

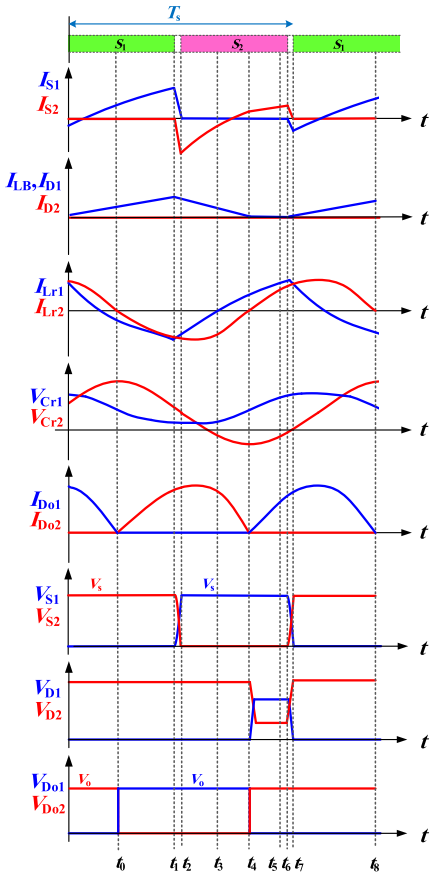

FIGURE 2. Theoretical key waveforms.

mode I_{LB} remains zero but the resonant network elements continue resonating and charge. This mode ends when I_{Lr1} and I_{Lr2} equals and V_{Cr1} reaches its maximum.

Interval 6 [t_5–t_6]: In this interval, I_{Lr2} exceeds I_{Lr1} and V_{Cr1} begins decreasing in a resonant manner. At t_6, S_2 is turned off and this mode ends.

Interval 7 [t_6–t_7]: By turning S_2 off, I_{Lr1} starts to discharge and charge C_{s1} and C_{s2}, respectively. When C_{s1} is fully discharged, S_1 body diodes turns on and this mode ends.

Interval 8 [t_7–t_8]: At t_7, S_1 is turned on under ZVS condition which forward biases D_1 and places V_s across L_B, thus, I_{LB} begins to increase linearly. The resonant network input voltage is zero and L_{r1} and C_{r1} are discharging, while L_{r2} and C_{r2} continue to charge. At t_8, I_{Lr2} reaches zero and D_{o1} turns off under ZCS condition and the next switching cycle starts.

III. STEADY STATE ANALYSIS AND DESIGN CONSIDERATION

A. TOTEM POLE BOOST CONVERTER

In order to provide an inherent PFC operation, the totem pole boost converter is designed in DCM. Therefore, assuming sinusoidal input voltage, the input current peak value is:

$$I_{s_{\max}} = \frac{V_{s_{\max}} D T_s}{L_B} \sin(\omega_g t) \tag{1}$$

where, D, T_s and ω_g are the main switches operating duty cycle, switching period and the line angular frequency, respectively. Due to DCM operation of L_B, the maximum required time for complete discharge of L_B is calculated as:

$$T_{off} = \frac{I_{s_{\max}} L_B}{V_{CB} - V_s(t)} = \frac{V_s(t) D T_s}{V_{CB} - V_s(t)}. \tag{2}$$

By replacing T_{off} = (1-D) T_s in (2), the boundary value of the main switches duty cycle is obtained to ensure the DCM operation of the totem pole boost converter:

$$D_{\max} \leq 1 - m \tag{3}$$

where,

$$m = \frac{V_{s_{\max}}}{V_{CB}}. \tag{4}$$

According to relations (1) and (2), I_{LB} average in a switching period is derived as:

$$\overline{I_{LB}} = k \left(\frac{m \sin(\omega_g t)}{1 - m \sin(\omega_g t)} \right) \tag{5}$$

where,

$$k = \frac{V_{CB} D^2 T_s}{2 L_B}. \tag{6}$$

Based on (5), the root mean square (RMS) value of the input current can be calculated:

$$I_{in(RMS)} = \sqrt{\frac{1}{\pi} \int_0^{\pi} I_s(t)^2 d\omega_g t} = \sqrt{\frac{1}{\pi} \int_0^{\pi} \frac{k^2 m^2 \sin(\omega_g t)^2}{1 - m \sin(\omega_g t)}} = km \sqrt{\frac{A}{\pi}} \tag{7}$$

where,

$$A = \int_0^{\pi} \frac{\sin(\omega_g t)^2}{1 - m \sin(\omega_g t)^2} d\omega_g t = \frac{2}{m(1-m)^2} + \frac{\pi}{m^2} + \frac{2m^2 - 1}{m^2 (1 - m^2)} \frac{2}{\sqrt{1 - m^2}} \left(\frac{\pi}{2} + \arctan \frac{m}{\sqrt{1 - m^2}} \right). \tag{8}$$

In Fig. 4(a), the converter theoretical input current waveforms for different values of m within a half-line cycle are illustrated. According to (4) as the DC-Link voltage (V_{CB}) increases, m reduces, and Fig. 4(a) indicates that the input current waveform becomes closer to the ideal sinusoidal waveform with higher input current PF. According to (7), the proposed converter input power and the input current power factor are calculated:

$$P_{in} = \frac{1}{\pi} \int_0^{\pi} V_s(t) I_s(t) d\omega_g t = \frac{V_{s_{\max}} kmB}{\pi} \tag{9}$$

$$\text{PF} = \frac{P_{in}}{V_{sRMS} I_{sRMS}} = \frac{B\sqrt{2}}{\sqrt{\pi A}} \tag{10}$$

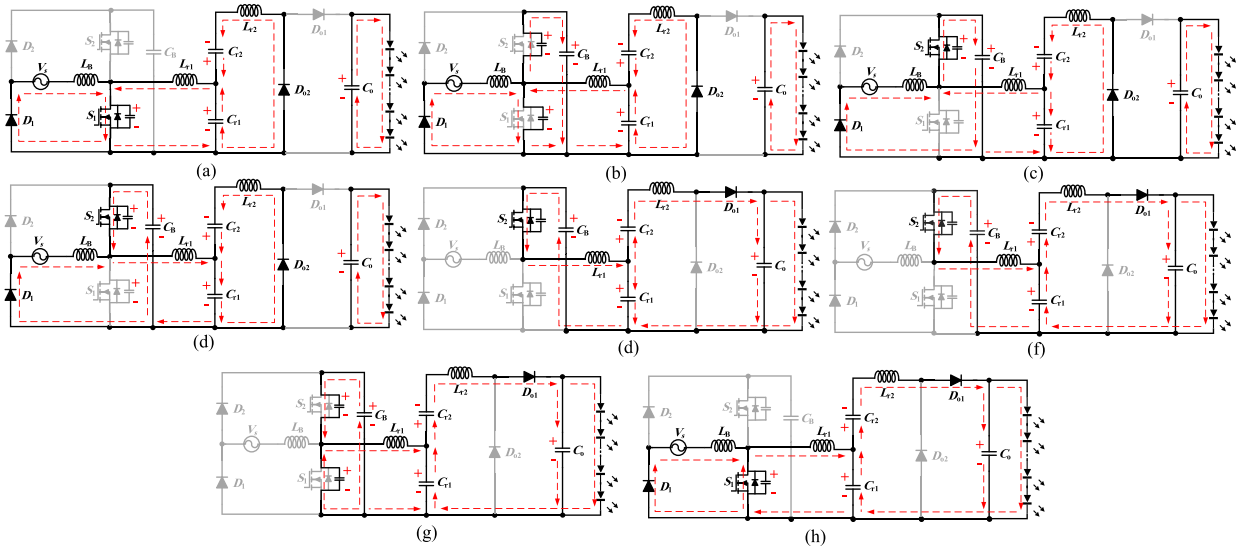

FIGURE 3. Equivalent circuit of each operating mode: (a) Interval 1, (b) Interval 2, (c) Interval 3, (d) Interval 4, (e) Interval 5, (f) Interval 6, (g) Interval 7, and (h) Interval 8.

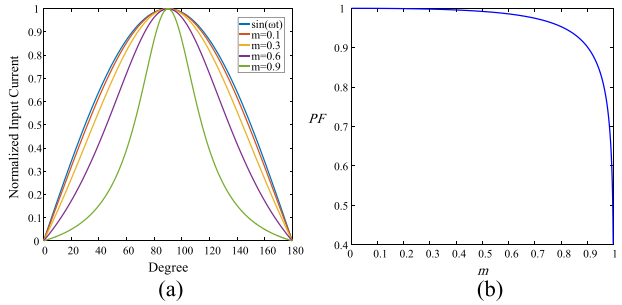

FIGURE 4. (a) Theoretical input current waveforms for different values of *m*, and (b) Input current PF diagram versus *m*.

where,

$$B = \int_0^{\pi} \frac{\sin(\omega_g t)^2}{1 - m\sin(\omega_g t)} d\omega_g t = \frac{2}{m^2\sqrt{1-m^2}} \left(\frac{\pi}{2} + \arctan\frac{m}{\sqrt{1-m^2}}\right) - \frac{\pi}{m^2} - \frac{2}{m}. \quad (11)$$

In Fig. 4(b), the input current PF graph is depicted. Regarding the IEC/EN61000-3-2 standard, at the worst condition, it is necessary for the input current PF to be larger than 0.95. Therefore, the maximum value of m must be selected smaller than 0.8 for the proposed converter.

B. LCCL RESONANT NETWORK

As is described, the proposed converter is designed to operate at fix frequency operation to take advantage of constant output current characteristic of LCCL resonant network. The detailed analysis of LCCL resonant network is provided in [21]. Using Fundamental Harmonics Approximation (FHA) the fundamental component of the LCCL network input voltage is obtained as follows:

$$V_{AB}^F = \frac{V_{CB}}{\pi}\sqrt{2(1-\cos(2\pi D))}\sin(\omega_s t + \phi) \quad (12)$$

where,

$$\phi = \arctan\frac{\sin(2\pi D)}{1-\cos(2\pi D)}. \quad (13)$$

Based on FHA analysis, the current gain equation $H(j\omega_n)$ of the proposed LCCL resonant network is calculated as:

$$H(j\omega_n) = \frac{jC_n\omega_n}{1-\omega_n^2(1+C_n+L_nC_n(1-\omega_n^2))+j\omega_n\frac{C_n}{Q_e}(1-\omega_n^2)} \quad (14)$$

where,

$$\omega_r = \frac{1}{\sqrt{L_{r1}C_{r1}}}, Z_r = \sqrt{\frac{L_{r1}}{C_{r1}}} \quad (15)$$

$$Q_e = \frac{Z_r}{R_{eq}}, Req = \frac{4R_o}{\pi^2} \quad (16)$$

$$L_n = \frac{L_{r2}}{L_{r1}}, C_n = \frac{C_{r2}}{C_{r1}}, \omega_n = \frac{\omega_r}{\omega_s}. \quad (17)$$

According to (14), the current gain of LCCL network becomes independent of the load condition at switching frequencies equal to the resonant frequency. Therefore, the LED current equation is given as:

$$I_o = \frac{V_{CB}\sqrt{2(1-\cos(2\pi D))}}{\pi^2 Z_r}. \quad (18)$$

Due to the single stage structure of the proposed LED driver, DC-Link capacitor C_B plays the power balancing role between the PFC stage and LCCL converter. Using (9) and (18), V_{CB} is obtained as follows:

$$V_{CB} = \frac{V_s^2 B L_{r1}}{V_o L_B}\frac{\pi^2 D^2}{\sqrt{2(1-\cos(2\pi D)}}. \quad (19)$$

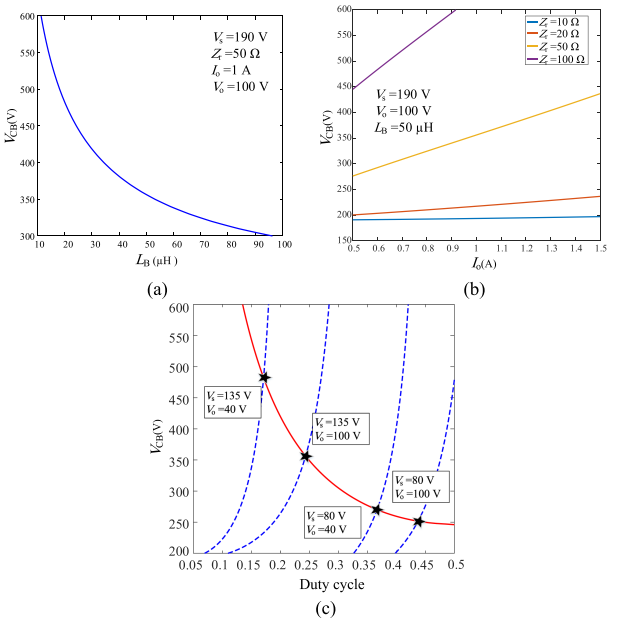

FIGURE 5. V_{CB} amplitude versus: (a) L_B values, (b) output current, and (c) operating duty cycle.

According to above equation, different parameters such as L_{r1}/L_B ratio, operating duty cycle, and the input and output voltage levels affect the DC-Link capacitor voltage and the voltage stress of the main switches. Fig. 5(a) demonstrates the V_{CB} voltage level versus the L_B value, indicating that increasing the L_B values, decreases the DC-Link voltage level. However, choosing a large L_B leads to the departure of totem pole boost converter from DCM operation region. In Fig. 5(b), the V_{CB} voltage levels with respect to the output current for different values of characteristic impedance Z_r are illustrated. It is evident that choosing small values of Z_r results in lower voltage stress on the DC-Link capacitor and power switches.

C. VOLTAGE AND CURRENT STRESS OF DEVICES

The switches voltage stress is equal to the maximum V_{CB} voltage and the voltage stress of the output diodes is V_o. In order to reduce the power switches voltage stresses, it is necessary to minimize V_{CB}. However, regarding Fig. 4, decreasing V_{CB} deteriorates the input current power factor.

Due to the single-stage structure of the proposed converter, during the positive input voltage half-line cycle, the S_1 current stress is equal to the summation of I_{Lr1} and I_{LB} at turn-off instant, while, the S_2 current stress is equal to I_{Lr1}. At the turn-off instant of S_1, the I_{LB} value is maximum and is obtained as:

$$I_{LB_{\max}} = \frac{V_{s_{\max}} D T_s}{L_B}. \tag{20}$$

Using FHA analysis, input current of the LCCL resonant network is obtained as:

$$I_{Lr1}(t) = \frac{2V_s}{\pi Z_r}\sqrt{\frac{1}{Q_e^2} + \frac{(1 + C_n(1 - L_n))^2}{C_n^2}}\sin(\omega_s t + \phi - \alpha) \tag{21}$$

where, α is calculated as:

$$\alpha = \arctan\left(Q_e\left(\frac{1 + C_n(1 - L_n)}{C_n}\right)\right). \tag{22}$$

According to (20) and (21) the L_B, L_n and C_n values impact the power switches current stress. For ($C_n \leq 1$) the I_{Lr1} amplitude and the switches current stress increases. Also, regarding 21, the optimal L_n value is unity to minimize the switches current. If ($L_n \leq 1$) is chosen, the amplitude of I_{Lr1} increases, resulting in higher switches current stress. Additionally, decreasing L_B increase the input current peak value, resulting in higher current stress. The average and the maximum current of the output diodes are almost independent of L_B, L_n and C_n as follows:

$$I_{Do1,\max} = I_{Do2,\max} = \pi I_o \tag{23}$$

$$\overline{I_{Do1}} = \overline{I_{Do2}} = I_o. \tag{24}$$

During the positive half-line cycle of the input voltage, the amplitude of I_{Lr1} at the S_1 turn-off instant is negative. Therefore, at t_1, (I_{Lr1}- I_{LB}) charges and discharges the capacitors C_{s1} and C_{s2} respectively and due to the sufficient stored energy in L_{r1}, a strong ZVS turn on is provided for S_2. However, at S_2 turn-off instant, I_{LB} is zero and only I_{Lr1} is responsible for providing ZVS turn on condition for S_2 at t_6. Since the stored energy of L_{r1} is lower than L_B, the ZVS turn on condition for S_1 is more critical. Therefore, if ZVS turn on condition is provided for S_1, the ZVS turn on condition of S_2 is guaranteed. The required stored energy of L_{r1} must be satisfied by the following relation:

$$C_s {V_{CB}}^2 < \frac{1}{2} L_{r1} I_{Lr1}^2(t_6) \tag{25}$$

where, C_{s1}=C_{s2}=C_s. According to (25) and substituting (21), it can be concluded that the ZVS turn-on condition can be maintained for the entire range of the input and output voltages by choosing the suitable values for L_n and C_n.

IV. DESIGN EXAMPLE AND EXPERIMENTAL VERIFICATION

In order to verify the theoretical analysis and effectiveness of the proposed LED driver operation, a prototype circuit is designed to supply a 100 W LED string load involving 30 numbers of series high-brightness (HB) white LEDs. The input voltage of the proposed converter is from 110 V_{RMS} grid with voltage variation range between 80–135 V_{RMS}. The detailed specifications of the prototype circuit are listed in Table 1.

A. DESIGN EXAMPLE

In order to employ the constant output current feature of LCCL resonant network effectively, the switching frequency is chosen equal to the resonant frequency and the output current is regulated using the main switches duty cycle. According to (19), the DC-Link capacitor voltage and the main

TABLE 1. Implemented Prototype Specifications

Parameter/Component	Symbol	Specification
AC input voltage range	V_s	80-135 V_{RMS}
Output power	P_o	100 W
Output current	I_o	1 A
Switching frequency	f_s	200 kHz
Input inductor	L_B	50 μH
Resonant inductors	L_{r1}, L_{r2}	39.7 μH
1st Resonant capacitor	C_{r1}	16 nF
2nd Resonant capacitor	C_{r2}	20 nF
DC link capacitor	C_B	10 μF
Output capacitor	C_o	10 μF
Main switches	S_1, S_2	IPW65R019C7
Input diodes	D_1, D_2	SCS210AG
Output diodes	D_{o1}, D_{o2}	STTH1002C

switches voltage stress depends on the main switches duty cycle, and the input and output voltage levels. In Fig. 5(c), DC-Link voltage variation versus duty cycle is illustrated. In this figure the LED current is assumed to be 1A and the maximum output voltage range is between 40–100V. In order to meet the IEC/EN61000-3-2 standard, the maximum voltage variation of the DC-Link capacitor is within the 250–500V range. According to Fig. 5(a), high values of Z_r increases the DC-Link capacitor voltage and improves the input current power factor. However, the main switches voltage stress is increased. Therefore, using a trade-off, the suitable value of Z_r is chosen equal to 50 Ω for simultaneously achieving high input current power factor with moderate switches voltage stress. Also, according to Fig. 5(b), low values of L_B increases the main switches voltage stress. In order to provide DCM operation of the totem pole boost converter with the DC-Link capacitor within the range of 250–500V, the proper value of L_B is chosen equal to 50 μH. Regarding the obtained characteristic impedance of Z_r, the value of L_{r1} and C_{r1} are calculated as follows:

$$L_{r1} = \frac{Z_r}{2\pi f_s} = 39.7\ \mu\text{H} \tag{26}$$

$$C_{r1} = \frac{1}{2\pi f_s Z_r} = 16\ \text{nF} \tag{27}$$

Selecting suitable values for C_{r2} and L_{r2} requires a tradeoff between the main switches ZVS range and RMS current. According to (21), C_n has a greater influence on the I_{Lr1} amplitude rather than L_n, and small C_{r2} values provides better ZVS condition. After some iterations, the proper values of C_n = 1.25 and L_n = 1 are selected. Therefore, the C_{r2} and L_{r2} values are obtained 20 nF and 39.7 μH respectively.

B. RESULTS

A 200 kHz prototype of the proposed LED driver is implemented and tested. The prototype circuit is shown in Fig. 6, and the control block diagram of the proposed converter is presented in Fig. 7. Due to the integration of the boost and LCCL resonant converter switches, the duty cycles of S_1 and S_2 are complementary, similar to those of a half-bridge inverter. According to this block diagram, a basic PWM controller is adopted to regulate the output current. Therefore,

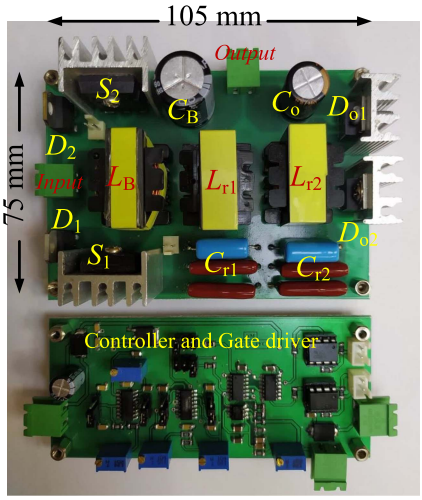

FIGURE 6. Prototype converter picture.

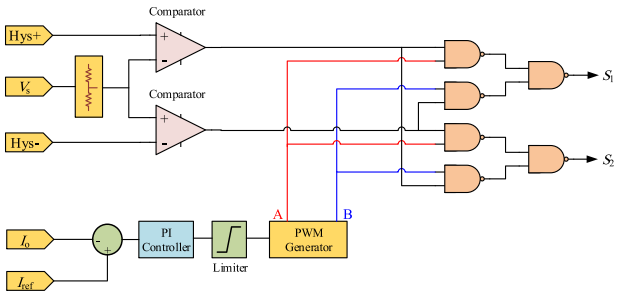

FIGURE 7. Control circuit block diagram.

based on the output current level of the converter, suitable complementary PWM signals with the required duty cycle are generated at the output terminals A and B.

A set of NAND logic gates, along with comparators, is used to identify the positive and negative half-cycles of the input voltage. Consequently, the main and synchronous switches are recognized in each half-cycle, and the appropriate gate signals are applied. It is worth noting that one of the main problems of the conventional totem pole boost PFC is the occurrence of current spikes on the main switches during the input voltage zero crossing. These current spikes are caused by several factors, including the reverse recovery of the switches body diodes, the reverse recovery of D_1 and D_2, sudden charging and discharging of the switches output capacitance, and the abrupt change in the switching sequence [27].

In this paper, a hysteresis region around the zero-crossing of the input voltage is created using two comparators. In this method, when the amplitude of the input voltage enters the hysteresis range, all switches are turned off. After passing through the near-zero voltage amplitude and the beginning of the next half-cycle, the main switches are activated again, and the gate signals are applied. In the control block diagram shown in Fig. 7, the reference voltages Hys+ and Hys- indicate the reference voltage levels of this hysteresis range. By using

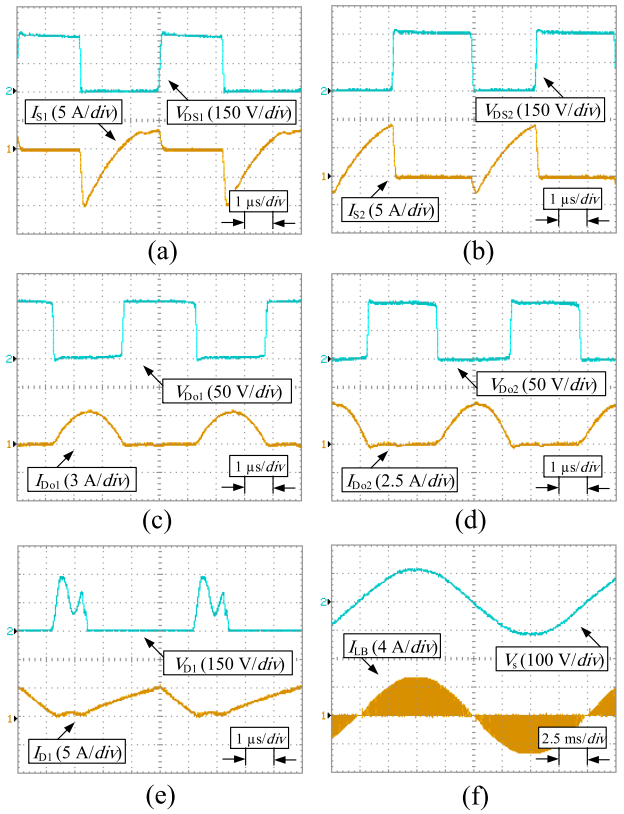

FIGURE 8. Experimental waveforms of semiconductor devices at 80 V_{RMS} input voltage: (a) S_1, (b) S_2, (c) D_{o1}, (d) D_{o2} and (e) D_1, and (f) Experimental waveforms of input voltage and current.

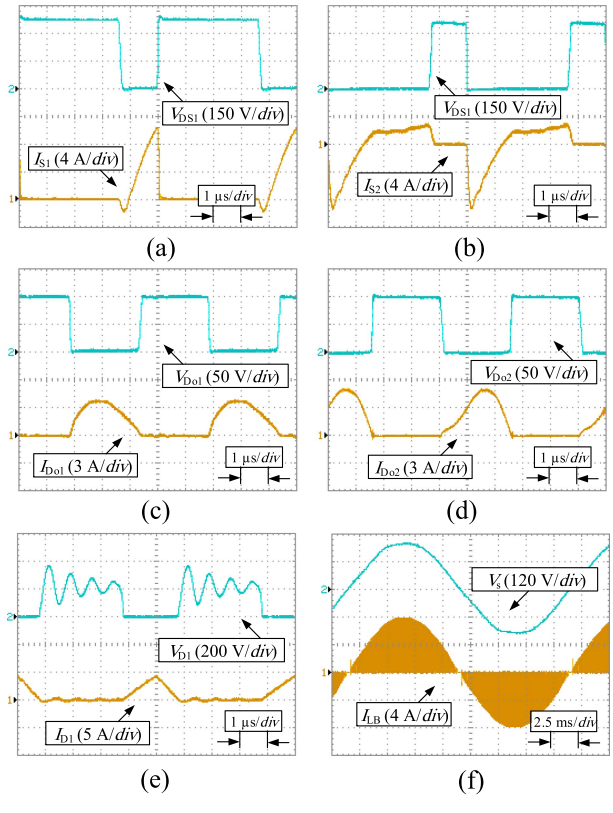

FIGURE 9. Experimental waveforms of semiconductor devices at 135 V_{RMS} input voltage: (a) S_1, (b) S_2, (c) D_{o1}, (d) D_{o2}, (e) D_1, and (f) Experimental waveforms of input voltage and current.

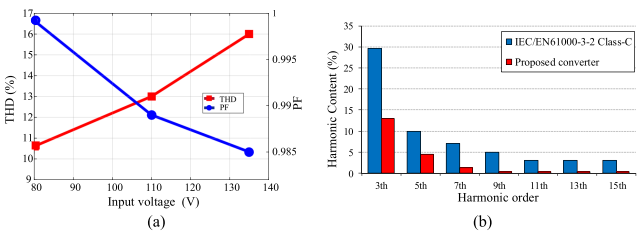

FIGURE 10. (a) Input current THD and PF, and (b) Comparison graph of input current harmonic content.

this method, it is possible to alleviate the occurrence of current spikes on the switches.

The experimental waveforms of the semiconductor devices for the minimum and maximum input voltage levels of 80 and 135 V_{RMS} are presented in Figs. 8 and 9, respectively. According to According to Figs. 8(a), (b), 9(a) and (b), the ZVS operation of the main switches is maintained for the entire input voltage range, and the voltage stress on S_1 and S_2 is limited to V_{CB}. Additionally, as observed in Figs. 7(c), 8(d), (e), 9(c), (d), and 9(e), the ZCS turn-off condition is fully realized for the output diode and the totem pole boost converter diodes, which alleviates reverse recovery loss. The voltage stress on D_1 and D_2 is equal to V_{CB}, while the voltage stress on D_{o1} and D_{o2} is equal to the output voltage of 100V. Furthermore, Figs. 8(f), and 9(f) illustrate the proposed converter input voltage waveform and the input current waveform without the input LC filter. The input current THD and PF for different input voltages are presented in Fig. 10(a), and the input current harmonic content of the proposed converter is compared with the IEC/EN61000-3-2 standard limit in Fig. 10(b). As observed, all harmonic levels of the input current fully satisfy the IEC/EN61000-3-2 Class-C standard. The efficiency diagram versus output power and the detailed loss analysis for different input voltage levels are also illustrated in Fig. 11(a) and (b), respectively. According to these figures, the totem pole boost PFC converter and output diodes have the most power losses than the other components, and the maximum full load efficiency is 96.4% at 135 V_{RMS} input voltage.

C. COMPARISON

A comparison between the proposed converter and similar bridgeless AC-DC converters in terms of component count, semiconductor voltage stress, soft switching operation, input current THD, input voltage range, control method, and reported full-load efficiency is summarized in Table 2. In In [11], the LLC converter and interleaved boost topology are merged to construct a single-stage AC-DC converter. To reduce the DC-Link voltage, both pulse frequency modulation and duty cycle control are adopted in In [11]. However, the component count is increased. The improved topology

TABLE 2. Comparision of the Proposed Single Stage LED Driver and Other Prominent Counterparts

Characteristics		Proposed	[11]	[12]	[13]	[14]	[16]	[24]	[25]	[26]
Number of	Switches	2	4	2	2	2	2	2	2	4
	Diodes	4	8	6	8	10	7	7	8	4
	Magnetics	3	4	5	4	5	3	4	4	3
	Capacitors	4	3	5	5	8	3	5	4	2
Inherent CC characteristic		Yes	No	No	No	No	No	No	No	No
Soft-switching		ZVS	ZVS	ZVS	ZVS	ZVS	ZVS	ZVS	ZCS	No
Control method		PWM	PFM-PWM	PFM	PFM	PFM	PFM	PFM	PFM	PWM
Input voltage (V_{RMS})		80-135	85-265	110	180-260	220	220	180-250	185-265	85-110
DC-Link voltage (V)		250-500	240-500	330	290-410	360	-	278-386	260-400	-
Switch voltage stress (V)		500	500	330	410	360	1200	386	400	-
Efficiency (%)		96.4	91	92.8	93.3	92.3	89.5	91.4	89.4	93.6
Nominal power (W)		100	300	100	100	100	200	150	50	100

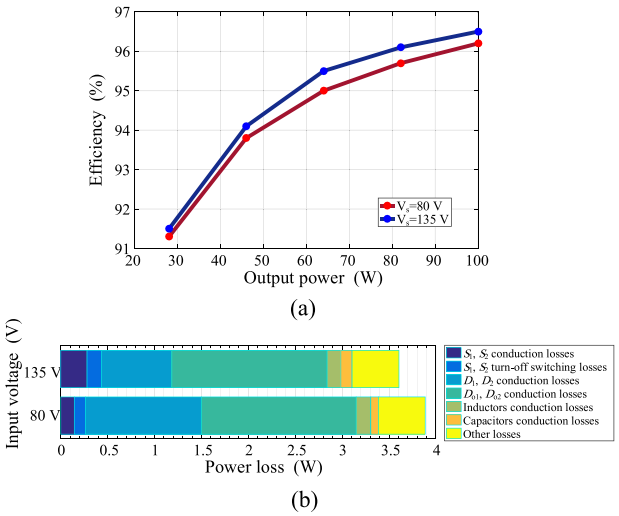

FIGURE 11. (a) Converter efficiency, and (b) Loss distribution at 80 V_{RMS} and 135 V_{RMS} input voltages.

presented in In [12] and In [14] employs a CLCL resonant network instead of the conventional LLC. However, PFM control is used, which features a constant output voltage. Additionally, despite the bridgeless structure, the existence of diodes in the power flow path reduces efficiency. In [13], a cascaded boost converter is employed before the LLC stage to reduce the DC-Link voltage. However, despite having a similar DC-Link voltage level to the proposed converter, the efficiency is reduced due to the cascaded structure and the increased component count. In [16], an improved buck-boost PFC converter is placed after a bridge rectifier, which improves the input current power factor (PF) and reduces the DC-Link voltage compared to the boost PFC. However, due to the bridge rectifier, efficiency is compromised, and the LLC stage is not suitable for wide input and output range operation. A Class E resonant converter and LLC are combined in the single-stage converter described in [24]. This topology is frequency-controlled, and the ZVS condition of the main switches, as well as the DC-Link voltage level, are sensitive to input voltage and load conditions. In [25], a coupled inductors-based series LC resonant converter is proposed for a single-stage AC-DC converter. However, the main switches operate at ZCS. The bridgeless boost PFC converter presented in [26] has a power ripple processing characteristic and employs a lower component count than single-stage converters. However, it is not suitable for wide-range LED driver applications due to its constant output voltage operation.

V. CONCLUSION

A novel single-stage bridgeless PFC converter using an LCCL resonant network is proposed for street LED lighting application. This converter, which features fixed-frequency operation and LCCL resonant characteristics, enables the delivery of a constant output current of 1 A to an LED string over a wide output voltage range of 40–100 V. The output current is regulated by the main switches duty cycle, ensuring a stable and efficient operation. The experimental results from a 100 W prototype demonstrate that the input voltage and current are in phase and nearly sinusoidal, with low input current THD that meets the IEC61000-3-2 standard. Furthermore, the converter achieves zero-voltage switching (ZVS) for the main switches and zero-current switching (ZCS) for rectifier diodes across the entire input voltage range, resulting in a maximum efficiency of 96.4% at full load. Additionally, detailed loss distribution results are provided for 80 and 135 V_{RMS} input voltage levels, highlighting the converter performance and efficiency.

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