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Investigating the Bounds of Quality Factor for Class-E Series-Tuned RF Power Amplifiers and Their Computer-Aided Optimization

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Abstract: This paper presents a comprehensive analysis of Class-E series-tuned radio-frequency power amplifiers (RFPAs), focusing on their design and optimization for high efficiency and performance. However, achieving optimal performance involves navigating trade-offs among efficiency, bandwidth, harmonic suppression, output power capability, and device stress. This work examines the trade-offs involved in the series-tuned ($L_s - C_s$) network and establishes the bounds for its quality factor using computer-aided harmonic balance (HB) simulations. Additionally, it explores optimal harmonic termination strategies to enhance the performance and efficiency of the design. Finally, a novel methodology using harmonic termination is proposed, simplifying the design process by eliminating the need for traditional load-pull extraction methods.

Keywords: RFPA; Class-E; efficiency; harmonics; simulations

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1. Introduction

Radio-frequency power amplifiers (RFPAs) play a crucial role in various scientific applications, extending from space exploration to everyday technologies. They are integral to driving acoustic optical tunable filters (AOTFs) used in space exploration [1] and are also employed in induction cooking and medical applications, such as magnetic resonance imaging (MRI) [2]. However, their substantial power consumption contributes notably to overall power dissipation, raising concerns about energy efficiency in RF systems. Furthermore, RFPAs generate harmonics, due to the inherent non-linearity of the transistor that can significantly interfere with the desired output signal. The heat produced by these amplifiers [3] can also adversely affect the precision of measurements in instruments where optical performance is critical [4,5].

In space-based applications, managing the thermal impact of RFPAs is crucial to maintaining the accuracy and reliability of optical measurements [6]. The RF signal used to drive these instruments generally falls within the medium frequency (MF) band, high frequency (HF) band (3–30 MHz), and very high frequency (VHF) band (30–300 MHz). However, designing RFPAs for these frequency ranges presents unique challenges, as the use of transmission lines becomes impractical. As a result, employing discrete or lumped *R*, *L*, and *C* components is crucial to ensure efficient operation and performance at these frequencies.

In this context, Class-F and Class-E amplifiers theoretically offer an efficiency of up to 100%. However, achieving the desired square waveform in Class F amplifiers requires the use of multiple resonators [7], complicating the design. As a result, Class-E amplifiers emerge as a promising alternative, providing a simpler yet highly efficient solution for RF power amplification.

From a technological perspective, gallium nitride (GaN) has emerged as a superior material for such high-efficiency power amplification, surpassing conventional materials

like silicon. GaN's intrinsic properties, particularly its substantial sheet charge density, facilitate the generation of high current densities [8]. This enables the reduction of transistor dimensions, leading to an exceptional watt-per-millimeter ratio of the gate periphery. Furthermore, the high saturated drift velocity of GaN contributes to achieving substantial saturation current densities and higher output power per unit gate periphery [9]. Consequently, GaN transistors exhibit lower output capacitance and drain-to-source resistance per watt, making them ideal for switch-mode amplifiers like Class-E and Class-F designs.

These combined attributes make AlGaN/GaN HEMTs highly suitable for high-efficiency RF applications and deliver excellent performance even in demanding environments. Comprehensive reviews of GaN-based device capabilities, particularly in the context of high-power and high-frequency applications, are provided by Pengelly et al. [10] and Husna et al. [11].

Building on the advantages of GaN-based devices, the design of Class-E RFPAs involves two widely recognized load network topologies, one where the effect of the finite DC feed is ignored [12] and another considering these effects [13]. Nevertheless, both configurations incorporate a series resonator, operating under the assumption of a high-quality factor (Q_s) to force the fundamental current into the circuitry [14].

Although some studies explored Q_s and bandwidth in specific contexts [15], these findings lacked broader generalizations and comparisons across various topologies. Analytical expressions for Class-E amplifiers with arbitrary duty cycles were introduced in [16] and later extended by [17] to account for varying Q_s. However, these equations often yield ambiguous values for Q_s, indicating the need for more comprehensive methodologies.

Similarly, Sokal and Raab [18] offered valuable insights into harmonic control and design criteria for harmonic suppression networks, but the calculations were complex and not widely applicable. Additionally, Sheikhi et al. [19] developed analytical expressions for 2nd-harmonic tuning parallel to the load, although the comparative analysis was insufficient. Furthermore, the study did not adequately address the impact of the efficiency-bandwidth trade-off on performance metrics, highlighting the need for a more generalized approach to understanding the theoretical limits of Q_s across different topologies and harmonic termination strategies. In contrast, this work employs a computer-aided harmonic balance (HB) analysis to offer a generalized approach to finding the bounds.

This work begins with mathematical modeling to derive the closed-form design equations for the Class-E RFPA, considering both infinite and finite DC feeds, as presented in Section 2. In the later sections, computer-aided analytical modeling is used to explore the impact of the series resonant circuit ($L_s - C_s$), tuned to the design frequency, which is critical for optimizing the performance of the RFPA.

It introduces the key design parameter quality factor, Q_s, which is a design parameter that affects Class-E performance and discusses its trade-offs with various performance metrics. Section 3 establishes a novel methodology for determining the bounds of Q_s, ($Q_{\text{min}} < Q_s \leq Q_{\text{sat}}$) through computer-aided HB simulations.

This study further extends to a detailed investigation of harmonic termination and its impact on improving efficiency and bandwidth, along with performance metrics in Section 4. Based on these analytical equations, a novel methodology is proposed in Section 5 for designing optimal Class-E RFPAs. This approach aims to eliminate the need for time-consuming load-pull extraction and unnecessary circuit optimizations.

This paper concludes by presenting simulated results and discussions that demonstrate the development of highly efficient Class-E RFPAs operating at 145 MHz, delivering 1 watt of output power. The results obtained underscore the robustness and effectiveness of the proposed methodology. The simulations were carried out using the nonlinear, large signal model of the CGH40010 transistor [20].

2. Mathematical Modeling of Class-E Series-Tuned RFPAs

This section explores the mathematical modeling of Class-E RFPAs. For simplicity, assumptions include a 50% switching duty cycle and zero on-resistance of the transistor.

The zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) are given by Equations (1) and (2) [21].

$$V(\omega t)|_{t=2\pi} = 0 \tag{1}$$

$$\left.\frac{dV(\omega t)}{d(\omega t)}\right|_{\omega t=2\pi} = 0 \tag{2}$$

Based on existing literature, two commonly used topologies are addressed in this work [22]: Topology 1, which assumes an infinite DC feed. It uses a DC choke to provide very high resistance to the RF signal, and Topology 2, which incorporates a finite DC feed. Topology 2 offers an infinite number of potential solutions; however, this work examines two cases, denoted as Topology 2.1 and Topology 2.2, to highlight key design considerations.

2.1. Class-E Load Network Topology with Infinite DC Feed

The schematic of a Class-E-tuned switched-mode power amplifier with a series-tuned resonator is shown in Figure 1a. The load network encompasses a parallel capacitance ($C = C_{dev} + C_{ext}$), which represents the device's inherent capacitance C_{dev}, along with any external capacitance C_{ext}, ensuring the current in and out of the switch-capacitor combination. For simplification, C_{dev} is neglected in this work.

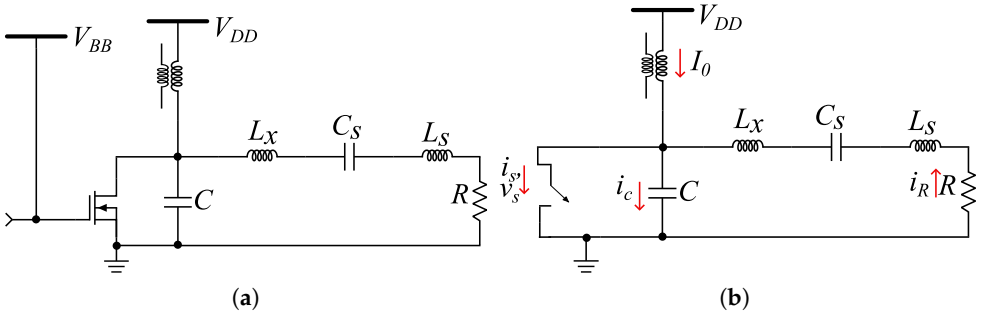

Figure 1. A Class-E amplifier with infinite DC feed (**a**) schematic and (**b**) its equivalent circuit, where the arrows show the direction of current flow.

The series inductance L_x produces a reactance jX with a series resonant circuit ($L_s - C_s$) tuned at the design frequency, f_o, which is then finally connected to the optimal load resistance, R. The supply voltage is V_{DD} and V_{BB} is the biasing voltage. i_s and v_s are the voltage and current in the ideal switch respectively. i_C, I_0, and i_R are the currents flowing through the capacitor C, RF choke, and load R, respectively. The equivalent circuit is shown in Figure 1b. The current flowing through the load is given by Equation (3).

$$i_R(\omega t) = I_R \sin(\omega t + \phi) \tag{3}$$

where ϕ is the initial phase shift, I_R represents the peak amplitude of the current, and $\omega = 2\pi f$.

With the initial on-state condition, the DC can be given as $I_0 = -I_R \sin(\phi)$, and the switch current is given by Equation (4).

$$i_s(\omega t) = \begin{cases} I_R[\sin(\omega t + \phi) - \sin(\phi)] & 0 \le \omega t \le \pi \\ 0 & \pi < \omega t \le 2\pi \end{cases} \tag{4}$$

With the switch being off, the current through the capacitor is given by Equation (5).

$$i_c(\omega t) = I_0 + I_R \sin(\omega t + \phi) \tag{5}$$

and the switch voltage is given by Equation (6), which can then be expanded to Equation (7).

$$v_s(\omega t) = \frac{1}{\omega C}\int_{\pi}^{\omega t} i_c(\omega t)d(\omega t) \tag{6}$$

$$v_s(\omega t) = \begin{cases} 0 & 0 \le \omega t \le \pi \\ -\frac{I_R}{\omega C}[\cos(\omega t + \phi) + \cos(\phi) - \omega t - \pi \sin(\phi)] & \pi < \omega t \le 2\pi \end{cases} \tag{7}$$

The primary objective of the problem is to find the unknown parameters I_R and ϕ. Applying the ZVS condition given by Equation (1), the unknown values can be calculated as $\phi = 57.5180$ and $I_{R,max} = 2.8621 I_0$. Finally, the optimal load resistance R and the values of L_x and C can be calculated using Equations (8)–(10).

$$R = 0.5768\frac{(V_{DD})^2}{P_{out}} \tag{8}$$

$$L_x = \frac{1.1525R}{\omega_0} \tag{9}$$

$$C = \frac{0.1836}{R\omega_0} \tag{10}$$

2.2. Class-E Load Network Topology with Finite DC Feed

The schematic of a Class-E-tuned switched-mode power amplifier with a finite DC feed is shown in Figure 2a. The load network consists of a feed inductance L, which supplies current to the transistor. The series reactance jX is connected to a series resonant circuit $(L_s - C_s)$ that is tuned to the design frequency f_o. This configuration is then connected to the optimal load resistance R.

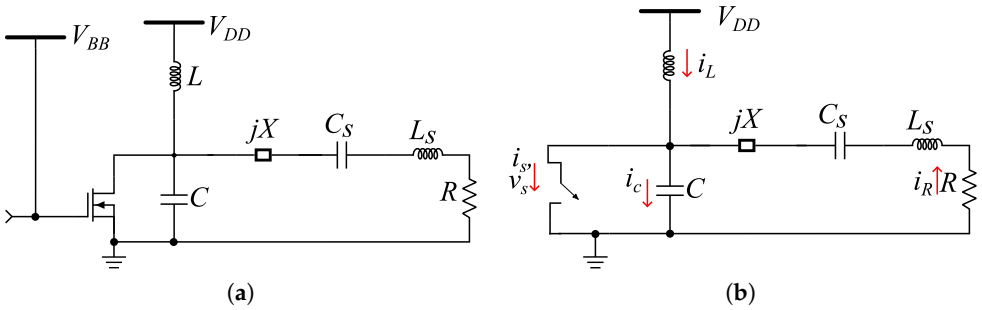

Figure 2. Class-E with finite DC feed (**a**) schematic and (**b**) its equivalent circuit, where the arrows show the direction of current flow.

Due to the finite inductance L, the supply current becomes time-varying, denoted as $i_L(\omega t)$, in contrast to the previous case where it was represented by a constant value I_0. The equivalent circuit is shown in Figure 2b. The load current is given by Equation (11).

$$i_R(\omega t) = I_R \sin(\omega t + \phi) \tag{11}$$

where ϕ is the initial phase shift and I_R is the peak amplitude of the current. For the time interval $0 \le \omega t < \pi$, the switch is on and the current flowing through the switch can be given by Equation (12).

$$i_s(\omega t) = \begin{cases} \frac{V_{DD}}{\omega L}\omega t + I_R[\sin(\omega t + \phi) - \sin(\phi)] & 0 \le \omega t \le \pi \\ 0 & \pi < \omega t \le 2\pi \end{cases} \tag{12}$$

When the switch is off, in the interval $\pi < \omega t \leq 2\pi$, the current through the switch becomes zero and the current through the capacitor can be given by $i_c(\omega t) = i_L(\omega t) + i_R(\omega t)$, with Equation (13) denoting the initial condition for the feed inductance L.

$$i_L(\pi) = \frac{V_{DD}\pi - \omega L\ I_R \sin(\phi)}{\omega L} \tag{13}$$

The switch voltage can be found by solving the differential equation as reported in [22]. The solution is provided by Equation (14), as follows:

$$v_s(\omega t) = \begin{cases} 0 & 0 \leq \omega t \leq \pi \\ V_{DD}[1 + C_1\cos(q\omega t) + C_2\sin(q\omega t) - \frac{q^2 p}{1-q^2}\cos(\omega t + \phi)] & \pi < \omega t \leq 2\pi \end{cases} \tag{14}$$

Without loss of generality, and using the initial off-state conditions, Equations (15)–(18) are obtained.

$$C_1 = -(\cos q\pi + q\pi\ \sin q\pi) - \frac{qp}{1-q^2}\left[q\cos(\phi)\cos(q\phi) - (1-2q^2)\sin(\phi)\sin(q\phi)\right] \tag{15}$$

$$C_1 = -(\sin q\pi - q\pi\ \cos q\pi) - \frac{qp}{1-q^2}\left[q\cos(\phi)\cos(q\phi) + (1-2q^2)\sin(\phi)\sin(q\phi)\right] \tag{16}$$

where q and p are given by Equations (17) and (18), respectively.

$$q = \frac{1}{\omega\sqrt{LC}} \tag{17}$$

$$p = \frac{\omega L\ I_R}{V_{DD}} \tag{18}$$

With variable q as a free parameter, the values for the unknown parameters, ϕ, and p, can be calculated, applying the ZVS and ZVDS conditions. Two equations with two unknowns can be solved using Equations (19) and (20) to obtain the required values, as follows:

$$-C_1 q\sin(2q\pi) + C_2 q\cos(2q\pi) + \frac{q^2 p\sin\phi}{1-q^2} = 0 \tag{19}$$

$$-C_1 q\sin(2q\pi)q^2 + C_2 q\cos(2q\pi)q^2 + \frac{q^2 p\cos\phi}{1-q^2} = 0 \tag{20}$$

The parameter, q, imposes limitations owing to the extensive design space and complex design equations. A comprehensive tutorial addressing these considerations was conducted by Casallas et al. [23]. This is simplified in this work by evaluating the following two scenarios: when $jX = L_x$ ($q = 0.5$) and when $jX = 0$ ($q = 1.412$).

- Case a: $jX = L_x$, known as the *sub-harmonic* with $q = 0.5$ [22]. Equations (19) and (20) can be solved to obtain the values of $p = 21.3$ and $\phi = -30.2$. This configuration is referred to as Topology 2.1 in this work. Finally the closed-form expressions for R, L, C and L_x can be calculated as follows:

$$R = 0.635\frac{(V_{DD})^2}{P_{out}} \tag{21}$$

$$L = 18.9\frac{R}{\omega} \tag{22}$$

$$C = \frac{0.212}{\omega R} \tag{23}$$

$$L_x = 1.058\frac{R}{\omega} \tag{24}$$

- Case b: $jX = 0$, known as the parallel class with $q = 1.412$ [24]. Similarly, Equations (19) and (20) can be solved to obtain the values of $p = 1.210$ and $\varphi = 15.155$. This configuration is referred to as Topology 2.2 in this work. The values for R, L, and C can be calculated as follows:

$$R = 1.365\frac{(V_{DD})^2}{P_{out}} \tag{25}$$

$$L = 0.732\frac{R}{\omega} \tag{26}$$

$$C = \frac{0.685}{\omega R} \tag{27}$$

3. Computer-Aided Analytical Modeling of Class-E Series-Tuned RFPAs

3.1. Key Design Parameter: Quality Factor and Its Trade-Offs

The resonant quality Q factor is a dimensionless parameter that describes the performance of a resonant circuit, such as an L-C tank circuit. It quantifies the sharpness of the resonance peak and the efficiency of the circuit. A higher Q value indicates a narrower bandwidth and greater selectivity, suggesting that the circuit has less energy loss and superior performance at its resonant frequency. The quality factor (Q_s) of the series-tuned tank circuit, which consists of an inductor L_s and a capacitor C_s, is defined by Equations (28) and (29), regardless of the specific Class-E topology used.

$$C_s = \frac{1}{\omega_0 Q_s} \tag{28}$$

$$L_s = \frac{Q_s}{\omega_o} \tag{29}$$

HB simulations are performed using the commercially available Keysight Advanced Design System (ADS) tool [25]. The ADS simulation setup of Topology 2.2 is depicted in Figure 3. For a comparative analysis, the input parameters are normalized to $f = 1$, $V_{cc} = 1$, and $P_{out} = 1$. This setup utilizes an input source, $V_{f\_pulse} = 1$, representing a voltage source with a Fourier series expansion of a periodic rectangular wave, characterized by various pulse widths and duty ratios, within an HB simulator setup. All other important parameters required to run the simulation setup are shown in Figure 3.

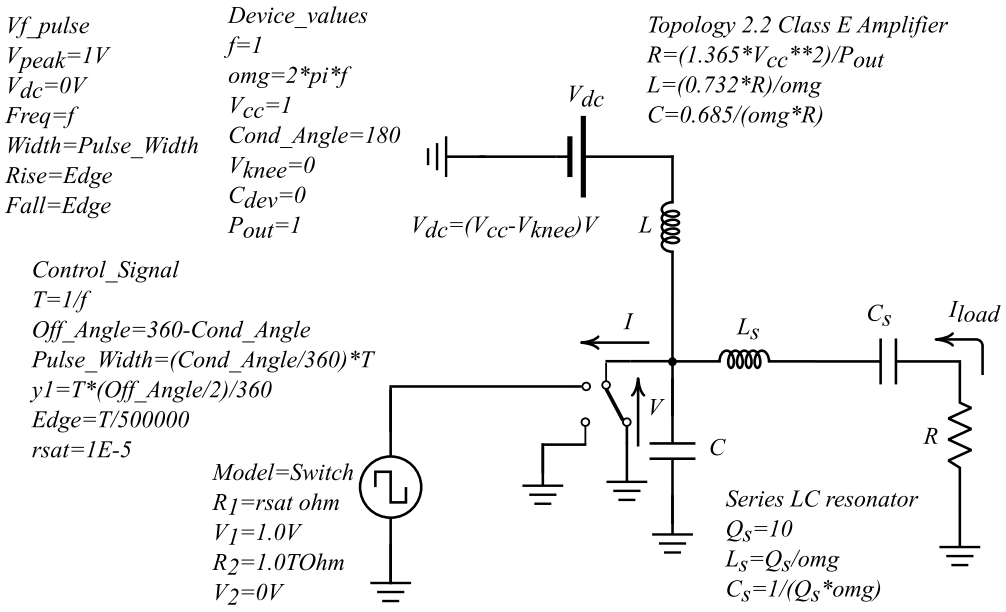

Figure 3. ADS simulation setup for idealized topology 2.2, Class-E.

3.2. Minimum Value of Q_s

The HB simulation was conducted for all three topologies. The efficiency versus Q_s plots shown in Figure 4 demonstrate exponential behavior, which can be modeled by Equation (30).

$$y = a + be^{-x} \tag{30}$$

where y denotes the efficiency and x represents Q_s.

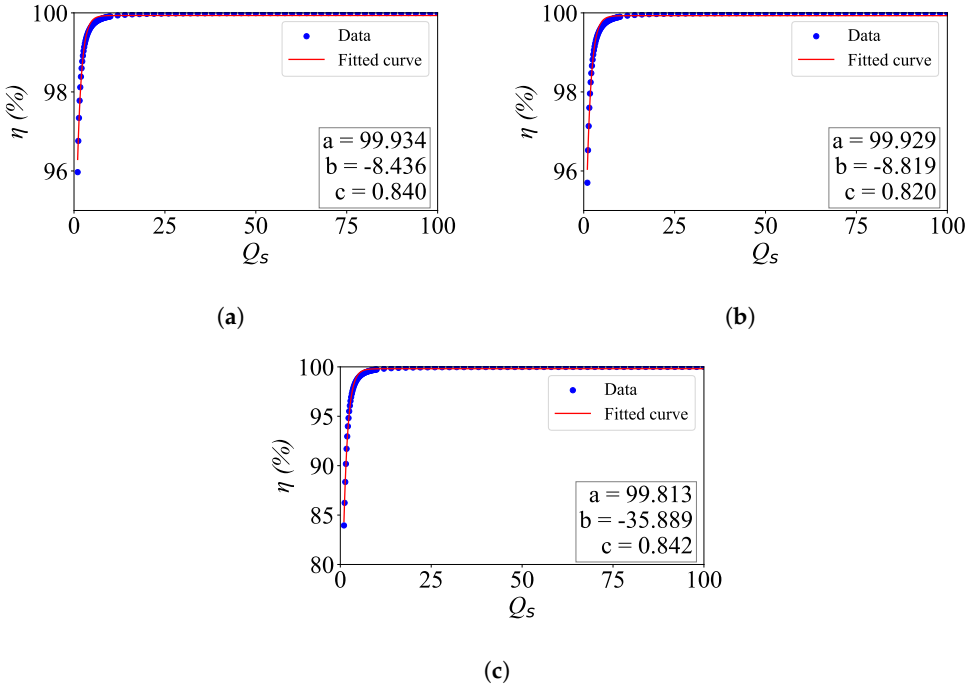

Figure 4. Efficiency vs. Q_s with curve fitted approximation for Q_{min} calculation for (**a**) Topology 1 (**b**) Topology 2.1, and (**c**) Topology 2.2.

The values of a and b were determined for the three topologies using the `curve_fit` tool from the `scipy` library in Python [26]. Optimal parameter values and their estimated covariances were returned by the function. The curve-fitting model was found to exhibit behavior almost identical to that of the simulation data, as shown in Figure 4.

Both Topology 1 and Topology 2.1 exhibit similar behavior, while Topology 2.2 has a different b value, as revealed by the data modeling. Nevertheless, for all three cases (Topologies 1, 2.1, and 2.2), the value of a is approximately 99.

The term Q_{min} is now defined as the value of Q_s, where a stable efficiency of at least 99% is achieved, assuming a 1% numerical error due to the HB simulation [27]. According to the requirements, this efficiency can be adjusted but must be no less than 99%. To determine Q_{min}, the curve-fitting model is used to solve Equation (31) for each topology respectively.

$$99 = a + be^{-cQ_{min}} \tag{31}$$

3.3. Maximum Value of Q_s

To further investigate the effect of the quality factor Q_s of the series resonator, the efficiency versus angular frequency is plotted. The variations on the x-axis are expressed as a $\pm$ percentage deviation from the designed angular frequency, using a normalized scale, as shown in Figure 5.

Additionally, performance metrics are given in Table 1, including the maximum peak voltage and current and the maximum output power capability, c_p defined by Equation (32), as follows:

$$c_p = \frac{P_{out}}{V_{peak,n} \cdot I_{peak,n}} \tag{32}$$

where P_{1out} is the output power [28]. Harmonic levels up to the third order are also included. These metrics were also compared with mathematical models reported in previous literature studies to validate the accuracy of the simulation.

Table 1. Various performance metrics for the three topologies compared to previous literature studies (references shown in square brackets).

Topology	Q	V_{peak}	I_{peak}	η (%)	c_p	2nd (dBc)	3rd (dBc)
1	3	3.839	2.844	99.231	0.09726	−18.929	−44.67
	5	3.739	2.85	99.684	0.09769	−21.846	−68.545
	6	3.712	2.852	99.773	0.0977	−23.576	−70.202
	10	3.654	2.855	99.911	0.09796	−28.355	−77.482
	25	3.6	2.859	99.983	0.09803	−36.687	−100.472
	50	3.581	2.86	99.994	0.09812	−42.848	−105.068
[22]	100	3.571	2.861	99.996	0.09807	−48.942	−104.933
2.1	3	3.843	2.82	99.158	0.097810	−15.887	−62.902
	5	3.743	2.827	99.653	0.09819	−20.819	−61.925
	6	3.716	2.829	99.75	0.09826	−22.565	−63.331
	10	3.659	2.833	99.902	0.09839	−27.381	−68.67
	25	3.605	2.837	99.981	0.09855	−35.753	−79.715
	50	3.586	2.839	99.993	0.09852	−41.93	−87.778
[22]	100	3.577	2.84	99.996	0.09853	−48.032	−95.024
2.2	3	3.967	2.76	96.981	0.09699	−7.428	−52.801
	5	3.851	2.644	98.919	0.10263	−12.166	−41.025
	6	3.818	2.618	99.255	0.10384	−14.172	−41.64
	10	3.751	2.572	99.736	0.10603	−18.749	−44.228
	25	3.689	2.538	99.957	0.10776	−27.214	−51.474
	50	3.668	2.525	99.987	0.10840	−33.435	−57.373
[14]	100	3.658	2.512	99.995	0.10904	−39.561	−63.352

Device stress is normalized relative to the supply voltage and is a crucial metric for assessing device reliability, as the peak voltage and peak current at the device can be up to $V_{peak,n}$ multiplied by the supply voltage and $I_{peak,n}$ multiplied by the supply current, respectively. Without loss of generality, the device referred to here is a transistor. If the breakdown voltage of the device is lower than this, the device is unsuitable for constructing the Class-E RFPA.

Based on these observations, an additional parameter to determine the upper bound of Q_s, referred to as $Q_{\textbf{sat}}$ in this work, is introduced. This upper bound ensures that the RFPA achieves its maximum output power capability (c_p). It is evident from Table 1 that while efficiency levels reach at least 99% at Q_{min}, the RFPA was not operating at its maximum c_p. Additionally, harmonic suppression was insufficient, highlighting the need to introduce an upper bound for Q_{sat}.

As shown in Figure 6, c_p also exhibits exponential behavior leading to saturation. Therefore, a similar methodology was employed using curve-fitting techniques to determine this upper bound but with some additional constraints. Mathematically, c_p is modeled using Equation (33), as follows:

$$c_p = a + be^{-cQ_s} \tag{33}$$

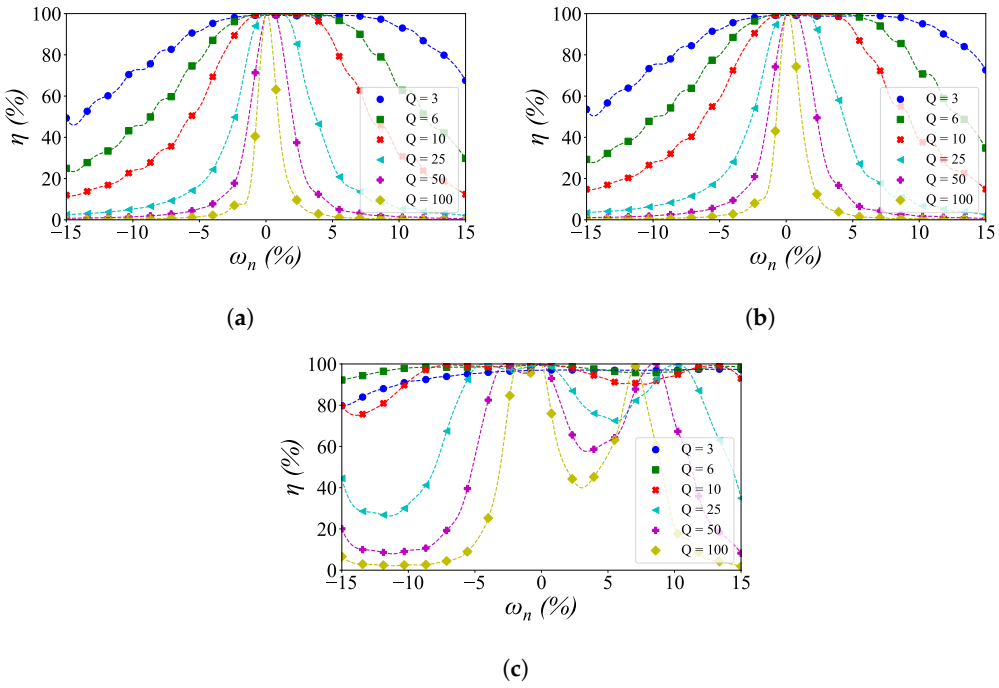

Figure 5. Efficiency vs. normalized angular frequency for various Q_s. (**a**) Topology 1, (**b**) Topology 2.1, and (**c**) Topology 2.2.

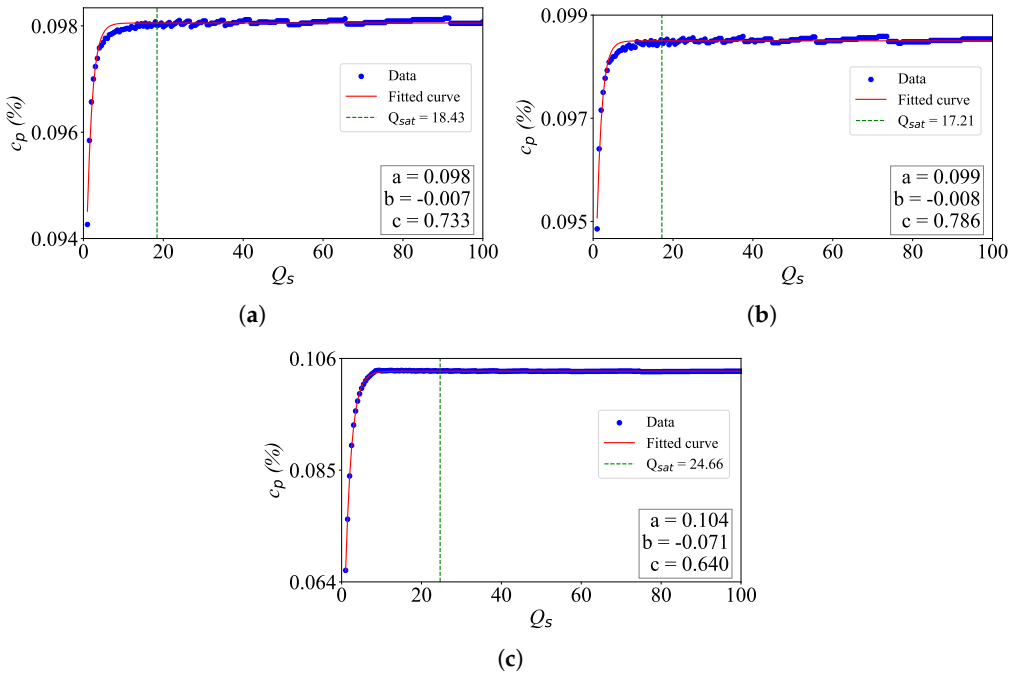

Figure 6. Q_{sat} model for (**a**) Topology 1, (**b**) Topology 2.1, and (**c**) Topology 2.2.

The condition of saturation arises when $c > 0$. Since the HB method solves nonlinear differential equations and only provides approximate solutions due to numerical errors, this upper bound is defined using perturbation theory with a small parameter ϵ [29]. As the value of Q_s increases, $e^{-cQ_s} \to 0$. For sufficiently large values of Q_s, c_p will exhibit negligible variation. This condition is defined by the inequality given in Equation (34).

$$e^{-cx} \leq \epsilon \tag{34}$$

where ϵ is a small value chosen corresponding to the accuracy requirement. The saturation point Q_{sat} is defined as the point where the inequality (34) becomes an equation.

$$e^{-cQ_{sat}} = \epsilon \tag{35}$$

By rearranging Equation (35), Equation (36) is obtained, which determines the value of Q_{sat}.

$$Q_{sat} = -\frac{ln(\epsilon)}{c} \tag{36}$$

Increasing Q_{sat} beyond this point does not enhance efficiency or other performance metrics significantly but instead narrows the effective bandwidth of the RFPA. The value of ϵ was set to 10^{-8} in this work.

The bounds for all three topologies are given in Table 2. Additionally, time-domain waveforms obtained from the ADS simulation for all three topologies are shown in Figure 7. These waveforms verify the non-overlapping voltage and current characteristics of standard Class-E operation.

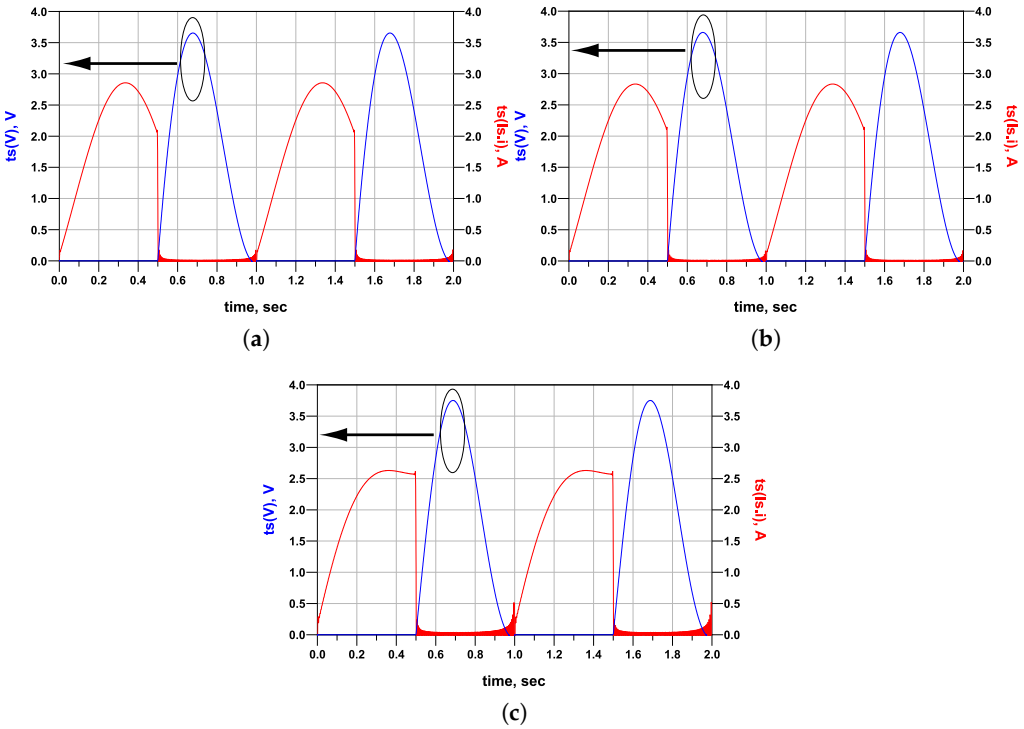

Figure 7. Time-domain normalized voltage (in blue, its corresponding axis is marked by the arrow) and current (in red) waveforms from ADS simulation results for (**a**) Topology 1, (**b**) Topology 2.1, and (**c**) Topology 2.2.

Table 2. Q_{min} and Q_{sat} for different topologies.

Topology	Q_{min}	Q_{sat}
1	2.6207	18.4306
2.1	2.7451	17.2098
2.2	4.4976	24.6607

This analysis illustrates the significant impact of effective harmonic suppression on the trade-offs between efficiency and bandwidth, as well as other critical performance metrics. Understanding and managing these trade-offs provides valuable insights into

optimizing the resonator's performance, particularly in the context of optimal Class-E series-tuned RFPAs.

A novel finding from this analysis is the relationship between the quality factor of the resonator and its impact on the amplifiers' overall performance, thereby defining the bounds on Q_s, which, to the authors' knowledge, has not been reported elsewhere. For optimal operation, Q_s must be carefully chosen within specific bounds, given by Equation (37), as follows:

$$Q_{min} < Q_s \leq Q_{sat} \tag{37}$$

where

Q_s: Quality factor of the resonator.
Q_{sat}: Saturation quality factor, defining the upper-performance limits.
Q_{min}: Minimum quality factor defining lower performance limits.

Increasing Q_s beyond Q_{sat} only degrades the efficiency-bandwidth response, making no significant improvement in the amplifier's performance. This inequality obtained through HB simulations establishes the fundamental bounds for Q_s, which can be applicable across various tuned topologies, guiding the design process to achieve the desired balance between efficiency, bandwidth, and overall performance.

It is important to note that the numerical values presented in this analysis, as reported in Table 2, are based on the assumption of normalized input parameters, as depicted in the simulation setup in Figure 3. Any variation in these normalized values will result in corresponding changes in the limits. Nevertheless, the techniques described in Sections 3.2 and 3.3 allow for the straightforward determination of these limits even under varying conditions.

3.4. Reactance Compensation Technique for Wide Bandwidth

The series resonator, consisting of L_s and C_s, can be replaced by L_0 and C_0, as defined by Equations (38) and (39):

$$L_0 = 1.026\frac{R}{\omega_0} \tag{38}$$

$$C_0 = \frac{1}{\omega_0^2 L_0} \tag{39}$$

This technique, commonly used to broaden the bandwidth in Class-E amplifiers, is known as the reactance compensation technique in standard literature [22]. In this paper, it will be referred to as Topology 2.2.1 without any loss of generality. The quality factor Q_s can then be expressed by Equation (40).

$$Q_{2.2.1} = 1.026R \tag{40}$$

By substituting the value of R from Equation (21) into Equation (40), $Q_{2.2.1}$ can be expanded into Equation (41),

$$Q_{2.2.1} = 0.65151\frac{(V_{DD})^2}{P_{out}} \tag{41}$$

With normalized values of $V_{DD} = 1$ and $P_{out} = 1$, $Q_{2.2.1} = 0.65151$ is obtained for this case. Since this topology is a subset of Topology 2.2, a comparison with the limits provided in Table 2 reveals that $Q_{2.2.1}$ does not fall within these bounds, indicating a potential compromise in the amplifier's performance.

The analysis reveals that Topology 2.2, when combined with the reactance compensation technique, achieves improvements in efficiency-bandwidth response but with certain trade-offs in performance metrics. This issue arises because the quality factor ($Q_{2.2.1}$) is lower than Q_{min}. This discrepancy leads to a significant reduction in theoretical efficiency, further constraining the amplifier's performance.

Despite these limitations, Topology 2.2.1 remains the most effective configuration for balancing efficiency and bandwidth. However, to address these limitations while adhering to the Class-E design equation, the addition of harmonic control circuitry is necessary, which will be discussed in the preceding section.

4. Modified Topology with Harmonic Control

The following section explores three strategies for incorporating harmonic tuning as shown in Figure 8.

i. Introducing a series resonator tuned to the 2nd and 3rd harmonics before the load resistance R.
ii. Transforming L_0 and C_0.
iii. Alternatively, a combination of both strategies.

These approaches aim to improve harmonic suppression while preserving the advantages of Topology 2.2.1 in balancing efficiency and bandwidth response. For the transformation of L_0 and C_0, there are four mathematically possible cases. Of these, only two yield valid solutions, as outlined below:

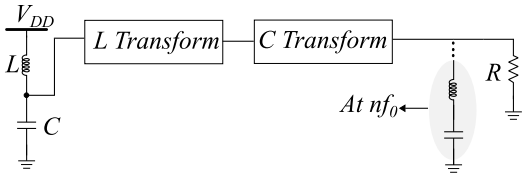

Figure 8. Possibilities of incorporating the harmonic tuning network.

The inductor L_0 and capacitor C_0 can be converted to an equivalent form as shown in Figure 9. This equivalent form consists of a parallel LC tank circuit, which can be tuned to resonate at $n\omega_0$ by applying Equation (42).

$$1 - n^2\omega_0^2 L_{pn} C_{pn} = 0 \tag{42}$$

Since there are multiple unknowns, additional equations can be constructed by applying the harmonic shorting condition at m, as given in (43).

$$\mathrm{Im}(Z_{\mathrm{net}}(m\omega_0)) = 0 \tag{43}$$

For most practical scenarios, considering harmonics up to the third order is sufficient [30]. With this, the following modifications are possible:

i. An inductor can be converted into an equivalent circuit consisting of another inductor in series with a parallel LC resonant circuit. The net impedance shown by Figure 9a is given by Equation (44)

$$Z_{\mathrm{net}}(j\omega) = j\omega L_{an} + \frac{j\omega L_{pn}^{L}}{1 - \omega^2 L_{pn}^{L} C_{pn}^{L}} \tag{44}$$

Two cases are possible:

(a) The parallel resonator is tuned to the 2nd harmonic and the net impedance is shorted at the 3rd harmonic. The different components are given by the following equations (refer to Appendix A.1 for the calculations):

$$L_{a2} = \frac{3}{8} L_0 \tag{45}$$

$$L_{p2}^{L} = \frac{15}{32} L_0 \tag{46}$$

$$C_{p2}^{L} = \frac{8}{15\omega_0^2 L_0} \tag{47}$$

(b) The parallel resonator is tuned to the 3rd harmonic, and the net impedance is shorted to the 2nd harmonic. This condition is not possible, as shown in Appendix A.1.

ii. Similar to an inductor, a capacitor can also be converted to a parallel LC resonant circuit connected by capacitance in series, as shown in Figure 9b. In this condition, the net impedance is given by Equation (48).

$$Z_{\text{net}}(j\omega) = \frac{1}{j\omega C_{an}} + \frac{j\omega L_{pn}^{C}}{1 - \omega^2 L_{pn}^{C} C_{pn}^{C}} \tag{48}$$

(a) The parallel resonator is tuned to the 2nd harmonic and the net impedance is shorted at the 3rd harmonic. This condition is also not possible as shown in Appendix A.2.

(b) The parallel resonator is tuned to the 3rd harmonic and the net impedance is shorted at the 2nd harmonic. The equivalent parameters are given by Equations (49)–(51) (Appendix A.2 contains the calculations):

$$C_{a3} = \frac{27}{32} C_0 \tag{49}$$

$$L_{p3}^{C} = \frac{40}{243\omega_0^2 C_0} \tag{50}$$

$$C_{p3}^{C} = \frac{27}{40} C_0 \tag{51}$$

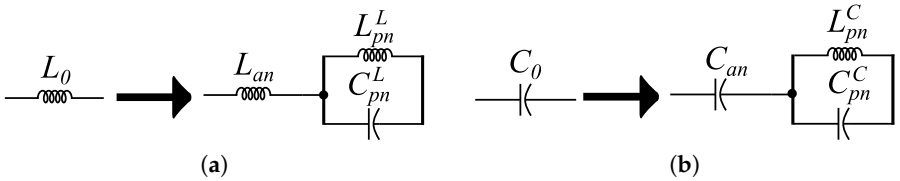

Figure 9. Transformation of components (**a**) L_0 transform, and (**b**) C_0 transform.

The comparative trade-off table evaluates various terminations, with performance metrics analyzed and presented in Table 3. The terminologies used in this paper are as follows:

i. 2.2.2: L_0 and C_0 with 2nd-harmonic tuning.
ii. 2.2.3: L_0 and C_0 with 3rd-harmonic tuning.
iii. 2.2.23: L_0 and C_0 with both 2nd and 3rd-harmonic tuning.
iv. 2.2.L: L_0 transformed as per Equations (45)–(47) with C_0 unchanged.
v. 2.2.C: C_0 transformed as per Equations (49)–(51) with L_0 unchanged.
vi. 2.2.L3: Final topology with L_0 transformed with C_0 unchanged while also adding 3rd-harmonic tuning before the load resistor, as shown in Figure 10.

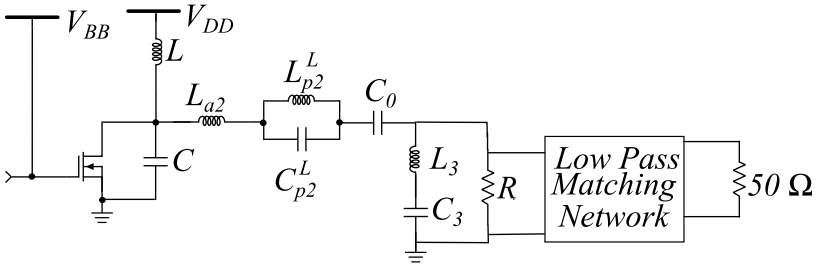

Figure 10. Final topology.

Table 3. Comparison of modified topologies.

Topology	V_{peak}	I_{peak}	η (%)	c_p	2nd (dBc)	3rd (dBc)
2.2.1	4.071	3.032	89.676	0.08312	−9.411	−21.292
2.2.2	4.593	3.123	99.05	0.08609	−94.6	−23.937
2.2.3	4.095	2.992	89.798	0.08390	−8.665	−89.68
2.2.23	4.626	3.065	99.934	0.08801	−58.633	−101.285
2.2.L	3.441	2.742	98.145	0.10291	−314.34	−38.905
2.2.C	4.884	5.639	88.806	0.03670	−295.8	−19.634
2.2.L3	3.348	2.748	99.128	0.10608	−314.705	−59.022

Among these strategies, the combination of the L_0 transformation with the addition of the 3rd harmonic offers the most favorable trade-off, as evidenced by the key performance metrics presented in Table 3. The efficiency-bandwidth response for this final topology, in comparison to the standard Topology 2.2.2, is illustrated in Figure 11, which shows a significant improvement over the bandwidth of 30%. Additionally, the time-domain current and voltage waveforms obtained from the ADS simulation are displayed in Figure 12.

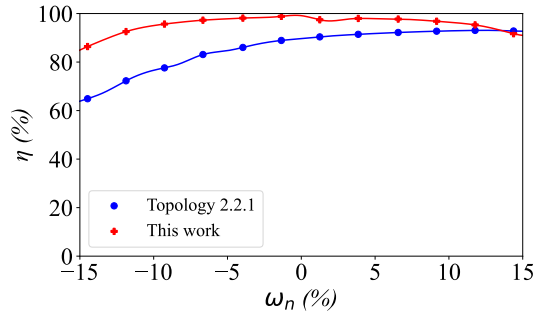

Figure 11. Efficiency-bandwidth comparison between the final topology and Topology 2.2.1.

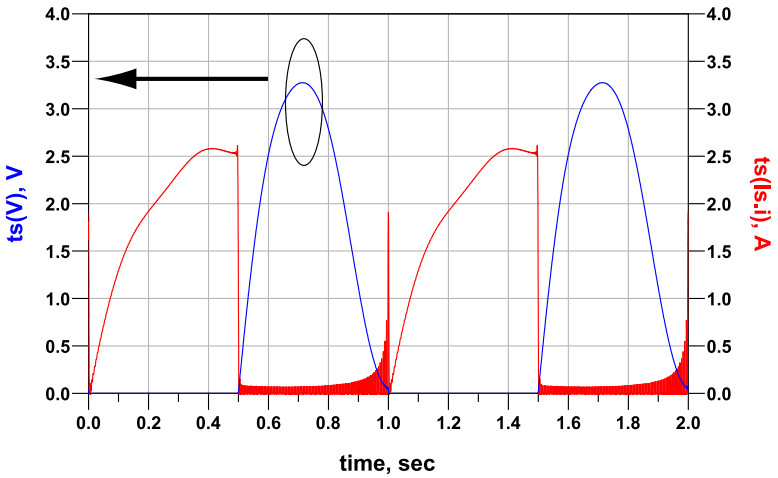

Figure 12. Time-domain normalized voltage (in blue, its corresponding axis is marked by the arrow) and current (in red) waveforms from the ADS simulation.

5. Results and Discussion

The CAD-based analytical modeling demonstrates that Topology 2.2. L3, referred to as the final topology, can achieve at least a bandwidth of 30% while maintaining optimal performance in other key metrics and ensuring an efficient response across the bandwidth. Improving one performance metric will, however, result in the degradation of others.

Building on the analytical expressions, a simplified design methodology was developed to assist designers. A complete circuit of the final topology is shown in Figure 10, where the idealized values can be calculated using the equations from previous sections.

Additionally, low-pass matching networks can be designed to match the load resistance R of the RFPA to the standard 50-Ω load of [31]. Since harmonics are already suppressed due to the modified topology, higher-order filters can be avoided, thus reducing losses associated with the filter. Based on the analytical expression, the following methodology is developed to assist designers. This methodology provides a systematic approach for optimizing Class-E RFPAs to achieve the best trade-off among all performance metrics. The methodology is outlined below.

i. Set the design frequency: The design frequency, set at which the RFPA is intended to operate, is a critical step that influences all subsequent parameters and choices.
ii. Determine required bias voltage levels: The necessary bias voltage levels are identified for the design. These levels are essential for ensuring the proper operation of the transistor and achieving the desired output power.
iii. Calculate idealized values: The ideal values for the lumped elements are then calculated using computed Equations (25)–(27), (38), (39) and (45)–(47). These calculations serve as a reference for the initial simulation and guide the optimization process. The values for L_3 and C_3 are selected such that the series resonator is tuned to the 3rd harmonic.
iv. Optimize all parameters: All design parameters are optimized, including a frequency range with the goals as follows:
    - The output power at the fundamental achieves the specified power level.
    - The efficiency is at least 95% (adjustable based on the requirements).

    The optimization is performed by searching within the range of [0.5–2] times the initial values for R, L, and C, and [0.5–3] times for L_{an}, L_{pn}^{L}, C_{pn}^{L}, C_0, L_3, and C_3 to find the optimal design parameters. This optimization accounts for package effects, which are critical to preventing potential design issues. Optimizing the ideal values ensures that package-induced variations do not compromise the design's performance.
v. Finalize the design: After completing the optimization, the design parameters are reviewed to ensure they meet the desired specifications. Necessary adjustments are made to fine-tune the design.
vi. Incorporate a matching network: A low-pass matching network is included to match the amplifier's optimal load resistance R to the standard 50-Ω load of the AOTF. This low-pass network further suppresses harmonics.

To validate the proposed methodology and demonstrate the design approach, schematic simulations were conducted using a non-linear device model of the CGH40010 transistor [20]. The transistor is operated at a drain bias voltage of −2.45 V with a gate supply voltage of 10 V for delivering an output power of 30 dBm with a driving input power of 20 dBm. The amplifier is designed to operate at a center frequency of 145 MHz with a span of 40 MHz. The ideal and optimized values derived from these simulations are presented in Table 4.

Table 4. Ideal and optimized values of different parameters of the final topology.

	R (Ω)	L (nH)	C (pF)	L_{a2} (nH)	L_{p2}^{L} (nH)	C_{p2}^{L} (pF)	C_0 (pF)	L_3 (nH)	C_3 (pF)
Ideal	136.50	109.67	5.51	57.64	72.05	4.18	7.83	182.93	0.73
Optimized	120.82	74.81	9.07	37.24	164.17	2.12	5.56	109.61	2.04

Figure 13a shows that the designed RFPA achieves an efficiency greater than 90% across the frequency range, resulting in a bandwidth of 27.59%, which closely aligns with

the predictions from ideal simulations where a 30% efficiency was achieved. Figure 13b and Figure 13c illustrate the output power and harmonic levels, respectively.

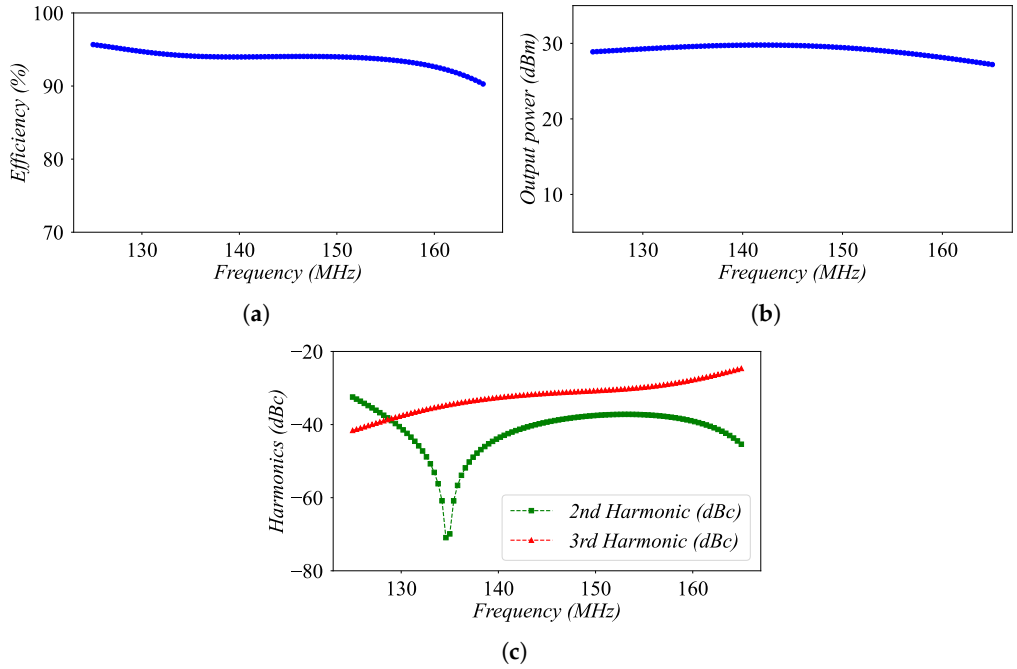

Figure 13. Simulation results for the RFPA design at 145 MHz delivering 1 watt of output power. (**a**) Efficiency (%), (**b**) output power (dBm), and (**c**) harmonics (dBc).

The designed RFPA achieves a maximum output power of 29.779 dBm, which closely aligns with the specified design goals. The harmonic levels are maintained below −25 dBc across the bandwidth. Additionally, the suppression of the 2nd harmonic is greater than that of the third harmonic, which aligns with the expected behavior of the proposed topology, as demonstrated by the ideal simulation results provided in Table 3. Finally, the schematic for the first-order low-pass matching circuit, along with the filter response, is presented in Figure 14, demonstrating additional suppression of harmonics.

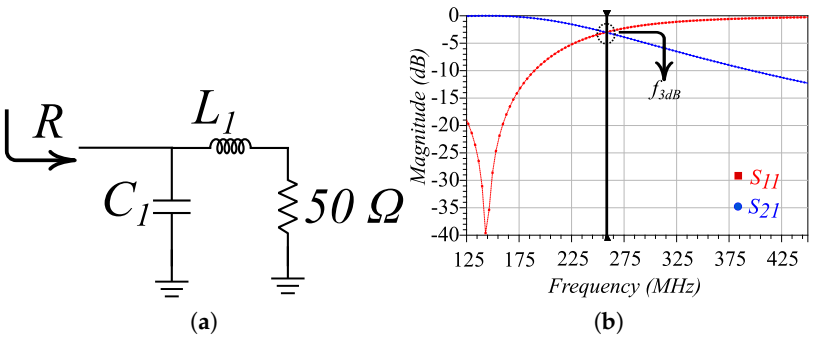

Figure 14. (**a**) Schematic for the matching network ($R = 120.8211\ \Omega$, $L_1 = 65\ nH$, and $C_1 = 11\ pF$), (**b**) filter response from the ADS simulation.

The transistor is capable of delivering a maximum power of 40 dBm, as specified in the datasheet. In this case, the biasing voltage can be set to 28 volts, and the circuit parameter values can be recalculated accordingly to ensure optimal performance and meet the design specifications. Additionally, since the typical gain of this transistor is around 10 dB, an input power of 30 dBm is required to drive the transistor into saturation.

6. Conclusions and Future Work

This paper presents a comprehensive design approach for series-tuned Class-E RFPAs, focusing on determining the bounds of the quality factor Q_s and implementing advanced harmonic control and suppression techniques. By establishing these bounds on Q_s and integrating harmonic control circuits, this study achieved a balance among high efficiency, bandwidth (up to 30%), and maximum output power capability. Simulations of the nonlinear device model demonstrated a bandwidth of approximately 27%, which is in close alignment with the predictions. Future work will involve incorporating matching networks directly into the design equations, followed by experimental validation through the fabrication and testing of the RFPA prototype.

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Abbreviations

The following abbreviations are used in this manuscript:

RFPA	radio-frequency power amplifier
HB	harmonic balance
MRI	magnetic resonance imaging
MF	medium frequency
HF	high frequency
VHF	very high frequency
ZVS	zero voltage switching
ZVDS	zero voltage derivative switching
V_{DD}	supply voltage
V_{BB}	biasing voltage
c_p	maximum output power capability
$Q_{2.2.1}$	quality factor for topology 2.2.1
Q_s	quality factor of the resonator
Q_{sat}	saturation quality factor for the upper limit
Q_{min}	minimum quality factor for the lower limit
L_0	original inductor
L_{an}	inductor obtained by modifying the original inductor for the n^{th} harmonic
L_{pn}^L, C_{pn}^L	inductor–capacitor pair obtained by modifying L_0 for the n^{th} harmonic
C_0	original capacitor
C_{an}	capacitor obtained by modifying the original capacitor for the n^{th} harmonic
C_{pn}^C, L_{pn}^C	inductor–capacitor pair obtained by modifying C_0 for the n^{th} harmonic
f_{3dB}	frequency at 3dB level

Appendix A

Appendix A.1. Calculations for Matching at Different Harmonics for an Inductor Converted to an Equivalent Circuit

The following two cases are possible:

1. The parallel resonator is tuned to the 2nd harmonic, and the net impedance is shorted at the 3rd harmonic. In this condition, the design equations are as follows:

$$1 - 4\omega_0^2 L_{p2}^L C_{p2}^L = 0 \tag{A1}$$

$$Z(3\omega_0) = 3j\omega_0 L_{a2} + \frac{3j\omega_0 L_{p2}^L}{1 - 9\omega_0^2 L_{p2}^L C_{p2}^L} = 0 \tag{A2}$$

$$j\omega L_0 = j\omega L_{a2} + \frac{j\omega_0 L_{p2}^L}{1 - \omega_0^2 L_{p2}^L C_{p2}^L} \tag{A3}$$

Substituting ω_0 from Equation (A1) into Equation (A2) and after simplification, a relationship between L_a and L_{p2}^L is obtained.

$$L_{a2} - \frac{4}{5} L_{p2}^L = 0 \tag{A4}$$

Now, using (A1) in (A3), we have the following:

$$L_0 = L_{a2} + \frac{4}{3} L_{p2}^L \tag{A5}$$

The parameters are given by Equations (45)–(47).

2. The parallel resonator is tuned to the 3rd harmonic, and the net impedance is shorted at the 2nd harmonic. Under that condition, the design equations are as follows:

$$1 - 9\omega_0^2 L_{p3}^L C_{p3}^L = 0 \tag{A6}$$

$$2j\omega_0 L_{a3} + \frac{2j\omega_0 L_{p3}^L}{1 - 4\omega_0^2 L_{p3}^L C_{p3}^L} = 0 \tag{A7}$$

$$j\omega L_0 = j\omega L_{a3} + \frac{j\omega_0 L_{p3}^L}{1 - \omega_0^2 L_{p3}^L C_{p3}^L} \tag{A8}$$

Using Equations (A6) and (A7), a relation can be derived between L_a and L_{p3}^L.

$$L_{a3} + \frac{9}{5} L_{p3}^L = 0 \tag{A9}$$

Equation (A9) implies that one of the parameters, L_a and L_{p3}^L, must be negative. Hence, this condition is not possible.

Appendix A.2. Calculations for Matching at Different Harmonics for a Capacitor Converted to an Equivalent Circuit

1. The parallel resonator is tuned to the 2nd harmonic and the net impedance is shorted at the 3rd harmonic. Under this condition, the design equations are as follows:

$$1 - 4\omega_0^2 L_{p2}^C C_{p2}^C = 0 \tag{A10}$$

$$\frac{1}{3j\omega_0 C_{a2}} + \frac{3j\omega_0 L_{p2}^C}{1 - 9\omega_0^2 L_{p2}^C C_{p2}^C} = 0 \tag{A11}$$

$$\frac{1}{j\omega_0 C_0} = \frac{1}{j\omega_0 C_{a2}} + \frac{j\omega_0 L_{p2}^C}{1-\omega_0^2 L_{p2}^C C_{p2}^C} \tag{A12}$$

Using Equations (A10) and (A11), a relation is obtained between L_{p2}^C and C_{a2}, as follows:

$$1 + \frac{36}{5}\omega_0^2 L_{p2}^C C_{a2} = 0 \tag{A13}$$

Again, Equation (A13) implies that either L_{p2}^C or C_{a2} must be negative. Hence, this condition is impossible.

2. The parallel resonator is tuned to the 3rd harmonic and the net impedance is shorted at the 2nd harmonic. Under that condition, the design equations are as follows:

$$1 - 9\omega_0^2 L_{p3}^C C_{p3}^C = 0 \tag{A14}$$

$$\frac{1}{2j\omega_0 C_{a3}} + \frac{2j\omega_0 L_{p3}^C}{1-4\omega_0^2 L_{p3}^C C_{p3}^C} = 0 \tag{A15}$$

$$\frac{1}{j\omega_0 C_0} = \frac{1}{j\omega_0 C_{a3}} + \frac{j\omega_0 L_{p3}^C}{1-\omega_0^2 L_{p3}^C C_{p3}^C} \tag{A16}$$

The equivalent parameters are given by Equations (49)–(51).

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