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Revitalizing polymer packaging for single-chip implants

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REVITALIZING POLYMER PACKAGING FOR SINGLE-CHIP IMPLANTS

REVITALIZING POLYMER PACKAGING FOR SINGLE-CHIP IMPLANTS

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
by the authority of the Rector Magnificus Prof. Dr. Ir. T.H.J.J. van der Hagen,
Chair of the Board for Doctorates
to be defended publicly on Monday 27 January at 15:00 o'clock

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SUMMARY

For over five decades, electronic implants have significantly improved the quality of life for millions of patients. With their great potential, substantial advancements have been made in developing new therapeutic devices, particularly in the fields of bioelectronic medicine and brain-machine interfaces. However, these emerging devices require novel approaches to packaging, as traditional hermetic enclosures no longer meet the physical and dimensional demands of modern systems. Polymer packaging offers a promising alternative, enabling device miniaturization and facilitating minimally invasive procedures. Polymer packaging was in fact one of the earliest methods used to protect electronics (implemented with discrete components) in the body. However, due to the inability of polymers to fully block moisture ingress, it soon became evident that the body's wet and corrosive environment could negatively impact device longevity. As electronic implants evolved from using discrete components to complex integrated circuits (ICs), the challenge of protecting these devices became even more critical. In this thesis, I aimed to tackle the challenge of ensuring the safe and reliable operation of polymer-packaged ICs for long-term implantable applications. To address this challenge, I pursued three key objectives: 1) I developed on-chip sensor platforms to carefully monitor the integrity of the IC structure. These tools provide critical data on the condition and performance of the chips, ensuring their expected functionality in clinical settings. 2) I investigated the electrical and material stability of IC structures by directly exposing them as bare die (uncoated) to physiological environments, assessing their durability in the body's corrosive conditions. By identifying potential degradation pathways, I proposed IC design guidelines that can potentially enhance the longevity of polymer-packaged devices. 3) I investigated if silicone rubber, as a polymer packaging material, could prevent or slow down the degradations seen in uncoated ICs. Separately, I also evaluated two thin-film packaging layers for their effectiveness in IC protection. Results demonstrated that IC structures can be inherently hermetic, enabling polymers, such as silicone, to serve as standalone packaging materials despite their moisture permeability. Furthermore, silicone was found to effectively prevent the degradations observed in bare-die ICs. Using advanced material analysis techniques, I derived degradation rates, showing that silicone-encapsulated ICs could last over 10 years in the body. These findings enable the development of long-lasting miniature implants, reducing the need for repeated surgeries and improving patients' quality of life.

SAMENVATTING

Al meer dan vijf decennia hebben elektronische implantaten de levenskwaliteit van miljoenen patiënten aanzienlijk verbeterd. Met hun enorme potentieel zijn er substantiële vooruitgangen geboekt in de ontwikkeling van nieuwe therapeutische apparaten, met name op het gebied van bio-elektronische geneeskunde en brain-machine interfaces. Echter, deze opkomende apparaten vereisen nieuwe benaderingen op het gebied van encapsulatie, aangezien traditionele hermetische omhulsels niet langer voldoen aan de fysieke en dimensionele eisen van moderne systemen. Polymeer-encapsulatie biedt een veelbelovend alternatief, dat miniaturisatie van elektronische implantaten mogelijk maakt en minimaal invasieve procedures vergemakkelijkt. Polymeer-encapsulatie was in feite één van de vroegste methoden die werden gebruikt om elektronica (met discrete componenten) in het lichaam te beschermen. Echter, vanwege de vochtpermeabiliteit van polymeren werd duidelijk dat de corrosieve omgeving van het lichaam de levensduur van het implantaat negatief kon beïnvloeden. Naarmate elektronische implantaten evolueerden van het gebruik van discrete componenten naar complexe geïntegreerde schakelingen (IC's), werd de uitdaging om deze apparaten te beschermen nog kritieker. In dit proefschrift bestudeer ik de veilige en betrouwbare werking van IC's in polymeer-encapsulatie voor langdurige implanteerbare toepassingen. Hiervoor stelde ik drie belangrijke doelen: 1) Ik ontwikkelde sensorplatformen op de chip om zorgvuldig de integriteit van de IC-structuur te monitoren. Deze sensoren leveren cruciale gegevens over de toestand en prestaties van de chips, waardoor hun betrouwbaarheid in klinische omgevingen wordt gewaarborgd. 2) Ik onderzocht de elektrische en materiaalstabiliteit van IC-structuren door ze onbedekt (niet ge-encapsuleerd) bloot te stellen aan fysiologische omgevingen, waarbij hun betrouwbaarheid in de corrosieve omstandigheden van het lichaam werd beoordeeld. Door mogelijke degradatiepaden te identificeren, stelde ik richtlijnen voor IC-ontwerp voor die de levensduur van implantaten met polymeer-encapsulatie mogelijk kunnen verbeteren. 3) Ik onderzocht of siliconenrubber, een polymeer encapsulatiemateriaal, de degradatie die bij onbedekte IC's wordt waargenomen, kan voorkomen of vertragen. Daarnaast evalueerde ik ook twee dunne-film encapsulatielagen op hun effectiviteit bij de bescherming van IC's. De resultaten toonden aan dat IC-structuren van nature hermetisch kunnen zijn, waardoor polymeren, zoals siliconen, ondanks hun vochtpermeabiliteit als op zichzelf staande verpakkingsmaterialen kunnen dienen. Bovendien bleek dat siliconen degradaties, die bij bare-die IC's worden waargenomen, effectief kunnen voorkomen. Door gebruik te maken van geavanceerde materiaalanalysetechnieken, heb ik degradatiesnelheden afgeleid waaruit blijkt dat IC's met een silicone-encapsulatie mogelijk meer dan 10 jaar in het lichaam kunnen meegaan.

1

INTRODUCTION

1.1. PACKAGING OF NEXT-GENERATION IMPLANTABLE ELECTRONICS

For more than 50 years, electronic implants have provided substantial therapeutic benefits, greatly enhancing the quality of life for millions of patients. In the last two decades, there has been a surge of research in two pioneering fields: bioelectronic medicine and brain-machine interfaces (BMI). Bioelectronic medicine offers a neuromodulation alternative to traditional pharmaceuticals by using tiny electrical pulses to stimulate neurons. [1, 2]. Deep brain stimulation (DBS) is perhaps one of the most successful applications of bioelectronic medicine [3]. Approved by the Food and Drug Association (FDA) in 2002, DBS has improved the lives of hundreds of thousands of patients suffering from Parkinson's disease and essential tremor. Besides DBS, there are numerous other potential applications of bioelectronic medicine. For example, occipital nerve stimulation (OSP) is currently being investigated as a potential neuromodulation solution for millions of patients suffering from drug-refractory migraine [4].

Brain-machine interfaces represent another emerging medical field with potentially transformative applications, bridging the gap between neural activity and external devices [2]. By recording and interpreting neural signals, these electronic implants can restore motor function in individuals with severe paralysis, enabling them to control prosthetic limbs and exoskeletons [5, 6]. This technology holds the promise of returning lost mobility, significantly improving the quality of life for patients suffering from spinal cord injuries or pharmaceutically untreatable neurodegenerative diseases [7].

Interacting with the body's nervous system, however, requires dedicated electronics that should be uniquely packaged to ensure biocompatibility, minimize the body's immune responses, and maintain long-term functionality and stability within the biological environment [8].

For electronics, without a doubt, the body is an inhospitable and extremely harsh environment. Therefore, packaging and protecting the electronics within the corrosive body environment has been a key challenge since the first electronic device was im-

planted for cardiac pacing [9, 10]. Driven by the demands for increased miniaturization and functionality, integrated circuits (IC) are becoming a necessity for these emerging implantable devices [11, 7]. The compact and highly integrated nature of the IC structure, however, demands even more attention against possible moisture and ion ingress [12]. Fortunately, the traditional metal hermetic (gas-tight) enclosures can guarantee such a dry and ion-free environment for >20 years in the body [13].

For future implantable devices, however, traditional hermetic enclosures, fall short of meeting the physical requirements: smaller millimeter-sized and lightweight packages (weighing only a few grams) that allow for minimally invasive procedures, minimizing the tissue response with reduced risk of device migration [14, 15, 5]. Polymer packaging is another solution with many favorable physical attributes such as flexibility, reduced weight, and the potential to miniaturize the device to sub-millimeter scales. The primary challenge, however, is to prevent performance loss or malfunction due to moisture or ion ingress over the functional lifetime of the implant [16].

This thesis tackles the challenge of ensuring the safe and reliable operation of polymer-packaged IC structures for long-term implantable applications. To achieve this, the electrical and material stability of bare-die (uncoated) ICs are evaluated after prolonged exposure to physiological environments, studying their performance over time to assess their durability within the body's corrosive environment. By identifying the potential degradation pathways of these bare structures, IC design guidelines are proposed along with sub-millimeter packaging solutions that can enhance the longevity of polymer-packaged ICs in the body.

Furthermore, this thesis proposes the development of new on-chip monitoring tools for assessing the long-term integrity of implantable ICs. These tools will provide real-time data on the chip's condition and performance, ensuring its reliability in implantable applications.

Successfully achieving these objectives will pave the way for engineering long-lasting low-profile devices, reducing the need for multiple invasive surgeries and significantly improving patients' quality of life.

1.2. OUTLINE OF THESIS

The thesis is structured as follows:

Chapter 1: Introduction. This chapter provided a preface to the packaging requirements of next-generation neural implants and gave the motivation for this thesis.

Chapter 2: State-of-the-art miniaturized packaging for implantable ICs. In this chapter, an overview of the latest advancements in miniaturizing the packaging for implantable ICs is provided. Two types of packaging solutions are discussed: void-free polymer packaging (e.g. silicone encapsulation) and thin-film conformal micro-packaging using polymers or ceramics (e.g. atomic layer deposition(ALD) coatings). A detailed review of recent scientific literature on both solutions is given, along with an analysis of their associated challenges. Based on the gaps identified in the literature, the research objectives of this thesis are defined and outlined.

Chapter 3: On-chip CMOS tools for integrity monitoring. Silicon-ICs will be an integral component for miniaturized implantable devices. The lack of a hermeticity test for polymer or thin-film packaged ICs demands new solutions to evaluate their integrity,

both before and during implantation. In this chapter, two novel on-chip monitors are proposed to evaluate the integrity of the chip structure or the applied thin coating. The first part of the chapter will be dedicated to the design and implementation of an on-chip moisture/ion integrity monitor for early detection of impurity ingress. The second part of the chapter introduces the concept of using the IC's silicon bulk to evaluate the integrity of the coatings that are applied for thin-film packaging.

Chapter 4: On the hermeticity and longevity of Silicon-ICs, bare-die and PDMS-coated. In this chapter, the hermeticity of IC structures is investigated by directly exposing them as bare die to accelerated in vitro and in vivo aging conditions over a 12-month period. Various factors, including the effects of different metallization layers and electric fields on IC longevity, are explored. Next, by identifying the potential degradation pathways of bare ICs, it is examined if polydimethylsiloxane (PDMS), used as a soft polymer package, could prevent or delay the identified degradation pathways and thus extend the longevity of the IC. Advanced material analysis techniques were employed to quantify the rates of observed degradations, which will help estimate the longevity of both bare-die and PDMS-coated ICs.

Chapter 5: In vivo biostability of ALD and Parylene-ALD multilayers as thin-film micro-packaging solutions for implantable ICs. Thin-film coating is an attractive solution for IC micro-packaging. The long-term in vivo stability and performance of these films, however, has always been a concern. In this chapter, the long-term biostability of two thin-film coatings over a 7-month in vivo animal study is investigated: a hafnia-based ALD multilayer, and an ALD/parylene-C hybrid multilayer.

Chapter 6: Conclusion and future work. In this chapter, the main contents are summarized, highlighting the key original contributions of the thesis. Finally, the remaining challenges and future directions are discussed that, if solved, could help further increase the reliability of polymer-packaged single-chip implants.

1.3. LIST OF ORIGINAL PUBLICATIONS

JOURNAL ARTICLES

- **Kambiz Nanbakhsh**, et al. "On the Longevity and Inherent Hermeticity of Silicon-ICs: Evaluation of Bare-Die and PDMS-Coated ICs After Accelerated Aging and Implantation Studies." Nat. Commun. In press.

- **Kambiz Nanbakhsh**, et al. "An in vivo Biostability Evaluation of ALD and Parylene-ALD Multilayers as Micro-packaging Solutions for Implantable ICs." in revision.

- Omer Can Akgun, **Kambiz Nanbakhsh**, Vasiliki Giagka, and Wouter A. Serdijn. "A chip integrity monitor for evaluating moisture/ion ingress in mm-sized single-chip implants." IEEE Transactions on Biomedical Circuits and Systems 14, no. 4 (2020): 658-670.

- Anna Pak, **Kambiz Nanbakhsh**, Ole Hölck, Riina Ritasalo, Maria Sousa, Matthias Van Gompel, Barbara Pahl, Joshua Wilson, Christine Kallmayer, and Vasiliki Giagka. "Thin film encapsulation for LCP-based flexible bioelectronic implants: comparison of different coating materials using test methodologies for life-time estimation." Micromachines 13, no. 4 (2022): 544.

- Callum Lamont, Timea Grego, **Kambiz Nanbakhsh**, A. Shah Idil, Vasiliki Giagka, Anne Vanhoestenberghe, Stuart Cogan, and Nick Donaldson. "Silicone encapsulation of thin-film SiO_X, SiO_XN_Y and SiC for modern electronic medical implants: a comparative long-term ageing study." Journal of Neural Engineering 18, no. 5 (2021): 055003.

CONFERENCE CONTRIBUTIONS

- **Kambiz Nanbakhsh**, Marta Kluba, Barbara Pahl, Florian Bourgeois, Ronald Dekker, Wouter Serdijn, and Vasiliki Giagka. "Effect of signals on the encapsulation performance of parylene coated platinum tracks for active medical implants." In 2019 41st Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), pp. 3840-3844. IEEE, 2019.

- **Kambiz Nanbakhsh**, Riina Ritasalo, Wouter A. Serdijn, and Vasiliki Giagka. "Long-term encapsulation of platinum metallization using a HfO_2 ALD-PDMS bilayer for non-hermetic active implants." In 2020 IEEE 70th Electronic Components and Technology Conference (ECTC), pp. 467-472. IEEE, 2020.

- Rodrigues G, Neca M, Silva J, Brito D, Rabuske T, Fernandes J, Mohrlok R, Jeschke C, Meents J, **Nanbakhsh K**, Giagka V. Towards a wireless system that can monitor the encapsulation of mm-sized active implants in vivo for bioelectronic medicine. In 2021 10th International IEEE/EMBS Conference on Neural Engineering (NER) 2021 May 4 (pp. 981-984). IEEE.

- **Kambiz Nanbakhsh**, Riina Ritasalo, Wouter A. Serdijn, and Vasiliki Giagka. "Towards CMOS Bulk Sensing for In-Situ Evaluation of ALD Coatings for Millimeter Sized Implants." In 2020 42nd Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), pp. 3436-3439. IEEE, 2020.

- Omer Can Akgun, **Kambiz Nanbakhsh**, Vasiliki Giagka, and Wouter A. Serdijn. "A chip integrity monitor for evaluating long-term encapsulation performance within active flexible implants." In 2019 IEEE Biomedical Circuits and Systems Conference (BioCAS), pp. 1-4. IEEE, 2019.

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2

STATE-OF-THE-ART PACKAGING SOLUTIONS FOR MINIATURIZED IMPLANTABLE ELECTRONICS

Packaging has been a major engineering challenge for implantable electronics intended to function reliably for years within the body. In this chapter, I provide an overview of state-of-the-art packaging solutions for next-generation miniaturized implants and detail the associated challenges. I begin with a brief introduction to the first packaging used for electronic implants and discuss in detail the issue of moisture and fluid ingress, which was a primary failure mechanism in these early packages. Next, I describe hermetic enclosures which are the current industrial standard for addressing the issue of moisture ingress. Then I review the latest advancements in implantable electronics, highlighting cutting-edge miniaturized packaging solutions and summarizing the requirements for future millimeter-sized devices. Finally, by examining existing literature, I identify the necessary key gaps for achieving long-term reliability in miniaturized packages. Based on these identified gaps, I conclude the chapter with a definition of the research objectives of the thesis.

2.1. PACKAGING OF IMPLANTABLE ELECTRONICS: HOW DID WE GET HERE?

Since the first pacemaker in 1958, implantable electronics (also known as "active medical implantable devices") have been successfully used to improve the quality of life for millions of patients [1]. Examples of these devices include cardiac pacemakers [2] (for controlling heart rhythm), spinal cord stimulators [3] (for chronic pain management), deep brain stimulators (for controlling symptoms of conditions, such as Parkinson's disease [4], essential tremor, epilepsy, and depression), cochlear implants (for hearing loss) and, more recently, occipital (ONS) and supraorbital nerve stimulation (SONS) (for pain

alleviation for drug-refractory headache disorders) [5]. Similar to any device incorporating electronics, dedicated packaging is required to guarantee the reliable operation of these implantable devices over their intended lifespan. The in vivo environment, however, dictates very stringent requirements for the choice of materials and fabrication methods. Specifically for the packaging, besides protecting the electronics from the body, it should also protect the biological environment from any exposure to toxic or non-biocompatible materials that are part of the active implant, such as metals (copper traces, aluminum, nickel) [3], [6].

Some of the first implanted electronic devices were not hermetically sealed; meaning that within the device's lifespan, the underlying electronics could be exposed and saturated with moisture [7]. These early devices were used for cardiac pacing and employed polymer encapsulation (epoxy) to package the electronics [2]. The first implantable pacemaker developed by Elmqvist consisted of two transistors and was over-molded in an empty shoe polish tin (see first image in Fig.2.1) [8]. As polymers have a higher permeability to gases (including moisture), all the electronics and interfaces could be saturated with moisture [9, 10]. At the time of the manufacturing of these devices, the electronics were based on discreet components: transistors, resistors, and capacitors, all assembled at a reasonable distance (a few millimeters) from each other. Reports on the failures of these early devices showed signs of cracking or delamination of the epoxy from wires and components, allowing the penetrated or diffused moisture to create corrosion and shunt leakage paths [8]. These failures were the first signs that the body's wet corrosive environment requires dedicated packaging that can guarantee a dry environment for the electronics in the body.

By increasing the functionality of implants, the electronics became more advanced, requiring integrated circuits (ICs) in addition to discrete components for their functionality [6, 11]. For such devices, it was believed that simple polymer encapsulation was not sufficient to provide the long-term reliability expected from a medical implant [8].

When it comes to long-term reliable electronic packaging, the aerospace and automotive industries tend to be the 'trendsetter'. Adopted from the high-reliability aerospace industry, hermetic enclosures were introduced into the active implantable industry [6]. Hermeticity was achieved using a metal or ceramic enclosure to house the electronics. The most common material currently used for making hermetic enclosures for implantable applications is titanium (Fig.2.1) [12]. This is largely due to 1) excellent corrosion resistivity, 2) biocompatibility, and 3) the reliable laser seam welding which has proven to be a reliable process for long-term applications [6]. In addition to the laser weld, hermetic feed-throughs are critical components to guarantee the hermeticity of the enclosure [13]. Without hermetic feedthroughs, the enclosure cannot be considered hermetic even if the enclosure material is made of metal, ceramic, or glass [14].

Hermetic housings have remained the industry standard for packaging life-critical battery-powered active implantable medical devices (AIMD). Since the appearance of the first hermetically sealed pacemaker, this packaging has enabled long lifespans (>20 years) [6]. It results, however, in a costly and bulky device which due to its size usually needs to be placed in a location far from the therapy delivery site, necessitating complicated invasive interventions for implantation [17].

An important advantage of hermetic enclosures is their testability based on the he-

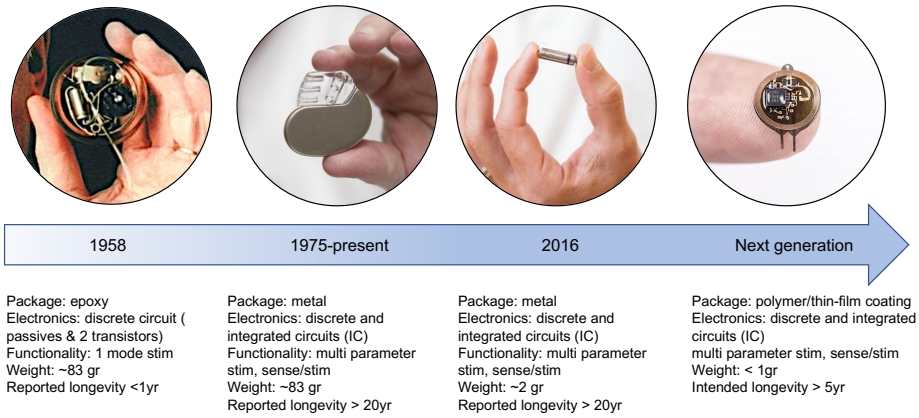


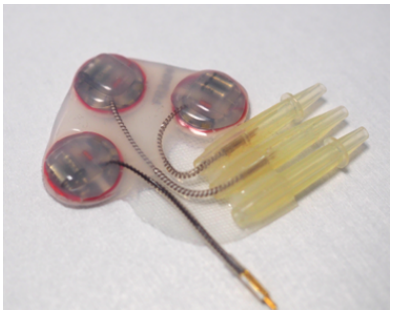
Figure 2.1: Evolution of packaging for implantable electronics [11, 15, 16]

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lium (He) fine leak test [6]. This test models water molecule ingress and is used to verify the hermeticity of the seal for each device before its use. It is noteworthy to mention that the helium leak test does not guarantee the long-term hermeticity of the enclosure [18]. This is done by selecting appropriate materials for the packaging (metal or ceramic) and carefully designed feedthroughs. By reducing the size of implantable medical devices, the amount of water necessary to increase the humidity to corrosive levels in the interfacial environment becomes exceedingly small [19]. Also, it takes a shorter time for moisture or ions to go through a narrower sealing wall or an interfacial pathway. For this reason, higher-quality bulk materials and void-free interfacial sealing are essential to achieve the same degree of hermiticity for smaller hermetic packages than bigger ones [20].

Despite the observed failures for epoxy-encapsulated cardiac pacemakers, one of the successful applications of polymer encapsulation is the Finetech-Brindley sacral anterior root stimulator (Fig.2.2) [21, 22]. This device used silicone rubber to package the electronics. The wirelessly powered device consisted of a receiver circuitry and a stimulator that was implemented using discrete components. In a follow-up study on the Finetech-Brindley stimulator, a mean time to failure of 19.6 years was reported for the device [23].

Based on the reported longevity, it can be understood that for this device the penetrated moisture through the silicone encapsulation was not so critical. This suggests that the selected components and interfaces were inherently moisture-resistant with long-lasting adhesion to the polymer, preventing any corrosion or shunt leakage paths [25]. These encouraging results show that polymeric encapsulation can be a viable solution for protecting implanted electronics for decades on the caveat that all the components underneath are carefully selected. The circuits used for the Finetech-Brindley are quite simple compared to modern ICs. Silicon-ICs incorporate thin-film ceramics and metals which may exhibit chemical degradation upon moisture exposure [26, 27]. A reduction in feature sizes compared to discrete-level electronics also results in higher electric fields



- Packaging: silicone elastomer
- Power source: battery-free/wirelessly powered
- Number of channels: 3
- Reported longevity: ≈ 20 years
- Electronics: discrete transistors and passive components
- Estimated usage/day: a few hours

Figure 2.2: Image of the Finetech-Brindley three-channel neurostimulator (courtesy of Callum Lamont [24])

which may impact the material stability when saturated with moisture [22].

Despite the longevity of silicone-packaged Finetech-Brindley stimulators, hermetic enclosures remain the golden standard for packaging electronic implants, especially for life-sustaining devices such as defibrillators and pacemakers. Driven by miniaturization, great engineering work has been targeted to shrink the size and weight of these devices while maintaining their high reliability. The latest example is the Micra^{TM} pacemaker (from Medtronic) which is only 2.0 g in weight and 0.8 cm^3 in volume (92% smaller than conventional pacemakers which weigh 20-50 g) (Fig.2.1).

As shown in Fig.2.3, most materials, if given enough time, will eventually allow moisture ingress [10]. Therefore, in addition to the permeability rate of the material and its thickness, the timescale is also a contributing factor in defining a package hermetic (gas tights). For better clarification, two examples are provided although being unrealistic. Example 1: if an implant were to have a lifetime of 1 second, a sub-mm thick silicone package would ensure that the relative humidity within the package would remain unchanged. In other words, a silicone package could be considered hermetic 'enough' for 1 second. Example 2: if an implant were to last >500 years, the currently used titanium enclosure with the thickness employed may not ensure a hermetic environment for such long timescales. Nevertheless, the current norm in defining a package hermetic is by assuming that the implant will have a lifetime of > 20 years [28]. For such lifetimes, and with the thickness and dimensions that are viable for an implant, only metals, ceramics and glass can guarantee a hermetic environment [29, 10].

Recently, cavity packages made from polymers such as liquid crystal polymer (LCP) or Polytetrafluoroethylene (PTFE) are known in the industry as "near-hermetic" or "substantially hermetic" [30, 31]. Despite being more resistant to moisture ingress compared to other polymers like polyurethane, epoxy, or silicone, they cannot guarantee a hermetic enclosure for decades-long lifespans [32].

The success of the Finetech neurostimulator demonstrated that silicone encapsulation could be a viable solution for devices requiring >10 years of lifetime. Compared to the three-channel Finetech stimulator, however, future implantable devices require

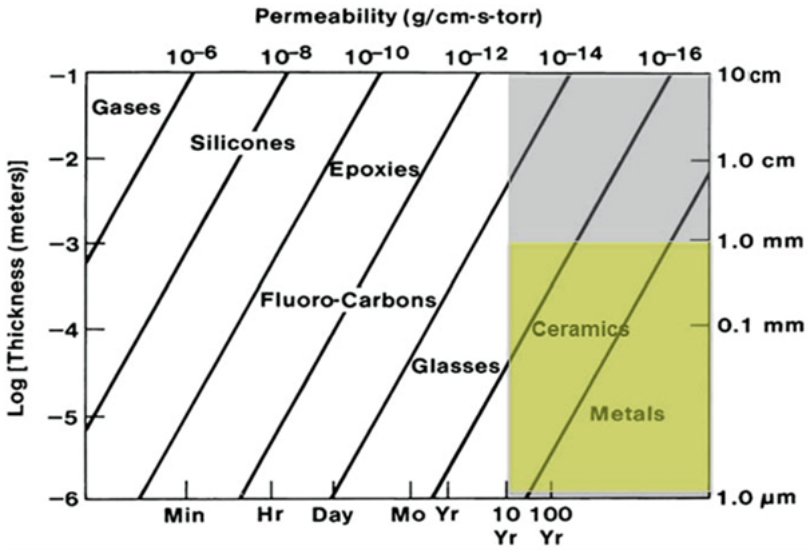


Figure 2.3: Material-dependent moisture permeability over time. The graph also provides information regarding permeability as a function of material thickness. [33]

ICs to satisfy their complex functionalities, small footprint, and tight power budget [34, 35]. One key question arises: can silicone-encapsulated ICs also reach ≈ 5-10 years of functional lifetime in the body?

2.2. NEXT-GENERATION IMPLANTABLE ELECTRONICS

In recent years, a new generation of non-life-sustaining implantable devices has emerged as exploratory tools for interacting with the nervous system. The two main applications currently in focus are 1) brain-machine interfaces (BMI), and 2) bioelectronics medicine. For BMI, the implanted electronics are intended to record neural signals from the human brain (or central nervous system) to control a computer or a prosthetic limb [36]. Bioelectronic medicine is another emerging application with the ultimate goal of replacing chemical drugs with neuromodulation [37]. Perhaps the best example of bioelectronic medicine that is currently in clinical practice is the deep brain stimulation (DBS) device. The DBS system has been in use for >10 years and has helped over 200 thousand patients suffering from life-debilitating diseases such as Parkinson's and essential tremors [38]. This example has demonstrated how neuromodulation can help assist patients where conventional chemical drugs fall short. In the last years, new applications of bioelectronic medicine have been investigated. Rheumatoid arthritis (RA), migraine, and chronic cluster headache are a few conditions that are currently being investigated for bioelectronic medicine [5, 35].

As explained in the previous section, hermetic enclosures are the golden standard, and will most likely remain to be, for packaging battery-powered life-sustaining devices. However, for the newly explored conditions which are non-life-sustaining, battery-free

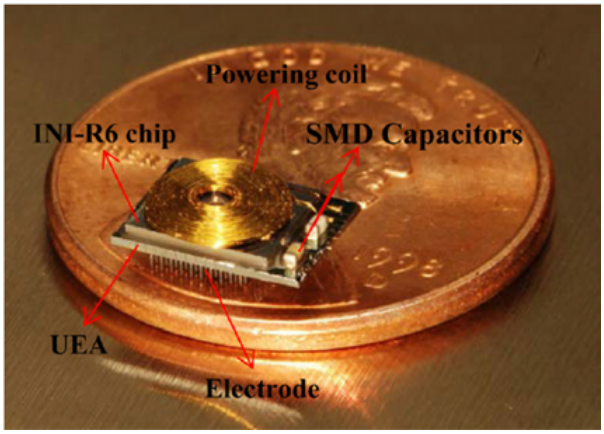


Figure 2.4: A battery-free wireless device with an IC connected to the Utah electrode array [40].

devices with wireless power delivery could be a viable powering solution. Moving away from the battery can help in the miniaturization process of the device but also open new possibilities for alternative packaging solutions, such as polymer packaging, that can further help in shrinking the overall size of the device. As a result of the miniaturization, such devices could be positioned in a minimally invasiveness manner, reducing the risks of surgery [35]. Given the non-life-sustaining application and minimal invasiveness, one could even argue that such implants may require shorter functional lifetimes ($\approx$ 5-10 years), further justifying an alternative packaging solution such as polymer packaging.

The next generation of implantable devices is expected to have more channel counts and embed more functionally compared to the simple 3-channel Finetech-Brindley stimulator. These devices will rely on ICs for their functionality. As an example, Fig.2.4 depicts a wireless device implemented using the Utah electrode array having 100 electrodes. The discrete components on the devices (capacitor and coil) together with the INI-R6 IC were packaged using a thin-film coating that resulted in a millimeter-sized implant [39].

2.3. THE HUMAN BODY: AN INHOSPITABLE ENVIRONMENT FOR IMPLANTABLE ELECTRONICS

The human body is an inhospitable environment for foreign materials. Electronic implants, designed to restore or enhance physiological functions, face relentless challenges from the body's biochemical and mechanical forces. Far from being a passive host, the body actively interacts with implant materials, often leading to their degradation over time. Studies of explanted devices have consistently demonstrated the detrimental effects of this environment on both metals [12] (e.g., titanium and stainless steel) and polymers [41, 42] (e.g., polyurethane and Parylene C). This degradation not only compromises device performance but can also alter the surrounding biological milieu, potentially undermining the biocompatibility of the device [43, 44]. The implantation

site plays a crucial role in determining the types and severity of stress factors that an implantable device experiences. These stress factors are broadly categorized into two groups:

Chemical Stress: Chemical stress in the body primarily comprises of the body's inherent properties and defense mechanisms. Moisture and body fluids are omnipresent in the biological environment, exposing electronic devices to a constant risk of corrosion and ionic infiltration. Additionally, inflammatory responses and foreign body reactions can exacerbate chemical stress by creating oxidative environments and enzymatic attacks [45]. The severity of this chemical stress depends on several factors, including the materials used in the device, its size and shape, and the degree of tissue trauma induced during implantation [46]. For example, larger or more rigid devices may cause greater tissue damage, amplifying inflammatory responses and increasing the exposure of the device to aggressive biochemical agents [47].

Mechanical Stress: The exerted mechanical stresses on implanted devices can be grouped into two categories: stress applied to the device during implantation and handling, and stress experienced during its lifetime use in the body. For the latter case, the extent of stress depends heavily on the size, shape, and flexibility of the device, as well as its implantation site. Implantation in more dynamic regions, such as near muscles, joints, or the cardiovascular system, would likely subject the devices to significantly greater mechanical forces, including compression, stretching, bending, or shear. Such forces can compromise the mechanical integrity of the device's encapsulation, potentially leading to microcracks, delamination, or structural failure [46, 48]. Mechanical stress also varies over time. For instance, scar tissue formation during the healing process can exert compressive forces on the device, while ongoing physiological movements subject it to cyclic loading [47]. In more extreme cases, mechanical stress could disrupt the electrode connections or fracture the encapsulation materials, allowing body fluids to infiltrate and compromise the device's functionality.

Combined Effects of Chemical and Mechanical Stress: The interplay between chemical and mechanical stressors further complicates the challenge of designing reliable packaging for implantable electronics [49]. Mechanical damage, such as cracks or delamination, can create entry points for body fluids, intensifying the chemical attack on the underlying materials. Similarly, chemical degradation of encapsulation materials can weaken their mechanical properties, making them more susceptible to stress-induced failure. These aspects highlight the need for a holistic approach to encapsulation design. Miniaturizing the implant can significantly reduce both chemical and mechanical stress by decreasing the surface area exposed to tissue and minimizing the mechanical forces exerted on the device [46, 43]. Implants targeting different locations in the human body, or designed for specific applications, whether battery-powered, life-sustaining, or non-life-sustaining, require specifically designed packaging solutions. The final packaging must be engineered to account for these factors, ensuring optimal performance and reliability while targeting the intended application and environment.

2.4. MINIATURIZED PACKAGING SOLUTIONS FOR IMPLANTABLE ICS

IC packaging is necessary to protect both the microelectronics within the die and the external interconnects from any environmental factors that could jeopardize their intended reliability. The IC packaging industry has undoubtedly been driven by the requirements in the automotive industry [50]. The high-reliability requirements in the automotive industry have pushed the packaging industry to increase the functional reliability of the chips while being subjected to harsh environments. In the automotive industry, harsh environments can be described as temperature fluctuations, vibration, and to a lesser degree, moisture ingress [51]. As temperature fluctuations are the primary reliability concern for ICs, packages have been engineered and optimized to withstand the stresses induced during these fluctuations experienced under the hood of the car. This has been done by minimizing the coefficients of thermal expansion (CTE) between the IC and the peripheral materials touching the die (polymer package, underfill, and printed circuit board) [51, 50]. For moisture stability, the automotive industry has also rigorous conditions. The current standardized tests for testing moisture robustness are various accelerated tests such as the 85 °C/85% relative humidity (RH) or the highly accelerated stress testing (HAST) [52]. These tests expose the packaged IC to for example 85 °C/85% RH or 120 °C/100% RH for HAST for 1000 and 90 hours, respectively. This test has been sufficient to ensure the moisture robustness of the chip throughout the used lifetimes in automobiles. In comparison to the auto field, for medical implants, temperature is not a concern given the body's constant temperature at 37 °C. Moisture ingress, on the other hand, is a concern as the implant will be exposed to corrosive liquids throughout its intended use in the body [29]. In addition to ionic ingress, the packaging must maintain its biocompatibility and biostability throughout its intended functional lifetime. This requirement severely narrows down the choice of materials and processes that could be used for packaging ICs for implantable applications [53].

Adopted from the automotive field, two methods are currently investigated for miniaturizing the packaging of implantable ICs: conformal (void-free) packaging and micro-cavity packaging ((Fig.2.5)). This thesis will focus on conformal packaging with the following sections providing an overview of the latest developments and associated challenges with this packaging solution. For micro-cavity packaging, the reader is referred to [54, 51].

2.5. CONFORMAL (VOID-FREE) PACKAGING

2.5.1. POLYMER ENCAPSULATION

As explained in the previous section, polymer packaging can be considered as an easy and low-cost method for conformal packaging of ICs. In this case, the die and the metal interconnects (wire-bonds or ball grid arrays) are all covered with a sub-mm thick polymer layer. In [55], a neurostimulator/recorder IC was encapsulated with silicone rubber (Dow 96-083 PDMS) (Fig.2.6). To test the reliability of their silicone packaging, a highly accelerated pressure cooker test was used exposing the packaged ICs to 121 °C and 100% RH for 120 hours. During the test, the ICs were electrically biased. During the stress testing, to monitor the functionality of the ICs reverse telemetry was used to record the

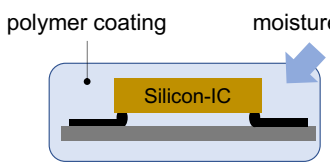
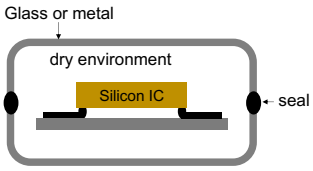
Conformal (void-free) packaging	Microcavity packaging
	
Advantages	
Smaller size: can shrink to IC or component size	Independent of the electronic components, their materials, and interface adhesion
Lower weight. Lower costs	Can include a moisture sensor to detect seal breaches. Could also include a desiccant to delay moisture increase in the enclosure
Disadvantages	
Functional lifetime relies on interfacial adhesion and moisture stability of underlying electronics.	Design and engineering of feedthroughs can be challenging.
Requires long-term testing and evaluation	Functional lifetime relies on the quality of the seal. Requires long-term reliability testing.

Figure 2.5: A comparison of conformal (void-free) vs. microcavity packaging.

internal IC power supply. Stress test results showed stability over the 30 days of testing for four (n=4) of their devices. These results, strengthen the potential of silicone encapsulation as an IC packaging solution for long-term applications.

Besides epoxy and silicone, polyimide is also used extensively in the chip packaging industry [51].

For medical applications, among the several types of polyimide, the BPDA/PPD type is the most commonly used [56]. This type, however, has not been reported to be long-term biocompatible [57]. Encapsulation using polyimide is based on spin coating on the substrate followed by curing at ≈ 400 °C [20]. Due to its excellent thermal and chemical stability, polyimide is compatible with most of the processes used in microelectromechanical systems. Similar to silicone, however, the moisture permeability of polyimide is a concern when implanting for long-term applications and considerations should be taken regarding the moisture-resistivity of the underlying interfaces and materials.

2.5.2. THIN-FILM COATINGS

In the last years, various thin-film coatings materials have been engineered and incorporated in the packaging for implantable ICs [59, 60]. These films have been engineered with one main goal in mind: to increase the moisture barrier properties of the packaging material and delay moisture/ion ingress. Thin-film coatings can be divided into two groups: organic and inorganic (ceramic).

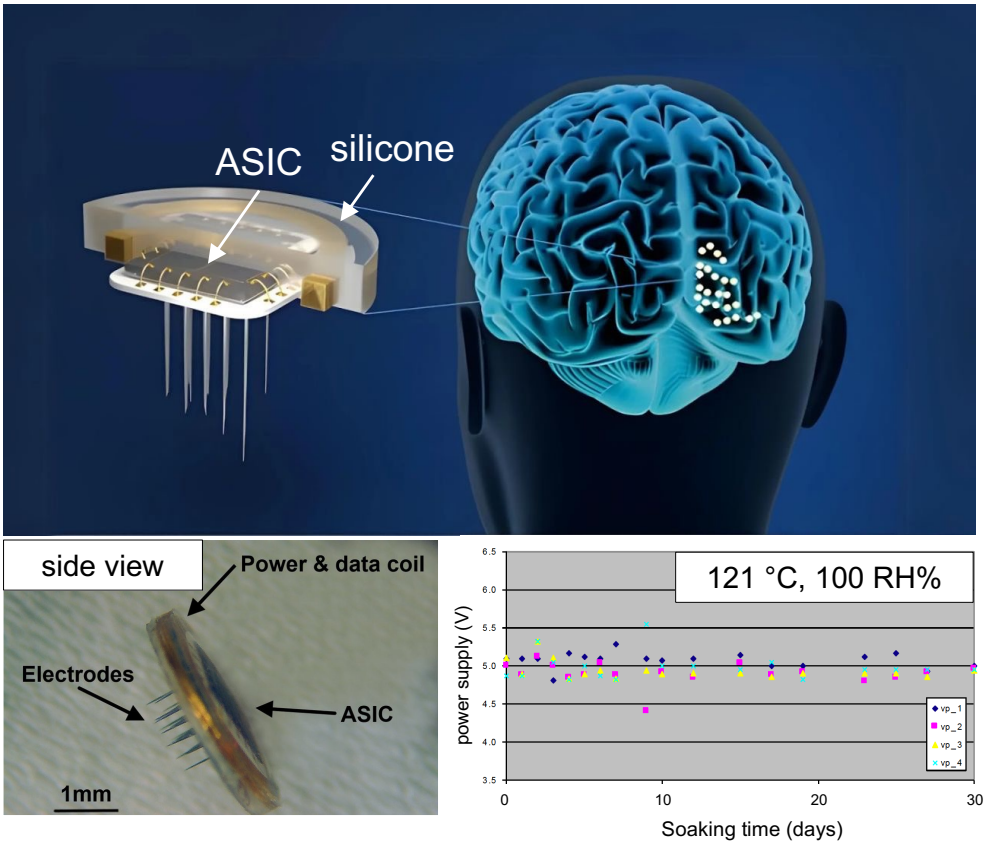


Figure 2.6: A silicone rubber (PDMS) encapsulated neurostimulator/recorder IC [58]. The left bottom image shows the functionality of the device over a 30-day stress test.

Organic thin-films: Parylene-C has been commonly investigated in the implantable medical field due to its demonstrated biocompatibility and protective properties [31]. It is perhaps the most commonly used polymer in the academic field mainly due to its ease of processing but perhaps also due to the wrong notion of its hermeticity. Parylene-C might have lower water vapor transmission rates (WVTR) compared to other polymers, but for the lifetimes intended for medical implants (> 12 months), a 1-5 μm Parylene layer is still permeable to moisture [61, 62]. Similar to epoxy and silicone encapsulation, conformal polymer packaging can be used to achieve a low form factor chip-scale micro-package for implantable ICs. Parylene-C films are applied using the chemical vapor deposition (CVD) process and can be done at room temperature [63]. The low-temperature deposition process makes it very attractive to coat materials and devices that require a low thermal budget. Due to the molecular level deposition process, a uniform and conformal film can be formed over substrate surfaces having complex micro-topography, including sharp edges and crevices providing a conformal, pinhole-free coating. Moreover,

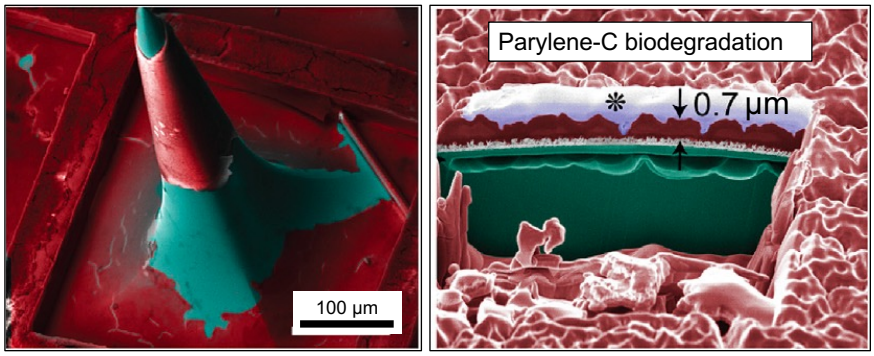


Figure 2.7: Scanning electrode microscope (SEM) images showing biodegradation of Parylene-C after 3.25 years in vivo seen as thinning (3 μm original in comparison to 0.7 μm after in vivo aging) [66].

its high dielectric strength makes it a suitable insulator in electronic packaging within the body. The typical thickness of Parylene-C can range from 1-10 μm.

Parylene-C has been reported to have low adhesion to various metals and silicon-based ceramics. The current industry standard for improving adhesion is the use of a silane-based adhesion promoter (A174) prior to layer deposition [64]. Nevertheless, as will be explained in the next section, weak adhesion can allow condensation of the permeated moisture, resulting in shunt current leakage paths between conductive metals.

Another drawback of Parylene-C is the reported in vivo degradation observed during long-term animal studies Fig.2.7. Degradation has been shown to be in the form of film thinning, cracking, and possible flacking of the material [65]. For packaged ICs employing Parylene-C, such degradation may act as an easy ingress point for body fluids, leading to chip failure.

Inorganic ceramic thin-films: adapted from the semiconductor industry, various thin inorganic ceramic coatings have been explored as barrier layers for implantable electronics. Various silicon-based and metal oxide ceramics such as SiN_X, SiO_2, SiC, Al_2O_3, HfO_2, TiO_2 are a few examples of such inorganic films [67]. Besides having lower WVTR rates compared to organic thin films like Parylene-C, these thin-film ceramics have also shown good biocompatibility [68, 69].

Thin-film ceramic films can be deposited using different processes requiring different temperatures. The best quality films are usually deposited using a low pressure chemical vapor deposition (LPCVD) technique, which is performed at above 800°C [70]. These films can have the highest densities and barrier properties. LPCVD films of silicon nitride, in conjunction with silicon dioxide, have been used to encapsulate conductors and have been shown to be stable in saline, under mechanical and electrical stress, for more than two years [63]. Within the semiconductor industry, the process and temperature usually used for depositing silicon nitride (SiN_X) is plasma enhanced chemical vapor deposition, done typically at $\approx$ 400 °C. The main challenge in using these barrier materials is that they typically require a high temperature to achieve a reasonable deposition rate and density. In some instances, these films are not quite as conformal as required by some applications. For higher conformality, atomic layer deposition (ALD)

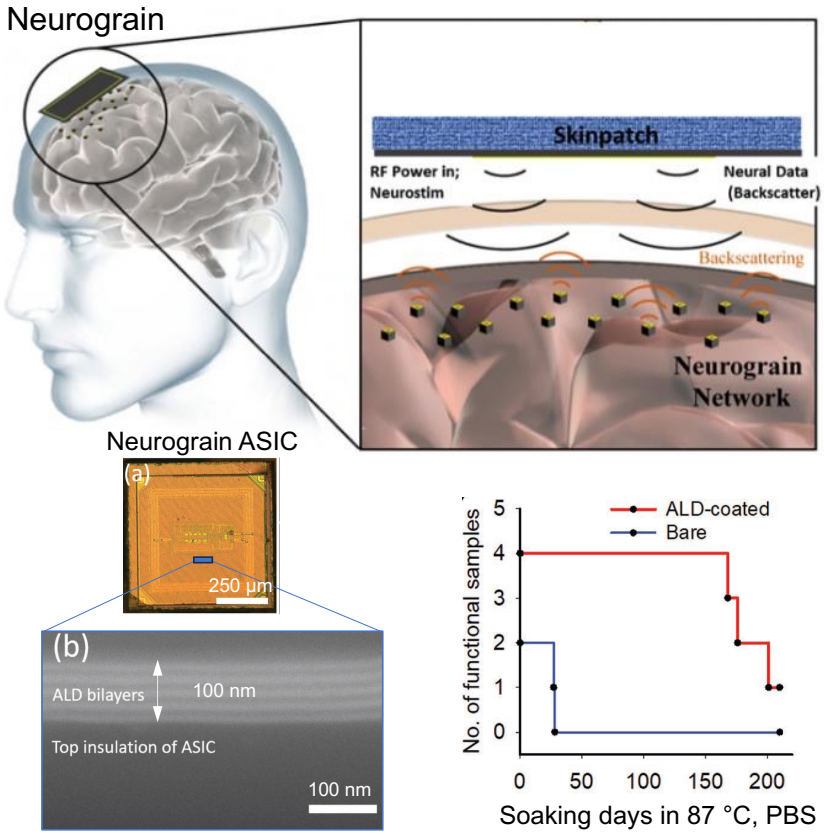


Figure 2.8: A neurostimulator/recorder ASIC coated with a thin-film ceramic ALD layer [74].

is well-suited for depositing high-density thin films with precise thickness [71]. ALD is usually used for applications that require high purity, precise film properties, and excellent control over film thickness (typically 1 – 100 nm). ALD equipment can be relatively complex and expensive due to the need for precise control over precursor delivery and reaction conditions. Fig.2.8 shows an ALD-coated neurostimulator IC also known as the 'Neurograin' [72]. To evaluate the longevity of the coating, stress testing in phosphate-buffered saline (PBS) solution at 87 °C on both coated and uncoated chips was done which showed an x5 increase in the functional lifetime of coated ICs compared to uncoated bare dice [73]. Failure was recorded as a shift in the backscattering frequency. The authors of the paper, however, do not explain the reasons for failure, of their uncoated and coated chips. Scanning electron microscope (SEM) cross-sectional investigations on the failed ALD-coated ICs demonstrated the presence of the ALD stack remaining intact throughout the stress-soaking.

One of the main issues with thin ceramic barrier layers is the presence of pinholes or defects which can negatively impact their barrier properties [75]. To mitigate this

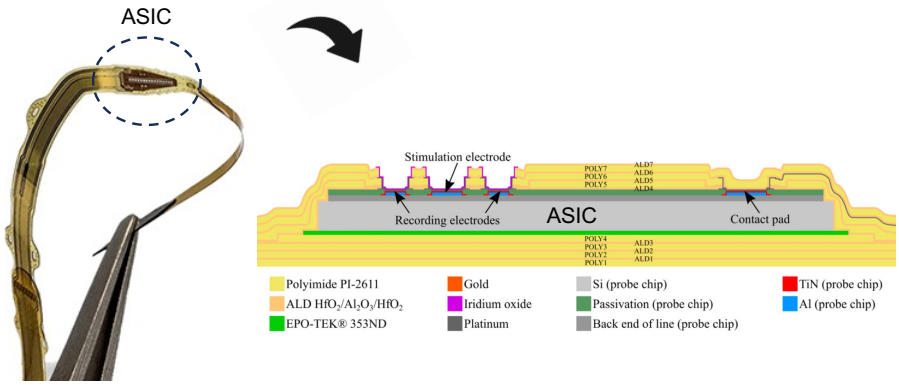


Figure 2.9: A neurostimulator ASIC coated with a hybrid polyimide/ALD thin-film layer [78].

issue, brittle ceramic films can be encapsulated with a final biocompatible polymer. The brittleness of these inorganic layers is also an issue that sets some requirements for the thermal budget and the polymer that is applied as the final coat. In [76], the use of a soft silicone final encapsulation on ALD was suggested. Given the low Young's modulus of silicone (≈1 MPa for silicone vs. 3 GPa for Parylene-C) it can be used as a mechanical buffer on top of the ALD while minimizing the stresses on the ceramic during silicone processing (expansion and shrinkage during curing) or the lifetime aging in the body (moisture-induced expansion of silicone).

Hybrid ceramic-polymer coatings: As discussed earlier, the presence of defects and pinholes together with brittleness are two major issues for inorganic ceramic films. To mitigate these drawbacks, another technique has been combining ceramic films with thin polymer layers with more flexible characteristics. A few examples of this combination are [75] and [77] where they combined ALD-deposited films with Parylene-C or polyimide.

As an example, Fig.2.9 shows an implantable device using a multilayer ALD/polyimide coating for packaging the IC.

2.6. CHALLENGES IN CONFORMAL PACKAGING OF IMPLANTABLE ICS

2.6.1. VOID AND DEFECT-FREE PACKAGING

One of the main challenges when packaging electronics with polymers like silicone or epoxy is to create a void-free environment within the package, specially around the sensitive components [63]. Voids in the polymer can be saturated with moisture when the device is implanted in the body [79]. If the voids are situated in a critical spot of the device, e.g. between two conducting metal lines, it can result in shunt electrical paths, altering the impedance between the two metal lines (Fig.2.10). Depending on the circuitry, the altered impedance can result in electrical malfunction, power drainage, or

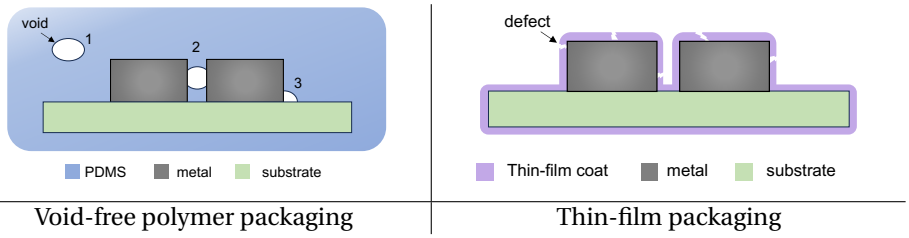


Figure 2.10: Schematics depicting voids and defects for polymer and thin-film coating applied on metallization structures. For void-free polymer packages, three types of voids could be present: 1) in the polymer away from critical devices, 2) in between critical metal traces, and 3) on substrate materials (metal or components) but not in between critical metallization.

total failure of the device. Other factors such as biasing between the metal lines and contamination can increase the condensation rate within the void [80]. As a result, the shunt impedance will have a lower resistance causing further power draining or functionality loss.

For thin-film coated electronics, any imperfection or openings in the coating will allow the ingress of ionic fluids. Similar to voids in a polymer, openings can interrupt the electrical performance when touching critical metal lines but also result in electrical open circuits by gradually degrading/corroding the metals [81].

With the miniaturization of the next generation of devices, ensuring a void-free packaging is even becoming more critical. In addition, these emerging applications will have neural sensing functionality with signals in the μV range where even tiny amounts of shunt leakage path can result in signal loss.

2.6.2. ADHESION

Adhesion between the coating and all the substrate materials is critical for the longevity of the implants [9, 82]. Adhesion is critical for both polymer-encapsulated and thin-film-coated devices. For thin-film barriers with low WVTR, film delamination can weaken the structural integrity of these barrier films and result in failure [75, 83].

Similar to voids, interfacial adhesion loss can result in gaps between the encapsulant and the underlying materials. Unlike visible voids, however, adhesion losses are undetectable right after coating and typically occur gradually over time as the device is stressed in the aging media (human body).

Adhesion depends not only on the coating materials but on the interfacial interaction that is made between the coating and the encapsulant [84, 83, 79]. Therefore, for proper design and selection of the packaging, a good understanding of all the substrate materials and electronic devices is necessary. Below, a few material examples typically used for implantable application are given which have demonstrated poor and good adhesion to silicone.

POOR ADHESION: PLATINUM AND GOLD

Platinum and gold are noble metals with excellent long-term biocompatibility and biostability with high corrosion resistance [29]. Due to these favorable properties, they have

been frequently used in the implantable medical device industry. However, their poor adhesion with polymers can limit their use in critical areas where strong long-lasting adhesion is needed [80, 85].

STRONG ADHESION: SILICON-BASED CERAMICS AND METAL OXIDES

Various ceramic materials such as alumina [9], silicon-based ceramics[86], and some metal-based oxides (such as HfO_2)[87] have been shown to have long-lasting underwater adhesion with silicone.

Besides strong adhesion, the cleanliness of the substrate materials is also critical in ensuring a successful and reliable encapsulation/coating. Contamination on the surface not only will prevent the formation of the desired chemical bond but will also accelerate the condensation of the permeated moisture on the substrate surface. The condensed moisture in combination with the surface contamination will result in more aggressive shunt leakage paths [82]. Therefore, the cleanliness aspect cannot be emphasized enough.

2.6.3. MOISTURE-RESISTANCE OF UNDERLYING ELECTRONIC COMPONENTS

As explained previously, all polymers, including Parylene-C and LCP, will allow moisture ingress over periods of 7 - 30 days at a 37 °C ambient (varying based on the thickness of the polymer) [32, 83]. This drawback for polymer packaging creates a key requirement for the underlying electronics: all materials and interfaces that are used in the electronic device should be moisture-robust [88]. This requirement further limits the choice of materials and processes that could be used for the fabrication of the electronics. For example, in [86] interdigitated aluminum metallizations were coated with a thin SiO_X ceramic and a final silicone overmold. Long-term Impedance measurements showed a gradual change in the spectra when the device was submerged in PBS solution at 67 °C. Optical microscopy did not show any material delamination, dissolution, or metal corrosion which could explain the change in the impedance spectra. However, when using detailed material analysis (X-ray photoelectron spectroscopy and SEM cross-sectional analysis) it was found that the SiO_X ceramic showed signs of chemical modification and hydration, which could alter the dielectric and insulation properties of the layer. Another example in the same literature was the corrosion of the Au-Al wire-bonds. The silicone-encapsulated Au-Al interface resulted in a galvanic reaction triggered by moisture [81]. Over time, the galvanic reactions resulted in the corrosion of the least noble metal, in this case, Al.

Overall, for silicon-ICs, if the materials used by commercial foundries are found to be unstable when exposed to moisture (100% RH), this would make the packaging a daunting task and limit their chronic application.

2.7. EVALUATION OF COATING PERFORMANCE AND LONGEVITY ESTIMATION

As explained in the previous section, one of the main advantages of hermetic enclosures is the standardized helium leak test. As this test is done on each individual device, the hermeticity of each implant can be verified prior to implantation. For the next genera-

tion of active medical implants employing void-free conformal packaging, there is no standardized test for determining functional longevity. As these packaging solutions could be a viable option for future implants, new techniques are required to evaluate and verify their reliability and targeted longevity. The current practice to evaluate the reliability of polymer-packaged electronics is to submerge the device in a physiological environment such as PBS which has a similar osmotic molarity and pH to body fluid [89]. Some studies have also proposed the use of adding hydrogen peroxide to the PBS solution to better mimic the radical oxygen species present during the first week to months of the implantation [65]. Nevertheless, all these in vitro environments are a simplified model of the complex chemical environment of the body. Therefore, one should validate the in vitro aging studies by performing a comparison with in vivo aging. As devices are getting smaller and more compact, observing and understanding potential reliability issues is much more challenging compared to larger devices [90]. Special tools must be applied to visualize defects or other issues throughout the development, manufacturing, and prior release of the device. Additionally, once the device is implanted, understanding the failure mechanisms and the effect of various stressors (chemical, mechanical, and electrical) can significantly help in increasing the reliability. This section will give a brief overview of the techniques that can be used for evaluating the performance of polymeric packages or thin-film coatings. Similarly, techniques that can be employed for evaluating the integrity of IC structures will be discussed.

2.7.1. INTERDIGITATED CAPACITOR STRUCTURES

Interdigitated capacitors (IDC) are useful test vehicles for evaluating encapsulation and adhesion performance. Using IDC structures various studies have evaluated the long-term performance of silicone, polyimide, Parylene-C, epoxy, and LCP [80, 83, 91]. These structures are also valuable for evaluating the barrier properties of thin ceramic coatings [86]. The main advantages of IDC structures compared to other encapsulation performance techniques are, 1) the capability of using sensitive electrical characterization techniques to measure insulation performance: DC current leakage, and electrochemical impedance spectroscopy (EIS), 2) the ability to evaluate the effect of various electrical signals (DC or AC) on the long-term aging of materials [80]. Fig.2.11, for example, shows an IDC structure that was used for evaluating the Parylene-C coating on platinum IDC metallization and SiO_2 (used as substrate). EIS measurements performed over the duration of aging can reveal various chemical and mechanical phenomena occurring on the materials and interfaces. For example, as shown in [92] changes in the EIS magnitude at lower frequencies (<10 Hz) can be used to demonstrate shunt current leakage paths developing between the comb structures (bottom left microscope image in Fig.2.11). The effect of continuous electrical biasing on the shunt leakage growth and/or material degradation can also be picked up using EIS measurements (Fig.2.11 right bottom).

The drawback of IDC structures is the detailed set-up development, cabling and interconnection required to ensure that the set-up is more reliable and robust throughout the aging than the test structure itself. In [91], the authors describe an apparatus that is carefully designed for such long-term material aging studies.

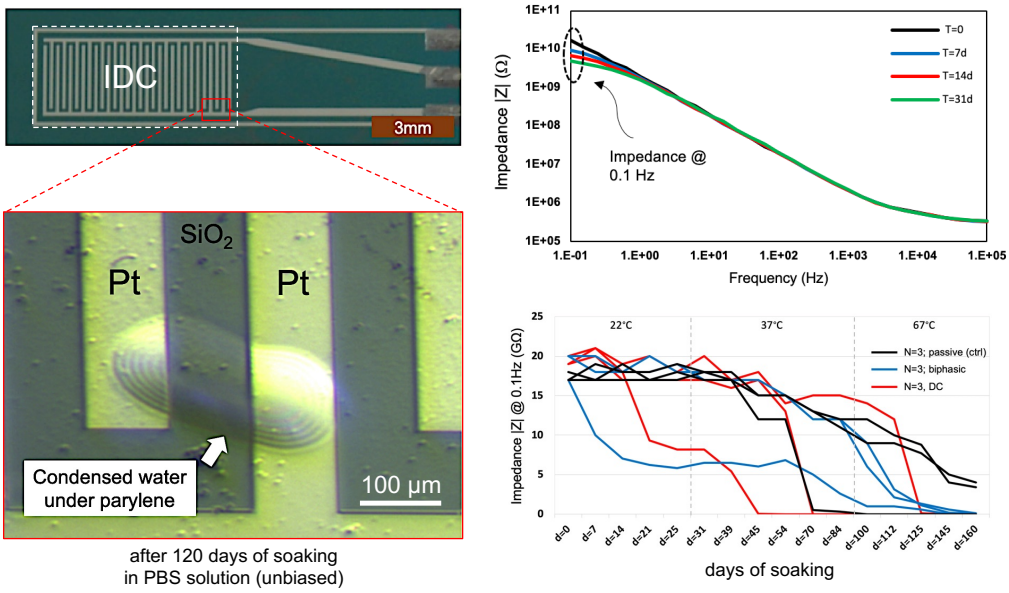


Figure 2.11: IDC test structures used for evaluating coating performance and the long-term effect of electric signals [93, 76].

2.7.2. ACCELERATED TESTING WITH ELECTRICAL BIASING

For medical devices intended for 5-10 years of functional lifetime, performing real-time aging (at 37 °C) is almost impractical. For this purpose, accelerated aging of the materials and the packaging can be used [91, 94]. The current method for accelerating the degradation of polymers and interfaces is by increasing the testing temperature [63, 20, 95]. In addition to aging the polymer, temperature will also play a role in accelerating moisture permeation within the polymer [63]. For interfaces and coatings, differences in the coefficient thermal expansion (CTE) can also result in stresses, accelerating delamination [90].

Electrical biasing can also play a role in aging electronics and accelerating device failure, especially when the device is exposed to high moisture levels. In [96] it was shown that unbiased devices had a ≈ x13 longer lifetime compared to biased devices. The tested device was a wirelessly powered ASIC comprised of a neural recording chip, and a few passive components (capacitors and a coil). The authors did not report the reason for the failure. Therefore, an in-depth understanding of the effects of biasing on failure(s) is lacking. In [97], to better understand the effect of biasing on failure, IDC structures were coated with a thin Parylene-C layer and subjected to three different stress signals: unbiased, DC-stress, and AC-stress. Results showed how different electrical signals can affect the insulation between the interdigitated metallization and lead to different failure mechanisms.

Similarly, in [76], the effect of DC electrical biasing on ALD-coated IDC structure was investigated. Without biasing, the ALD coating maintained a relatively stable electrical

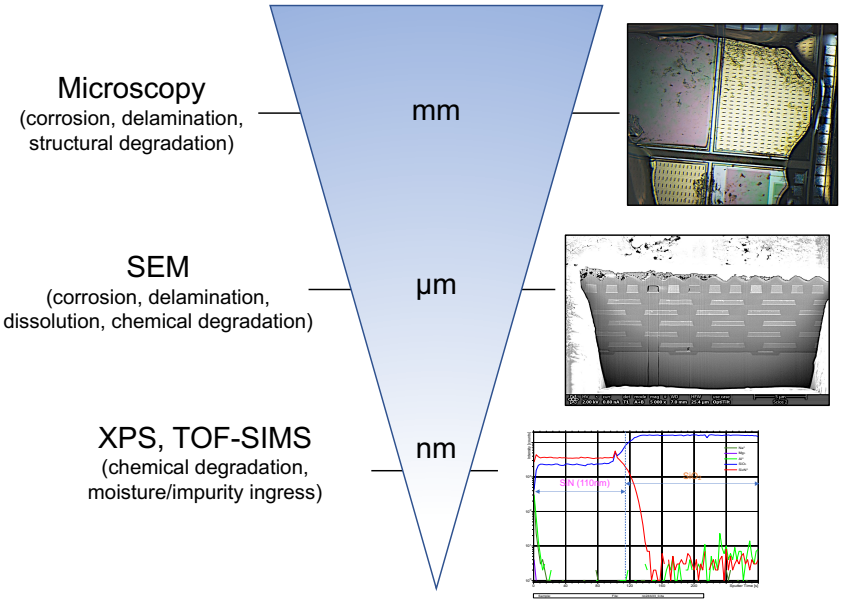


Figure 2.12: Various material characterization techniques used for capturing overview (mm-level) and surface level (nm-level) info from the coating and materials used for IC packaging.

impedance for over 400 days when submerged in PBS solution. However, after one day of electrical biasing, all the ALD coating on the biased metals cracked (WE and CE), exposing the metals to PBS solution.

These findings highlight the importance of investigating the effect of electrical biasing when evaluating the functional lifetime of implantable electronics.

2.7.3. MATERIAL EVALUATION TECHNIQUES

Complementary to the electrical measurements, material analytical techniques can be valuable tools for evaluating coating performance. For example, for silicon-IC, various material analytical techniques are used for failure analysis [98]. Below a few of these techniques will be briefly described. As shown in Fig.2.12, these techniques provide information on the materials at different scales.

MICROSCOPY

During microscopy, the exterior of the package can be evaluated in detail. Depending on the transparency of the polymer, various failures can be identified: cracking of the polymer, delamination of polymer from the substrate materials (usually seen as Newton rings or bulging and blisters), and polymer degradation (seen as color change). Microscopy can be used from low magnification (x4) for acquiring overviews of the device, to higher magnifications (x200) to observe film defects, cracks, or blisters in both polymers and ceramics.

For silicon ICs, microscopy can be a quick and useful technique for chip inspection

and acquiring an overview of the entire chip: pads and wire-bonds, top metallization, IC passivation (final top dielectric), and all four side walls of the structure. It is also useful in identifying the possible location of failure(s), helping further steps in the root cause analysis process. Microscopy is also a practical tool for corrosion inspection on the pads and wire-bonds. Early film delamination within the IC's material stack could be picked up with microscopy.

SEM CROSS-SECTIONAL ANALYSIS

Scanning electrode microscopy can be used for higher magnification (x100K) for a closer inspection of the failure. SEM surface analysis at high magnification is extremely valuable for identifying cracks or defects in the film. For analyzing cross sections of the material stack, focused ion beam (FIB) can employed in the SEM machine. SEM inspections on the FIB cuts can provide valuable insights on layer losses (due to dissolution), film delamination or chemical modification [86, 90].

CHEMICAL CHARACTERIZATION

Understanding the chemical stability and ionic/moisture barrier properties of the materials post long-term aging (in vitro or in vivo) is key in engineering long-lasting devices. Time-of-flight secondary ion mass spectrometry (TOF-SIMS) is perhaps one of the most sensitive analytical techniques that is frequently used within the semiconductor industry. During IC fabrication, owing to its high sensitivity, ToF-SIMS is used to detect trace levels of impurities that could arise due to contamination or diffusion. Another key advantage of ToF-SIMS is the ability to generate detailed molecular and elemental maps with high spatial resolution. In the depth profiling mode, ToF-SIMS can provide information, with parts-per-billion-level (ppb) detection limits, from the surface of the material all the way into the micrometer depths of the layer.

The main drawback of ToF-SIMS, however, is the lack of quantitative data due to the matrix effect. The matrix effect makes it difficult to perform quantitative analysis because the signal intensity for a given element or molecule can vary depending on the surrounding matrix, leading to inaccurate concentration measurements [99]. To resolve these drawbacks, ToF-SIMS can be complemented with X-ray photoelectron spectroscopy (XPS) analysis. XPS is a surface-sensitive analytical technique that detects the elemental composition and chemical states of materials. In comparison to ToF-SIMS, it has lower sensitivity, capable of detecting elements in concentrations as low as 0.1 atomic percent. However, one of its main advantages is the ability to provide detailed chemical state information (for example capable of identifying how silicon is bonded to oxygen in a SiO_2 network). Similar to ToF-SIMS, XPS operates under ultra-high vacuum conditions, typically around 10^{-9} to 10^{-10} torr, to prevent contamination and ensure accurate measurements. XPS cannot detect hydrogen (H) and helium (He) because these elements lack core-level electrons that can be ionized by the X-ray source. It also has lower sensitivity for light elements like lithium (Li), beryllium (Be), and boron (B), making accurate detection more challenging. ToF-SIMS is generally used for these elements [98].

ON-CHIP MONITORS

For automotive ICs, cracking of the die passivation layers has always been a major reliability concern [51, 100, 101]. Various investigations have shown passivation cracking to be induced by the expansion of the polymer packaging which is generally an epoxy composite with high Young's modulus [50, 98, 102]. Variations in the thermal expansion coefficient between the packaging polymer and the die passivation can result in interfacial shear stresses causing cracks in the brittle passivation. For this purpose, various on-chip complementary metal-oxide semiconductor (CMOS) crack sensors have been proposed that can monitor and map possible stresses on the die surface [103, 104, 105]. Moisture-induced expansion of the epoxy or any other polymer package could also result in stresses at the interfaces [100]. For an IC exposed to 100 % RH, a cracked die passivation can pose an even greater risk as it provides an easy entry point for moisture and ions. [106].

Similar to the top passivation, the sidewalls of the chip can be a point of impurity ingress. Especially during die singulation, stresses can be exerted on the IC's material stack, causing cracking [90]. For sidewall protection, both as an impurity barrier and a crack stop, the IC industry has been using die seal rings [107]. Die seal rings, as the name suggests, are metal rings around the die made of different metal stacks and vias present in the IC process. In [108], the authors incorporated a sensor within the seal rings to monitor the potential penetration of impurities from the sidewalls.

As ICs will be integral components for future miniaturized electronic implants, monitoring their integrity is essential for ensuring a reliable operation. I believe such an on-chip monitor will be an essential component for polymer-packaged implantable ICs.

2.7.4. LONGEVITY ESTIMATION

As explained previously, the lack of an equivalent test similar to the helium leak test for polymer-packaged implants is perhaps one of the main challenges when evaluating and verifying the package. This drawback can also make the design and development process challenging as long lead times are needed to evaluate and identify possible defects, especially when long lifetimes are required. Accelerated testing in combination with in vivo studies can be valuable when combined with detailed material and electrical analysis techniques [66]. Data from various analytical techniques can enable early identification of possible degradation pathways which could help in the longevity estimation of the device.

2.8. RESEARCH OBJECTIVES OF THESIS

Through an examination of existing literature, two main gaps have been identified and will be addressed in this thesis:

1. **On-chip moisture/ion integrity monitors**: For implantable ICs, moisture/ion ingress in the silicon die can cause unpredictable and unintended functionality, raising potential safety risks.

2. **Long-term evaluation of materials**: The degradation of materials in the implant environment is usually a very slow process, requiring a dedicated set-up and special analytical tools. Therefore, it is not usually pursued as an academic project.

Nevertheless, this thesis aimed to evaluate the long-term performance of three components: 1) bare-die IC structures, 2) PDMS as a soft but moisture-permeable packaging material for ICs, and 3) two thin-film coating barriers as chip-scale micro-package solutions.

Based on these identified gaps, the following research objectives are defined.

Research objective #1: develop on-chip CMOS tools for monitoring moisture/ion ingress and coating performance (chapter 3).

Research objective #2: evaluate the long-term stability of bare-die silicon ICs in physiological media (chapter 4).

While existing research primarily focuses on developing and evaluating new coating materials for implantable IC packaging, this objective seeks to investigate the often-overlooked aspect of the long-term stability of bare silicon ICs within physiological environments. By analyzing the behavior of bare ICs over extended periods, this research aims to contribute valuable insights into enhancing the durability and reliability of implantable devices and identify potential areas for improvement in IC packaging.

Research objective #3: evaluate the long-term stability of PDMS-coated silicon ICs (chapter 4). Complementing the examination of bare silicon ICs, this goal delves into the performance of silicon ICs coated with PDMS, a soft and compliant material commonly used in implantable device packaging. By comparing the degradation patterns between bare-die ICs and PDMS-coated counterparts, this research aims to elucidate the protective capabilities of PDMS.

Research objective #4: evaluate the long-term stability of two potential thin-film coating solutions (HfO_2-based ALD and hybrid Parylene-ALD multilayers) for silicon IC packaging (chapter 5). This objective focuses on evaluating the effectiveness of two distinct thin-film coating barriers, namely, a 100 nm HfO_2-based ALD multilayer, and a 6 μm hybrid Parylene C titanium-based ALD multilayer, in preserving the long-term stability of silicon ICs. By implanting the coated ICs in rat animal models for a 7-month duration, this research seeks to elucidate the protective mechanisms offered by these coatings and their suitability for enhancing the reliability of implantable ICs.

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3

ON-CHIP CMOS TOOLS FOR INTEGRITY MONITORING

Silicon-ICs will be integral components for miniaturized implantable devices. However, the lack of a hermeticity test for polymer or thin-film packaged ICs necessitates the development of new methods to assess their integrity, both before and during implantation in the body. In this chapter, I proposed two novel on-chip monitors for evaluating the integrity of the coating and the chip itself. The first part of this chapter presents the design and silicon validation of an on-chip moisture/ion integrity monitor developed for early detection of impurity ingress within the die structure itself. The second part focuses on a concept that uses the IC's silicon bulk to evaluate the integrity of coatings applied for IC packaging. This chapter is a verbatim copy of the following papers [1, 2], and only section and figure numbers were changed to comply with the format of this thesis. The IC design for the first part of the chapter was done by Ömer Can Akgun. The ALD coating in the second part of this chapter was done by Riina Ritasalo at Picosun Oy.

3.1. A CHIP INTEGRITY MONITOR FOR EVALUATING LONG-TERM ENCAPSULATION PERFORMANCE

3.1.1. INTRODUCTION

Striving towards less invasive therapies and inspired by scaling within the semiconductor industry, in the past years, tremendous efforts have been made to miniaturize active implantable medical devices (AIMDs) [3]. Further scaling of AIMDs, however, has always been limited by the physical constraints of the battery [4]. In this regard, wireless energy transfer techniques using electromagnetic [5] and acoustic energy [6] have been recently proposed as alternative energy delivery solutions that can circumvent the size restriction of the battery and enable the realization of free-floating mm-sized single-chip implants. These mm-sized AIMDs can be instrumental in the expansion of new research fields within biology and medicine, e.g. implantable sensors [7], brain-machine interfaces [8], neuroprosthetics [9], and bioelectronic medicine [10]. Furthermore, the low

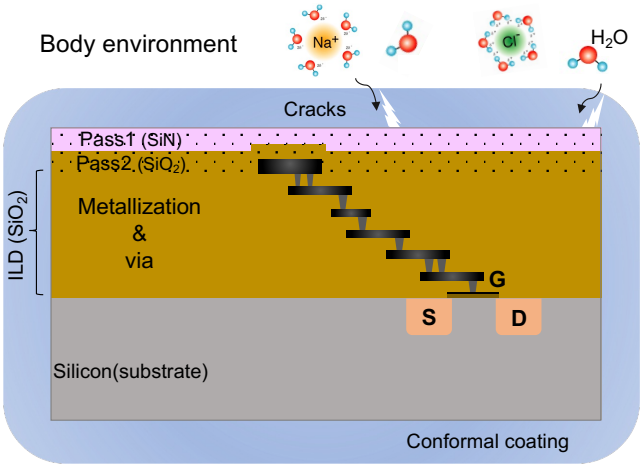


Figure 3.1: Schematic illustration of moisture/ion ingress through cracks for a conformally coated silicon die (dimensions not to scale).

footprint of these devices is expected to limit scarring and tissue inflammation, making them ideal tools for pre-clinical and clinical research, and later on, for long-term therapy delivery [11].

Despite these great efforts, one of the remaining hurdles for introducing such tiny devices for clinical applications is ensuring their intended lifetime functionality when exposed to biofluids [12]. In wet ionic environments like the human body, failure of electronics can occur due to the ingress of moisture and ions through the packaging. For silicon integrated circuits, such ingress through the top passivation and interlayer dielectrics (ILD) would result in parameter changes in the passive (capacitive/resistive) and active (MOS transistor) components, as well as shorts and/or hard opens that would eventually lead to device failure [13]. Conventionally, AIMDs such as pacemakers and cochlear implants have relied on titanium (Ti) packages for protecting the inside electronics against the surrounding fluids [14]. This packaging solution, however, no longer meets the dimensional requirements of mm-sized implants. For this reason, various biocompatible polymeric [15] and/or thin ceramic conformal coatings [16] have been proposed which add minimally to the overall size and weight of the device and could make possible the realization of more flexible implants [17]. These protective coatings usually feature high barrier properties and aim at increasing the lifetime operation of the chip by blocking moisture and ions ingress. Despite this protection, ingress of moisture/ions could still occur either through delamination or imperfections such as cracks in the coating (see Fig.3.1) and result in device malfunction and potential safety hazards.

To justify the use of conformally coated mm-sized implants for pre/clinical practices, their operational functionality has to be guaranteed for the intended duration of the study. So far, the lifetime functionality of AIMDs has been predicted using the standardized helium leak test method [18]. This test, however, cannot be applied to conformally coated single-chip implants, mainly due to their small size and lack of cavities [12]. In these cases, a statistical prediction is used instead, which is based on accelerated aging

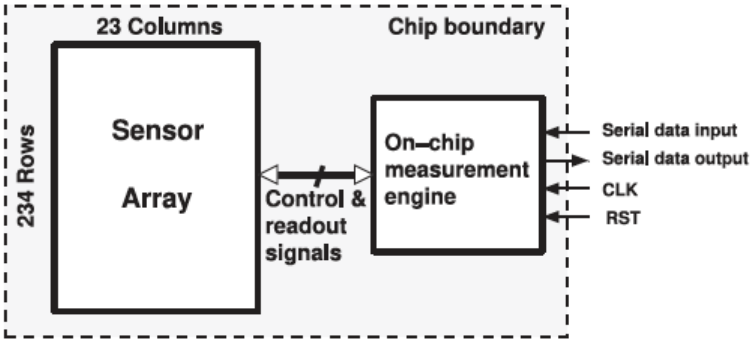


Figure 3.2: Block diagram of the implemented system showing the sensor array used for ion and moisture ingress experimentation and the measurement engine used for automatic control, readout, and transmission of the measurement results to off-chip for further processing.

tests on a large group of samples. During such tests, incipient detection of moisture/ions ingress will grant a better understanding of the failure mechanisms within the chip and ultimately result in a more accurate lifetime prediction [19, 13].

This chapter proposes and presents the implementation of an in-situ sensor array for early detection of moisture/ion infiltration within a CMOS chip. The measurement principle employed for such a sensor array, supported by a proof of principle, was first presented in [1]. Here, in this extended manuscript, previously unpublished circuit analysis and details on the design and implementation of the proposed sensor are reported. Furthermore, additional characterization of the system in wet environments shows the more complete functional capabilities of the system. The presented and employed sensing method is based on tracking the resistance change in the interlayer dielectrics between successive metal layers in the chip, which act as ingress sensors. To verify the functionality and capability of the ingress sensors, we implemented a platform that can track the resistance change throughout the 234 × 23 sensor array and at different depths of the chip. The block diagram of the implemented system is shown in Fig.3.2. Time-mode operation as described in [20] is used, where a pulse width carries the measurement information and quantization of pulse width measurements are used to detect the changes in the ILD with a tuneable measurement range and measurement accuracy.

3.1.2. ILD RESISTANCE MEASUREMENT

MEASUREMENT CONCEPT

The proposed ILD resistance measurement method is based on measuring the (RC) time constant of the ILD between two successive metal layers (see Fig. 3.3(a)). In this method, a node with extremely high resistance in parallel to a capacitance, in this case the upper metal layer, is charged. The lower metal is hardwired to the ground. Later, that same charged node is left floating to discharge through the ILD resistance. By measuring the actual time needed to discharge the capacitance and accounting for the known value of

the total node capacitance, it is possible to calculate the ILD resistance.

A simple model of the method is shown in Fig.3.3(b). **n1** is the node that is charged and then left floating when the switch opens, R_{ox} is the resistance of the ILD oxide, representing the irregularities in the oxide structure that is intended to be monitored, C_{ox} is the oxide capacitance between the floating node and the ground plane, and R_{shunt} represents all the other current leakage paths due to the active elements connected to **n1**. As the model in Fig.3.3(b) shows, a familiar parallel RC circuit is created once the switch opens. The total stored charge on the capacitor will discharge through the resistors as shown in Fig.3.3(c). The voltage at **n1** is VDD just before the switch opens, and after that, at time t, it is given by

$$\mathrm{V}_{\mathbf{n1}}(t) = \mathrm{VDD} \cdot e^{-t/R_{eq}C_{eq}} \tag{3.1}$$

where $R_{eq} = R_{ox} /\!/ R_{shunt}$ and C_{eq} is the combination of all the capacitances to ground at node **n1**. By measuring the time it takes for node **n1** to be discharged to a specific value, in our case VDD/2, the RC time constant between **n1** and ground may be measured with a very high accuracy. For a target discharge threshold of VDD/2, the discharge time and the RC time constant at **n1** are given by

$$\mathrm{T}_{\mathrm{discharge}} = \ln(2) \cdot R_{eq}C_{eq} \tag{3.2}$$

$$R_{eq}C_{eq} = \frac{\mathrm{T}_{\mathrm{discharge}}}{\ln(2)} \tag{3.3}$$

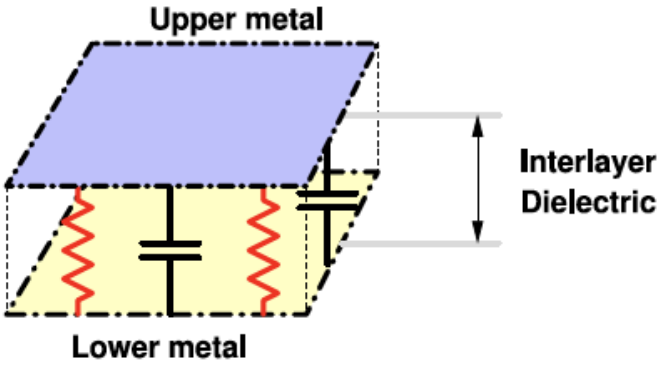
SENSING PERFORMANCE

The measurement capability of the implemented pixel depends on the sensor element design and process parameters. The ILD resistance, which is the quantity to be measured, is given by

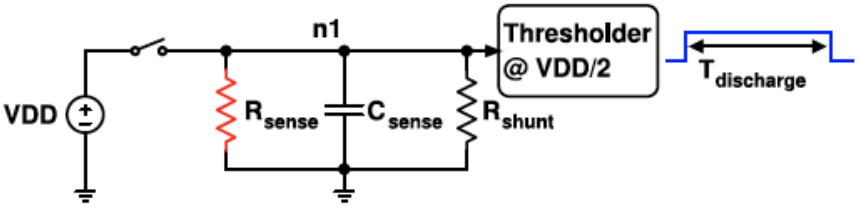
$$R_{sense} = \rho \frac{L}{A} \tag{3.4}$$

where R_{sense}, ρ, L, and A are the resistance, electrical resistivity, length, and area of the ILD between the sensor plates, respectively. As reported in [21], ingress and absorption of moisture/ions in SiO_2 films can reduce their electric resistivity. The reduction rate, however, may not necessarily be linear and depends on the properties of the dielectric layer, e.g. composition, density, porosity, and levels of defects [22]. As the change in electrical resistivity is monotonic with increasing ingress but not linear, the platform proposed in this work is designed to track the changes in the dielectric resistance, and linear change in the electrical resistivity is not a requirement for correct operation. For the 0.18 μm process used, the distance between the metal plates (L) is 1 μm and for the chosen sensor implementation that will be presented in the next section, the area is 58.17 μm^2. The value of ρ depends on the manufacturing process and its value ranges between 10^{12} Ωm [23] and 10^{16} Ωm [24]. Based on these values, the ILD resistance of the sensor is expected to be in the peta-ohm to exa-ohm [10^{15} - 10^{18}] range. The measurable time constant of the sensor pixel is given by

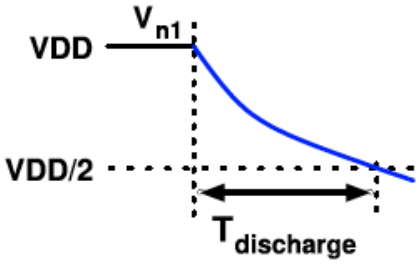
$$\tau = R_{meas} \cdot C = R_{meas} \cdot C_{sense} + R_{meas} \cdot C_{upper} \tag{3.5}$$



(a) Interlayer dielectric (ILD) RC components



(b) Simple model of the proposed measurement method



(c) Discharge operation and timing

Figure 3.3: Proposed ultra-high resistance measurement method.

where τ is the time constant, R_{meas} is the effective measurable resistance between the metal layers of the sensor element, C_{sense} is the capacitance between the metal layers, and C_{upper} is the total capacitance (except that of the sensor plates) to the ground connected to the upper metal layer of the sensor. The resistance R_{means} is the parallel equivalent of two resistive elements, the ILD resistance (R_{sense}) and a resistance value (R_{shunt}) denoting the leakage is due to the active elements connected to the charged node, and is given by

$$R_{meas} = R_{sense} /\!/ R_{shunt} \tag{3.6}$$

$$R_{meas} = \frac{R_{sense} \cdot R_{shunt}}{R_{sense} + R_{shunt}} \tag{3.7}$$

As we are interested in the changes in R_{sense} due to an ingress event, how a change in R_{sense} results in a change in the measurable resistance R_{means} is of importance. The unit change in R_{meas} due to a unit change in R_{sense} is given by

$$\frac{\partial R_{meas}}{\partial R_{sense}} = \frac{R_{shunt}^2}{(R_{shunt} + R_{sense})^2} \tag{3.8}$$

$$\Delta R_{meas} = \underbrace{\frac{R_{shunt}^2}{(R_{shunt} + R_{sense})^2}}_{\text{resistance transfer coefficient}} \cdot \Delta R_{sense} \tag{3.9}$$

For our implementation and the process used, the total leakage current from the upper metal plate (node **n1**) is simulated to be 3.42 fA, resulting in an average R_{shunt} value of 526 TΩ. This value of R_{shunt} matches perfectly with our measurements presented in Section V and sets the upper limit of measurable resistance. Furthermore, any change in R_{sense} will be measured after being multiplied by the resistance transfer coefficient (RTF) in (12). In (12), as R_{shunt} gets larger, i.e., as any of the leakage currents of the active elements connected to the measurement node get smaller, RTF gets larger resulting in a larger ΔR_{meas}, i.e., a greater change in the measured resistance. Therefore, during the design of the measurement pixel, care should be taken to minimize the current leakage from the measurement node.

3.1.3. SENSOR PIXEL CIRCUIT DESIGN

SENSOR PIXEL SCHEMATIC

The ILD resistance measurement concept presented in the previous section has been designed and implemented in a 0.18 μm standard CMOS process with 6 metal layers. The schematic of the novel resistance sensor pixel is presented in Fig.3.4. The implemented pixel consists of CMOS logic gates from the standard cell library (3-state buffers, an inverter, and a D-latch with active-low reset), a MOS capacitor (MOSCAP), a high-threshold PMOS transistor, and sensor metal plates. The MOSCAP (MN1) in each pixel is used to store charge and reduce the effect of parasitic capacitances and process mismatch capacitance variations at n1, reducing the pixel-to-pixel variation on the calculated resistance. In our implementation, we used an NMOS MOSCAP. During the operation of the pixel, node n1 varies between VDD when fully charged and VDD/2 just

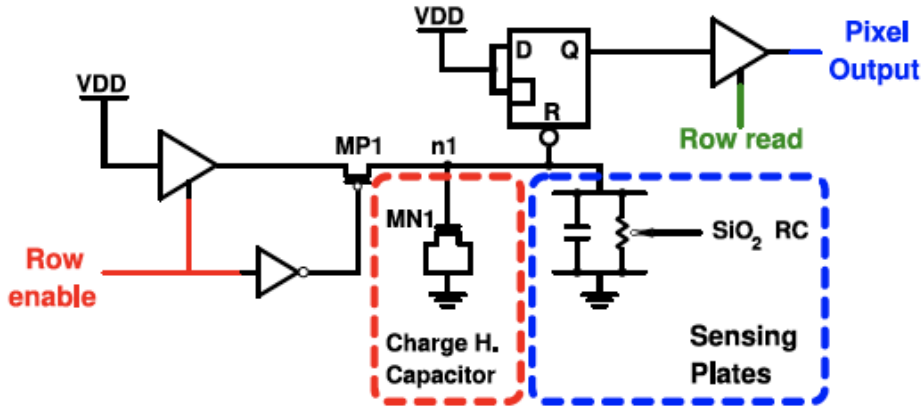


Figure 3.4: Schematic of the measurement pixel. The charge-holding MOS capacitor and the sensing plates for measuring the oxide degradation are marked.

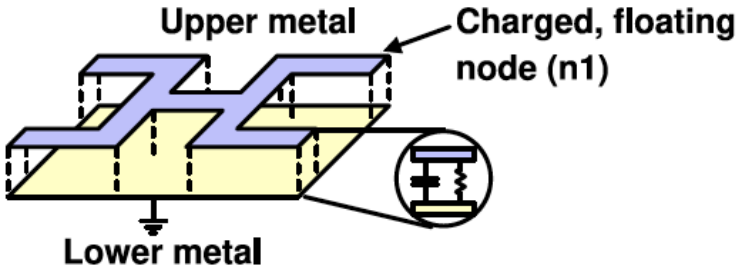


Figure 3.5: Capacitor structure for sensing the changes in the SiO_2 between the metal plates.

before the pixel output switches down. As MN1 is always in strong inversion during operation, and the source, drain, and bulk of MN1 are all tied together to the ground node, the change in the effective gate-bulk capacitance of MN1 is minimal. In our simulations, for a very slowly changing (over 1 s) gate-bulk voltage from VDD to VDD/2 the instantaneous gate-bulk capacitance of MN1 varied between 17.26 fF and 17.54 fF and had an average capacitance value of 17.5 fF.

The high-threshold PMOS transistor (MP1) is used to further reduce the current leakage path through the 3-state buffer. By the insertion of MP1, measurement node current leakage is reduced from 7.93 pA to 3.42 fA, effectively increasing the maximum measurable resistance from 227GΩ to 526 TΩ. When transistor MP1 is turned off, this will result in charge injection, effectively charging node **n1** to a value slightly greater than VDD. However, this injected charge amount does not change from cycle to cycle, i.e., from reading to reading for a pixel, and is a fixed amount. Thus, this will result in a fixed increase in the pulse width generated by the pixel. As the targeted measurement

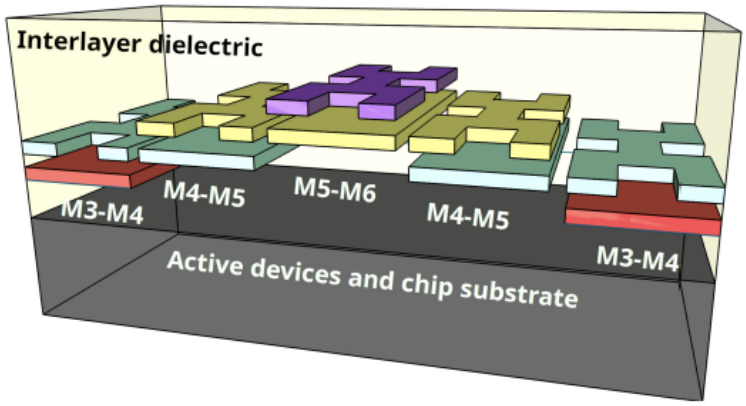


Figure 3.6: Schematic giving the placement of 6 pixels implemented using different metal stacks.

methodology is based on comparing every reading of a pixel to a reference golden reading, i.e., when the surface of the chip is dry and there is no ingress, the results of both the dry and wet readings will be shifted by the same amount as the capacitance at **n1** doesn't change. Therefore, the effect of charge injection at **n1** is inconsequential and does not affect the expected results from the measurements.

Finally, sensing metal plates to sense the change in the ILD oxide over the pixel, as explained in the previous section, are placed over the active circuitry during the implementation. Depending on the metal layers used, ILD capacitance between the sensing plates varies between 6 and 7 fF and the implementation details of the sensor plates are presented next.

SENSING PLATES IMPLEMENTATION

Based on our sensor area optimization analysis presented earlier, I opted for a sensor structure as shown in Fig.3.5 to evenly distribute the possible ingress paths over the sensor within the constraints of the layout rules. In each pixel, two successive metal layers are used as the sensing plates to monitor the changes in the properties of the oxide over the pixel (Fig.3.5). The top plate of the sensing structure is connected to node n1 (the measurement node) and the bottom plate is connected to the ground. In the implementation presented in this work, there are three different versions of the sensor pixel shown previously in Fig.3.4, with the same active circuitry and with different metal layer pairs, namely M6-M5, M5-M4, and M4-M3.

In the layout of the sensor array, the active circuitry for each sensor cell is the same, and cells with different sensor capacitors are placed alternatingly in each direction, i.e., x and y. For example, an M6-M5 cell is followed by an M5-M4 cell, which is followed by an M4-M3 cell. Such a placement is presented in Fig.3.6. In the extracted layout, it was seen that the total capacitance at n1 varies between 23.5 and 24.5 fF, depending on the used metal layer pair. With such an implementation, different metal combinations give us the ability to track the changes at different depths of the ILD over the chip surface area.

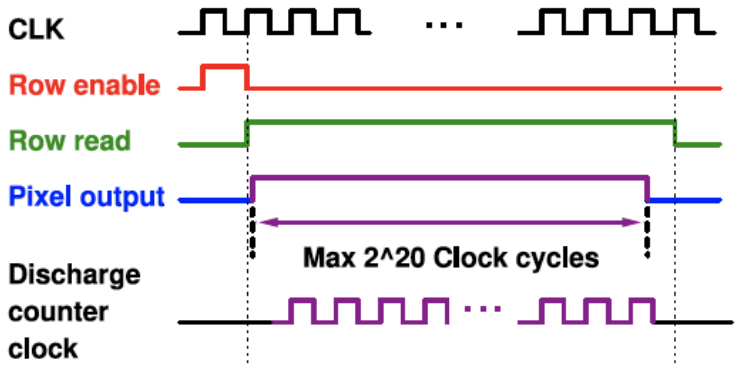


Figure 3.7: Timing and operation of the measurement pixel.

OPERATION AND THE CONTROL OF SENSOR PIXEL

The timing diagram of the pixel is shown in Fig.3.7. Row enable and Row read signals are controlled and supplied by digital pixel control circuitry. The operation of the pixel is as follows: When the ILD resistance of a pixel is to be measured, the Row enable signal for the chosen pixel row is raised for one clock cycle. During this cycle, the input 3-state buffer and the high-threshold PMOS transistor MP1 are turned on, charging node n1 to VDD through the 3-state buffer. The node charge is stored on the MOSCAP, the SiO_2 capacitance of the sensing plates, and the parasitic capacitances at n1. The MOSCAP is the main charge-holding element due to its capacitance, i.e., 17.5 fF. As soon as node n1 is charged, the reset of the latch is released, and the output of the latch is automatically set to VDD, as both the D input and enable signals of the latch are connected to VDD. In the next clock cycle, two things happen in parallel: i) Row enable is lowered, effectively stopping the charging process by turning off both MP1 and the input 3-state buffer, thus, leaving node n1 floating, and ii) Row read is raised to read the pixel output at the column output. It should be noted that the output 3-state buffer is used for an array implementation as explained next. If the sensor pixel is to be used in a standalone fashion, e.g., as one of the integrity monitor sensors spread over the chip area, it can be safely removed from the pixel to reduce the area and power consumption.

In the test chip to be presented, an array of sensor pixels and a digital measurement engine for controlling the pixels and quantizing the time measurement were implemented. During the operation, the pixel to be measured is selected through the use of Row enable and Row read signals by the measurement engine. As soon as the pixel output is enabled with the Row read signal and raised (the Q output of the latch is already at VDD), the 20-bit counter in the measurement engine becomes enabled and starts counting with CLK. The count stops when either node n1 is discharged below the reset threshold (VDD/2) of the resetting latch (Q goes low), or a count of $2^{20}-1$ is reached. Thus, by counting the clock cycles the quantization of the time pulse generated at the output of the pixel is realized.

ILD RESISTANCE MEASUREMENT PROCESS

The measurement process of the ILD oxide change uses the self-reset feature of the latch in Fig.3.4 and is as follows. When node n1 is left floating after Row enable goes low, the possible discharge paths are through the oxide resistance of the ILD and the current leakage paths of the active elements are denoted by the shunt resistance connected to this node in the model. The active element current leakage paths are the leakage path through MP1 and the output of the 3-state buffer, the gate leakage through the latch, and the gate leakage of MN1. It is first assumed, and later proven through measurements, that, in the presence of water or ions in the ILD layer, the dominant discharge path for n1 will be through the ILD oxide. Therefore, we use the variation in the discharge time of node n1 to track the changes in the resistance (dominant) and capacitance (less pronounced) of the SiO_2 layer between any two metal layers that act as our sensing plates (Fig.3.5). Finally, we deduce the time it takes n1 to discharge to VDD/2 by monitoring the output of the pixel (Q) convert the pulse width at Q to a time count, and calculate the measured resistance using this time count.

In the absence of water molecules and ions in the ILD SiO_2 layer between two successive metals, the resistance of the ILD will be very high (in the order of peta-ohms, 10^15 ohms) and in a dry state, the dominating resistance at node n1 will be mainly from the active element leakage currents. However, as the chip integrity is breached and water molecules and ions penetrate the ILD layers, there will be multiple changes but mainly: I) the conductance of the ILD SiO_2 that has been breached will increase (i.e., the resistance will reduce), and ii) due to the presence of water molecules and ions, the dielectric constant of the SiO_2 will increase, hence increasing the capacitance of the layer. In such a case, if a lower discharge time count is monitored, we can conclude that the reduction in the resistance is higher than the increase in the capacitance. Moreover, during the measurement process, we expect the discharge time of n1 to be reduced proportionally to the reduced resistance, which in turn is inversely proportional to the amount of ions and molecules in the ILD.

NOISE PERFORMANCE

One other metric that affects the quality of the resistance measurement of the ILD is the inherent noise that is coming from the active circuitry. As the measurement is done in time-mode, i.e., the width of a pulse is measured, jitter of the generated pulse should be used as the noise metric. Therefore, the signal-to-noise (SNR) ratio of the measurement pixel can be defined as:

$$\text{SNR} = \frac{T_{discharge}}{\sigma_{jitter}} \tag{3.10}$$

where σ_{jitter} is the jitter that is caused by the noise sources in the measurement pixel.

RMS noise voltage σ_n can be transferred from the voltage domain to jitter (σ_{jitter}) by using eq.(3.11). In this equation, change in time is slow and is dominated by $T_{discharge}$, therefore ∂t can be taken to be equal to $T_{discharge}$. Furthermore, assuming the discharge operation ends at VDD/2, we can take ∂V to be equal to VDD/2 and rewrite eq.(3.11) as eq.(3.12).

$$\sigma_{jitter} = \sigma_n \cdot \frac{\partial t}{\partial V} \tag{3.11}$$

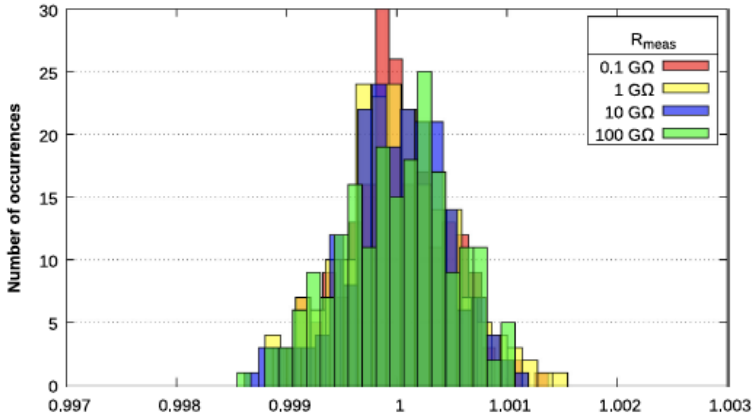


Figure 3.8: $T_{discharge}$ variation due to the noise in the system.

$$\sigma_{jitter} = \frac{2\sigma_n}{VDD} \cdot T_{discharge} \tag{3.12}$$

$$\sigma_{jitter} = \frac{2}{VDD} \cdot \sqrt{\frac{k \cdot T}{C}} \cdot T_{discharge} \tag{3.13}$$

The pixel operation can be thought of being akin to a sampled system and an integrator. As the discharge happens through a passive element and off transistors (through gate leakage), the RMS noise voltage in eq.(3.12) and eq.(3.12) can be defined as the thermal noise on the total capacitance connected to the measurement node, i.e., $\sqrt{\frac{k \cdot T}{C}}$. By replacing the σ_n in eq.(3.12) with the thermal noise, we reach the final equation for the σ_{jitter} of the measurement pixel in eq.(3.13). By combining eq.(3.10) and eq.(3.13), the SNR of the pixel is given by:

$$\text{SNR} = \frac{VDD \cdot \sqrt{C}}{2 \cdot \sqrt{kT}} \tag{3.14}$$

In eq.(3.14), it should be noted that the SNR of the measurement pixel does not depend on the discharge time and is solely set by the discharge threshold (VDD/2 in this case) and the total capacitance connected to the measurement node. For a capacitance value of 24 fF to ground, the SNR of the pixel at room temperature is calculated to be 2167, which translates to an SNR of 66.72 in dB.

To verify our calculations, transient noise simulations were run on the extracted pixel netlist using HSPICE. As the transient noise simulations require extensive computing resources for long simulations, the value of R_{shunt} was reduced artificially by adding a much lower valued resistor in parallel, effectively reducing the equivalent measured resistance R_{meas}, and hence the discharge time as given in eq.(3.2). 200-point transient noise simulations were run for R_{eq} values of 0.1, 1, 10, and 100 GΩ and the results are

given in Fig.3.8. The figure shows the normalized transient noise simulation results. The discharge time values for each forced R_{meas} are normalized to their respective means and are plotted together to show that the variation due to the noise does not depend on the effective resistance measured. In the simulations, the SNR of the pixel varied between 65.88 dB and 67.06 dB for different R_{meas} values, confirming our derivations

3.1.4. CHIP IMPLEMENTATION AND TEST SETUP

SYSTEM IMPLEMENTATION

To verify the proposed ILD resistance measurement method, an array of sensor pixels is implemented as shown in Fig.3.10. The array consists of 234 rows and 23 columns. To control the pixels during the measurement and to measure each pixel's value, a fully-digital measurement engine that can automatically scan all the cells for integrity and degradation within the SiO_2 ILD is implemented. In the array, Row enable enables a row of pixels for sensing, and Row read enables the output of the chosen row's pixels. All columns from the array are fed to the measurement engine (Pixel outputs) and the column to be measured is selected inside the measurement engine, and the pulse at the chosen pixel is quantized.

To ease the handling of the device during tests in wet environments, we minimized the number of bonding pads to 6 in total by using a serial-in, serial-out architecture. The clock (CLK) and reset (RST) signals together with the data-input port (dataIn) are used for controlling the on-chip measurement engine externally, and the output is sent off-chip through dataOut.As will be shown later, it is possible to change both the accuracy and the maximum resistance measurement capability of the system by changing the clock frequency, hence adapting the system for different measurement conditions.

A prototype system containing the sensor array and the measurement engine core is implemented in a 0.18 μm standard CMOS process. Fig.3.9(a) shows the implemented chip together with the polydimethylsiloxane (PDMS) covering the pads and wire bonds. For proof of concept, in this paper, all the dry and wet measurements are done with bare dies where the top passivation is the only insulating layer. For this aim, PDMS is only applied over the pads and wire bonds leaving the sensor array fully exposed. The total chip area including the bonding pads is 1.1 mm × 1.1 mm. The sensor array consists of 5382 sensor pixels, with varying metal sensor plate structures, as explained previously. The size of each pixel is 3.92 μm by 29.68 μm.

3.1.5. TEST SETUP

The custom test setup consists of a PCB, a power supply, and an FPGA board (Ultra96) to control the on-chip measurement engine, and to save and process the data from the chip in real-time (Fig.3.9(b)). The custom-designed PCB and the measurement and processing code running on the FPGA accommodate measuring three packaged chips at the same time. A setup for both dry and wet measurements is shown in Fig.3.9(b). To facilitate wet measurements, a tube was placed and glued to the lid opening of the chip package to hold the test liquid. The tube joints were further supported by the PDMS to minimize the risk of liquid leakage to the electronic measurement setup.

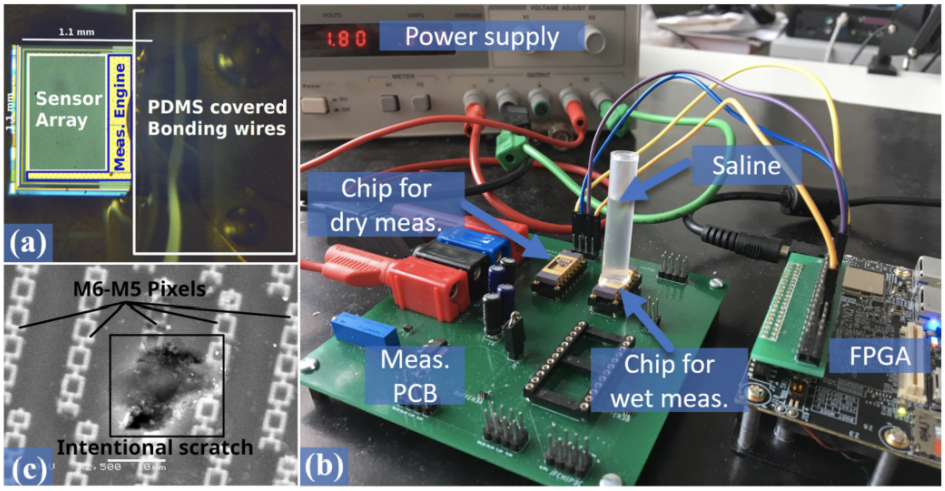


Figure 3.9: (a) Chip photo showing the sensor array, measurement engine, and polydimethylsiloxane (PDMS) covered bonding wires. (b) Measurement set-up showing the custom-designed PCB used for both dry and wet measurements. (c) SEM image illustrating the intentionally scratched passivation surface of the chip. Pixels with M6-M5 sensor plates are marked.

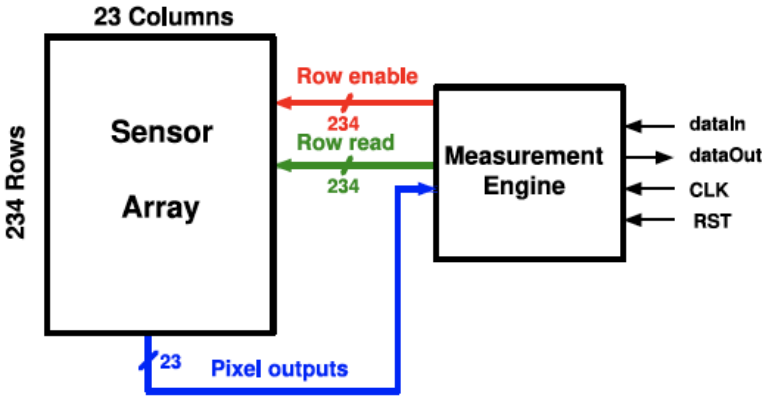


Figure 3.10: Implemented sensor array with on-chip measurement engine showing top-level signals.

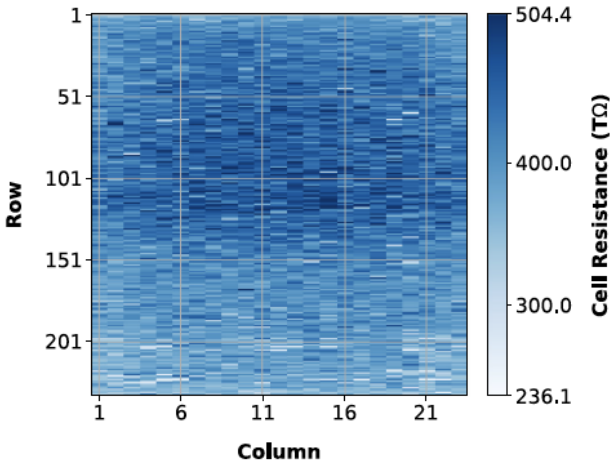


Figure 3.11: Dry measurement results for the whole sensor array performed at room temperature. Calculated resistance varies between 0.236 PΩ and 0.504 PΩ due to intra-die process variation and the environment temperature changes during the measurements. Note that the image presents all the pixel measurement results (M6-M5, M5-M4, and M4-M3) covering the x,y, and z(depth within the die) of the entire pixel array.

3.1.6. MEASUREMENT RESULTS

All the measurements presented in this section were done while the chip was supplied by a 1.8 V voltage source and the average current consumption during the measurements was 4.78 mA, which also includes the consumption of the ESD protection circuitry. The measurement engine consumes 2.72 mA while being operated with a 75MHz clock and per-pixel current consumption during the pixel measurement is 18.34 μA.

DRY MEASUREMENTS

The first measurements are done in dry conditions to verify the correct operation of the system and determine the measurement capabilities. For each chip, the dry measurement results also serve as the golden reference for comparing to the wet measurements and for calculating the possible amount of ingress. The external clock for the measurement engine is generated and supplied by the FPGA board and is adjustable from 75 MHz down to 125 kHz.

The tuning of the clock frequency allows for the measurement of the discharge time with varying accuracy and maximum resistance limits. For example, for a clock frequency of 50 MHz, the minimum discharge time-step that can be measured is 20 ns. Using (3), and an average value of 24 fF for Ceq, it can be calculated that the minimum measurable resistance change for a 50 MHz clock is 1.2 MΩ. Any changes greater than 1.2MΩ will be captured by the system as a change in the discharge counter, with a maximum measurable value of 1.26 TΩ. To increase the measurement range, the external clock can be reduced to a lower frequency, e.g., 125 KHz, where the maximum measurable resistance becomes 0.504 peta-ohm [$0.504 \cdot 10^{15}$ Ω].

The upper limit of applicable clock frequency is due to the critical path of the on-

chip measurement engine and any input clock frequency higher than 75 MHz will result in functional errors. The lower limit of the clock frequency is set by the maximum measurable resistance due to the active element leakage currents, i.e., due to R_{shunt}. Any clock frequency lower than 125 kHz will not improve the maximum measurable resistance and will only increase measurement time. To measure all the pixels with a 125 kHz clock, approximately 12.5 hours are needed. Results of such a measurement, which also serve as a reference for the wet measurements for this particular chip, are presented in Fig.3.11, showing the measurement capabilities of the implemented platform. The implementation details and the capabilities of the system are summarized in Table 3.1 above.

Operating voltage	1.8 V
Total current consumption (including ESD)	4.78 mA
Total chip area	1.21 mm^2
Pixel area	116.35 μm^2
Number of pixels	5382
Sensor array area	0.643mm^2
Max. measurable ILD resistance	0.504 PΩ
Min. detectable ILD resistance change	0.8 MΩ
Per pixel current consumption	18.34 μA
Measurement engine (ME) area	0.14 mm^2
ME max. operation frequency	75 MHz
ME current consumption @75 MHz	2.72 mA

Table 3.1: Specifications and performance summary

WET MEASUREMENTS

In the next verification step, we performed wet measurements to verify the ILD resistance change concept and the capabilities of the implemented platform in tracking water/ion ingress through the ILD stacks. Earlier wet experiments, after two weeks of continuous soaking of the test chips in saline showed no changes in the array resistances when compared to dry measurements. This suggests the good insulating properties of the chip passivation provided by the foundry. Therefore, to test the ingress monitoring functionality of the proposed circuit in a controlled environment, modifications were made to the chip passivation surface.

In the first test sample, we intentionally introduced three scratches on the chip passivation layer using an ultrasonic cutter. This allowed faster propagation of water/ions into the chip ILD layer. A SEM image of one such scratch is shown in Fig.3.9(c). After scratching the surface of the chip, measurements under different conditions, i.e., dry and wet, were made using a 50MHz measurement clock. This clock value was chosen to increase the accuracy of the measurements as explained previously. Fig.3.12 shows the results of these measurements. In the first step, a dry measurement of the chip was done to serve as the reference (Dry@ 0min). The scratched areas on the chip are seen as lighter

colour pixels compared to the rest of the array in the figure. The lighter colours in the dry measurement (Dry@ 0-min) indicate a faster discharge time and could either be due to an introduced damage in the sensor metals upon scratching the passivation surface or due to foreign particles that got stuck in the ILD, reducing the measured resistance.

In the second step, we tested the chip in a phosphate-buffered saline (PBS) solution with a pH of 7.4 at room temperature. The solution was continuously kept on the sensor array using the tube (Fig.3.9(b)). Results of the measurement after soaking the chip in the solution for 90 minutes (Wet@ 90-min), and the difference between the dry reference and wet measurements are shown in the middle and right panes of the top row of Fig.3.12, respectively. When the test sample was soaked, ingress occurred reducing the measured ILD resistance of the pixel. At 120 minutes after soaking the chip, another measurement was taken to verify both the effects of continuous exposure to the liquids and the resulting change in the oxide properties. The results for this measurement are shown in the second row of Fig.3.12. From the difference plot in this row, it is seen that ingress continues through the pixels and is reflected by further reduction of the cell ILD resistance.

Finally, another experiment was performed to verify the ILD resistance changes when the liquid is removed. The liquid was removed from the tube, and after waiting for 60 minutes (180 minutes after the beginning of the measurements), another set of measurements were taken. The results are shown in the middle pane of the bottom row of Fig.3.12 (Dry @180-min). During this final set of measurements, it was observed that as the liquid was removed from the chip surface, the ingress stopped, and actually, reversed, reflected by the higher resistance values, i.e., darker pixels in the figure, when compared to the Wet @ 120-min measurement. The results presented in Fig.3.12 show the monitoring capabilities of the chip in detecting changes in the ILD resistance as water/ions propagate in the chip structure over time, both through the damaged and undamaged neighboring cells.

Further measurements (Fig.3.13) were performed on another test chip to verify the real–time measurement capabilities. In this second test chip, the top passivation layers of a single pixel were removed using a focused ion beam (FIB) as shown in Fig.3.14. A different measurement protocol was followed for these measurements. An array of 3×3 pixels, where the FIB'ed pixel is in the center, was measured continuously while the chip was soaked in a PBS solution. The measurement plots are shown in Fig.3.13. In the figure, only the FIB'ed pixel is affected by the ingress due to the removed passivation layers. The measurement steps taken were as follows. i) Put the PBS solution on the chip at t = 0, ii) at t = 127 minutes remove the PBS solution from the tube and continue the measurements. Just after putting the PBS solution on the chip at t = 0, the measured sensor resistance decreased rapidly due to ingress, saturating around t = 127 minutes at a resistance value of 3 G. After the removal of the PBS, at t = 127 minutes, the resistance began to increase slowly due to the lack of liquid, hence the stopped ingress and slow evaporation, on the chip surface and the ILD. Then, after t = 364 minutes, the rate of increase of resistance increased due to the evaporation of the water molecules from the ILD. After t = 480 minutes the rate of evaporation decreases, finally saturating the resistance of the pixel in the >300 TΩ range. It should be noted that, during the measurements, the first cell to be read from is the top-left cell, therefore the beginning process of ingress, which

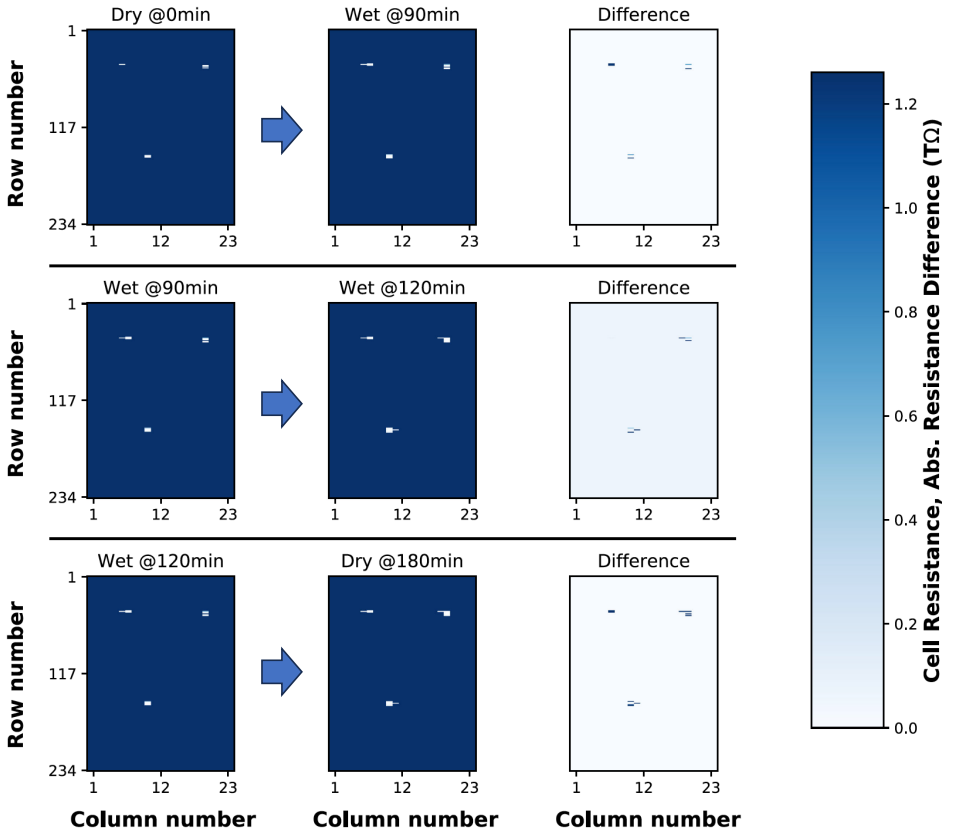


Figure 3.12: Dry (0min), wet (from 0min to 120min), and re-dried (from 120min to 180min) measurement results for a chip with scratched passivation showing how water/ion ingress through the scratched area can change the resistance in neighboring pixels.

is very fast in the beginning, is not captured. This is reflected in our measurement as the first measurement value from the fibbed pixel is around 10 TΩ.

3.1.7. DISCUSSION

With the goal of higher miniaturization, great efforts have been put into realizing free-floating single-chip implants. For such devices, the first step to miniaturization has been to replace the bulky battery power source with wireless energy transfer techniques, e.g. electromagnetic and ultrasound. The second step has been to incorporate most of the discrete components, capacitors, and coils, inside the chip. The works reported in [25, 26] are examples of such single-chip implants. For such systems, the chip integrity will determine the overall lifetime of the device. Therefore, we developed this platform with two main goals in mind: i) to be used as an investigational tool for evaluating the insulating properties of the added packaging layers, and ii) as an integrity monitor for free-

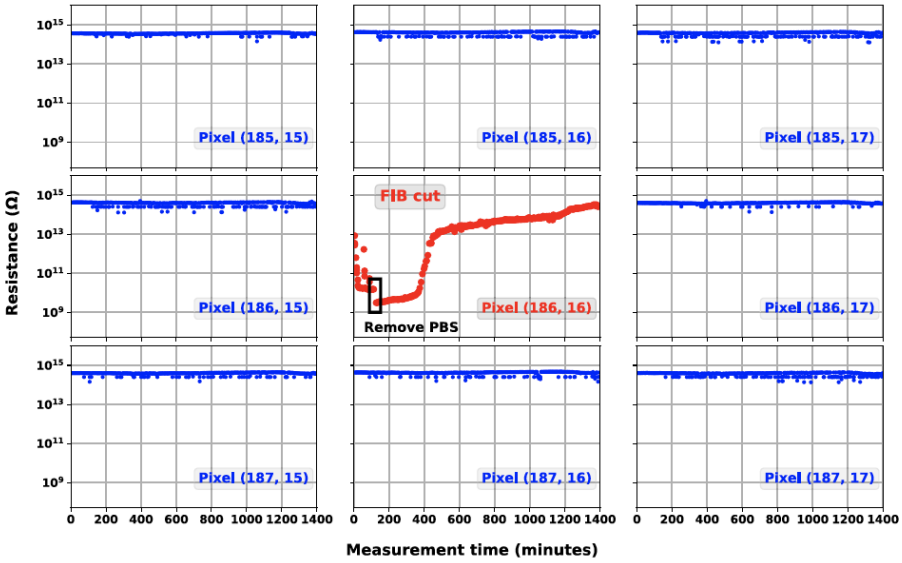


Figure 3.13: Measurement results for a second chip with an opening created in the IC passivation using focused ion beam (FIB). Results show a scanned array of 3 × 3 with the FIB cut sensor pixel in the center. The array was scanned pixel-by-pixel continuously and both the ingress and evaporation after the removal of the PBS were observed. Note that the first measurement (0 min) was done when saline was just placed on the sensor array.

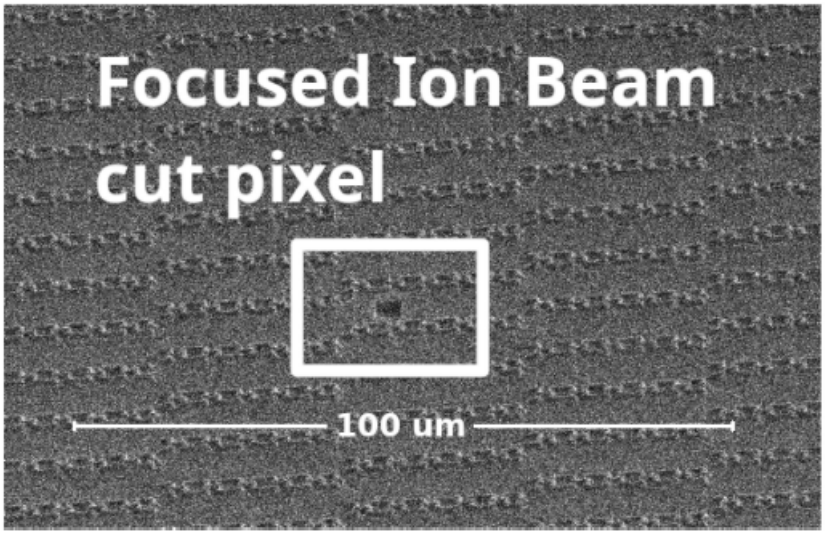


Figure 3.14: Close–up scanning electron microscope (SEM) image of the sensor pixel with a cut-out top passivation layer. The cut was made in the region between two M6-M5 pixels.

floating single-chip implants.

EVALUATION AND SELECTION OF MATERIALS

1) Thin Conformal Coating Materials: One critical challenge in realizing single-chip implants is the right selection of coating materials that can guarantee the correct functionality of the device during and after its implantation. As previously explained, various biocompatible conformal coatings have been reported with the potential of being the suitable packaging solution for mm-sized implants. Nevertheless, the insulating properties of these layers are greatly affected by various factors, such as: adhesion of the coating to the substrate material, thermal expansion coefficient mismatch between the coating and the substrate and the coating deposition process. As an example, the protection offered by polymeric coatings, such as PDMS or parylene greatly relies on its good adhesion to the substrate material [27, 28], as any adhesion failure would result in water condensation on the chip due to the no-hermetic nature of polymers. Factors such as adhesion failure or moisture/ions ingress through the micro/nano cracks of the coating could only be evaluated during accelerated lifetime testing [29]. During these tests, employing the platform presented in this work would allow for an early evaluation of the coating on representative CMOS materials, thus increasing the certainty in the lifetime prediction of the active implant.

2) CMOS Foundry Materials: Once the top coating has been breached, the CMOS passivation and ILD layers will act as barriers for protecting the metals and active components underneath. CMOS passivation layers are meant to block moisture and ions ingress, typically present in ambient environments, until their final packaging is done. The passivation and ILD layers are generally deposited using a plasma-enhanced chemical vapor deposition (PECVD) process, making their mechanical and chemical properties considerably dependent on the deposition parameters [30, 23]. Various studies have been investigating the underwater barrier properties of PECVD SiO_2 and SiN_X layers [31, 32], all confirming the properties of such inorganic layers to be greatly dependent on their deposition parameters. Accordingly, the properties of the materials deposited by the CMOS foundries would also vary from the ones investigated elsewhere and should, therefore, be evaluated separately. Using the presented platform in bare silicon die (similar to the wet measurements given in the previous section) would allow for an evaluation of the barrier properties of the materials deposited by the CMOS foundries.

Another application of the sensor array could be to derive the time points for which moisture will propagate through the top passivation into the lower subsequent stacks of the ILD. Such information can potentially help in better understanding the failure mechanism of chips in ionic media and, therefore, help derive a better estimate of their lifetimes.

In general, we would like to emphasize that the appropriate selection of materials, both for the conformal coating and the CMOS passivation/ILD, will greatly affect the overall lifetime of single-chip implants.

WIRELESS MONITORING FOR CHRONIC STUDIES

The platform reported in this work was originally meant to be used as an investigational tool for the sensitive evaluation of the coating and characterizing the ingress of water

molecules and ions on the chip. Therefore, a sensor array was realized which occupied the majority of the chip surface. Furthermore, due to the required number of internal control signals to control the array, measurement engine internal column, and row selection logic, and required high precision and resolution measurements, the measurement engine both occupies a substantial area and is power hungry. Nevertheless, the measurement concept can still be used by spreading the sensing cells on critical or sensitive areas of the chip. This way, the power consumption of the sensing platform could be radically reduced, as a single pixel is very power efficient, i.e., 0.97 nW and 33.01 μW are consumed for 0.6 V and 1.8 V operation, respectively. By coupling the presented pixel and time-mode measurement approach with an energy-efficient communication protocol such as single pulse harmonic modulation [33] as done in [34], it is both possible and feasible to create a monitoring unit for single-chip wirelessly powered or energy harvesting implants. In such a case, the distributed integrity sensing cells could be used to monitor the hermeticity of the chip in vivo. One can even imagine a scenario in which the sensor would communicate to the patient that a replacement of his implant is needed in the next six months, or in extreme cases, as a fuse, where the implant would stop its electrical functionality before any hazardous malfunction.

In the presented system, a fast clock is required for a more accurate conversion of the generated pulse width to a digital value for a limited maximum measurable ILD resistance, e.g., 0.84 TΩ for a 75 MHz clock. As can be seen in Fig. 3.12, whenever there is an ingress event, the measured ILD resistance changes over a range of 6 orders of magnitude, from peta-Ohms to giga-Ohms. In a wireless implant scenario where the presented sensors are used for ingress detection, we are interested in the first detectable ingress event. Therefore, it is enough to sense a change occurring in the peta-ohms range, and when the proposed measurement method is implemented in an implant, a slow clock in the low 100 kHz range should suffice. Furthermore, this generated clock is used for operating a counter. As the counter in the present implementation is 20-bits long, it effectively averages the jitter coming from the clock source by a factor of 220, i.e., the jitter noise power in the pulse width measurement is reduced by 60 dB. Hence, we believe that the requirements for on-implant clock generation for the presented system are very relaxed and will not cause any problems in future implantable applications.

3.1.8. CONCLUSION

In this paper, a fully integrated, standard-CMOS, chip integrity monitor array for investigative purposes has been presented. The sensor array chip has been implemented in a 0.18 μm standard CMOS process and utilizes novel charge/discharge-based, time-mode pixels that monitor the changes in the sensing element's oxide through ultra-high resistance measurements. In addition to the sensor array, a digital measurement engine that continuously monitors the sensor readings is also implemented. The system measures the ILD resistance values up to 0.504 peta-Ohm, with controllable measurement steps that can be as low as 0.8 MΩ.

3.2. TOWARDS CMOS BULK SENSING FOR *In-Situ* EVALUATION OF ALD COATINGS FOR MILLIMETER SIZED IMPLANTS

3.2.1. INTRODUCTION

The main aim of bioelectronic medicine is to one day replace conventional chemical drugs with millimeter-sized implants. This way, tiny electrical pulses will be locally delivered to a small group of neurons to influence and modify biological functions. Developing such implants, however, has brought many new challenges both in the technological and biological domains. One such technical challenge is the packaging of such tiny devices [35]. Conventional active medical implants such as pacemakers have relied on a titanium (Ti) case for packaging the implantable electronics. In recent years, driven by the increased functionality offered by CMOS technologies and the need for further miniaturization, tremendous efforts have been made in designing miniaturized implants and integrating the majority of the components on a single chip [36, 37]. Such a single-chip approach, however, would require novel packaging solutions since the Ti case would consume significantly more weight and volume compared to the chip and greatly limit the flexibility of the final implant [38].

Atomic layer deposition (ALD) is a chemical vapor deposition process that can create thin (ten to a few hundred nanometers) and conformal coating layers with near-hermetic barrier properties [16, 39]. Previous studies have also reported on the biocompatibility and biostability of these layers, making them an attractive packaging solution for mm-sized implants [26]. Such layers, however, could contain micro flaws and defects [40] that could reduce their coating performance and lead to device failure. In conventional Ti packages, the helium leak test is a common method for hermeticity evaluation [41]. This test method, however, is not suitable for mm-sized devices given the lack of cavities within such tiny implants. In the absence of permeable polymers, previously reported humidity sensors are also not applicable [42].

For evaluating the encapsulation performance of ALD coating layers, DC current leakage and impedance measurements have been reported as sensitive methods for detecting defects in the layer [43, 44]. So far, these measurements have been performed on ALD-coated 2D planar structures and/or on unrepresentative material substrates which will differ from the final device. The barrier properties of thin coatings, however, are greatly affected by the surface characteristics of the substrate, such as contamination, roughness, and aspect ratio [45]. As a result, once the coating has been evaluated and optimized on 2D structures, there is still uncertainty regarding the hermeticity when applied on more complex 3D structures such as an implantable chip. Hence, an evaluation test is still needed for the final device to justify its implantation.

Here, for the first time, I explore the possibility of using the bulk of the implantable chip as a platform for evaluating the barrier properties of its protective coating. The evaluation method is based on measuring the DC leakage or impedance between the bulk and an exposed platinum (Pt) electrode. This simple approach takes advantage of the conductivity of the bulk and would allow a 3D in-situ evaluation of the coating, thus increasing confidence in its hermeticity prior to implantation. Fig.3.15 schematically illustrates the concept where a bare CMOS chip is coated with a thin ALD layer. The majority volume in such a single-chip implant is occupied by the conductive CMOS bulk, while

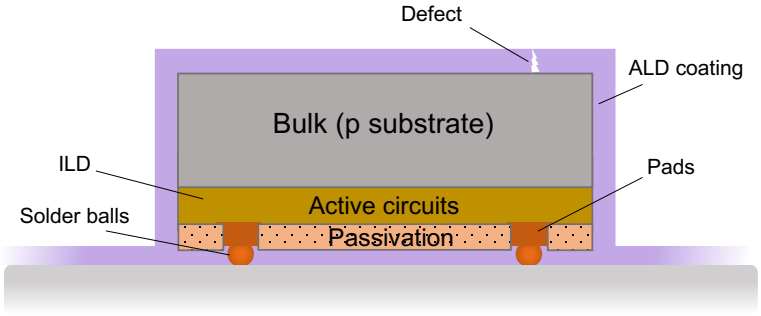


Figure 3.15: Schematic illustration of a CMOS die connected using solder balls and encapsulated with an ALD coating layer (dimensions not to scale).

the metals and active circuits in the chip are protected by the interlayer dielectrics (ILD) and passivation layer. We, therefore, have selected the bulk to be the sensing platform. The advantage of this approach is its simplicity and obviating the need for the design and fabrication of a dedicated sensing platform within the implant.

3.2.2. EXPERIMENTAL DETAILS

1. Sample

   (a) CMOS chip

   The bulk within standard CMOS processes is typically made of lightly doped silicon [46]. This makes the substrate a low-ohmic layer which will be used in this work as a measurement platform. As a proof of concept, chips were fabricated in a standard 6-metal 0.18 μm CMOS process. For connection to the bulk, a p+ diffusion area of 10 μm $\times$ 10 μm was used. This creates a low-ohmic contact with the bulk. The chips were glued on a ceramic (alumina) plate and wire bonded to a metal connection on the plate. For mechanical protection of the wire-bonds and electrical insulation of the metals on the alumina ceramic, polydimethylsiloxane (PDMS) was used. This would enable us to only measure through the bulk and exclude the metal interconnects. PDMS was applied carefully with a dispenser to intentionally leave part of the bulk (bottom and sidewalls) exposed (Fig.3.16).

   (b) ALD coating

   Two samples out of four were coated with an alternating ALD multilayer. The samples were first cleaned with isopropyl alcohol and then dried. The thermal ALD process was made using the Picosun R-200 Advanced ALD reactor under reduced pressure (N2 atmosphere) of about 1 mbar. The ALD is layer-by-layer deposited with N_2-purge in between to separate the different precursors. The deposition started with the growth of the first ALD material with the needed amount of precursor cycles to reach the required thickness. The same procedure was followed for the second ALD material. The deposition of the first and second material was repeated 10 times, resulting in a 100

nm ALD multilayer. More information regarding the ALD multilayer can be found in [47]. Fig.3.17 gives a schematic illustration of the ALD-coated chips used for this study.

2. Experimental Set-up

   All samples (2 non-coated and 2 ALD-coated) were placed in soak within 50 ml vials filled with 1X phosphate-buffered saline (PBS) with a composition of 0.0027 M KCl and 0.0137 M NaCl having a pH of 7.4. All experiments were done at room temperature (23 °C). In this work, to evaluate the barrier properties of the ALD coating, DC current leakage and electrochemical impedance spectroscopy (EIS) was used. Both measurements were carried out using the Solartron Modulab where for EIS, the potentiostat in combination with a frequency response analyzer (FRA) was used. In addition, for measuring sub-picoamp current levels, a femtoammeter was connected in series with the module while placing all samples inside a dedicated Faraday cage (more information regarding the measurement module can be found in [43]). All measurements were performed using a two-cell electrode configuration between the CMOS bulk, being the working electrode (WE), and a 2 mm Pt wire, being the counter electrode (CE). Fig.3.18 gives a schematic illustration of the soak set-up. DC leakage measurements were carried out by applying a 0.6 V signal between the WE and CE, keeping the WE at ground potential. For EIS, a 10 mV RMS sinusoidal signal in the frequency range of 10 mHz to 100 kHz was used. A low amplitude signal has been chosen to minimize the effects from the measurement signal on the samples. During EIS measurements, the open circuit potential (OCP) between the WE and CE was set to -0.4 V (with the bulk being negative to the Pt). This OCP was measured between the bulk of a non-coated sample and the Pt wire. The OCP for ALD-coated samples, however, could not be measured due to the presence of the ALD insulation. Therefore, this potential was used for all EIS measurements.

3.2.3. RESULTS

Fig.3.19 shows the DC measurement results for two ALD-coated samples. For comparison, results for one of the non-coated samples is also given in which the current is measured between the bulk and the Pt wire. Results show that for both of the coated samples, the leakage currents were <1 pA, while for the non-coated samples, the current is four orders of magnitude larger. These results are in agreement with previously evaluated ALD multilayers, confirming their high barrier properties [48]. Impedance measurements were used to characterize and compare the non-coated and coated samples.

Fig.3.20 shows the impedance data given as Bode magnitude (|Z|) and phase angle plots over the measured frequency range. For the non-coated sample, a clear constant phase element (CPE) behavior is seen in the middle frequencies (1- 100 Hz). The higher frequencies represent the spreading resistance together with the parasitic capacitance present between the connecting WE and CE cables. However, the resistance is more dominant which results in a phase angle around -40 °C. For the two ALD-coated samples, a more capacitive behavior is dominant across the entire measured spectrum. This is the

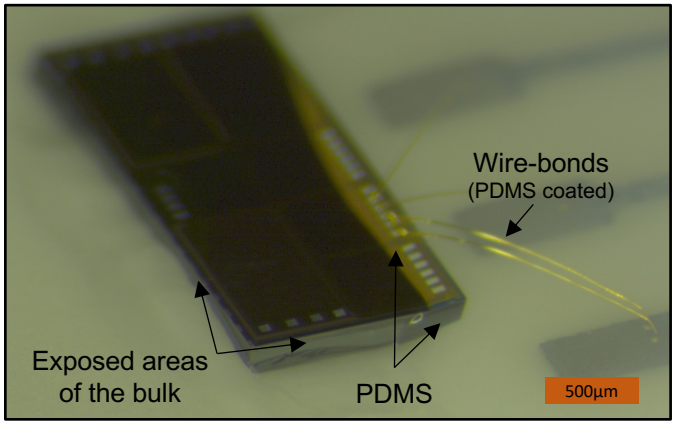


Figure 3.16: A microscopic image of a chip sample after wire-bonding and PDMS coating. The proposed bulk sensing method is designed for flip-chip solder ball-connected ICs, where a larger surface area of the IC bulk is available for sensing. However, due to the unavailability of tools required for connecting solder balls, wire bonding was used as an alternative connection method.

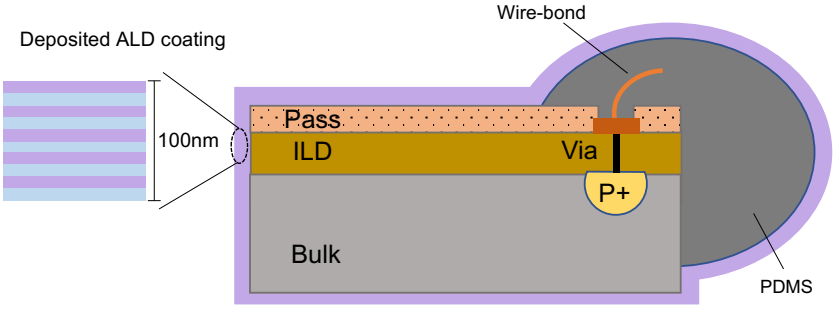


Figure 3.17: Schematic illustration of the multilayer ALD coating deposited on the sample (dimensions not to scale). The ceramic substrate is not shown in this illustration.

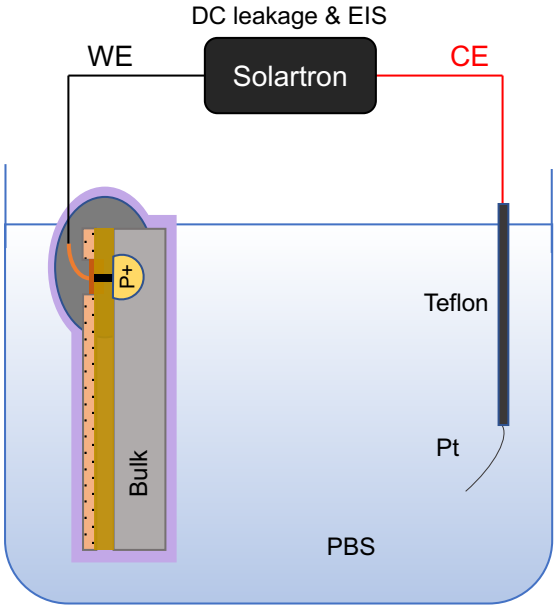


Figure 3.18: Schematic illustration of the set-up used for DC leakage and EIS measurements. The ceramic substrate is not shown in this illustration.

expected behavior when considering the interface to be a parallel plate capacitor with the ALD as the dielectric. The slightly higher impedance magnitude for ALD-coated-#2 is mainly due to the manual dispensing of the PDMS, which covered one sample more than the other.

To better understand the impedance data, Fig.3.21 gives the equivalent circuit model for the non-coated and coated samples. For the exposed bulk (Fig.3.21(a)), the silicon creates a thin native oxide layer with a thickness in the range of a few nanometers. As it is seen from the Bode plots, however, this layer is not uniform and thick enough to create a capacitive behavior. Therefore, the exposed bulk to electrolyte interface can be modeled as a CPE in parallel with a resistor representing the polarization resistance (RF). For the ALD-coated sample (Fig.3.21(b)), in the absence of any defects, the interface can be represented by a capacitor. Given the higher thickness of the ALD compared to the native oxide, a lower interface capacitance and therefore, higher impedance is measured for the ALD-coated samples. A defect in the layer, however, would expose the silicon bulk to the electrolyte creating a parallel CPE path. Depending on the ratio of these paths, the EIS data will change with the phase angle deviating from an ideal capacitor (-90°) to a more CPE like value (-70 °to -80 °). The total impedance response of such an interface, therefore, will depend on the aggregate dimensions of these defects and how they will dominate the impedance response at different frequency regimes.

To investigate how the level of defects could be captured in the impedance results, scratch tests were performed on one of the ALD-coated chips (ALD-coated-#2). Scratch testing is a standard technique for adhesion evaluation of thin-film coatings on vari-

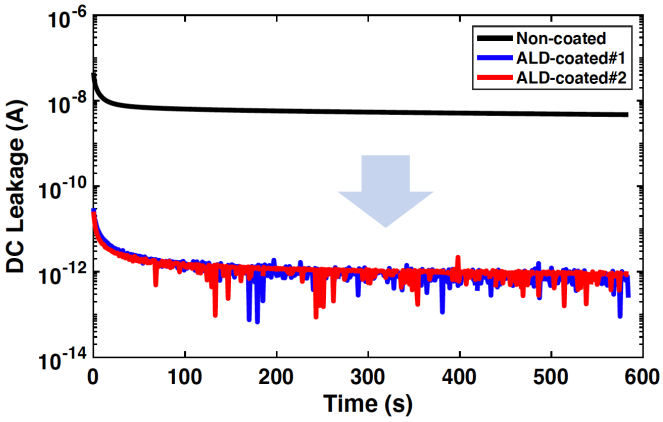


Figure 3.19: Measured DC current leakage over a duration of 10 min.

ous substrates [49]. In this work, however, the goal was to intentionally introduce a defect in the ALD layer and observe the change in impedance. Two scratches were made across the 1.7 mm sidewalls of the bulk with the second scratch being applied with more force. Measurements were performed in between by placing the sample back in the PBS solution. Scratches were made using a microprobe needle with a 10 μm tip. Fig.3.22 shows the impedance magnitude and phase after the first (Scratch #1) and second scratch (Scratch #2). By comparing the results, it can be seen that as more ALD layers are being removed, the impedance results deviate from the initial capacitive behavior and exhibit more a CPE behavior, similar to the non-coated sample. To investigate the reproducibility of the test, a scratch was also created on the ALD-coated#1 sample, with results showing a similar drop in impedance. These results show that EIS measurements with the bulk as the sensing platform, can be used for detecting defects in the ALD layer.

3.2.4. DISCUSSION

Thin-film coatings are a promising packaging solution for bioelectronic medicine. Failure of the coating, however, will result in various chemical and electrochemical reactions that could, in turn, result in performance loss or total device failure [29]. The focus of our group is realizing sensing and monitoring platforms for in-situ evaluation of hermeticity for thin-film coated bioelectronic medicine. In [50] a monitoring platform was introduced for tracking water/ion ingress within the different ILD stacks of CMOS chips. Water/ion ingress, however, will only be sensed once penetrated through the top coating, passivation, and ILD oxide layer. Evaluation of the outer coating, therefore, would require a different sensing platform which is the focus of this work. Using the bulk takes advantage of the conductivity of the CMOS substrate and enables a simple in-situ evaluation platform for detecting cracks or defects in the outer coating.

The ultimate goal of this work is to have an on-chip measurement unit with the bulk being the sensing platform. This would enable an implant with autonomous in-situ hermeticity evaluation. Such an autonomous platform could also be used for long-term

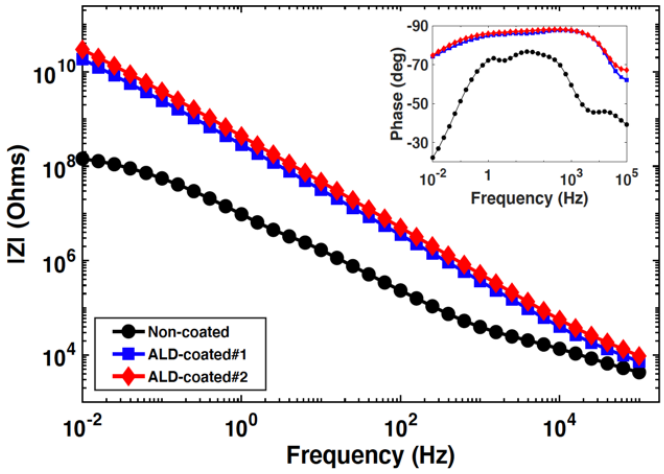


Figure 3.20: EIS measurements presented as Bode magnitude and phase angle (inset) plots.

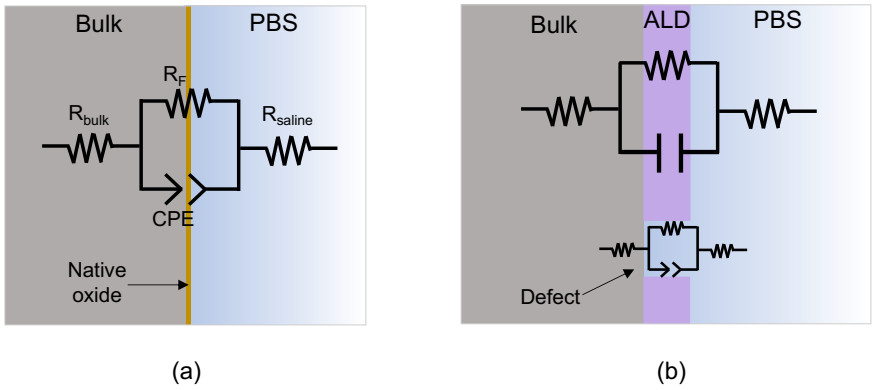


Figure 3.21: Schematic illustration of the equivalent circuit model for (a) bulk-saline interface, and (b) bulk/ALD-saline interface. (dimensions not to scale).

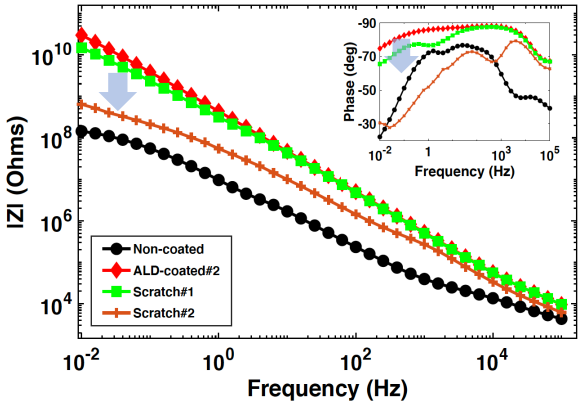


Figure 3.22: EIS measurement results for an ALD coated sample after first (Scratch#1) and second (Scratch#2) scratch tests on the ALD surface.

hermeticity evaluation during the implant's lifetime. For this reason, we opt for a low-voltage impedance measurement method since the measurement signal is biphasic and no DC current is applied to the exposed electrode. In this study, measurements were carried out between the bulk and a Pt wire. Within the implant, however, it is envisioned that the measurements will be done on chip, between the bulk and a Pt micro-electrode (the electrode intended for stimulation/recording). We do believe that the results reported here are still representative, given that the impedance is dominated by the coated substrate with respect to the exposed Pt wire.

In microelectronic design, the bulk of the chip is usually connected to the ground of the circuit, i.e. the lowest potential. Using the bulk as a sensing platform would, therefore, require novelty in the circuit design. For example, the added circuitry should neither increase the noise nor interfere with the normal operation of the implant. Currently, we are working on the design of a circuit that can perform the measurements on-chip.

3.2.5. CONCLUSION & FUTURE WORK

In this work, I demonstrated the feasibility of using the CMOS bulk as a platform for evaluating the hermeticity of thin coating layers on implantable chips. As a proof of concept, off-chip DC leakage and EIS measurements were performed in saline on chips fabricated in a standard CMOS process, with and without a deposited coating layer. The coating used in this study was an ALD multilayer with a total thickness of 100 nm. EIS was chosen over DC leakage as a more suitable measurement technique. As the ultimate goal of this work is to enable a fully integrated platform for hermeticity testing, further work is needed for the design of an on-chip measurement circuit with the silicon bulk as the sensing platform. In microelectronic design, the bulk of the chip is usually connected to the ground of the circuit, i.e. the lowest potential. Using the bulk as a sensing platform would, therefore, require novelty in the circuit design. For example, the added circuitry should neither increase the noise nor interfere with the normal operation of the implant.

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4

On the longevity and hermeticity of silicon-ICs: Evaluation of Bare-Die and PDMS-Coated ICs After Accelerated Aging and Implantation Studies

In this chapter, I evaluated the inherent hermeticity of foundry-fabricated IC structures (Chip-A from foundry A and Chip-B from foundry B) by directly exposing bare-die chips to accelerated in vitro and in vivo conditions for 12 months. I also aimed to identify the potential degradation pathways that can lead to failure. Various aspects such as the presence of different metallization layers and electric fields were also explored. In parallel, I investigated if polydimethylsiloxane (PDMS), as a soft but moisture-permeable coating, can prevent or delay the identified degradation pathways. Using advanced material analysis techniques, I derived rates for the different identified degradation pathways which could help in estimating the longevity of bare and PDMS-coated ICs. This chapter is a verbatim copy of the paper given in [1] which is currently in revision for publication, and only section and figure numbers were changed to comply with the format of this thesis. The Chip-A design and implementation were done by Federico Mazza and Timothy G. Constandinou from Imperial College London, and Nick Donaldson from University College London.

4.1. Introduction

Since the insertion of the first silicon integrated circuit (IC) into the brain for sensing neural activity [2, 3], tremendous efforts have been made to exploit the high performance and power efficiency offered by the semiconductor industry in opening new applications in the field of healthcare: brain-machine interfaces [4, 5, 6], flexible bioelectronics [5, 7, 8, 9, 10], biosensors [11, 12, 13, 14], active silicon probes [7, 15, 16], and optogenetics [17, 18].

Driven by the need for miniaturization, these emerging applications are moving away from the hermetic metal enclosures traditionally utilized for IC protection in the body and are opting for newly engineered thin organic and inorganic coatings [19, 20, 21, 22, 23, 24]. This shift, however, introduces reliability risks by bringing the chip closer to the corrosive body environment. Silicon-ICs are liable to failure if penetrated by body fluids: field effect transistors are susceptible to mobile ions (e.g., Na^+, K^+) that might reach the gate oxide [25, 26], and water anywhere in the intricate sub-micron structures of the IC will facilitate corrosion and leakage currents [27, 28]. Additionally, the body itself should be protected from the electrical bias voltages on the chip, which could pose a hazard if the IC's insulation is breached. With the growing interest in miniaturizing active neural implants, these reliability risks, and the uncertainty regarding the longevity of the IC have been identified as one of the main obstacles limiting the widespread clinical adoption of these emerging applications, particularly for chronic use [29, 30, 31, 32, 33, 34, 35].

The long-term reliability of implantable ICs relies on the stability and integrity of their constituent materials. Thus far, studies have been evaluating the stability of 'IC-related' thin-film materials such as silicon nitride (SiN_X) and silicon dioxide (SiO_2), mainly as standalone material films fabricated in research cleanrooms [22, 36, 37, 38]. Limited data, however, exists on the long-term stability and inherent hermeticity of actual foundry-fabricated IC structures as a whole.

Here, I evaluated the hermeticity of IC structures sourced from two complementary metal-oxide-semiconductor (CMOS) foundries by monitoring their electrical and material performance over long-term in vitro and in vivo studies. The primary objectives of this investigation were: **1)** to determine the longevity of bare ICs when directly exposed to physiological media by identifying the degradation pathways that can lead to failure, and **2)** to evaluate the possibility of utilizing polydimethylsiloxane silicone rubber (PDMS) as a soft but moisture-permeable coating to extend the longevity of implantable ICs.

Silicon ICs are intricate multilayer structures comprised of conducting metallization layers and insulating ceramic layers that are used as intermetallic dielectrics (IMD). Between the different metal layers, metal vias are used for making vertical interconnections. All layers of the IC stack are deposited onto a silicon substrate (Fig.4.1). The chemical composition of the materials used in the IC can vary depending on the technology node and the deposition processes utilized by the IC foundry [39]. For the metallization, aluminum (Al) or copper (Cu) are generally used; for the vias tungsten (W) and the insulating IMD layers, silicon dioxide is commonly employed [40]. The topmost insulating layers, known as the "passivation" layers, are usually a dual layer of silicon nitride (SiN_X) and silicon dioxide (SiO_2). These layers are deposited by plasma-enhanced chemical va-

por deposition (PECVD) techniques, coating the entire surface of the IC except for the openings used as bonding pads. The passivation layers have been included explicitly in the CMOS process to protect the IC against ambient humidity and contamination. The IC's sidewalls, however, are not protected by the passivation layers. For this reason, the CMOS industry has used a die seal ring (a stack of metallization encircling the die) as a side metal barrier to protect the inner circuitry from any impurity ingress and to provide structural support during dicing [41]. From the bottom, the IC is protected by the 200 - 300 μm thick silicon substrate, which has high density and high barrier properties [42]. Given the protections from the bottom and the sidewalls, the longevity of the IC largely depends on the top passivation layer's chemical stability and barrier properties. Both these properties are determined by the material type and the deposition processes utilized by the CMOS foundry.

When implanted as bare die, the IC passivation layers serve as the main protecting barriers. However, pre-existing defects, pinholes, or nanopores have been reported for PECVD ceramic layers, which could compromise their protection in wet ionic environments such as the human body [43]. Water molecules may also cause interlayer delamination in the IC stack when reaching interfaces, causing mechanical damage and failure [44, 43]. PECVD silicon nitride and dioxide layers have also been reported to dissolve when exposed to wet ionic media [37, 36].

When coated in PDMS, the IC is protected from direct exposure to tissue and body fluids. Nevertheless, due to PDMS's high moisture permeability [45], the IC material may still undergo degradation when implanted in the body. In our previous work [46], we demonstrated that not all silicon-based dielectrics are equally suitable for long-term implantation as diffusing moisture through the PDMS may also penetrate the dielectric layer and gradually degrade its insulating and dielectric properties. Thus, for PDMS-coated ICs, having long-lasting moisture barrier properties is a key requirement for the IC materials when targeting chronic use. Besides barrier properties, strong adhesion between the IC material and the PDMS ensures long-term electrical functionality. Strong interfacial adhesion is required to maintain electrical insulation between the wire-bonded pads [47]. Adhesion stability itself is influenced by the surface chemistry of the IC's passivation layer and the PDMS type [48].

In this investigation, ICs were partially coated with PDMS, intentionally leaving most of the IC's passivation surface and sidewalls exposed as bare die (Fig.4.1(a-b)). Where bare, the chip's intricate metallization and transistor structures are only protected by the IC's own passivation and IMD layers. In the PDMS-coated region, PDMS serves as additional protection but also insulates the wire bonds and the bonding pads through its adhesion to the IC passivation. ICs were either subjected to a one-year accelerated in vitro aging study in phosphate-buffered saline (PBS) solution at 67 °C or implanted in rats for a year.

Three test structures were implemented on the ICs: **1)** interdigitated capacitors (IDC), **2)** metal oxide semiconductor (MOS) transistors, and **3)** a dielectric sensor array with on-chip measurement and processing circuitry (Fig.4.1(c-e)). Using these structures, the electrical performance of the ICs is periodically monitored throughout the accelerated in vitro study, contributing to the long-term evaluation of the IC materials and the applied PDMS interfaces.

Complementary to the electrical measurements, several material analysis techniques were used to evaluate and compare the degradation mechanisms in the bare die and PDMS-coated regions of the aged chips. For both regions, the impact of two aging environments (PBS solution at 67 °C and rat) was also evaluated and compared. For this purpose, for the first time, advanced material analysis techniques have been used on CMOS foundry ICs to explore the bio-chemical degradation mechanisms after their long-term exposure to the implant environment.

The study presented here advances our understanding of the electrical and material stability of silicon-ICs in the implant environment, both as bare die and when coated with PDMS. The newfound insights from this study will inform and enable the design of state-of-the-art chip-scale active neural implants intended for chronic implantation.

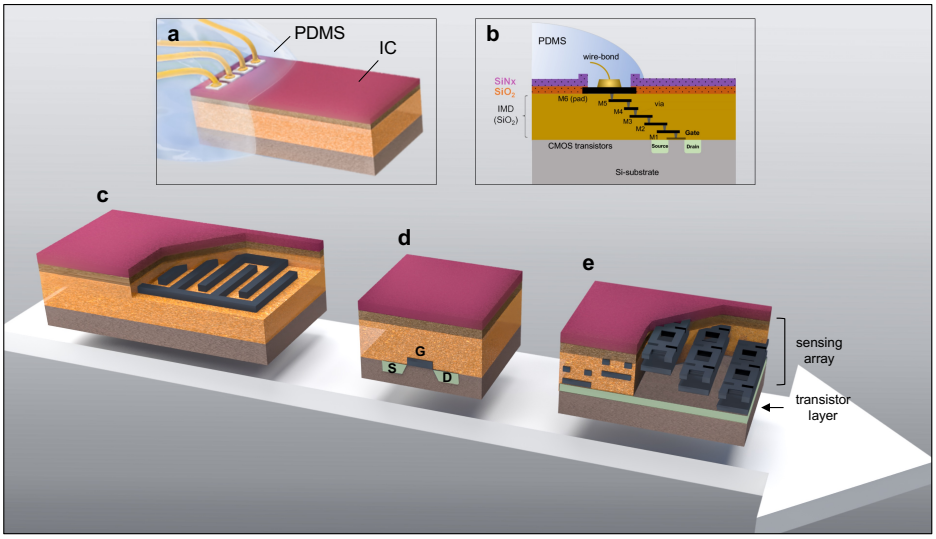


Figure 4.1: Schematic illustrations of silicon-IC test structures (dimensions not to scale). a) A wire-bonded IC partially coated with PDMS, covering the wire-bonds and regions of the outer IC surface, leaving most of the IC structure and sidewalls exposed. b) A cross-sectional schematic demonstrating the multilayer stack of a representative 6-metal CMOS process, from bottom to top: the source and drain diffusion regions implanted in the Si-substrate, metal layers 1 to 6 (M1 to M6) with M6 being the top-most metal, and where each metal layer is insulated with a SiO_2 intermetallic dielectric (IMD), and the final passivation layers generally made of SiO_2 and SiN_X. c) – e) Schematic of implemented test structures in silicon-IC, from simple to more advanced with, c) an interdigitated capacitor (IDC) structure implemented using the top metal layers where the structure is closer to the surface, d) A planar metal oxide semiconductor (MOS) transistor with the drain, source and gate implemented in the Si-substrate boundary, making the MOS structures the most buried structure. e) A dielectric sensor array with on-chip sensing circuitry for in situ monitoring of insulation and dielectric changes. Dielectric changes between different metal layers (M6-M5, M5-M4, and M4-M3) are sensed using on-chip MOS transistor circuitry.

4.2. RESULTS

4.2.1. IC DESIGN, FABRICATION, AND PDMS COATING

Here, I present the custom-designed IC test structures fabricated using two commercial CMOS foundries (hereafter called Chip-A and Chip-B). All ICs were partially PDMS-coated and subjected to either a one-year accelerated in vitro study in PBS solution at 67 °C or a one-year in vivo animal study in rats.

For the accelerated in vitro study, bare dice were glued on ceramic adaptors with pre-printed Pt/Au tracks, gold wire-bonded, and then partially coated with PDMS (Fig.4.2(a), details in Experimental Section 4.5). By partially coating the ICs, two distinct regions are created on the same chip: **1)** an exposed "bare die" region and **2)** a "PDMS-coated" region (Fig.4.2(b)). During the aging studies, both regions were simultaneously stressed and evaluated. On all prepared samples, the test structure under investigation was mainly left exposed (as bare die). This approach enabled us to evaluate how effectively the IC's own passivation and dielectric layers can protect the sensitive test structures underneath while being subjected to the different aging media.

In the PDMS-coated region, critical interfaces are created between the PDMS and the IC material (i.e., SiN_X, aluminum pad, silicon substrate). Strong long-lasting adhesive bonds at these interfaces are key in preventing voids and shunt water leakage paths that are required to ensure the long-term electrical functionality of the IC. On our structures, the most critical PDMS interface is with the SiN_X passivation at the PDMS-edge area (Fig.4.2(b)) and Fig.4.8, Supporting Note). In this area, the PDMS-SiN_X interface is directly subjected to the PBS solution. Interfacial debonding would allow lateral ingress of the solution, causing significant failure when the electrolyte reaches the electrically biased wire-bonds.

During the accelerated in vitro study, the IDC test structures were electrically biased. This was done either by applying a DC electrical voltage between the combs of the IDC or between the combs and the PBS solution. The main objectives for biasing the IDC structures were to: **1)** electrically stress the dielectrics and passivation layers while being directly exposed to liquid PBS solution in the uncoated regions, or to diffusing moisture (gaseous water) in the PDMS-protected regions, **2)** accelerate failure in the directly exposed region in case of microcracks or defects in the passivation layers, as previously reported [49, 50], and **3)** in the PDMS-coated region, investigate if the combined effects of a continuous electric field and moisture would weaken the PDMS-SiN_X interface adhesion, potentially leading to debonding and lateral ingress of saline.

A key factor in the design of the test structures is the presence or absence of a metal "shield (SH)". The shield is a metal layer implemented using the top metal of the process and designed to further protect the test structures underneath from any moisture/ion ingress. Additionally, around each test structure, a wall-of-via (WoV) is implemented which is a side metal barrier similar to the CMOS die seal ring. The WoV is included around each individual test structure to reduce the possibility of moisture/ion penetration from the edges (sidewalls) of the test structure.

Chip-A test structures were fabricated in a 0.35 μm CMOS 4-metal process. Two IDC test structures were implemented on Chip-A: **1)** M3-IDC and **2)** M4-SH/M3-IDC (Fig.4.2(d) and Fig.4.9, Supporting Note). M3-IDC (area: 1150 μm x 850 μm) contained 606 interdigitated fingers implemented in M3 (one layer below the top metal). It is pro-

tected by the IMD and the top SiN_X/SiO_2 passivation layers, each being ≈1 μm thick, as presented in the cross-sectional scanning electron microscope (SEM) image in Fig.4.2(b). The adjacent M4-SH/M3-IDC test structure used a similar M3-IDC interdigitated structure but included a thick top metal shield (≈ 2.8 μm thick) implemented in M4 (See cross-sectional SEM image in Fig.4.9, Supporting Note).

Chip-B test structures were fabricated using a 0.18 μm 6-metal process and contained three types of structures: **1)** IDCs, **2)** MOS transistors, and **3)** a dielectric sensor array (Fig.4.2e and Fig4.12, Supporting Note).

The IDC structures on Chip-B were implemented in Metal 5 (M5-IDC) or Metal 6 (M6-IDC). One IDC structure was also implemented with a shield on top (M6-SH/M5-IDC). In the M5-IDC structure, the comb metallization is in M5 and is protected by the IMD and the top SiN_X/SiO_2 passivation layers, each having a thickness of ≈ 0.6 μm and ≈ 1.1 μm, respectively (see cross-sectional SEM image in Figure 4.2e). M6-IDC is implemented in the top metal layer of the process and has the comb metallization protected only by the SiN_X/SiO_2 passivation layers (Fig4.10, Supporting Note). M6-SH/M5-IDC has the comb metallization on M5 and a shield layer on M6 (≈1 μm thick).

There are two MOS transistor structures with or without a shield barrier. All transistors have a W/L of 20 μm / 0.36 μm. The shield barrier for the MOS structure is a double-layer metal implemented in M5 and M6.

The dielectric sensor was diced and separated from the other test structures on Chip-B to ease the wire bonding and sample preparation required for long-term accelerated in vitro aging. The custom-designed sensor can measure IMD resistance values in the 10^{14} Ω range with the sensitivity to detect changes at a sub-M Ω resolution [51]. This sensor was designed and tested with two goals in mind: **1)** to verify if a complex CMOS circuit could operate when fully submerged in PBS solution at 67 °C, and **2)** to acquire more sensitive measurements of the dielectric changes and capture a 3D mapping of the possible moisture/ion penetration pathways into the chip.

For the accelerated in vitro aging study, the IDC structures (n=21 for Chip-A and n=34 for Chip-B) were fully immersed in PBS solution at 67 °C while continuously electrically biased. For biasing, three voltages were used: unbiased (n=13), 5 V DC (n=22), and 15 V DC (n=21) (Fig.S5a-b, Supporting Note). These voltages were selected based on their relevance for neurostimulator ICs [31]. Fig.4.13, Supporting Note, provides an overview of all the samples and the respective test conditions used in the study. The electrical performance of the IDCs was monitored monthly using electrochemical impedance spectroscopy (EIS) for a duration of at least 12 months. The NMOS test structures (n=5) and dielectric sensor (n=1) were immersed in PBS at 67 °C and monitored monthly while in soak for a 12-month duration (Fig.4.15, Supporting Note).

For the long-term in vivo study, n=12 ICs (n=6 from each IC foundry) were placed on PDMS substrates and implanted in 6 rats for a maximum duration of 12 months (Fig.4.2(f) and Fig.4.16, Supporting Note). While implanted, the ICs were neither powered nor electrically monitored. Explanations were phased at 3 months, 7 months, and 12 months. At every phase, two chips from each IC foundry were explanted.

On a group of reference samples (as received from the foundry), the chemical composition of the IC passivation layers was characterized using time-of-flight secondary ion mass spectrometry (ToF-SIMS) and X-ray photoelectron spectroscopy (XPS). The sil-

icon nitride on both Chip-A and B ICs was measured to be non-stoichiometric with a Si: 50% and N: 50% (N/Si: ≈ 1), typical for PECVD deposited SiN_X layers [52]. The hydrogen content in the nitride layers was measured using ToF-SIMS to be ≈ 20% and ≈ 15% for Chip-A and B, respectively (See Fig.4.17 and Fig.4.18, Supporting Note).

The SiO_2 passivation layer for Chip-A showed a stoichiometric layer (Si: ≈ 33% and O: ≈ 67%, O/Si of ≈ 2). For Chip-B, the silicon dioxide is comprised of two oxide layers. XPS results showed both layers having an O/Si of ≈ 2 (Si: ≈ 33% and O: ≈ 67%). However, ToF-SIMS results showed the top ≈ 100 nm oxide layer having a slightly higher [OH^-] intensity (x2.5) than the bottom layer. The bottom SiO_2 layer had similar [OH^-] intensities to the Chip-A SiO_2 passivation layer. The passivation layers contained very low carbon levels with no other detectable impurities (See ToF-SIMS depth profile results in Fig.4.17, Supporting Note).

Note that for both ICs, the chemistry of the passivation layers is uniform across the entire IC. However, the thicknesses and conformality of the passivation layers are affected when using the topmost metal layers: M4 for Chip-A and M6 for Chip-B (See Fig.4.16 and Fig.4.17, Supporting Note).

The IMD layers for both chips were analyzed using energy-dispersive X-ray (EDX) elemental mapping on the IC cross-sections which were created using a focused ion beam (FIB). Silicon dioxide is used as the IMD material for both chips, with Chip-B IMDs being slightly fluorinated (SiOF) (Fig.4.10, Supporting Note). Fluorination is done for more modern processes to reduce the dielectric constant of the IMD layers (from k ≈ 4.0 for SiO_2 to ≈ 3.5 in the fluorinated case) [53].

4.2.2. ELECTRICAL PERFORMANCE IN PBS SOLUTION AT 67 °C

Figure 4.3 gives a representative set of electrical results for ICs aged in the accelerated in vitro study in PBS solution at 67 °C. Figure 4.3a presents the electrical performance results at three different time points for M5-IDC and M6-SH/M5-IDC test structures (Chip-B). During the 12-month aging, the structures were continuously biased while in soak (5 V DC). EIS results (shown as Bode plots) demonstrate stable capacitive characteristics (phase ≈ -90°) and high impedance values (at 0.01 Hz $|Z| > 10^{11}\Omega$) throughout the 12-month accelerated aging for n=4 samples from each test structure. Results for other tested IDC structures, from both Chip-A and Chip-B and biased at 15 V DC, also showed similar stable capacitive behavior over the 12-month accelerated study (Fig.4.198, Supporting Note).

These results indicate three important characteristics of the IC materials and the applied interfaces: **1)** the stable capacitive behavior (phase ≈ - 90°) indicates that the passivation and IMD ceramic layers contain no nano-defects or pinholes, which might have otherwise created parallel resistive leakage paths through the PBS solution. **2)** They show the electrical stability of the IC passivation and IMD layers surrounding the IDC metals when fully submerged in PBS solution, for at least a year, while being continuously subjected to a maximum electric field of 0.25 MV/cm (at 15 V DC). This is irrespective of the fluorinated silicon dioxide used in the Chip-B IMD stack, which has been reported to be unstable in the presence of moisture [54]. **3)** Regarding the PDMS coating, these results demonstrate that PDMS effectively prevents water leakage paths by forming long-lasting interfacial adhesion to the IC's nitride passivation. In addition, they attest to the stable

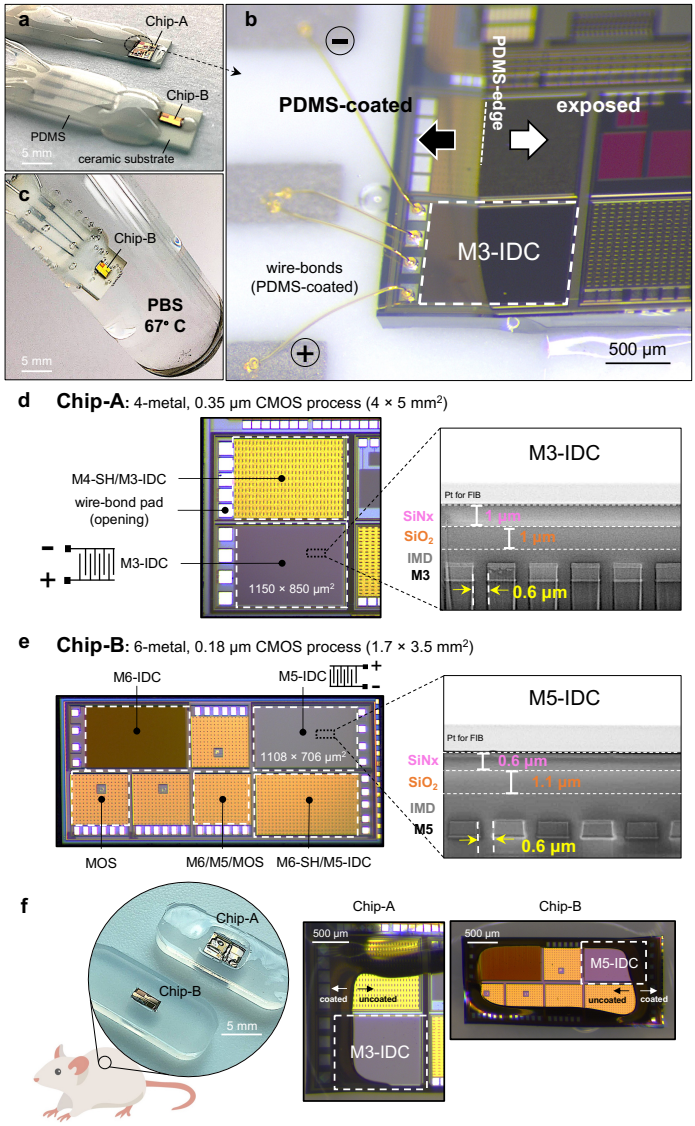


Figure 4.2: Silicon-IC test structures prepared for long-term accelerated in vitro and in vivo aging. a-c) ICs wire-bonded and prepared for in vitro accelerated aging (voltage and temperature) in phosphate-buffered saline (PBS, pH ≈ 7.4) at 67 °C, a) Optical image of a Chip-A and B IC placed on ceramic substrates, wire-bonded and partially PDMS-coated, b) Tilted optical micrograph of a representative Chip-A sample with the M3-IDC test structure wire-bonded and locally PDMS-coated, leaving most of the chip surface and sidewalls exposed, c) Optical image of a partially PDMS-coated Chip-B fully immersed in PBS solution at 67 °C. d-e) Top view optical micrographs and cross-sectional SEM images of Chip-A and B ICs with d) Optical micrograph of a Chip-A IC fabricated in a 0.35 μm 4-metal CMOS process with two IDC test structures (left). Cross-sectional SEM image of the M3-IDC test structure showing the interdigitated metal structures and the top SiN_X/SiO_2 passivation layers. e) Optical micrograph of Chip-B showing various IDC and MOS transistor test structures fabricated in a 0.18 μm 6-metal CMOS process (left). Cross-sectional SEM image of M5-IDC test structure showing Metal-5 and the top SiN_X/SiO_2 passivation layers (right). f) ICs subcutaneously implanted in rats. Chip-A and Chip-B ICs are positioned on soft PDMS substrates and locally coated with PDMS, covering the aluminum pads and regions of the top passivation while leaving most of the IC surface exposed to the body. Note that ICs used for the animal study are not wire-bonded.

electrical insulation properties of PDMS while submerged in PBS solution.

A few of our samples (14 out of 56) showed EIS irregularities (See Fig.4.20, Supporting Note), which were attributed to either, **1)** wire-bond corrosion (See Fig.4.21 and Fig.4.22, Supporting Note), **2)** stress-induced cracking of the passivation layers, or **3)** poor conformality of the passivation layers. Notably, the latter two failure scenarios on both IC foundries were found to be influenced by the use of the top metallization [55, 56] (Fig.4.23 and Fig.4.24, Supporting Note). The poor conformality or cracks expose the IDC metals to the PBS solution and when electrically biased, result in severe degradation and short-term failures. All other IDC structures implemented with lower metallization (M3 in Chip-A and M5 in Chip-B) showed no EIS irregularities.

NMOS transistors on Chip-B, both with (n=1) and without (n=4) the double shielded metal barrier, showed stable VGS-IDS characteristics over the 12-month accelerated aging (Fig.4.3(b)). For the NMOS structures without the shield metal barriers, the passivation and IMD stack serve as the protective barriers between the ionic solution and the MOS structure.

Fig.4.3(c) presents the results for the exposed dielectric sensor (Chip-B) after 5 months of aging in PBS solution at 67 °C. During aging, the chip's top surface and three side walls were intentionally left exposed. Comparing the results at 0-month and 5-month shows minimal change in the average and standard deviation results for the entire array. Testing on this chip stopped due to an intermittent wire-bond connection failure. The results, however, demonstrate the stability of the dielectric materials on Chip-B (fluorinated silicon dioxide). More significantly, these results demonstrate the stable electrical functionality of a complex CMOS IC designed in a 0.18 μm CMOS process when submerged as a bare chip in a 67 °C PBS solution.

4.2.3. MATERIAL PERFORMANCE: EXPOSED VS. PDMS-COATED

In the previous section, the electrical stability of various IC test structures was demonstrated over a 12-month accelerated in vitro aging study in PBS solution at 67 °C. Despite the electrical stability, exposure to ionic fluids may still degrade the IC's materials without causing discernible changes in the electrical characteristics. Given that identification of the degradation pathways can aid in the longevity estimation of the ICs, as a next step, we analyzed the materials on both the exposed (bare die) and PDMS-coated regions of the aged ICs. Our investigation began by using cross-sectional SEM imaging to evaluate the stability of the IC's entire multilayer stack. We were particularly evaluating the stack for any instances of interlayer delamination or intralayer degradation. Next, we examined the chemical stability and barrier properties of the IC's SiN_X/SiO_2 passivation layers using ToF-SIMS and XPS depth profiling. During the material evaluations, a comparative analysis was also conducted to understand the impact of the two aging environments on degradation: PBS solution at 67 °C and the in vivo animal environment at 37 °C. Finally, we investigated the effect of long-term exposure to electrical fields by focusing on a subset of IDC structures continuously subjected to electrical biasing (5 V and 15 V) in PBS solution at 67 °C for 12 months.

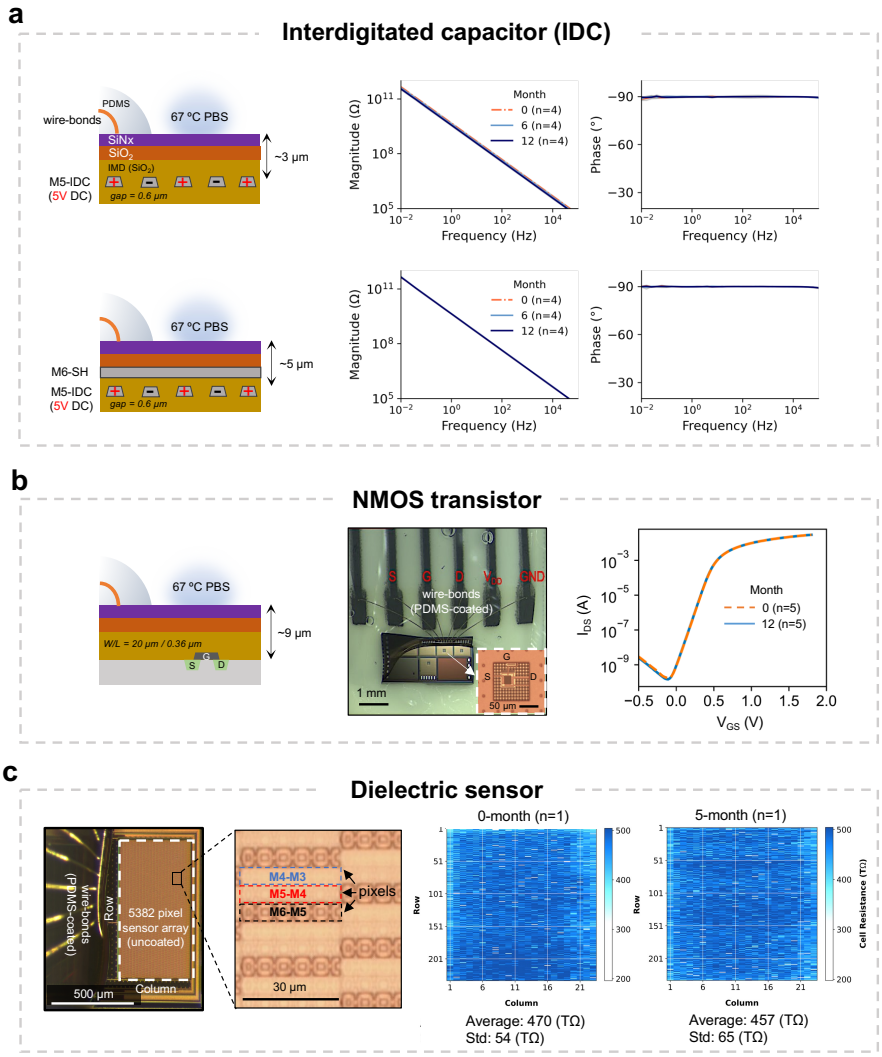


Figure 4.3: Long-term electrical performance of test structures on Chip-B during accelerated aging in PBS solution at 67 °C. a) Electrochemical impedance spectroscopy (EIS) results of representative M5-IDC test structures without (top, n=4) and with a top-metal (M6) shield (bottom, n=4), showing stable capacitive characteristics over the duration of aging. Results are given as average and standard deviation (n=4). b) Top view optical micrograph and average VGS-IDS transfer characteristics of NMOS transistors at 0-month and 12-month (n=4 unshielded and n=1 shielded MOS structures). Schematics show the distance between the test structures and the surface of the IC which is exposed to PBS solution (dimensions not to scale). c) Top view optical micrograph of the dielectric sensor with a high magnification image of the pixels (left). Measurement results giving the value of each pixel within the array (total 5382 pixels) at 0-month and 5-month (n=1). Comparing the average and standard deviation of the entire array at 0-month and 5-month shows minimal change (right). All electrical measurements are performed while the ICs and their PDMS-coated wire bonds are fully submerged in PBS solution.

EFFECT OF ENVIRONMENT: PBS SOLUTION (67 °C) AND RAT (37 °C) (UNBIASED)

Stability of IC multilayer stack The stability of the IC's multilayer stack was first evaluated using optical microscopy and later by SEM, examining the surface and various cross-sections across the chip. For both Chip-A and B samples, cross-sections were created using focused ion beam (FIB) at three different locations on the IDC test structures (corner, center, and PDMS-edge). Fig.4.4(a-c) shows representative cross-sectional SEM images taken at the PDMS-edge for two M3-IDC test structures (from Chip-A) at two different time points, 3 and 10 months. SEM results show intact metallization and no sign of interlayer delamination in the IC stack. Higher magnification imaging, however, reveals a thinning of the top SiN_X passivation in the exposed region, while no such degradation is observed for the PDMS-coated region (Fig.4.4(b-c)). At 3-month, ≈ 640 nm of the entire 1 μm SiN_X passivation remains on the sample, corresponding to a nitride dissolution rate of ≈ 120 nm/month for Chip-A. Cross sections on other locations of the IDC showed the dissolution to be uniform. Based on this dissolution rate (Figure S20, Supporting Note), at ≈ 8.5-month, a complete loss of the entire nitride is expected. Fig.4.4(c) shows a cross-sectional SEM image of a similar test structure aged for 10 months where only the SiO_2 passivation is present in the exposed region, corroborating the previously calculated SiN_X dissolution rate. Note that despite the complete loss of the SiN_X layer after ≈ 8.5 months, EIS results for the M3-IDC test structures on Chip-A remained stable for at least 12 months of aging in PBS solution. Based on the SEM images, from months 8.5 to 12, the SiO_2 passivation is exposed, and together with the intermetallic dielectric layer (IMD), they serve as the protective barriers on the M3-IDC. Similar cross-sectional SEM investigations for a Chip-B sample also showed a chemical dissolution of the exposed nitride layer (Fig.4.25).

A group of Chip-A (n=10) and Chip-B (n=8) ICs were aged for longer than 12 months in PBS at 67 °C. After 12 months, optical microscopy on all these Chip-A ICs showed gradual signs of delamination near the sidewalls of the chip. SEM investigations revealed the delamination to be between the silicon substrate and the entire IC stack (See Fig.4.26, Supporting Note). The delamination, however, was only observed on the side walls directly exposed to the PBS solution with the PDMS-protected regions remaining intact. Chip-B samples aged for longer than 12 months showed no signs of delamination (Fig.4.27, Supporting Note).

Next, the explanted ICs were investigated using SEM cross-sectional imaging and atomic force microscopy (AFM). The 3-month explanted ICs were examined using optical microscopy and cross-sectional SEM imaging (Figures S16 and S17, Supporting Note). Besides nitride dissolution on the directly exposed regions, no other degradation in the IC material stack was observed for the 3-month explanted chips. The PDMS-coated regions showed no observable SiN_x dissolution. More notably, it was found that even thin PDMS layers (< 1 μm) protected the SiN_X from degradation as it prevented tissue and body fluid contact with the IC (see Fig.4.28 and Fig.4.29).

The 7-month and 12-month explanted samples were analyzed using optical microscopy and AFM. Samples were first cleaned from tissue residues, PDMS decapsulated and later analyzed using optical microscopy and AFM on a 20 μm x 20 μm area at the PDMS-edge (Fig.4.4(d-e) and Fig.4.30, Supporting Note). Optical inspections revealed a non-uniform color on the exposed regions of the chip surface, indicating possible non-uniform disso-

lution of the passivation. The non-uniform dissolution could be due to the non-homogeneous coverage of various enzymes and tissue on the IC's surface. After decapsulation, PDMS-protected regions were similarly inspected, showing no signs of degradation (See Figure S18, Supporting Note). AFM analysis on the 7-month and 12-month explanted ICs showed a loss of the SiN_X passivation (Figure 4.4(d-e) and Fig.4.31, Supporting Note). Based on the calculated dissolution rates, on the 12-month explanted Chip-A samples, the 1 μm SiN_X passivation layer had completely dissolved after ≈ 8 months, leaving the SiO_2 passivation directly exposed to the body for ≈4 months. Despite the 4-month direct exposure, AFM results show the depth to be no less than 1 μm, indicating that the SiO_2 passivation on Chip-A did not dissolve after 4 months of direct exposure to the body environment. Similarly, for the 12-month explanted Chip-B samples, based on the dissolution rate of the SiN_X (Fig.4.32, Supporting Note), after the complete dissolution of the SiN_X at month ≈ 10, the SiO_2 passivation was directly exposed for 2 months to the body environment. The AFM profile at 12-month showed a loss of ≈ 700 nm, indicating that in addition to the ≈ 600 nm SiN_X dissolution, the top SiO_2 passivation on Chip-B has also experienced a ≈ 100 nm loss within the two months of exposure to the body. As revealed in section 2.1, the SiO_2 passivation on Chip-B contains two oxide layers, with the topmost layer (≈ 100 nm) having an x2.5 higher [OH^-] intensity (Figure S7, Supporting Note). Higher hydroxyl groups in SiO_2 PECVD ceramics have been reported to reduce their density and chemical stability, making the layer more vulnerable to dissolution in wet environments [57].

Regarding the biocompatibility of the implanted ICs, no adverse inflammation or tissue reaction was observed for all the animal models throughout the 12-month implantation, despite the gradual dissolution of the SiN_X passivation on both IC groups (See Fig.4.33 and Fig.4.34, Supporting Note).

In Figure 4.4(f), we compare the dissolution rates of SiN_X passivation after exposure to various aging environments. A comparison of the dissolution rates in PBS solution at 67 °C (120 nm/month for Chip-A and 22 nm/month for Chip-B) and in vivo at 37 °C (≈125 nm/month for Chip-A and ≈54 nm/month for Chip-B) clearly illustrates the body's more aggressive environment for silicon nitride dissolution compared to PBS at 67 °C.

Supporting experiments were conducted by aging some ICs in de-ionized (DI) water at 67 °C (see Fig.4.13, Supporting Note). The lower dissolution rate of SiN_X in DI water compared to PBS solution at the same temperature indicates that the dissolution process for SiN_X is not entirely hydrolytic (water-driven) but that the ions present in the solution (Na^+, Cl^-, $PO4^-$) significantly affect the dissolution kinetics. Dissolution of thin-film ceramic materials has been reported in previous literature [37, 36], showing the chemical instability of these PECVD-deposited ceramics when exposed to wet ionic environments.

When comparing the SiN_X dissolution rates on Chip-A and B, a higher dissolution rate for Chip-A material is observed in all aging environments. This is despite the similar N/Si for both chips (Chip-A and B both having a N: 50% and Si: 50%) as given in Fig.4.17, Supporting Note. The higher SiN_X dissolution rate for Chip-A could be due to the slightly higher hydrogen (H) content in the layer (≈ 20% for Chip-A and ≈ 15% for Chip-B). Other factors such as the morphology (atomic arrangements) could also play a role in the chemical stability when exposed to wet environments [58].

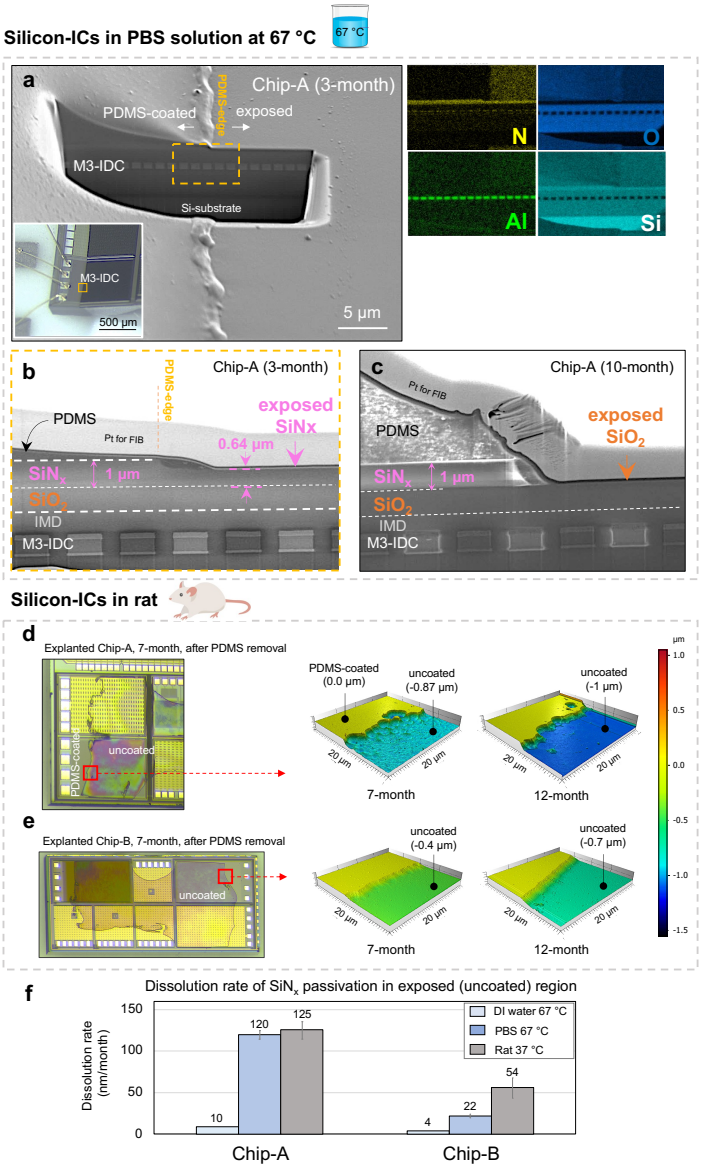


Figure 4.4: Stability of IC multilayer stack and top passivation layers after accelerated in vitro and in vivo aging. a-c) Representative cross-sectional SEM images of Chip-A samples after accelerated in vitro aging in PBS solution at 67 °C, a) Cross-sectional SEM image on the PDMS edge of an M3-IDC (Chip-A) structure after 3 months of aging in 67 °C PBS showing the IMD material stack from surface to silicon substrate. Inset: optical micrograph of the area used for cross-section analysis. Right, EDX elemental analysis shows intact aluminum IDC metallization. b) Magnified cross-sectional SEM image at the PDMS-edge showing a thinning of exposed SiN_X passivation (≈ 360 nm) after 3 months of aging in 67 °C PBS. c) Cross-sectional SEM image of a Chip-A sample after 10 months with complete loss of SiN_X passivation in the uncoated region, leaving the SiO_2 passivation exposed to the PBS solution. d-e) Representative optical micrograph and 3D AFM surface profiles of explanted Chip-A and B samples after PDMS decapsulation. All AFM profiles were taken within a 20 μm × 20 μm window around the former PDMS-edge (red square). AFM profiles were taken after 7 and 12 months of implantation in rats. f) Dissolution rates of exposed SiN_X passivation from Chip-A and B in different aging media (n≥2, with each sample measured on two different locations).

Ionic barrier properties of IC passivation layers Next, we investigated the ionic barrier properties of the SiN_X/SiO_2 passivation after their long-term exposure to physiological media.

The ingress of various cations (Na^+, K^+, Ca^+, and Mg^+) and anions (Cl^-, $PO_4{}^-$, S^-) in the exposed regions of the ICs was measured by positive and negative mode ToF-SIMS depth profiling, respectively. Depth profiles were taken from the surface to ≈ 200 nm within the SiO_2 passivation layer. Figure 4.5 presents the positive mode depth profiles of Chip-A and B ICs, explanted after 7 and 12 months in vivo. In the positive mode, [Si_2N^+] and [SiO^+] cluster ions were used to identify the SiN_X and SiO_2 passivation layers [59]. For the 7-month explanted ICs, ≈ 100 nm and ≈ 200 nm of the SiN_X passivation remained on Chip-A and Chip-B, respectively. These results support the AFM measurements showing the dissolution and thinning of the SiN_X passivation when exposed to the body (Fig.4.4d-e). Despite the dissolution and long-term exposure, no ingress of alkali metals is present in the remaining SiN_X layers, indicating that the SiN_X passivation from both IC foundries maintained its ionic barrier properties over the long-term exposure in vivo.

On the 12-month explanted ICs, no SiN_X was detected on either chip, leaving the SiO2 passivation directly exposed to the body environment. Based on the estimated SiN_X dissolution rates in Fig.4.4(f), after the complete SiN_X dissolution, the SiO_2 passivation is exposed to tissue for approximately 4 and 2 months for Chip-A and Chip-B samples, respectively. Interestingly, no ionic ingress was detected for the exposed SiO_2 layers from either IC foundry. Negative mode depth profiles also did not reveal any ingress of anions and do not contain additional information; thus, they are not presented.

These results indicate that both SiN_X and SiO_2 passivation layers from the two selected silicon-IC foundries are effective long-term barriers against ionic ingress from the body. Note that in some profiles, a slight increase in the aluminum (Al) intensity was found in the deeper depths of the SiO_2 as the profile was getting closer to the IDC metallization. Closer to the surface or in the SiN_X, however, no aluminum was detected, indicating that the passivation layers act as a two-sided barrier, preventing ionic ingress into the chip, but also inhibiting the out-diffusion of IC metals into the body.

Chemical stability and moisture barrier properties of IC passivation layers (unbiased) Next, we investigated the chemical stability and moisture barrier properties of the SiN_X and SiO_2 passivation layers on the directly exposed and PDMS-coated regions of the aged ICs. It has been reported that moisture can dissociate the Si-N, Si-O, and Si-Si bonds in silicon-based ceramics and create silanol groups (Si-OH) in the atomic structure [60]. For ICs, these silanol groups can have detrimental effects as they could increase the dielectric constant of the insulating layers and lower their ionic barrier properties, facilitating ion penetration within the IC [57].

For this purpose, we used negative mode ToF-SIMS depth profiling to evaluate the chemical stability of the SiN_X and SiO_2 passivation layers. The [SiN^-] and [$SiO_2{}^-$] cluster ions were used to evaluate the layers [61]. The moisture barrier properties of the passivation layers were also analyzed by monitoring the intensity of the [OH^-] cluster ion within the depth profiles [59]. In all cases, results on aged ICs were compared to depth profile results from reference ICs (as-is-from-foundry).

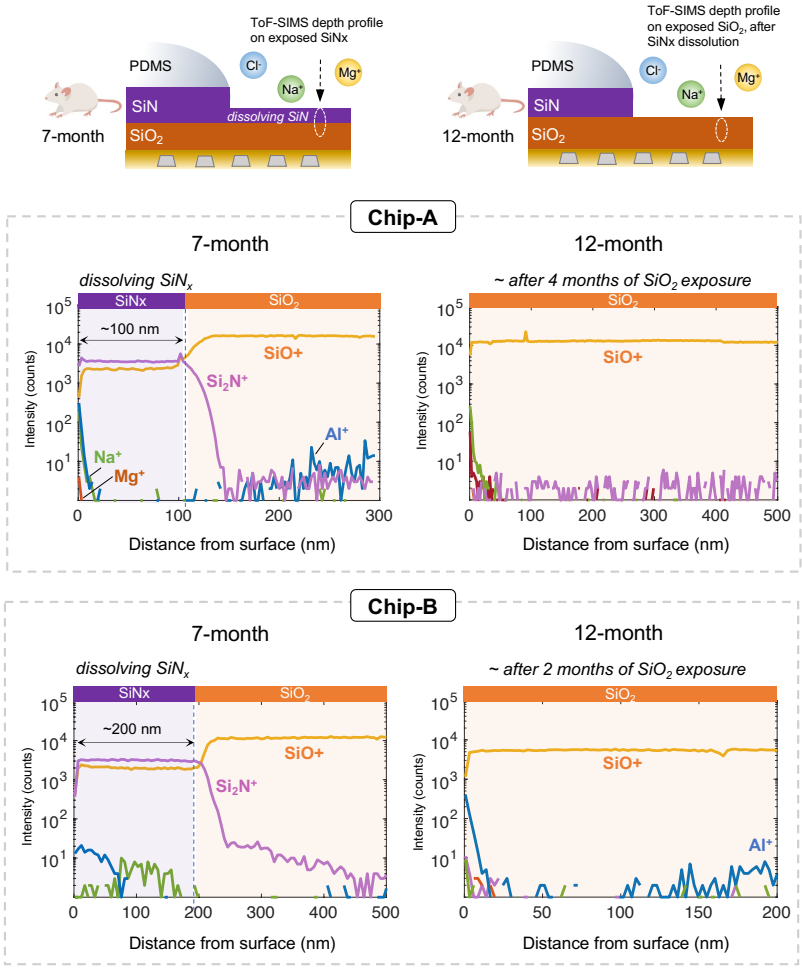


Figure 4.5: Positive mode ToF-SIMS depth profiles analyzing the ionic barrier properties of the exposed passivation layers after 7 and 12 months implantation in rat. After 7 months, ≈ 100 nm and 200 nm of the dissolving SiN_X remained on Chip-A and B samples, respectively. Despite the dissolution, no detectable ionic penetration is found within the remaining SiN_X layers. After 12 months, with the complete dissolution of SiN_X, the SiO_2 passivation is directly exposed for ≈ 4 and 2 months for Chip-A and B, respectively. Nevertheless, no signs of ionic penetration are detected within the SiO_2 passivation layers.

Profiling was done at three different depths: SiN_X-surface (analyzed from 0 - 15 nm), SiN_X-bulk (analyzed from 50 - 100 nm within the SiN_X layer), and SiO_2-bulk (analyzed from 100 to 200 nm within the SiO_2 passivation layer). Surface analysis (0 - 15 nm) was conducted with sub-nanometre (0.139 nm) step sizes (See Experimental Section 4.5). All bulk profiles were collected using ≈ 1 nm step sizes.

The schematic in Fig.4.6 summarizes the findings from the depth profile analysis. In the exposed regions, a thickness increase in the surface oxidation of the SiN_X passivation is observed. Within the oxidized layer, a slight increase in ionic impurities is also seen.

In the PDMS-coated region, on the other hand, only an increase in oxidation thickness was found with no increase in the ionic impurities.

Fig.4.6a-b presents the negative mode depth profiles of a representative Chip-A sample after 7 months of implantation in rats, comparing the first 15 nm of the SiN_X passivation in the PDMS-coated and exposed regions. In both regions, the first 5 nm demonstrated low intensities of [SiN^-] with high intensities of [OH^-] and [$SiO_2{}^-$]. This pattern indicates a surface oxidation of the SiN_X, revealing an additional degradation mechanism affecting the SiN_X passivation on the ICs. In the exposed region, slightly higher chlorine [Cl^-] and sulfur [S^-] intensity was also detected in the oxidized layer. These ions could be a result of biofluids and amino acids touching the oxidized layer and penetrating within the layer [62]. In the PDMS-coated region, on the other hand, the oxidized SiN_X layer showed lower [Cl^-] and [S^-] intensities, similar to reference level ICs. To compare the thickness of the oxidized layers between the two regions, the depth in which the [SiO_2-] intensity is higher than the [SiN^-] intensity is used to identify the oxidized layer on the SiN_X passivation. Results show a slightly thicker oxidized layer in the exposed region of the IC. Similar surface ToF-SIMS depth profile results for a 7-month explanted Chip-B can be found in Figure**??**, Supporting Note.

Fig.4.6(c) compares the thicknesses of the oxidized SiN_X layer in the exposed and PDMS-coated regions for Chip-A and B after 7 months in vivo. The oxidized layers on Chip-B, for both regions, show a thinner layer compared to Chip-A, suggesting the higher density and stability of the nitride passivation on Chip-B. Fig.4.6(d) shows the thickness of the oxidized SiN_X in the PDMS-coated regions over time. After 12 months of implantation in rats, ≈ 7.8 nm (0.78% of total SiN_X thickness) and ≈ 4.9 nm (0.75% of total SiN_X thickness) of the nitride passivation has been oxidized for the Chip-A and B ICs, respectively. Note that for reference ICs (as-is-from-foundry, 0-month), a ≈ 3.5 - 4 nm oxide layer is already present on the surface of the SiN_X passivation. Assuming a linear oxidation rate, a ≈ 3.9 nm/year and ≈ 1.4 nm/year oxidation rate can be anticipated for PDMS-protected Chip-A and B ICs when implanted in the body.

Figure 4.6(e) compares the effect of the two aging environments (PBS solution at 67 °C and rat at 37 °C) on the oxidation of the nitride passivation in the PDMS-coated region. After 12 months, ICs soaked in 67 °C PBS solution showed a thicker oxidized layer on the SiN_X. These results indicate that the 67 °C accelerates the moisture diffusion and oxidation process within the SiN_X passivation layer.

Within the SiN_X-bulk, the [OH^-] and [SiN^-] signals were evaluated by averaging the intensities within the 50 - 100 nm depth of the SiN_X layer. Fig.4.6(f) presents the [OH^-] intensities within the SiN_X-bulk for exposed and PDMS-coated regions after 7 months of implantation in rats showing slightly higher [OH^-] in the exposed regions. In the PDMS-coated regions, the [OH^-] intensity was also evaluated over time (Fig.4.6(g)), indicating a gradual increase in the intensity with time. When comparing the two aging environments at 12 months, a marked increase in the [OH^-] intensity is observed for the ICs soaked in PBS solution at 67 °C, possibly resulting from the higher diffusion rate of moisture with temperature.

Fig.4.6(i-k) gives the [SiN^-] intensity in the bulk region, showing stable intensities for all samples except those soaked in PBS solution at 67 °C. The decreased [SiN^-] intensity observed in samples soaked in PBS solution suggests that elevated temperatures

accelerate moisture diffusion and promote the breakage of Si-N bonds within the SiN_X passivation layer.

Next, the SiO_2-bulk was examined by evaluating the [OH^-] and [SiO_2^-] intensities in the layer (averaging the intensities between 100 - 200 nm). Figures 4.6l-m show the average intensities for the exposed and PDMS-coated regions after 12 months of exposure to both aging environments. On both Chip-A and B samples, a stable [OH^-] intensity is seen in the SiO_2 layer for the PDMS-coated regions. A slight increase in [OH^-] intensity is recorded for the exposed areas for Chip-B. Note that the SiO_2 passivation can be directly exposed to the aging environments (either PBS or body) for the exposed (uncoated) regions after the complete dissolution of the nitride passivation. In the PDMS-coated regions, however, the SiO_2 is always protected by both PDMS and the top SiN_X passivation layer.

The [SiO_2^-] intensity within the bulk SiO_2 layer also revealed stable intensities for both exposed and PDMS-coated regions after 12 months of aging, suggesting the chemical stability of the bulk SiO_2 passivation layer on both IC foundries.

EFFECT OF ELECTRICAL FIELD: DC ELECTRICAL BIAS IN PBS SOLUTION AT 67 °C

Given that implantable ICs will be subjected to electrical bias voltages during their lifetime operation, as our final investigation, we evaluated the long-term effect of electric biasing on the stability of the IC materials and the PDMS interfaces. Note that a group of biased IDC structures experienced short-term (1 - 2 months) failures (See Table Fig.4.20, Supporting Note). For all these samples, the top metallization of the IC (M4 for Chip-A and M6 for Chip-B) was used which resulted in poor conformality or stress-induced cracking in the passivation. For investigating the longer-term effects of electrical biasing, M3-IDC (Chip-A) and M5-IDC (Chip-B) test structures were used.

Fig.4.7(a) gives a schematic representation of a partially PDMS-coated IC applied to electrical bias (between the IDC metallization and solution) in PBS solution at 67 °C. During biasing, both combs of the IDC were connected to the negative (-) potential, and +5 V or +15 V DC was connected to a stainless-steel rod in the PBS solution. The polarity was chosen to drive the alkaline ions (Na^+ and K^+) towards the IC passivation. The right schematic in Fig.4.7a gives an overview of the findings demonstrating the effect of the continuous biasing on the exposed and PDMS-coated regions of the chip.

Microscopically, structures continuously biased with 15 V DC voltage (n=6 from Chip-A and n=10 from Chip-B) showed signs of discoloration across their surface in the exposed region, as demonstrated in a representative M3-IDC structure from Chip-A (arrows in Fig.4.7(b)). In contrast, areas protected by PDMS showed no discoloration. Note that despite the discoloration in the exposed regions, stable capacitive behavior was recorded over the 12-month aging duration when measured between the comb structures and PBS (Fig.4.19, Supporting Note).

Figure 4.7c presents a cross-sectional SEM image taken at the PDMS edge. In both the PDMS-coated and exposed regions, intact aluminum metallization was observed with no noticeable difference in the buried IC's multilayer stack. However, the exposed region showed the presence of a thinned SiN_X passivation layer ($\approx 0.33\ \mu m$). This contrasts with the unbiased Chip-A sample where complete dissolution of the SiN_X was observed after 10 months of direct exposure to PBS solution at 67 °C (Fig.4.4(c)). Figure

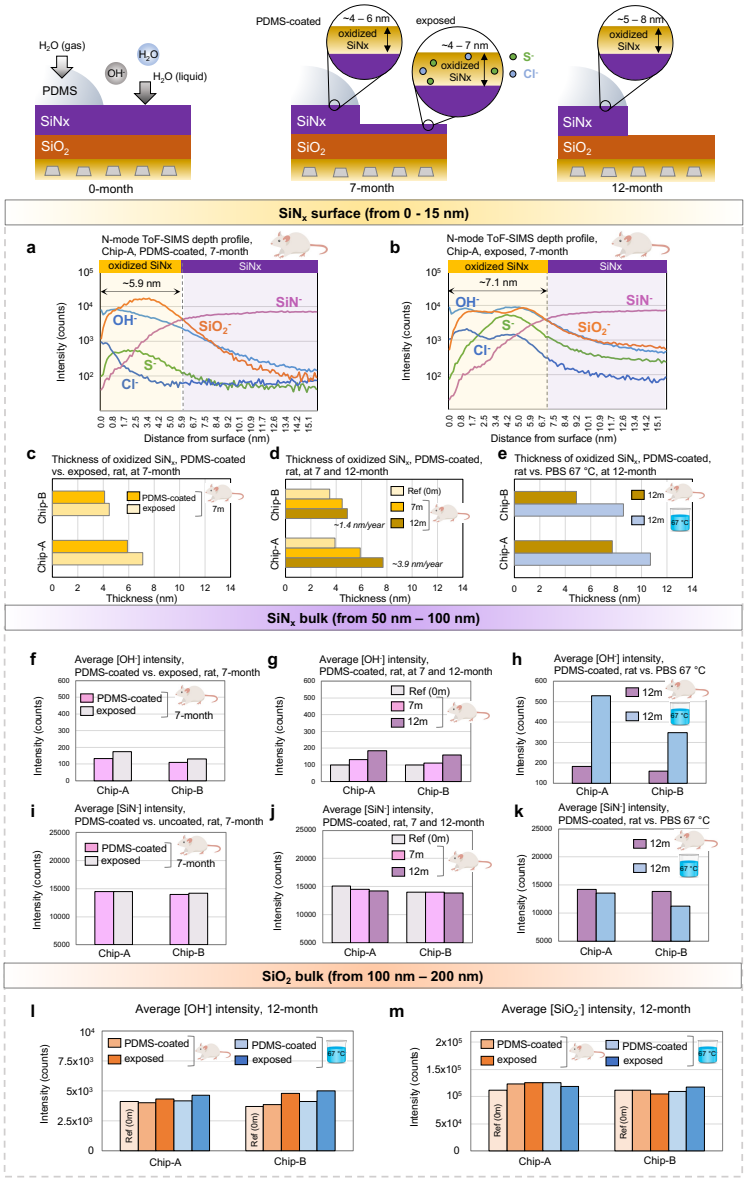


Figure 4.6: Chemical stability and moisture barrier properties of PDMS-coated and exposed passivation layers after accelerated in vitro and in vivo aging analyzed using negative mode ToF-SIMS depth profiling. a-b) Representative ToF-SIMS surface depth profiles from 0 - 15 nm of the PDMS-coated and exposed regions of a 7-month explanted Chip-A sample (acquired with 0.1 nm step-size). Surface depth profiles show oxidation of the SiN_X passivation with higher chlorine (Cl) and sulfur (S) impurity ions in the oxidized layer for the exposed region. c - e) Comparing the thicknesses of the oxidized SiN_X at different time points and aging media (in 7m or 12m, 'm' denotes month). c) Comparing the thicknesses in the PDMS-coated and exposed regions after 7 months in vivo, d) Comparing the thicknesses in the PDMS-coated regions after 7 and 12 months in vivo with that of a dry reference sample, and e) Comparing the thicknesses in the PDMS-coated regions after 12 months exposure to accelerated in vitro and in vivo environment. f-n) average [SiN^-] and [OH^-] intensities within the SiN_X passivation bulk (averaged ToF-SIMS depth profile data from 50 - 100 nm). n-o) average [OH^-] and [$SiO_2{}^-$] intensities within the SiO_2 passivation bulk (averaged ToF-SIMS depth profile data from 100 - 200 nm). Note that in the uncoated region, at 12 months, the SiO_2 passivation is directly exposed to the body environment. Data is presented as average of 4 measurement results, performed on n=2 samples with 2 measurements per sample.

4.7c also reveals a different contrast between the thinned SiN_X layer in the exposed region and the PDMS-protected region. The PDMS-protected region showed the expected thickness for the SiN_X passivation (1 μm).

Negative and positive mode ToF-SIMS depth profiling was used to evaluate the chemical stability and barrier properties of the exposed and PDMS-coated regions of the ICs. For analysis, M3-IDC (n=2, Chip-A) and M5-IDC (n=2, Chip-B) test structures were used which were continuously biased for 12 months with 15 V DC in PBS solution at 67 °C. Fig.4.7(d) presents the depth profiling results for the exposed region on a representative M3-IDC structure (Chip-A). Negative mode depth profile results revealed a ≈ 120 nm oxidized layer on top of a 100 nm SiN_X layer. Within the oxide layer, high intensities of [SiO_2^-], [OH^-], and carbon [C^-] were found. Positive mode depth profiles also revealed high intensities of [Na^+] and [K^+] ions in the top ≈ 120 nm oxidized layer. Beyond the 120 nm depth, once the profile enters the remaining ≈ 100 nm SiN_X layer, a marked drop in the impurity ions was observed, demonstrating that the remaining SiN_X still acts as an ion barrier.

XPS depth profiling was used to quantify the chemical composition and ionic impurity levels within the oxidized layers (See Fig.4.36, Supporting Note). The chemical composition of the oxidized SiN_X layer indicated a slightly off-stoichiometric oxide film for Chip-A (Si: 28%, O: 58%) and Chip-B (Si: 28%, O: 62%) samples. For the ionic impurities, despite the high intensities detected by ToF-SIMS, XPS found a 2 - 3% sodium (Na) incorporation in the oxidized layer for both Chip-A and B samples. Note that the sensitivity levels of the ToF-SIMS measurement to Na+ and K+ ions can be 3 to 5 orders of magnitude higher than XPS (See Experimental Section).

In comparison to the exposed region, depth profiling on the PDMS-coated region of the biased IDC structures showed a stable [SiN^-] profile within the entire ≈ 1 μm SiN_X passivation layer (Fig.4.7(e)). A thin (≈ 12 nm) oxide layer was observed on top of the SiN_X layer with no ionic penetration. The absence of ionic penetration in the oxidized layer is due to the ionic barrier properties of the PDMS coating [63], in this case, even in the presence of an electrical field.

As explained in the previous section, due to PDMS's inherent moisture permeability, a gradual oxidation of the SiN_X passivation can be expected in the PDMS-coated regions of the IC. To examine if the applied electrical fields affected the oxidation rate of the SiN_X, the thicknesses of the oxidized layer in the PDMS-coated regions were measured for a group of samples that were biased with a 5 V (n=2) or 15 V (n=2) DC voltage (between IDC and PBS) during the 12-month aging study in PBS solution at 67 °C (Fig.4.7(f)). At 5 V DC (n=2 from each chip), no significant change in oxide thickness was measured compared to unbiased IDC structures. However, at 15 V DC (n=2 from each chip), both Chip-A and Chip-B samples showed a slightly thicker oxidized layer, suggesting that higher electrical fields may enhance the oxidation rate of SiN_X in the PDMS-coated region.

Fig.4.7(g-h) gives the average [OH^-] intensity in the bulk (averaging the intensities between 100 - 200 nm) of the SiN_X and SiO_2 passivation layers. In the SiN_X layer, higher [OH^-] intensities were observed on samples subjected to continuous 15 V DC voltages as compared to 5 V and unbiased chips (Fig.4.7g). The [OH^-] incorporation may result from the higher applied voltage, as higher electrical fields may introduce strain in the molecular structure of the dielectric [64], making the structure more susceptible to

moisture attack. It should be noted that the increased [OH^-] incorporation in the SiN_X layer was exclusively detected using ToF-SIMS due to its enhanced sensitivity. XPS depth profile results in the SiN_X passivation revealed no oxygen and a N/Si ratio of ≈ 1 (similar to reference, as is from foundry ICs) for both Chip-A and Chip-B samples (Fig.4.36, Supporting Note). The SiO_2 passivation was similarly investigated (Fig.4.7i), where a slightly higher [OH^-] intensity was observed for devices under 15 V continuous DC biasing.

4.3. DISCUSSION AND GUIDELINES FOR LONGEVITY

In this work, we intended to determine the functional lifetime of bare and PDMS-coated ICs in physiological media by testing devices until failure. However, through the 12-month accelerated in vitro study, very few IC failures were recorded on the n=62 tested chips. Therefore, complementary material evaluation techniques were performed on the in vitro and in vivo aged ICs to detect alternative degradation pathways that could help estimate the longevity of ICs in the body.

In the exposed bare die regions, we demonstrated the long-term moisture and ionic barrier properties of the SiN_X and SiO_2 passivation layers from both CMOS IC foundries. Nevertheless, as bare-die, the dissolution of the SiN_X passivation was observed to be the primary degradation pathway in vivo (dissolution rate of ≈ 125 and ≈ 54 nm/month for Chip-A and B, respectively). Despite the nitride dissolution, the SiO_2 passivation underneath also exhibited excellent ion and moisture barrier properties, suggesting that uncoated/unprotected ICs can maintain their functionality in the body for at least 12 months. Note that this is only when the top metallization is not used. When the top metal is used, due to the poor conformality of the PECVD passivation layers, the top metal could be exposed to tissue within 6-7 months of implantation, causing metal corrosion (see cross-sectional SEM images in Fig.4.37, Supporting Note). Besides device malfunction, this would pose toxicity and safety risks as it would expose the body to electrical DC voltages. Therefore, for applications requiring the use of the top metal layer of the IC (nominal or thick top metal), applying a PDMS coating or a thin conformal coating is advised [65].

In the PDMS-coated regions, gradual surface oxidation of the SiN_X passivation was observed after 12 months in vivo (oxidation rate of ≈ 3.9 and 1.4 nm/year for Chip-A and B, respectively). With this rate, it would take decades for the entire SiN_X passivation to oxidize. Nevertheless, in the case of total oxidation of the entire nitride layer, the SiO_2 passivation underneath would still serve as the second barrier protecting the underlying circuits. Taking a conservative estimate and considering the oxidation of the SiN_X to be the main degradation path for PDMS-coated ICs, we believe PDMS-coated ICs have the potential to reach decades of functional lifetime in the body.

At first, it may seem unlikely that PDMS, a polymer with low moisture barrier properties, would be suitable for the long-term protection of ICs. However, in this investigation, it was demonstrated that the IC's passivation layers can have excellent moisture barrier properties. Therefore, other material characteristics of PDMS are key in achieving a long lifetime: **1)** Low stress/strain ratio. Moisture-induced expansion of the polymer packaging may introduce stress on the IC's ceramic layers [66]. Shear stress cracking of the IC's passivation has been reported to be one of the main failure mechanisms for epoxy-packaged chips [67, 66]. PDMS's soft and compliant properties make it an ideal poly-

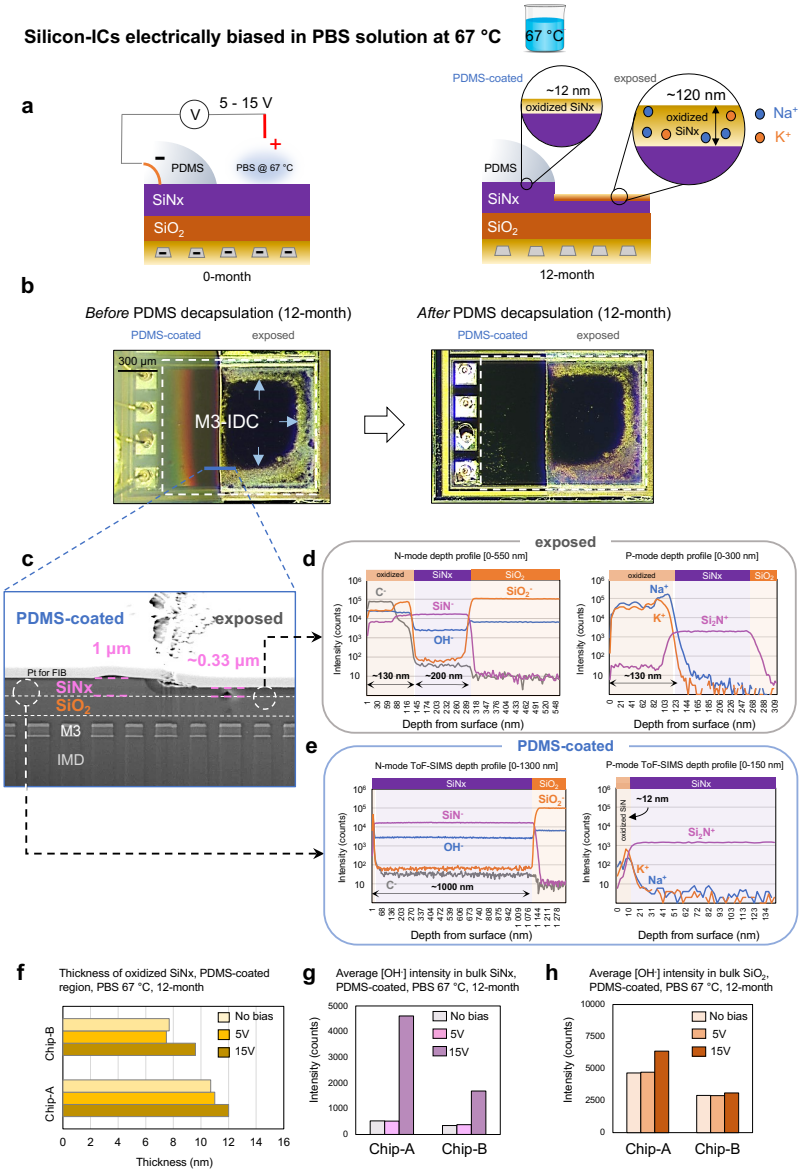


Figure 4.7: Chemical stability and moisture and ion barrier properties of PDMS-coated and exposed passivation layers after continuous DC biasing in PBS solution at 67 °C. a) Left schematic: biasing configuration with DC voltage applied between the IDC metallization (combs) and an electrode in PBS solution. Right schematic: the effect of the continuous biasing on passivation. b) Top view optical micrographs of a representative M3-IDC structure (Chip-A) sample after 12 months of continuous 15 V biasing between M3-IDC and PBS showing the color change in the exposed region. Right image after PDMS decapsulation. c) Cross-sectional SEM image of the Chip-A sample at the PDMS edge. d-e) Positive and negative mode ToF-SIMS depth profiles of the exposed and PDMS-coated regions. f) Thickness of the oxidized SiN_X surface for Chip-A and Chip-B ICs in the PDMS-coated region after continuous biasing at five and 15V between IDC and PBS. For Chip-B samples, electrical biasing was applied between the M5-IDC structure (negative polarity) and PBS (positive polarity). g-h) Average [OH^-] intensities in the bulk of the SiN_X and SiO_2 passivation layers (averaged from 100 - 200 nm within the layer) in the PDMS-coated region after continuous electrical biasing with 5 or 15 V DC.

mer for packaging implantable ICs. **2)** Long-term biostability. In addition to its optimal biocompatibility, PDMS is one of the most biostable, medically used polymers [68]. In vivo, degradation of other medical grade polymers, e.g., parylene C, has been reported through processes such as cracking [69]. **3)** Long-term underwater adhesion to the IC's surfaces, especially to the nitride passivation. Other polymers like epoxy and polyimide, typically used for IC packaging, have been reported to have weak bonds to IC passivation when exposed to moist environments [70].

For emerging implantable applications incorporating an IC, selecting a CMOS process suitable for chronic implantation requires extensive and long-term testing, often not within the scope of academic research groups. Therefore, we encourage researchers to use the technology nodes evaluated in this work when designing their ICs. In smaller CMOS technology nodes (90 nm and smaller), significant changes have been made in the IC's materials. Most importantly, copper has replaced aluminum metallization to reduce resistance and crosstalk. For the IMD layers, new porous dielectric materials such as silicon oxycarbide (SiOC) have been adopted [60]. Various investigations have reported the instability of these porous dielectrics in the presence of moisture [54]. Therefore, if smaller technology nodes are to be used for implantable applications, accelerated testing in combination with the methodology used in this work can be a valuable tool in evaluating the stability of the IC material.

Accelerated in vitro testing in PBS solution has been extensively investigated as a model to estimate the longevity of novel implantable devices [71, 20, 72]. It has also been shown that in the PDMS-coated regions, elevated temperatures could be used as a model to accelerate moisture penetration and degradation. However, for the exposed bare die regions of the tested ICs, it was found that PBS solution is not an ideal model to mimic the complex in vivo environment as a $\approx$ 20 times higher nitride dissolution rate was observed in the body environment compared to the estimated dissolution rate in PBS solution at 37 °C [73] (assuming an Arrhenius acceleration factor from 37 °C to 67 °C). Higher in vivo dissolution rates for silicon-based dielectrics have been previously reported [36]. In this work, using ToF-SIMS analysis, we compared the chemistry of the first few nanometers (0 - 5 nm) of the dissolving SiN_X layers, revealing slight differences in their chemistry after exposure to different aging media (PBS at 67 °C and rat). All aged ICs created an off-stochiometric oxidized (SiO_X) layer with high [OH^-] on top of the nitride passivation. ICs exposed to PBS solution created a slightly thicker oxidized layer with higher [$SiO_2{}^-$] and lower [OH^-] intensity compared to the ICs exposed to the body. Si-O bonds are thermodynamically more stable than Si-N bonds. Therefore, the created oxidized layer on top of the nitride passivation can act as a protective layer preventing or delaying attack by water molecules [74]. The higher in vivo nitride dissolution rate could be due to the thinner top oxide layer making the Si-N bonds more readily available for attack and dissolution. The theory of nitride dissolution rate relying on the off-stochiometric oxidation reactions has been proposed before [75] and has been experimentally suggested in this investigation. The thinner oxidized layer on the SiN_X passivation in vivo could be due to a similar mechanism observed for the corrosion of titanium metal implants [76], where the body's proteins and enzymes covering the implant inhibit the surface oxidation of the metal, allowing more bulk metal to be available for corrosion.

In this work, the 12-month accelerated aging study found no change in the electrical performance of both metal-shielded and unshielded test structures. For more extended applications, however, we believe using a top shield and extra wall-of-vias (WoV) around the IC may increase the chip's longevity by creating a metal cage around the entire IC structure. These metal barriers could be explored to extend the chip's longevity, especially for implantable ICs fabricated using smaller CMOS technology nodes incorporating porous dielectric layers. In addition, a simplified version of the dielectric sensor used in this study could be employed for implantable ICs fabricated in smaller CMOS technology nodes to detect early moisture ingress.

In the accelerated in vitro study, corrosion of interconnect wire bonds was found to cause failure for some of the devices. Corrosion is believed to be driven by moisture and galvanic reactions between the gold wire bond and aluminum pads, causing the corrosion of the pad [77, 78]. Non-bonded aluminum pads showed no signs of corrosion (Fig.4.21, Supporting Note), mainly due to a native oxide layer on the aluminum, which has been reported to create strong interface adhesion bonds with PDMS [48]. Given PDMS's moisture permeability, dissimilar metals should be avoided in the interconnect regions. For this purpose, we propose using aluminum wire bonds instead of gold as it can prevent galvanic reactions and result in a stronger adhesion between the wire bonds and the PDMS [79].

As demonstrated in this work, the longevity of implantable ICs significantly relies on the passivation layers. Any stress-induced cracking during packaging or post-processing could undermine the protection offered by these layers. Die thinning, for example, has been explored as a technique to enable die-embedded flexible bioelectronicsc[80]. This technique, however, may introduce stress and cracks in the passivation and dielectric layers. Moreover, as the silicon substrate becomes thinner, moisture penetration through this route may need further research. Therefore, as a future investigation, one can investigate how thin the ICs can be made without compromising the barrier properties of the IC's passivation layers and silicon substrate.

The effect of continuous electric fields on the stability of IC materials was investigated by analyzing a group of samples applied to DC bias voltages between the IDC metals and the PBS solution. Using ToF-SIMS analysis, we identified enhanced [OH^-] incorporation in the SiN_X and SiO_2 passivation layers for the ICs exposed to 15 V DC in comparison to unbiased ICs. For lower voltages typically used for implantable ICs (5 V), the applied bias was found to have no long-term effect on the stability of the passivation layers. Based on these insights, for implantable ICs operating at higher voltages (>15 V DC), further investigations may be required to determine the long-term stability of the materials and interfaces.

4.4. CONCLUSION

Ensuring the longevity of the IC in the body will be a key challenge when developing next generation miniaturized active neural implants. The work presented here demonstrated that IC structures can be inherently hermetic likely due to the advanced materials and processes applied by the CMOS foundries. Evaluation results on ICs fabricated by two CMOS foundries demonstrated the excellent moisture and ion barrier properties of the SiN_X/SiO_2 passivation layers, maintaining the IC's electrical functionality for at least a

year, even when exposed to PBS solution as bare die. Exposure of the IC to the physiological environments, however, resulted in the degradation of the IC material, with the most prominent degradation being the dissolution of the nitride passivation. PDMS coating of the ICs, on the other hand, was shown to prevent the observed degradation, making it a promising soft biocompatible encapsulant for multi-year implantations. The authors believe the insights collected in this work are critical to the next step in engineering long-lasting active neural implants.

4.5. Experimental Section

Fabrication of silicon-IC test structures. The main text details the fabricated test structures. Data on the exact technology nodes is available upon request.

Sample preparation and PDMS coating for the long-term accelerated in vitro aging study. All ICs were glued on ceramic (alumina) substrate adaptors with thick-film Pt/Au tracks. The adaptors were soldered to Teflon-coated stainless-steel wires. Subsequently, the ICs were mounted and wire-bonded to the adaptor using 30 μm diameter gold wires. Before wire-bonding, samples were placed in a plasma chamber (RF power 400 W, 80% Argon, 20% Oxygen) for 180 seconds to surface activate the aluminum pads on the IC for optimal wire-bonding. To electrically insulate the metal tracks on the ceramic substrates and the connecting wire bonds, PDMS (DOW CORNING 3140, see Fig.4.14, Supporting Note) was locally applied using a dispenser. For optimal PDMS adhesion, samples were surface activated using UV-ozone for 15 minutes before PDMS coating. PDMS curing was done according to the manufacturer's guidelines. The ceramic adaptors were subsequently connected to bungs. Full details of the sample preparation can be found elsewhere [46, 73]. All samples were fully immersed in phosphate-buffered saline (PBS) solution and aged in a dedicated apparatus [81] (Fig.4.15, Supporting Note). Every three months, samples were taken out, microscopically inspected, and placed back in fresh PBS solution.

Sample preparation and PDMS coating for the long-term in vivo animal study. For animal studies, the chips were placed on 3 mm thick, soft PDMS substrates fabricated from medical-grade silicone rubber (MED2-4213, NuSil, see Fig.4.14, Supporting Note). For manufacturing the PDMS substrates, a custom-made polytetrafluoroethylene (PTFE) mold was filled with uncured PDMS, which was then semi-cured in the oven at 100 °C for 30 minutes. At the same time, for optimal PDMS adhesion, the ICs were surface activated and cleaned using UV-ozone for 15 minutes with their top passivation facing the ozone lamp. The ICs were then placed in the center of the semi-cured PDMS substrates. After positioning, all aluminum pads and parts of the IC passivation were coated using the same medical grade PDMS (MED2-4213, NuSil). Finally, the samples were fully cured in the oven at 100 °C for two hours.

Animals, implantation, and explanation procedures. All experiments were performed per the EC Council Directive of September 22, 2010 (2010/63/EU). All procedures were reviewed and approved by the Animal Care Committee of the Research Centre for Natural Sciences and the National Food Chain Safety Office of Hungary (license number: PE/EA/1253-8/2019). The implantation procedures were carried out as follows. Wistar rats (n=6; weight, 315.5 ± 59.6 g at the initiation of the treatment; 3 females, 3 males) were anesthetized by an intraperitoneal injection of a mixture of ketamine (75mg/kg of body

weight; CP-Ketamin, Produlab Pharma B. V., Raamsdonksveer, The Netherlands) and xylazine (10mg/kg of body weight; CP-Xylazin, Produlab Pharma B. V., Raamsdonksveer, The Netherlands). A body temperature of 37 °C was sustained with an electric heating pad connected to a temperature controller (Supertech, Pécs, Hungary). Before implantation, samples were sterilized by immersing them in isopropyl alcohol for at least 20 min and then washing them with a continuous stream of distilled water for 2 min. To reduce the number of animals used, each animal was subcutaneously implanted with two ICs: Chip-A on the right and Chip-B on the left side of the back close to the neck. The incision was closed using interrupted sutures followed by a standard combined postoperative analgesic regimen. Samples were explanted at three time points: months 3, 7, or 12. Before explantations, rats were initially anesthetized in the same way as described above. After anesthesia induction, the animals were overdosed with isoflurane (5% in 100% oxygen) until breathing stopped. Before explantations, the skin around the implants was examined for any inflammation. After long-term implantation, a tissue pocket was formed around each sample. The samples were removed from the pocket to analyze the tissue pocket. The pocket was immersed in 4% paraformaldehyde solution for 24 hours, then washed in 0.1M PBS and stored in PBS. The tissue samples were then sectioned and stained with hematoxylin and eosin stain, and photomicrographs were taken for tissue analysis. Explanted microchips were carefully rinsed with DI water, blow-dried, and stored in a dried condition for a week before analysis.

Electrical characterization of IDC structures: Electrochemical impedance spectrometry (EIS). EIS was conducted with a Solartron Analytical Modulab XM equipped with a Potentiostat, Frequency Response Analyzer, and a Femtoammeter (Fig.4.15). For low-current measurements, the samples were placed in a dedicated Faraday cage with the shield of the Solartron coaxial cable connected to the cage. Unless stated otherwise, all EIS measurements were performed between the interdigitated combs in a frequency range of 0.01 Hz to 100 KHz using a 100 mV (RMS) sinusoidal voltage drive.

Electrical characterization of transistor structures. The transistor structures were characterized using an HP4145AB parameter analyzer, which monitored the transistor drain-source current (IDS) over a range of gate-source voltages (-0.5 V < VGS < 1.8 V) while having the VDS at 1.8 V DC.

PDMS decapsulation. PDMS decapsulation was performed post-aging to analyze the IC materials protected by the PDMS coating. Decapsulation was done in two steps: 1) gently removing the excess PDMS material using a scalpel without damaging the ICs, and 2) dissolving the remaining PDMS material using a PDMS solvent (DOWSIL™ DS-2025). The first step of removing the excess PDMS on the samples would reduce the required exposure time to the solvent. The samples were, therefore, placed in the solvent for only 30 minutes. Decapsulated ICs were then thoroughly rinsed in acetone, IPA, and DI water, and finally, blown dry. All samples used for surface analysis were prepared similarly.

IC multilayer stack characterization: Scanning electron microscopy (SEM) and energy-dispersive X-ray (EDX). For SEM, samples were coated with a thin (10 - 20 nm) evaporated carbon layer. The carbon-coated samples were investigated in a Thermo Scientific SCIOS2 system with a Pt deposition gun filled with Me3PtCpMe and a Sidewinder gallium liquid metal ion source (LMIS) for focused ion beam (FIB). Before cross-sectioning,

Pt was deposited in situ to develop the cross-sectional images' structure properly. EDX was done with an Oxford Xmax 20 SDD (silicon drift detector). The applied Ga milling parameters were 30 keV and 15-30 nA, depending on the trench dimensions for coarse milling. Later, the cross-section surface was polished with 30 keV, 5 nA.

Surface characterization: Atomic force microscopy (AFM). The Bruker Icon was used in tapping and PeakForce Quantitative Nanomechanics (QNM) mode. After PDMS decapsulation, a 20 μm x 20 μm area on the PDMS-edge (boundary between the PDMS-coated and exposed region) was used for AFM scanning. On the explanted ICs, AFM was used to determine the loss of the SiN_X and SiO_2 passivation layers.

Chemical composition of IC passivation layers pre and post-aging: X-ray photoelectron spectroscopy (XPS) depth profiling. XPS analysis was carried out in a Quantera Hybrid SXMtm from ULVAC-PHI at Eurofins EAG Laboratories, The Netherlands. The measurements were performed using monochromatic AlK-radiation (25 Watt) and a take-off angle 45 °. The information depth during surface measurement is approximately 7 nm at this angle. A spot size of 100 μm in diameter was used for the analyses. First, at the surface, a survey scan was recorded. Subsequently, accurate narrow scans of Si, N, O, C, Al, Na, Cl, and F have been measured for quantification in the depth profiles. Standard sensitivity factors were used to convert peak areas to atomic concentrations. For Chip-A and Chip-B ICs, XPS analysis was done on the M3-IDC and the M5-IDC test structures, respectively, as they contained flat surfaces with no microtopography.

Chemical composition and barrier property of IC passivation layers pre- and post-aging: Time-of-flight mass spectrometry (ToF-SIMS) depth profiling. ToF-SIMS analyses were performed using an ION TOF IV instrument at Eurofins EAG Laboratories, The Netherlands. The instrument was operated in positive and negative mode using 2 keV O2+ and 2 keV Cs+ sputtering ions, respectively. At negative mode, sputtering was carried out using the 2 keV Cs+ primary ion beam to enhance the detection level of the electronegative species [O-], [OH^-], and [H-]. The sputtered area was 250 x 250 μm^2, and the analyzed area was 50 x 50 μm2 centered in the sputtered area. The analysis was done with a beam of 25 keV Bi+ ions. To increase the sensitivity for lighter elements like hydrogen [H-], all samples were stored in the instrument under ultra-high vacuum (< 10^-9 bar) for 64 hours before analysis. The quantification of the hydrogen content (H) in the SiN_X passivation was done in ToF-SIMS software using a relative sensitivity factor (RSF). The RSF was derived from measurement results performed on known SiN:H reference layers. The hydrogen content on these SiN:H reference layers has been previously calibrated using elastic recoil detection (ERD). Like XPS, all ToF-SIMS measurements were performed on the M3-IDC and the M5-IDC test structures for Chip-A and Chip-B, respectively, where the surface of the chip is flat. The depth scale has been calibrated using known SiN_X reference samples and has a measurement error of ≈ 10% (including a possible systematic error due to differences in stoichiometry). Shallow depth profiles (down to ≈ 20 nm) have been measured with 500 eV Cs+ ions for better depth resolution. For analyzing the SiN_X and SiO_2 passivation layers, the selected positive and negative cluster ions have been selected based on existing literature and are given in the main paper. Given the high sensitivity of ToF-SIMS compared to XPS (ppm to ppb for some species vs. 0.1 – 1.0 at. % for XPS), certain elements could be identified but not quantified. For this reason, all data on aged ICs have been compared to the levels measured on

reference (as is from foundry) samples.

4.6. SUPPORTING NOTES

De-bonding of PDMS could affect the electrical measurements during the in vitro accelerated aging study. Fig.4.8 presents the 6 PDMS interface bonds on the test structures. The most critical interface is the PDMS-SiN_X interface bond which is composed of two regions: (1) the region between the IC pads and (2) the region extending to the PDMS edge. Both interface regions are crucial for maintaining a stable electrical performance. The interface at the PDMS edge is directly exposed to phosphate-buffered saline (PBS) solution where interfacial debonding between the PDMS and SiN_X will allow lateral ingress of ionic liquid. All other interfaces are protected from the ionic fluid by PDMS. Nevertheless, due to the moisture permeability of PDMS, these interfaces will be subjected to moisture (gaseous water). At the regions between the IC pads, debonding of the PDMS-SiN interface would allow the condensation of the diffused moisture, resulting in shunt water-leakage paths between the pads. Given the narrow ≈ 100 μm gaps between the pads, PDMS de-bonding in this region will impact the electrical performance.

Supporting note 1: The IDC structures were created either on the top-most metal layer available in each process, i.e. Metal-4 (M4) or Metal-6 (M6), for Chip-A and Chip-B, respectively, or on the metal layer directly below, i.e. Metal-3 (M3) or Metal-5 (M5). For the second case, two variations were included: 1) leaving the top-most metal unused; or, 2) using it to cover the underlying IDC, creating a shield (SH) on top, with the intention that it would act as a metal barrier, further delaying moisture or ion penetration. The shield is not a continuous layer of metal but is a slotted (3 μm x 30 μm and 5 μm x 5 μm slots for Chip-A and B, respectively) to comply with the metal density rules specified by the foundries. In both Chip-A and B, the IDCs were designed to have a relatively large area (700 μm x 600 μm). The gap between the comb metals in the IDCs was 0.6 μm. The larger IDC area would allow a larger area of the IC passivation layers to be evaluated for possible defects. Increasing the area would also increase the capacitance making it large enough to be measurable with the Solartron Modulab at the lowest frequency (0.01 Hz). However, increasing the capacitance value of the IDC test structure would lower the sensitivity threshold of the impedance characterization. Here, the IDC were designed to have a capacitance of ≈ 60 - 70 pF.

Optical microscopy (up to 200x magnification) was done on all devices.

1. For some test structures, samples were taken out at months 3, 6 or 10 for material analysis. 2. All electrical measurements were done monthly until the end of the in vitro accelerated aging. 3. For samples that were analyzed using both SEM and ToF-SIMS/XPS, the SEM analyses was performed after the ToF-SIMS/XPS analysis. 4. ICs were first analyzed using ToF-SIMS, both in positive and negative modes. For quantification, ICs were further analyzed using XPS. During the ToF-SIMS analysis of aged ICs, reference ICs (pristine, as is from foundry) were also used for comparison. 5. In vivo samples were first microscopically inspected, decapsulated and again inspected using microscopy. AFM at the PDMS-edge boundary was used to determine the thickness of the SiN_X/SiO_2 passivation. Later, samples were analyzed using ToF-SIMS and XPS. Finally, the ICs were inspected with SEM.

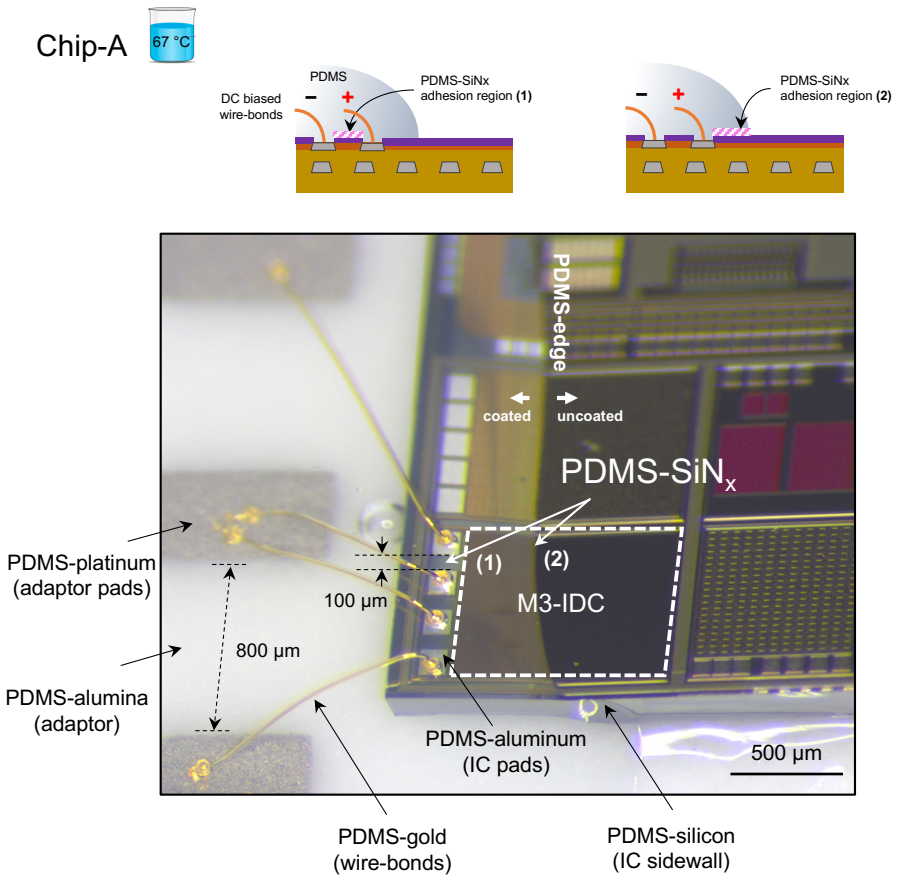


Figure 4.8: A tilted optical micrograph of a representative wire-bonded M3-IDC test structure (Chip-A) used for the accelerated in vitro aging study demonstrating the 6 critical PDMS interface bonds on the test structure.

For this investigation, the key material properties of the two selected PDMS elastomers were: 1) softness (Durometer-A), 2) strong and long-lasting underwater adhesion to silicon-based ceramics, and 3) a low-temperature curing system. The lower temperature curing system minimizes the interfacial stresses created with PDMS. Additionally, the long-lasting adhesion properties were already demonstrated in our prior experiences with these materials.

During the accelerated in vitro aging study, a group of samples showed irregularities in the electrical results. Fig.4.20 gives an overview of these test structures. These samples were taken out from the remainder of the accelerated study and were analyzed using optical and electron microscopy. Results showed failures to be either due to wire-bond corrosion, stress-induce cracks in the passivation or poor conformality of the passivation layer.

In this study, a few number of IDC samples (n=5 out of in total n=56) showed change

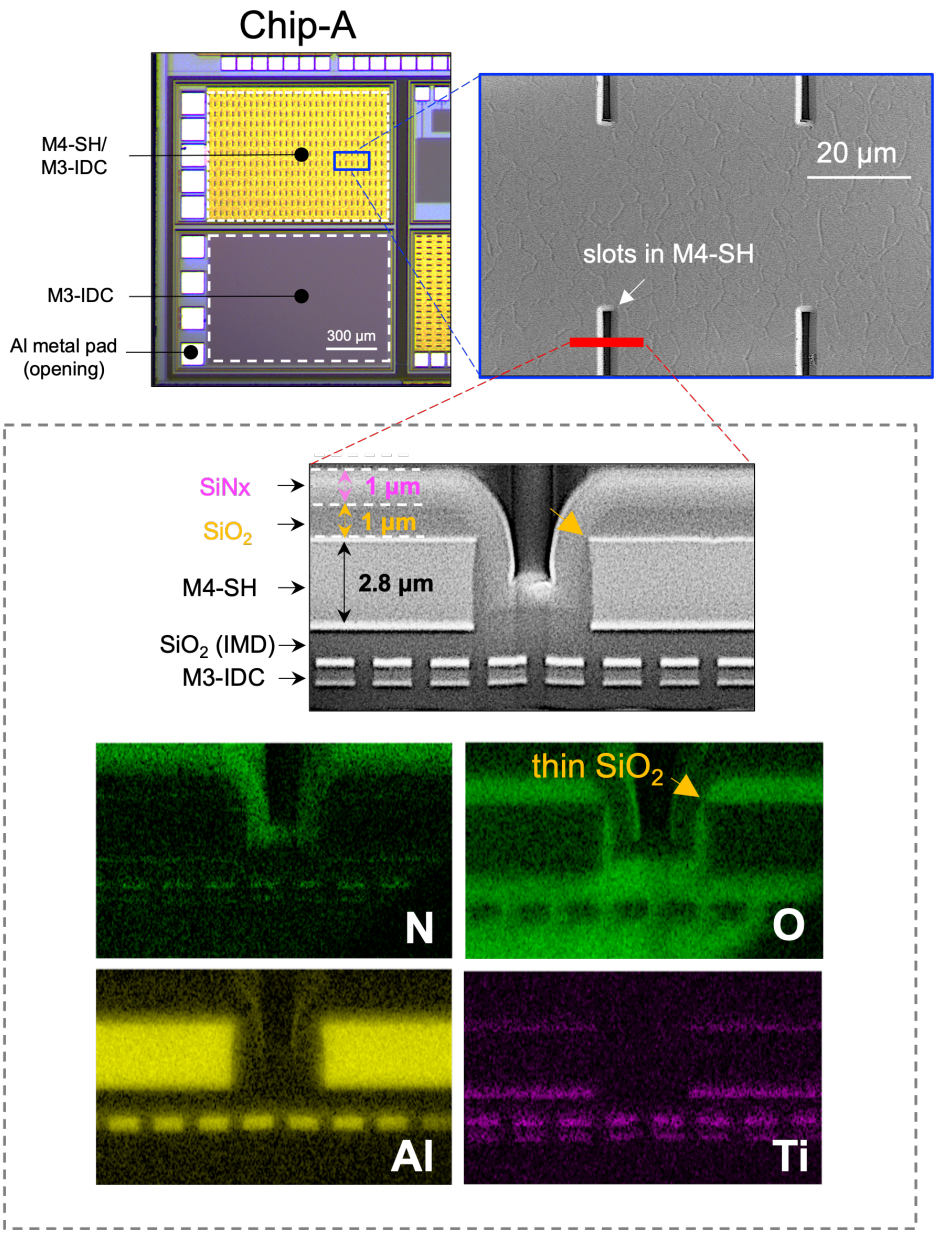


Figure 4.9: Optical and scanning electron microscopy (SEM) micrographs of the M4-SH/M3-IDC (shield layer in Metal-4 and IDC in Metal-3) test structure (Chip-A). Top right SEM depicts the surface microtopography created due to the slots in metal 4 (top metal). Slots are created in the metal layer to obey metal density rules defined by the IC foundry. Red line indicates the focused ion beam (FIB) cut for creating the cross section. SEM micrograph and energy dispersive X-ray (EDX) elemental mapping of the cross-section showing the top material stack of the IC: SiN_X/SiO_2 passivation layers, Metal-4 shield layer, and the M3-IDC structure. The presence of the top metal creates poor conformality in the passivation layers, resulting in a much thinner SiO_2 passivation layer (< 100 nm) on the edges of Metal-4.

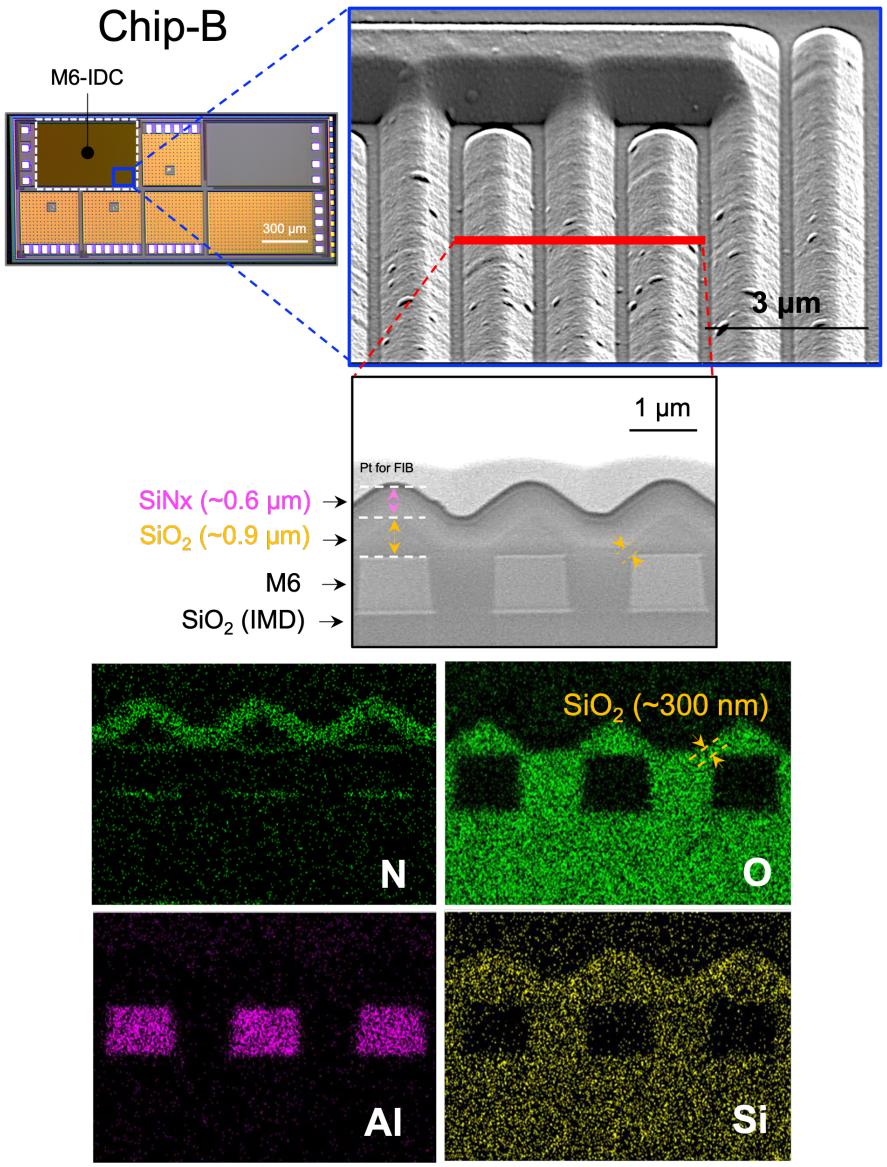
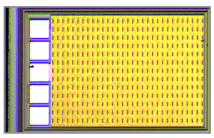


Figure 4.10: Optical and electron micrographs of a M6-IDC test structure (Chip-B). The tilted SEM image shows surface microtopography created due to the use of the top metal layer (M6) for the interdigitated test structure. Red line indicates the FIB cut for cross sectioning. SEM and EDX elemental mapping of the cross-section depicts the top few layers showing the SiN_X and SiO_2 passivation. Due to the presence of the top metallization, poor conformality of the oxide passivation can be observed resulting in a thinner (≈300 nm) SiO_2 passivation on the edges of the metal fingers.

Structure	Image	Design parameters
M3-IDC (1.15 x 0.85 mm)		IDC implemented in Metal 3 Pads in Metal 4 (top metal) Bond pads size: 150 x 150 μm^2 Passivated everywhere except pads Wall of via (WoV) around the whole structure Finger width = 1 µm Finger gap = 0.6 µm Number of fingers = 716 (358 each electrode) Finger length = 844 µm
M4-SH/M3-IDC (0.97 x 0.68 mm)		IDC implemented in Metal 3 Pads in Metal 4 (top metal) Shield implemented using thick Metal 4 (2.8 µm height) Bond pads size: 150 x 150 μm^2 Passivated everywhere except pads WoV around the whole structure Finger width = 1 µm Finger spacing = 0.6 µm Number of fingers = 606 (303 each electrode) Finger length = 664 µm

The two test structures on Chip-A were fabricated adjacent to other circuity intended for a different project which was not used in this investigation.

Figure 4.11: Test structures on Chip-A with specifications.

in EIS results in the frequency range of 10 Hz to 100 KHz. Optical microscopy revealed that these samples experienced wire-bond corrosion which resulted in a high ohmic wire-bond connection to the IDC structure. Closer examination revealed the corrosion to mainly only occur on pads connected to wire-bonds (Fig.4.21). For PDMS-coated wire-bonds, this type of corrosion has been reported before [82, 79] and is most likely due to the galvanic corrosion at the Al-Au interface which is triggered by moisture. The galvanic corrosion results in the degradation of the less noble metal, in this case, aluminum (Al). PDMS-coated aluminum pads without gold (Au) wire bonds, on the other hand, did not exhibit any corrosion on all tested samples during the accelerated study in PBS solution at 67 °C.

Metal pads are openings in the passivation to allow for electrical connections to the chip. Due to the opening, we were concerned if the corrosion of the aluminum pads would allow any liquid ingress, specially from the edges of the pads (the boundary between metal and the passivation). For this purpose, to evaluate the worst-case scenario, during the in vitro accelerated aging, some pads were left uncoated and exposed to PBS solution. Fig.4.22 shows an exposed pad connected to the M4-SH layer. After 10 months severe corrosion. Despite the severe corrosion, cross-section SEM imagining and EDX elemental mapping revealed intact buried Al metallization. The thin titanium nitride (TiN) layer, used as a metal diffusion barrier, is also visible with no signs of corrosion,

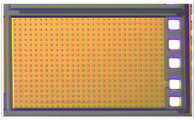
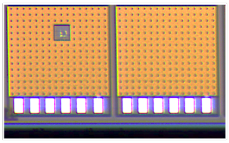
Structure	Circuit layout	Specifications
M5-IDC (1.1 mm x 0.7 mm)		IDC implemented in Metal 5 Pads in Metal 6 Bond pads size: 80 x 80 μm^2 Passivated everywhere except pads Wall of via (WoV) around the whole structure Finger width = 1 µm Finger gap = 0.6 µm Number of fingers = 716 (358 each electrode) Finger length = 700 µm
M6-SH/M5-IDC (0.9 mm x 0.6 mm)		IDC implemented in Metal 5 Pads in Metal 6 Shield implemented using Metal 6 (1 µm height) Bond pads size: 80 x 80 μm^2 Passivated everywhere except pads Wall of via (WoV) around the whole structure Finger width = 1 µm Finger gap = 0.6 µm Number of fingers = 606 (303 each electrode) Finger length = 609 µm
M6-IDC (1.1 mm x 0.7 mm)		IDC implemented in Metal 6 Pads in Metal 6 (top metal) Bond pads size: 80 x 80 μm^2 Passivated everywhere except pads Wall of via (WoV) around the whole structure Finger width = 1 µm Finger gap = 1 µm Number of fingers = 716 (358 each electrode) Finger length = 704 µm
NMOS	**Shielded** 	NMOS transistors, with and without shield. Pads in Metal 6 (top metal) Shield in Metal 5 and 6 (double shielded) Passivated everywhere except pads NMOS total W = 400 µm (W = 20 µm with N = 20 fingers) NMOS L = 0.36 µm Electro static protection used for all pads

Figure 4.12: Test structures on Chip-B with specifications.

Chip	Test structure	Aging	DC bias	Aging duration[1] (month)	Electrical[2]	SEM[3]/ AFM	ToF-SIMS/ XPS[4]
A (n=30)	M3-IDC	PBS @ 67 °C	Unbiased (n=4)	3, 6, 10, 16	EIS	n=4	n=1
			5 V (n=4)	6, 12	EIS	n=2	n=2
			15 V (n=6)	6, 12, 16	EIS	n=3	n=3
		DI @ 67 °C	15 V (n=2)	16	EIS	-	n=1
		rat[5]	Unbiased (n=6)	3, 7, 12	-	n=6	n=3
	M4-SH/ M3-IDC	PBS @ 67 °C	5 V (n=8)	10, 12, 16	EIS	n=2	-
B (n=54)	M5-IDC	PBS @ 67 °C	Unbiased (n=4)	6, 12, 16	EIS	n=2	n=1
			5 V (n=4)	6, 12	EIS	n=2	n=2
			15 V (n=6)	12, 16	EIS	n=2	n=2
		DI @ 67 °C	15 V (n=2)	16	EIS	-	n=1
		rat[5]	Unbiased (n=6)	3, 7, 12	-	n=6	n=3
	M6-IDC	PBS @ 67 °C	Unbiased (n=4)	16	EIS	n=1	-
			5 V (n=6)	12	EIS	n=2	-
			15 V (n=6)	12, 16	EIS	n=2	-
	M6-SH/ M5-IDC	PBS @ 67 °C	15 V (n=4)	12	EIS	n=2	-
	MOS	PBS @ 67 °C	Unbiased (n=4)	12	V_{GS} - I_{DS}	n=2	-
	M6/M5-SH/ MOS	PBS @ 67 °C	Unbiased (n=1)	12	V_{GS} - I_{DS}	-	-
	Dielectric	PBS @ 67 °C	Unbiased (n=1)	5	array measurements	-	-

Figure 4.13: Overview of test structures used in different aging environments and the material analysis tools used for each structure.

	Dow Corning 3140	NuSil MED2-4213
Aging study	Accelerated aging	In vivo anmial
Medical grade	No	Yes
Processing	Dispensing	Dispensing
Cure System	1-part acetoxy	2-part heat addion cure
Mix ratio	-	1:1
Cure time and temperature	3 days @ 25 °C	2 hours @ 100 °C
Adhesive	Yes	Yes
Youngs's modulus (MPa)	0.7	0.6
Tensile strength (MPa)	3	6.9
Durometer shore A	31	15
Uncured viscocity (mPa*s)	34400	80000
Volume resitivity (Ohms*cm)	2.1 x 10^{14}	-
Dielectric strengh kV/mm	15	-

Figure 4.14: Properties of the two PDMS materials used during the long-term aging studies.

demonstrating its high stability in PBS solution at 67 °C. Results indicate no ingress of corrosive liquid into the chip from the pad openings.

Passivation planarity and stress-induced cracks

In the fabrication process of a silicon IC, each metal layer is covered by an insulating layer. For the deep metal layers, i.e. M1-M3 or M1-M5, for Chip-A and Chip-B, respectively, this insulating layer is the SiO_2 interlayer dielectric, and is always followed by a planarization step. When a topmost metal is used, i.e. M4 or M6, for Chip-A and Chip-B, respectively, the IC passivation (PECVD layer of SiO_2 followed by SiN_X) is directly deposited instead with no final planarization step. In this case, no planarization step is performed, and the microtopography of that topmost metal layer will define the planarity of the IC passivation (Fig.4.9 and Fig.4.10). A non-planar passivation layer may experience stress at high-aspect ratio features that can result in cracks. Such stress-induced cracking would greatly compromise the barrier properties of the passivation and allow water/ion ingress points within the IC. In our study, such stress was shown to be a source of failure in test structures where the topmost metal was included in the IDC design. In

Figures Fig.4.23 and Fig.4.24 depict the observed passivation cracking and subsequent metal corrosion which was introduced or accelerated while biasing the topmost metal, both for Chip-A and B. All the IDC structures that did not use top metal did not show similar failures, as was demonstrated.

Utilizing the top-most metal results in microtopography on the IC surface. Fig.4.23 shows the M4-SH/M3-IDC test structure on two different Chip-A samples after accelerated in vitro testing. On these test structures, the presence of slots in the top shield (M4-SH) metal layer creates microtopography on the IC's surface. Such microtopography may lead to poor conformality and stress in the IC's passivation layers, gradually exposing the IDC metals to PBS solution. When applied to a DC electrical voltage, severe degradation is observed as a result of water electrolysis and gas evolution (H_2 and O_2).

All tissue samples were stained with hematoxylin and eosin to visualize the cell nuclei and the cytoplasm. Qualitative analysis of the stained samples showed mature fibrotic tissue with mast cell infiltration in 12-month implants, whereas less mature, more cellular tissue was seen in the case of 7-month-old implants for both PDMS and silicon-IC implants. Results showed no inflammation or tissue damage after 1-year of subdermal implantation of two CMOS foundry ICs in rats. These results are despite the observed SiN_X dissolution observed for both ICs foundries which suggest the biocompatibility of CMOS ICs after long-term implantation.

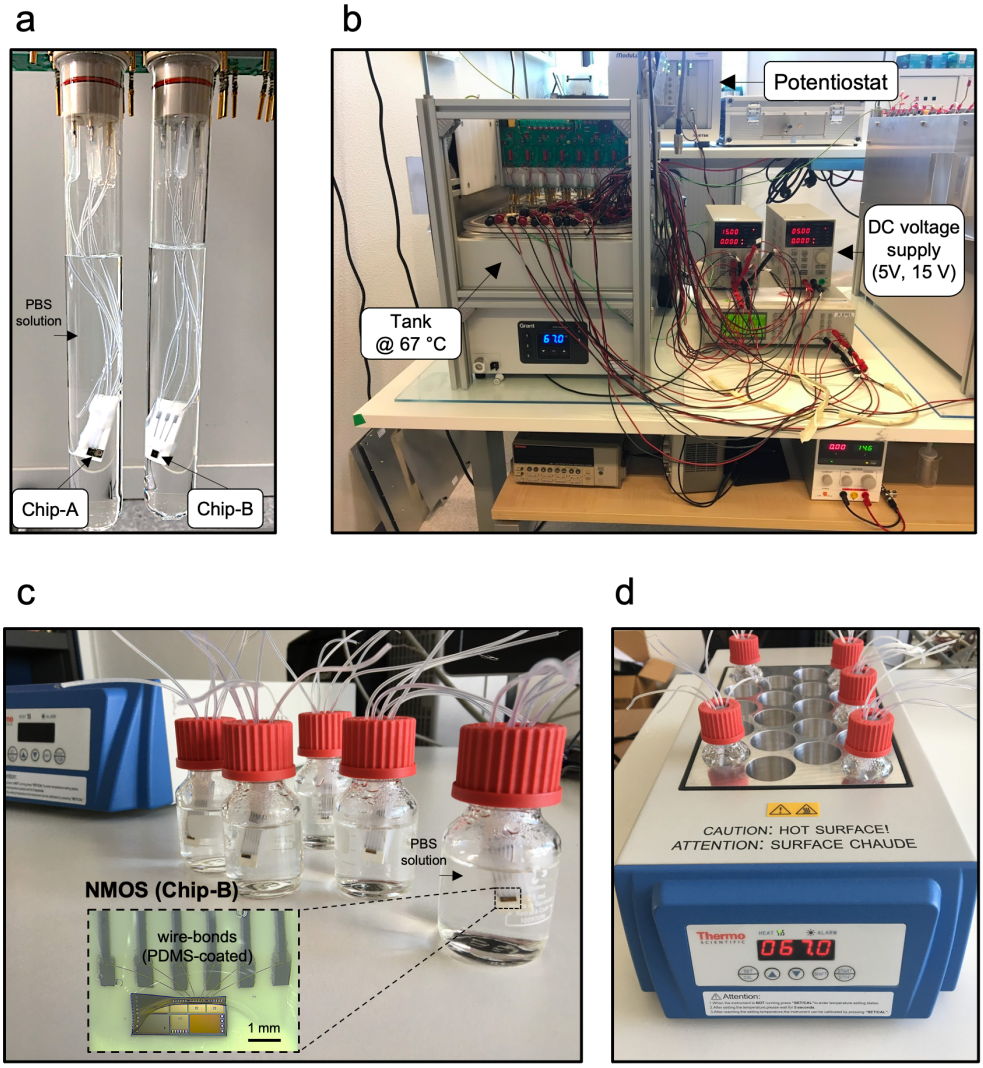


Figure 4.15: Set-ups used for the accelerated in vitro aging studies. a-b) Set-up used for aging the interdigitated capacitor (IDC) structures. a) Chip-A and B ICs connected to 3-contact ceramic (alumina) adaptors while immersed in vials filled with 50 ml of phosphate buffered saline (PBS) solution. b) Heat-regulated water-bath tank and voltage supplies (5 V and 15 V DC) used for accelerated aging and electrical stressing of IDC test structures. Potentiostat used for electrochemical impedance spectroscopy (EIS). c) N-channel metal oxide semiconductor (NMOS) transistors (Chip-B) wire-bonded to 6-contact ceramic substrates (inset), partially PDMS-coated and immersed in PBS solution, d) heater used to maintain a constant temperature at 67 °C.

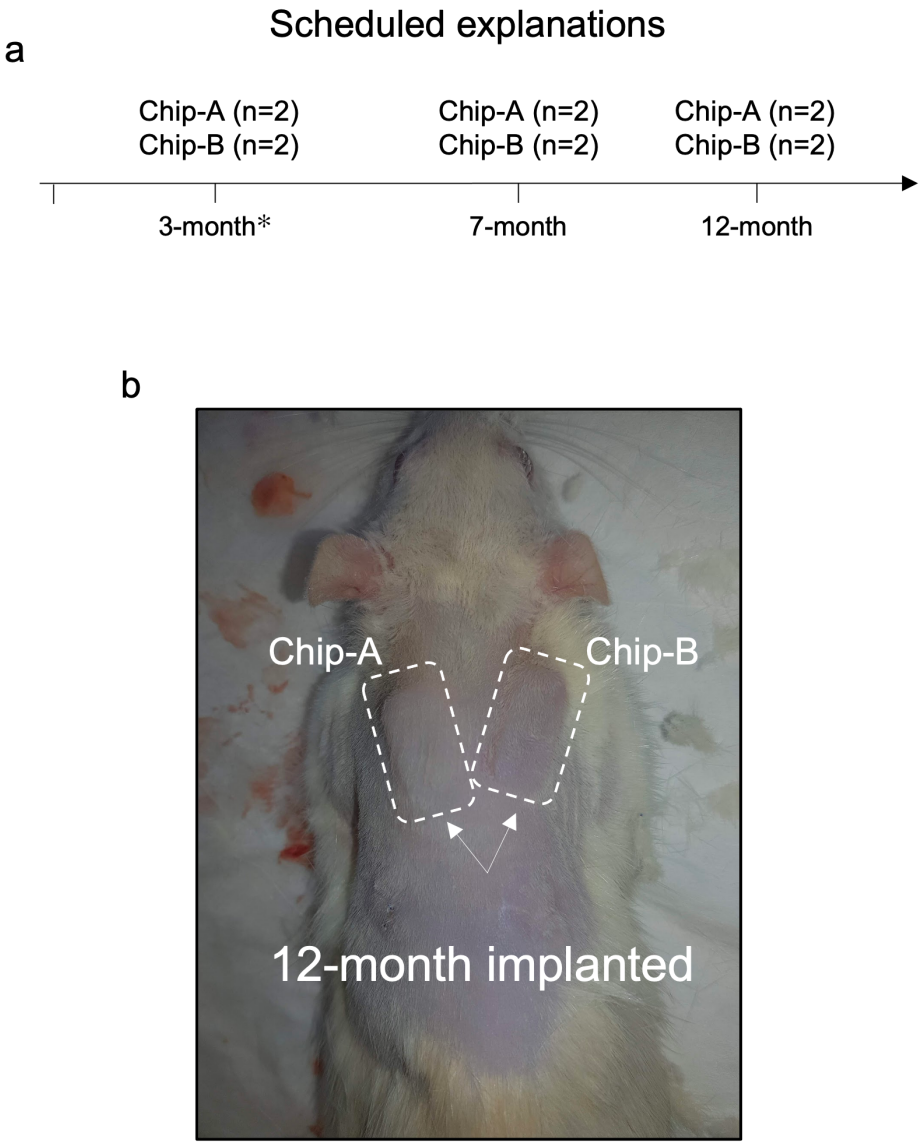


Figure 4.16: a) Explantations for the implanted Chip-A and B ICs in rats. b) image of a rat animal model after 12 months of implantation with complete wound healing and no observable inflammation around the two implanted chips. (One animal died during the study due and was incinerated with the device still implanted.)

Chip A	Measured Depth (nm)	Si (at%)	N (at%)	O (at%)	C (at%)
SiNx	0[a]	29.9	7.9	39.8	21.8[b]
	5	49.7	45.5	4.8	0
	10	51.5	48.5	0	0
	14	50.6	49.4	0	0
SiO_2	1050	33	0	67	0
Chip B	**Measured Depth (nm)**	**Si (at%)**	**N (at%)**	**O (at%)**	**C (at%)**
SiNx	0[a]	26.7	10.8	36.1	26.3
	5	49.6	47	3.5	0.1
	10	49.4	49.3	1.3	0
	14	49.0	51	0	0
SiO_2	1100	32.7	0	67.3	0

[a] For XPS surface measurement, the information depth is approximately 7 nm.
[b] The carbon detected on the surface is from ambient environment (adventitious carbon).

Figure 4.17: Chemical composition of the SiN_X and SiO_2 passivation layers for Chip-A and B ICs (as is from foundry), determined using XPS surface and depth profiling analysis. The measured carbon (C) is from surface contamination and is generally found at the surface of samples exposed to ambient air. After 1 sputter cycle the carbon contamination is removed.

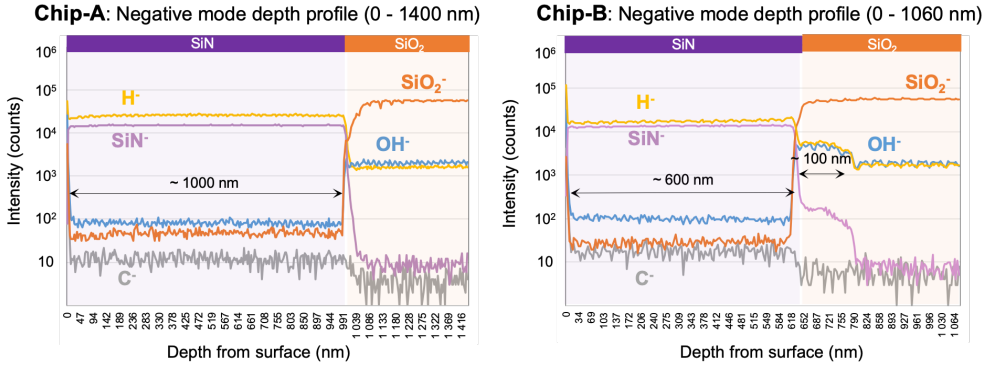


Figure 4.18: Negative mode ToF-SIMS depth profiles of Chip-A (right) and Chip-B (left) ICs (as is from foundry).

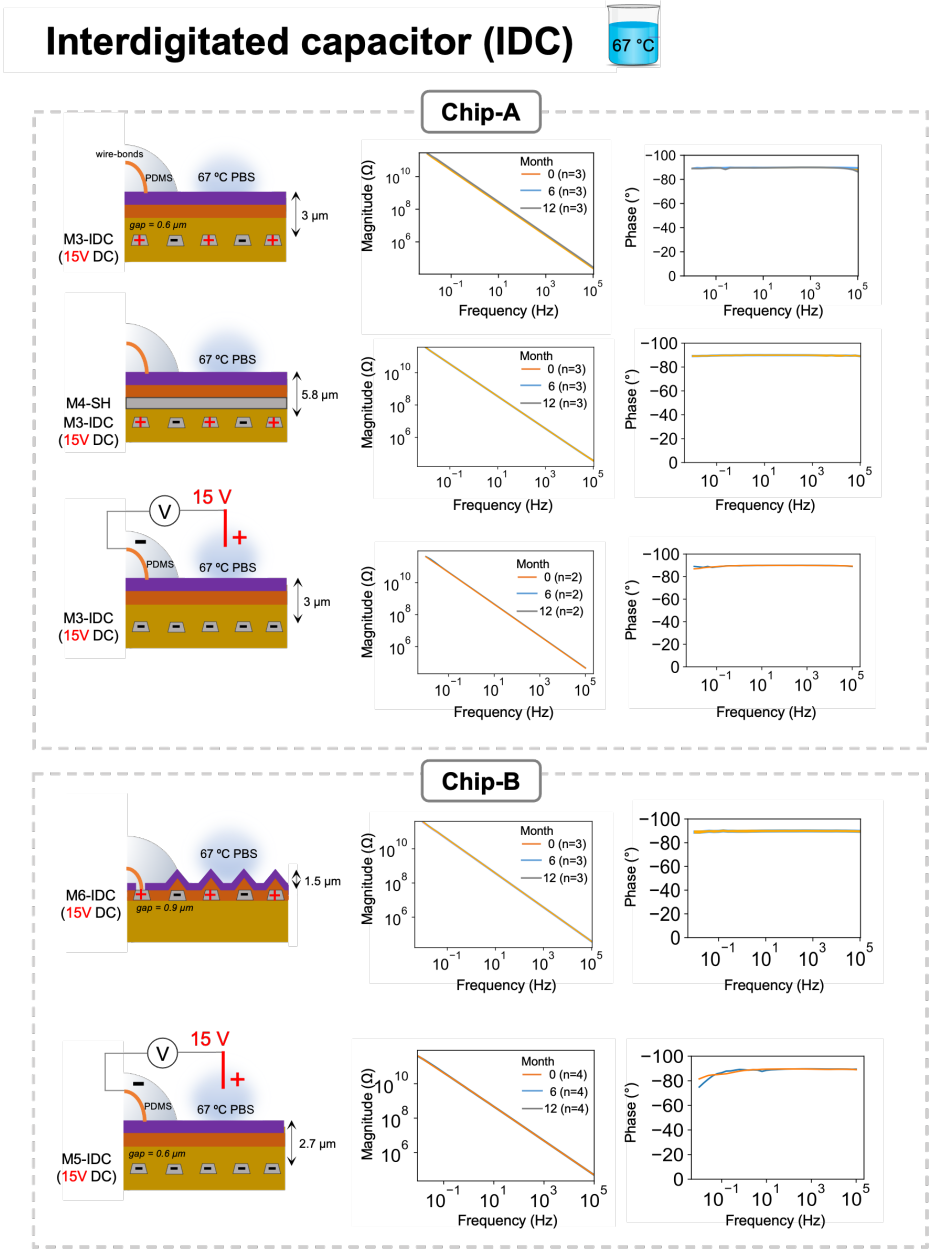


Figure 4.19: Electrochemical impedance spectroscopy (EIS) results of interdigitated capacitor (IDC) test structures on Chip-A and Chip-B ICs over the 12-month accelerated in vitro aging in PBS solution at 67 °C. Schematics show the distance between the test structures and the surface of the IC which is exposed to PBS solution (dimensions not to scale).

Electrical failures 

Chip	Test structure	Aging	DC bias	Duration in test (months)	Time to failure	Failure
A	M3-IDC	PBS @ 67 °C	unbiased	6, 10, 12, 16 (n=4)	7-month (n=1)	Wire-bond corrosion
			5 V	12 (n=4)		
			15 V	12, 16 (n=6)	3-month (n=1)	Wire-bond corrosion
		DI @ 67 °C	15 V	16 (n=2)	5-month (n=1)	Wire-bond corrosion
		rat	Unbiased	3,7,12 (n=6)	-	-
	M4-SH/ M3-IDC	PBS @ 67 °C	5 V	10, 12 (n=8)	7-month (n=3) 5-month (n=1)	Passivation Wire-bond corrosion
B	M5-IDC	PBS @ 67 °C	unbiased	6, 12, 16 (n=4)		
			5 V	12 (n=4)		
			15 V	12, 16 (n=6)		
		DI @ 67 °C	15 V	16 (n=2)		
		rat	unbiased	3,7,12 (n=6)	-	-
	M6-IDC	PBS @ 67 °C	unbiased	16 (n=4)	3-month (n=2)	Passivation crack
			5 V	12 (n=6)	1-month (n=1) 3-month (n=1)	Passivation crack
			15 V	12, 16 (n=6)	1-month (n=2)	Passivation crack
	M6-SH/ M5-IDC	PBS @ 67 °C	15 V	12 (n=4)	10-month (n=1)	Wire-bond corrosion
	MOS	PBS @ 67 °C	unbiased	12 (n=4)	-	-
	M6-M5-SH/ MOS	PBS @ 67 °C	unbiased	12 (n=1)	-	-
	Dielectric	PBS @ 67 °C	unbiased	5 (n=1)	5-month (n=1)	Wire-bond corrosion

Figure 4.20: Electrochemical impedance spectroscopy (EIS) results of interdigitated capacitor (IDC) test structures on Chip-A and Chip-B ICs over the 12-month accelerated in vitro aging in PBS solution at 67 °C. Schematics show the distance between the test structures and the surface of the IC which is exposed to PBS solution (dimensions not to scale).

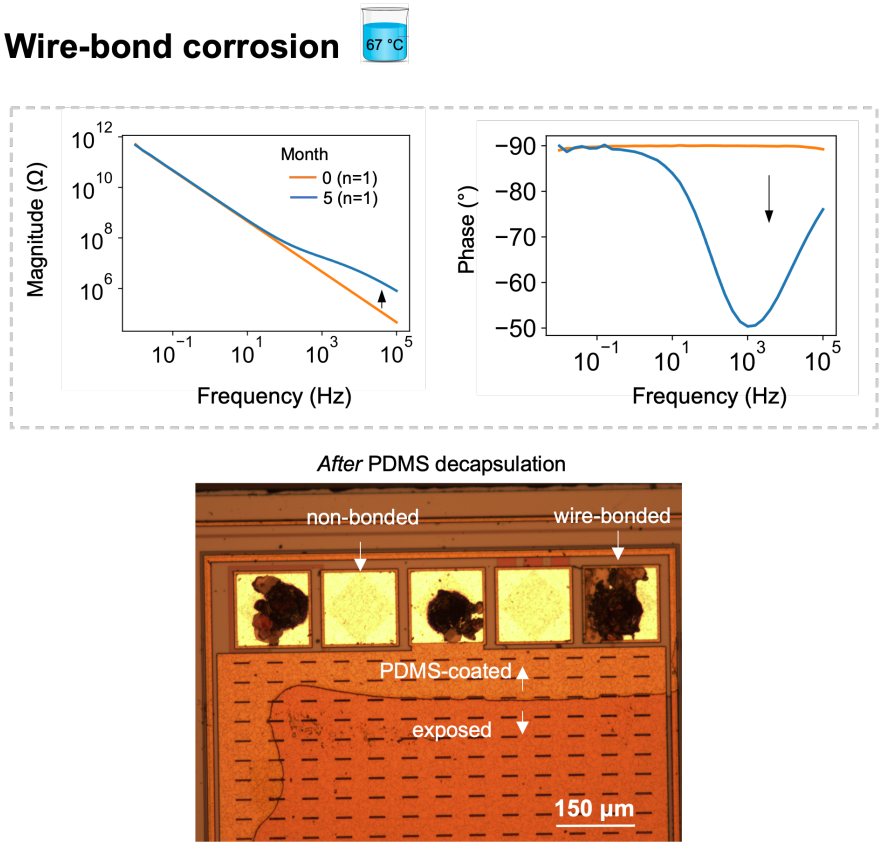


Figure 4.21: EIS results and optical micrographs of sample with wire-bond corrosion in the PDMS-coated region after 4-months of soaking in PBS solution at 67 °C. EIS results presented as Bode plots for a M4-SH/M3-IDC test structure (Chip-A) at 5-month show change in higher frequency ranges. An optical micrograph of the structure after PDMS decapsulation shows aluminum corrosion on the wire-bonded pads. No corrosion is seen for the non-bonded pads.

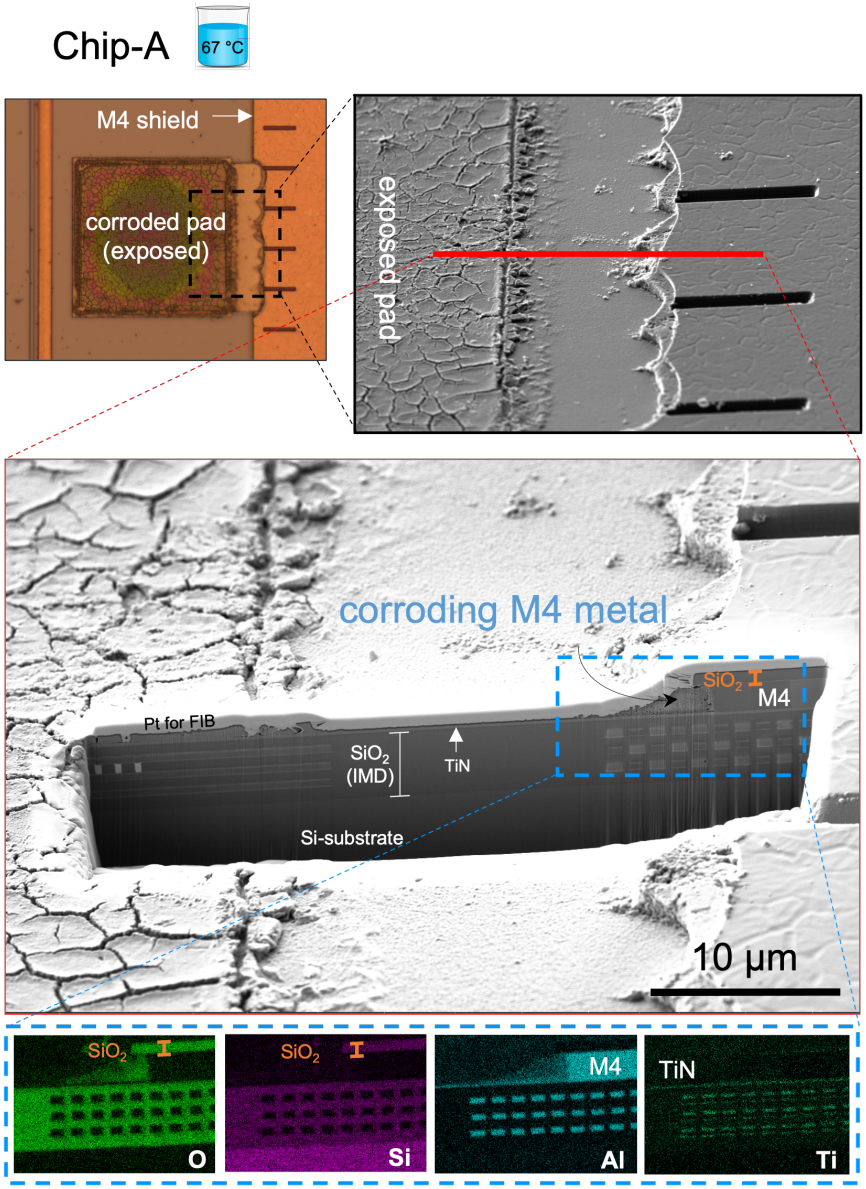


Figure 4.22: Optical and electron micrographs and EDX elemental mapping of an exposed aluminum pad connected to top metal shield (M4-SH) on a Chip-A sample after 10 months immersion in PBS solution at 67 °C. Red line indicates the FIB cut for cross-section analysis.

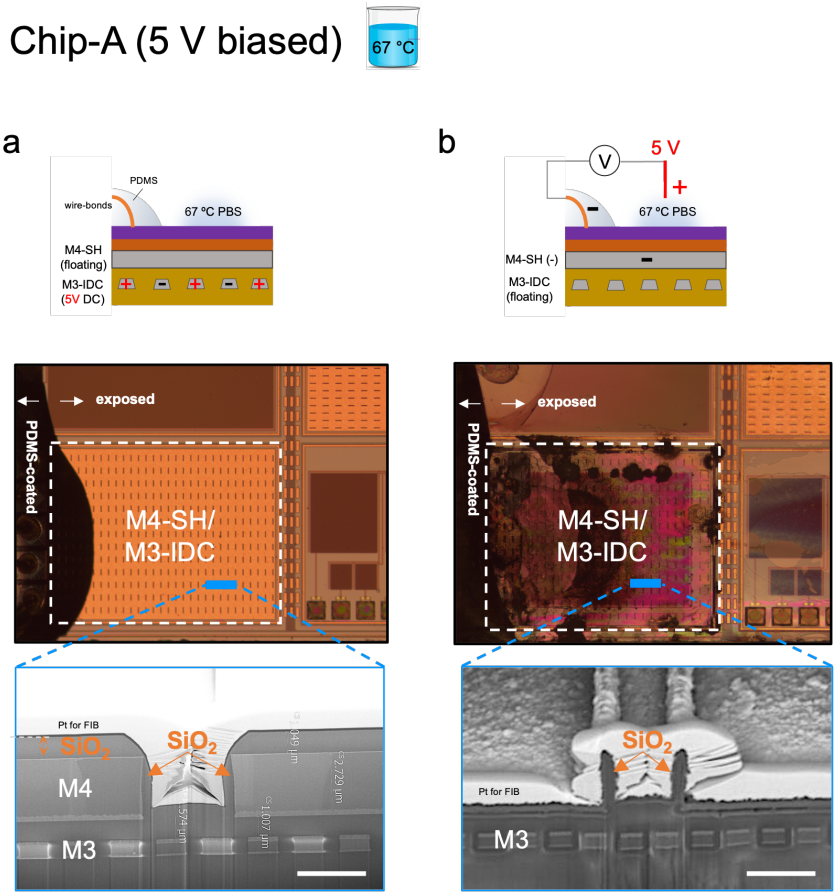


Figure 4.23: Optical micrograph and cross-sectional SEM images of two M4-SH/M3-IDC test structures (Chip-A) after accelerated in vitro testing with biasing. a) Optical micrograph of a sample after 10 months of accelerated aging at 67 °C with a continuous 5 V bias applied between the combs of the M3-IDC. M4-SH was not biased and was left floating. Blue line indicates FIB cut for cross-section analysis. Cross-sectional SEM image showing the total dissolution of the SiN_X passivation after 10 months of soaking, nearly exposing the edges of the M4 metal to the PBS solution. b) Optical micrograph of a different sample with a similar test structure. After 9 months of 5 V DC bias between the M4-SH metal and PBS solution, severe degradation is visible. Cross-sectional SEM image of the damaged area shows complete loss of both passivation layers (SiN_X and SiO_2) and the M4-SH (2.8 μm) metal layer, leaving only the SiO_2 edge side walls. The M3-IDC and other buried material stacks remained intact despite the aggressive electrolysis due to the DC biasing (scale bar is 3 μm).

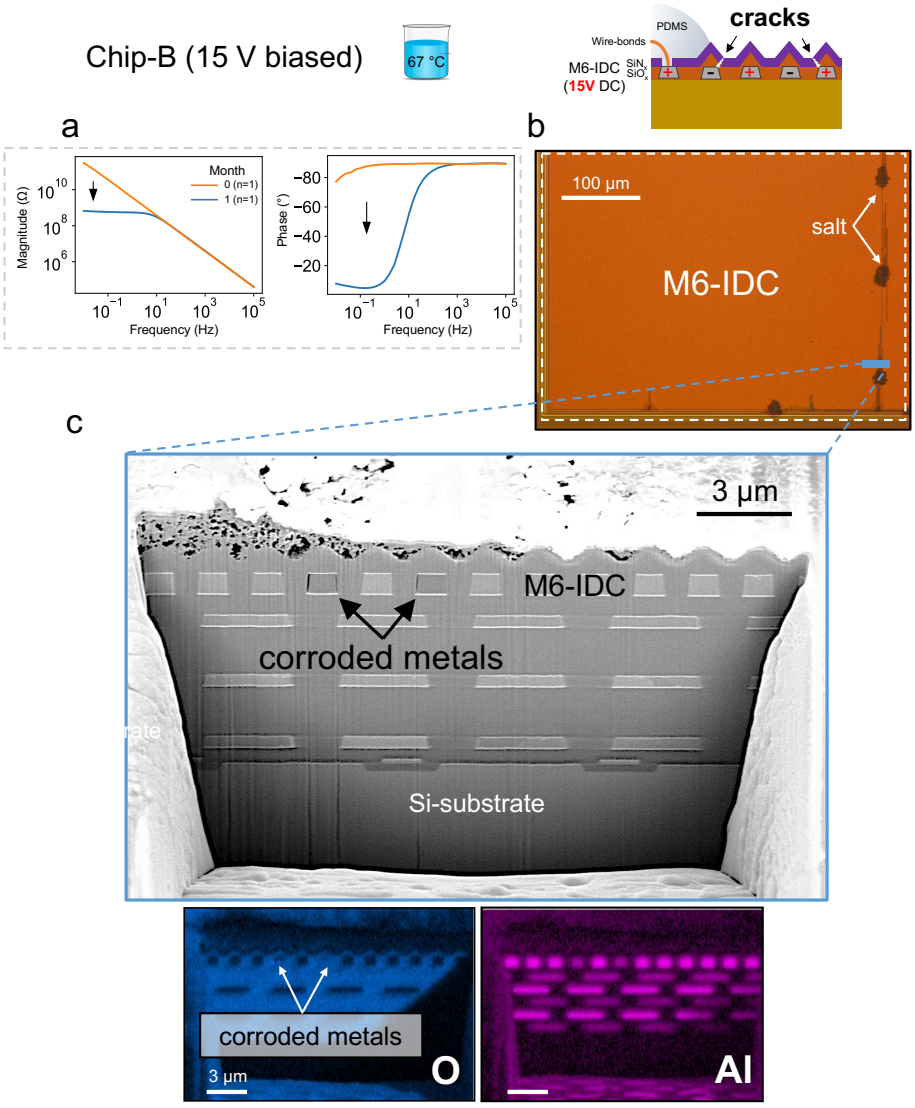


Figure 4.24: Failure on biased M6-IDC test structure. a) EIS results are given as Bode plots for a representative M6-IDC (Chip-B) structure showing EIS irregularities after being applied to a 15 V DC bias voltage for 1-month. EIS results at 1 month show a significant drop in magnitude with more resistive behavior (phase ≈ -20) at frequencies below 10 Hz. b) Optical micrograph of the representative M6-IDC structure with noticeable metal corrosion and salt residue on the corroded sites. Blue line indicates the FIB cut used for cross-section analysis. c) Cross-sectional SEM image and EDX elemental mapping showing higher oxygen content for the corroded aluminum fingers.

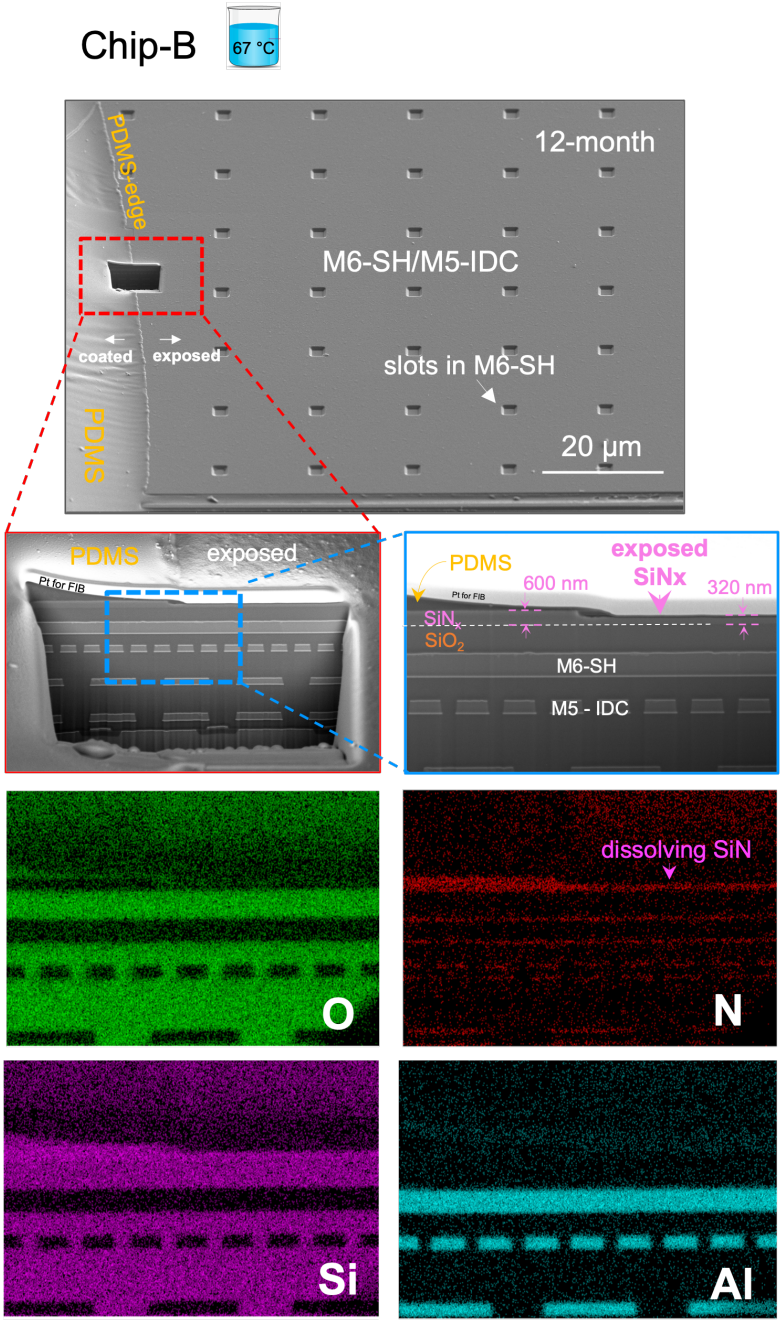


Figure 4.25: Tilted SEM surface image of a M6-SH/M5-IDC structure (Chip-B) after 12 months accelerated aging in PBS solution at 67 °C. Slots in M6 barrier result in microtopography on the IC surface. Slots are created to obey the metal density rules specified by the IC foundry. FIB cut (red square) on the PDMS-edge is used to evaluate the IC multilayer stack stability. Magnified SEM images and EDX elemental mapping of the cross-section reveal a dissolution of the SiN_X passivation in the exposed area, leaving 320 nm of SiN_X in the exposed region of the IC. This results in a dissolution rate of ≈ 22 nm/month for the SiN_X on Chip-B in PBS solution at 67 °C. The PDMS-coated area appears intact (≈ 600 nm).

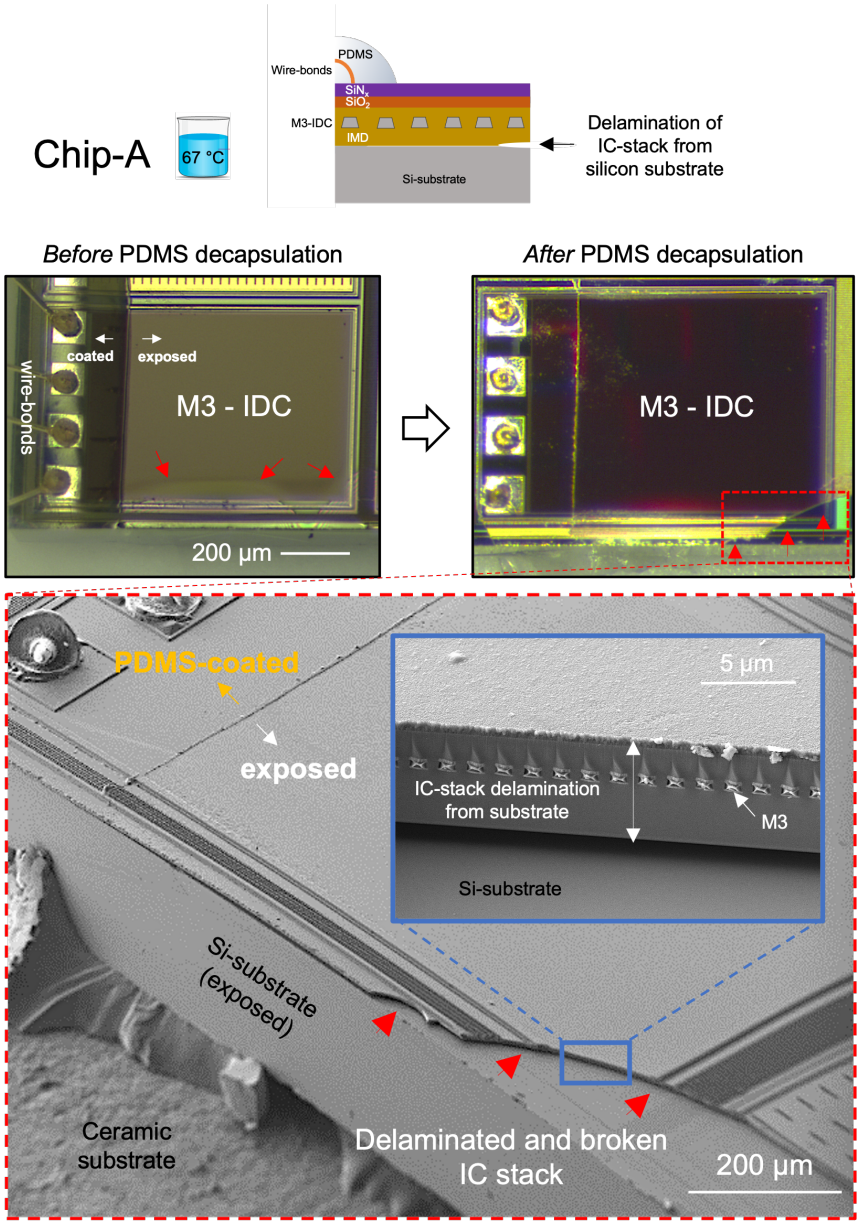


Figure 4.26: Tilted optical and electron micrographs of a M3-IDC test structure (Chip-A) showing delamination of IC-stack from silicon substrate after 16 months aging in PBS solution at 67 °C. In optical micrographs, delamination is seen as color fringes on the IC edge near the sidewall in the uncoated region, shown with red arrows (left). After PDMS decapsulation, a section of the delaminated area broke off due to handling, shown in red dashed square (right). Tilted SEM image of the chip sidewall after PDMS decapsulation (bottom). Inset: magnified SEM image from the broken area where delamination of the entire IC stack from the Si-substrate is visible. The metallization used for the M3-IDC test structure is also visible.

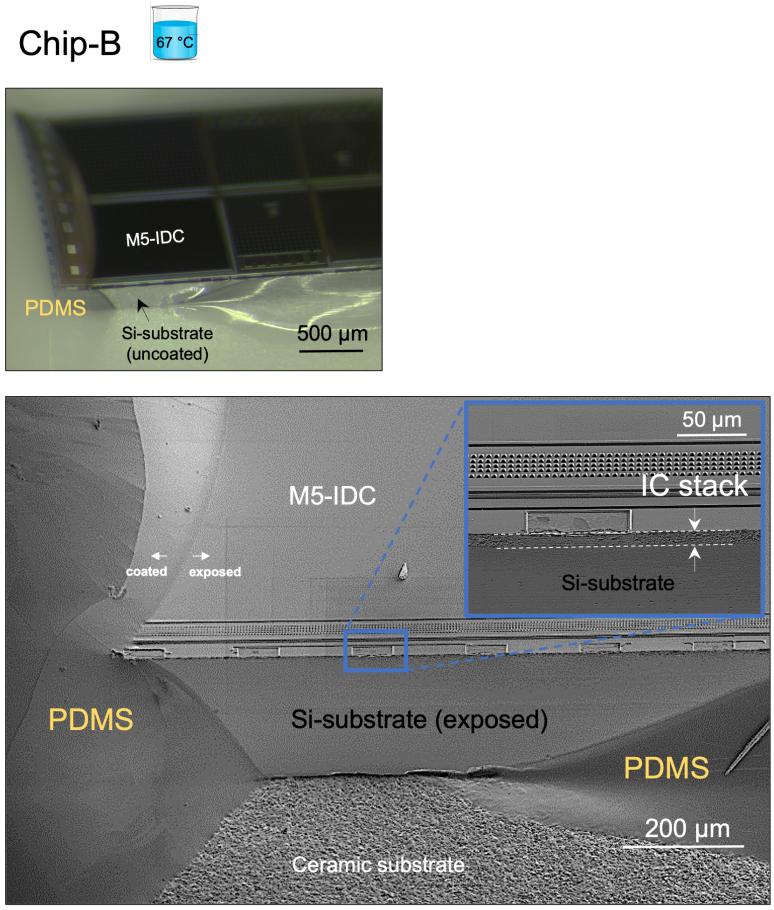


Figure 4.27: Tilted optical and electron micrograph of a M5-IDC test structure (Chip-B) after 16 months of accelerated aging in 67 °C PBS solution showing no delamination on the chip side wall in the exposed region. Inset: magnified electron image where no delamination is observed between the IC stack (≈ 9 μm) and the Si-substrate.

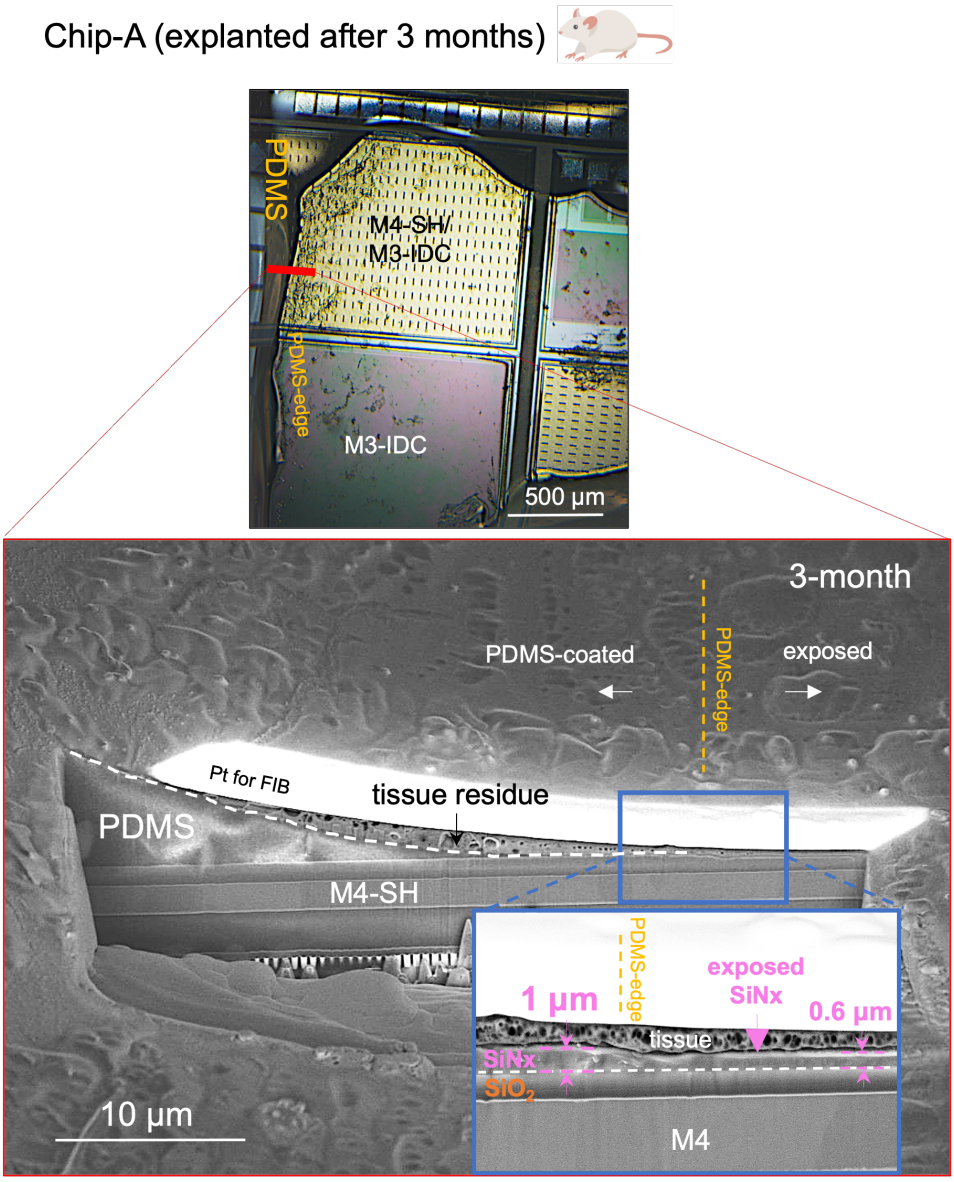


Figure 4.28: Optical micrograph of a Chip-A sample explanted after 3 months in rat, before tissue removal (top). Red line indicates FIB cut used for cross-section analysis. Cross-sectional SEM image near the PDMS-edge of the M4-SH/M3-IDC test structure showing the IC material stack (bottom). Inset: magnified SEM image of the cross-section near the PDMS-edge, comparing the top SiN_X and SiO_2 passivation layers in the PDMS-coated and exposed (uncoated) regions. Dissolution of the SiN_X passivation in the exposed region is visible, while no dissolution is observed in the PDMS-coated region. The thickness of the PDMS coating near the PDMS-edge is much less than 1 μm. At this region, the thin PDMS is still preventing the SiN_X passivation from tissue contact and dissolution. The remaining IC material stack (IMD and metallization) show no signs of delamination or degradation and remain intact.

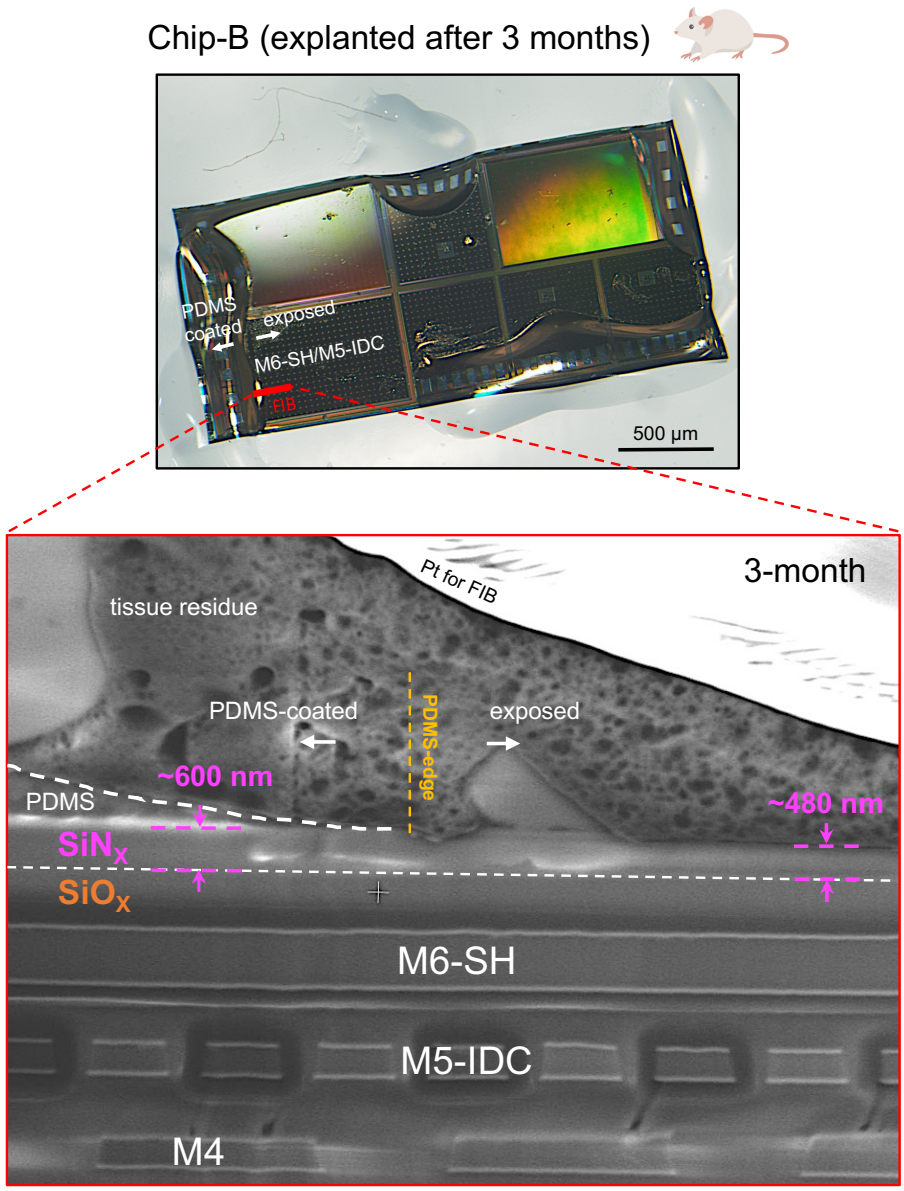


Figure 4.29: Optical micrograph of an explanted Chip-B sample after 3 months exposure to body environment (before tissue removal). Red line indicates FIB cut used for cross-section analysis. SEM cross-sectional image on the PDMS-edge of M6-SH/M5-IDC test structure show visible dissolution of SiN_X passivation in the uncoated region. The remaining IC material stack (IMD and metallization) show no signs of delamination or degradation and remains intact. Note that the thickness of the PDMS coating near the PDMS-edge is less than 1 μm and is still protecting the SiN_X passivation from tissue contact and dissolution.

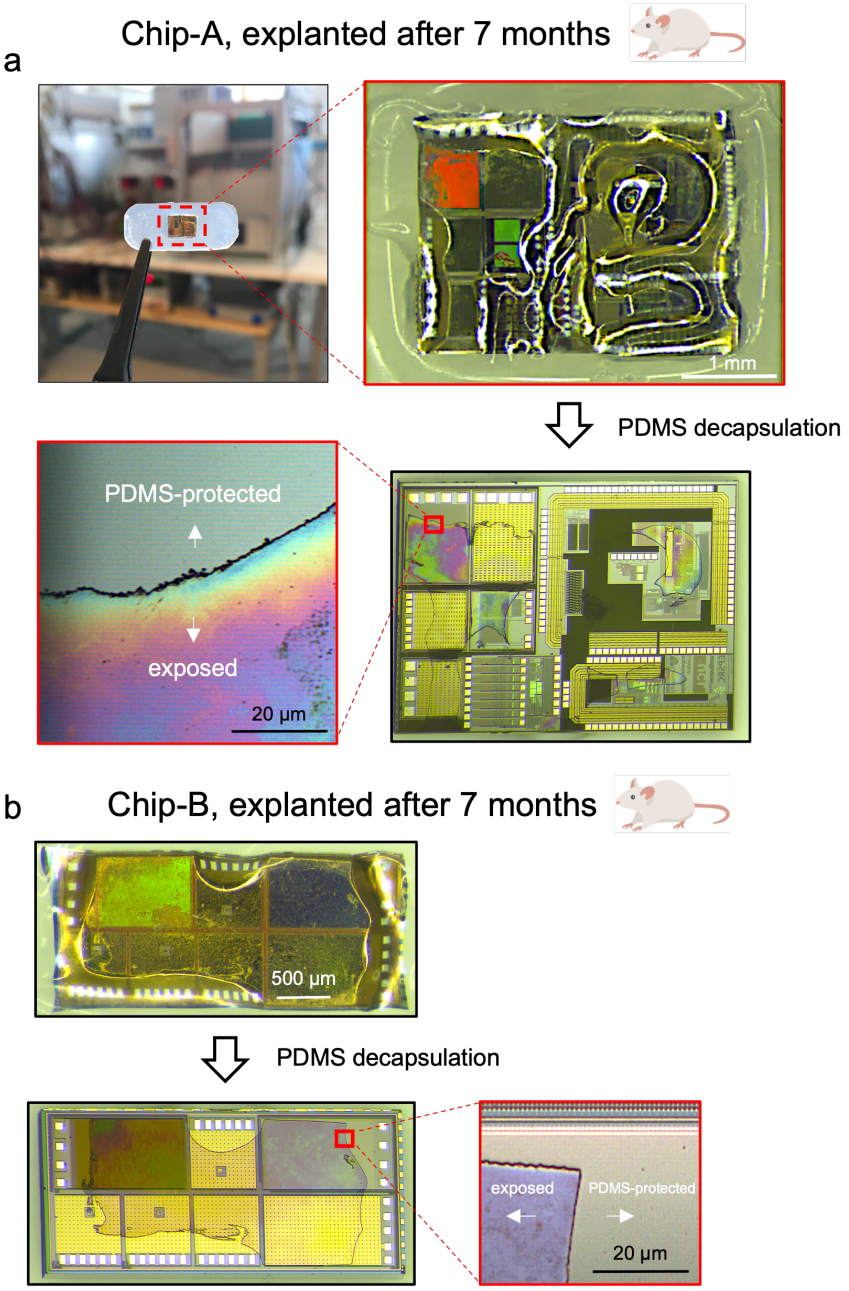


Figure 4.30: Representative optical micrographs of 7-month explanted chips, before and after PDMS decapsulation. a) optical microscopic image of a Chip-A sample after 7 months of implantation in rat. A noticeable color difference is observed between the PDMS-coated and exposed regions which is due to the in vivo degradation of the IC's SiN_X passivation. b) Optical micrograph of a Chip-B sample explanted after 7 months. Note that for both Chip-A and B ICs, the PDMS-coated aluminum pads remained intact.

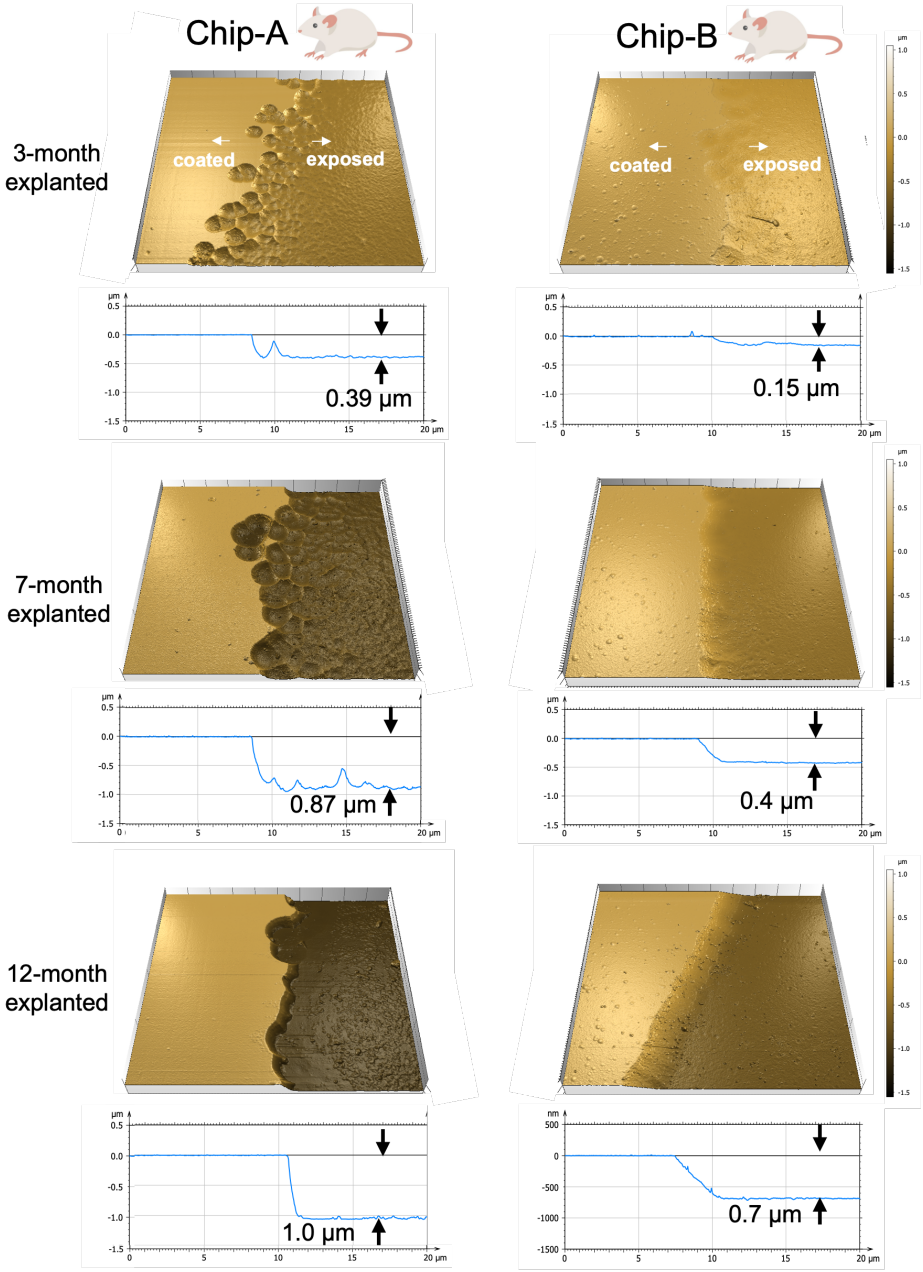


Figure 4.31: AFM surface topography of explanted ICs analyzed on a 20 μm × 20 μm area at the PDMS-edge after PDMS decapsulation. Chip-A and Chip-B ICs explanted at different time points showing gradual dissolution of the SiN_X layer in vivo.

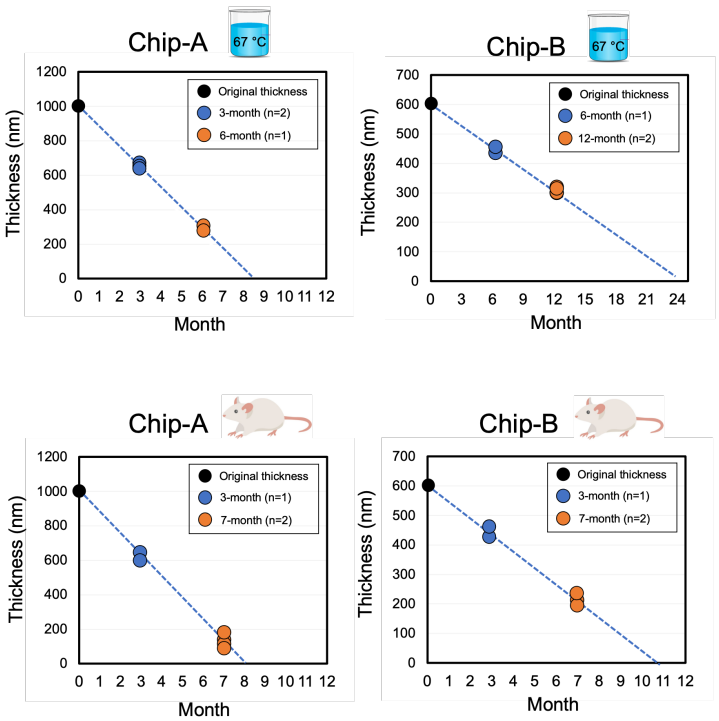


Figure 4.32: In vitro and in vivo SiN_X passivation loss over time for Chip-A and B ICs. For each sample, two measurements were done at different locations. Extrapolated line (blue dashed line) shows the expected time points where the entire SiN_X passivation will have dissolved.

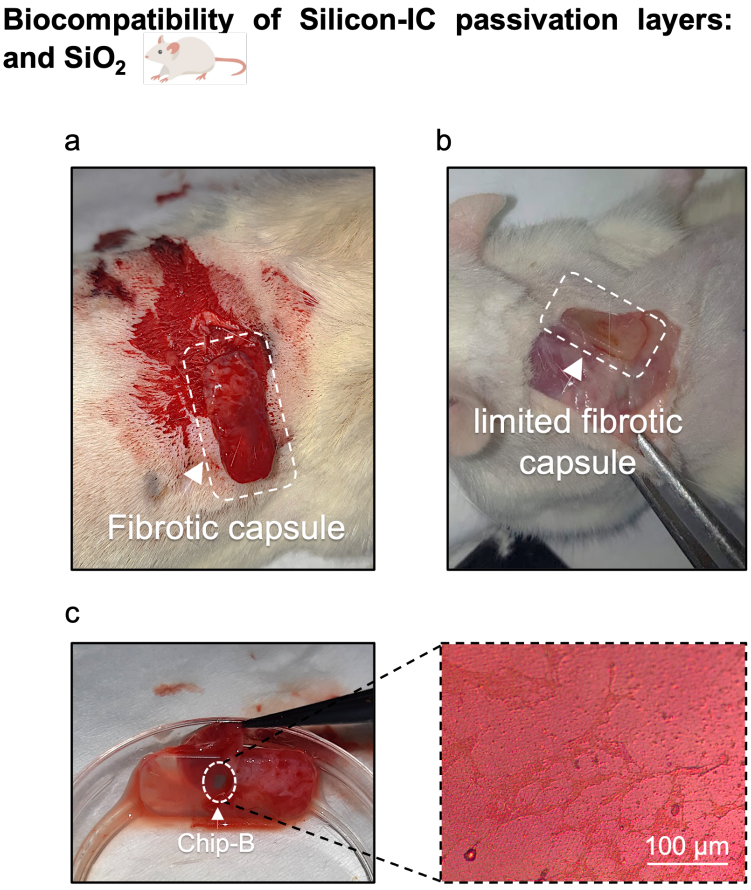


Figure 4.33: Images of explanted ICs. a) Tissue pocket formation around an implanted sample (Chip-A) after three months of implantation. b) Explanted sample with limited tissue pocket formation around the samples after 7 months of implantation where the PDMS substrate is clearly visible. c) Easy tissue pocket removal from a 7-month explanted Chip-B IC showing no tissue adhesion to the IC passivation surface or the surrounding PDMS. Optical micrograph of the passivation surface showing fibroblasts covering the SiN_X (left).

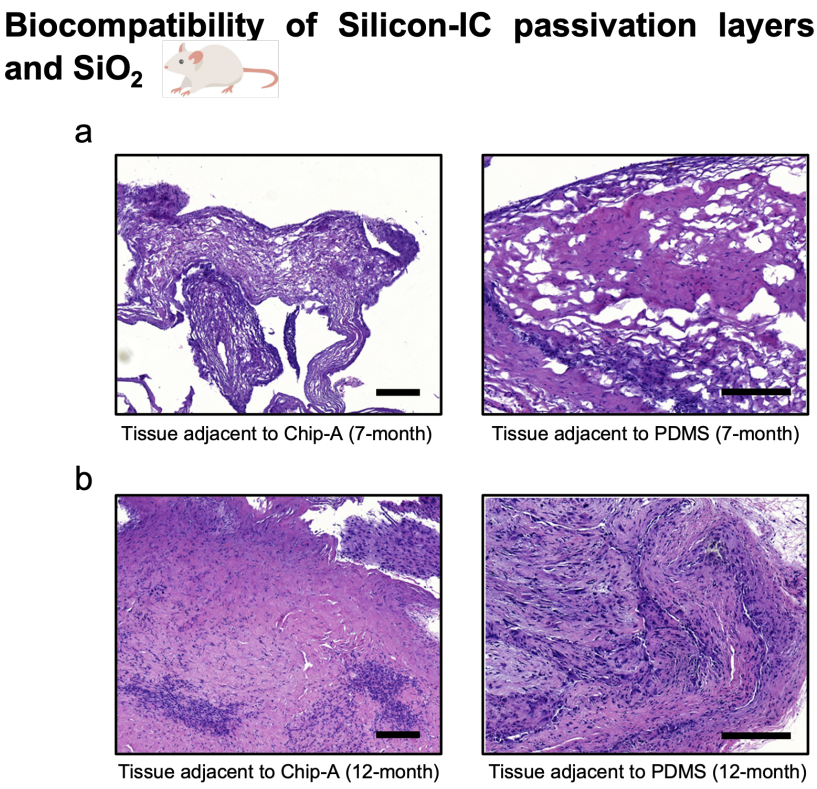


Figure 4.34: Histology images comparing the hematoxylin and eosin (HE) stained tissues adjacent to the silicon-IC (Chip-A) and PDMS substrate (used as control). a) Histology of a 7-month explanted Chip-A. At 7 months, the surface of the IC is SiN_X. b) Histology of a 12-month explanted Chip-A. For Chip-A, at month 12, the SiO_2 passivation is exposed to tissue for approximately 4 months. Scale bar in all images, 200 μm.

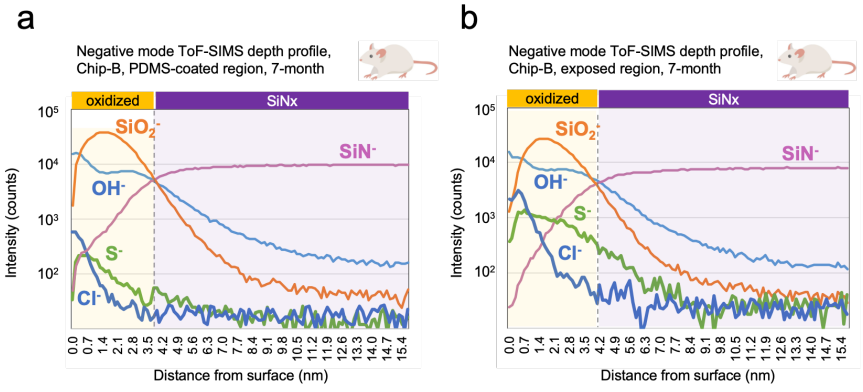
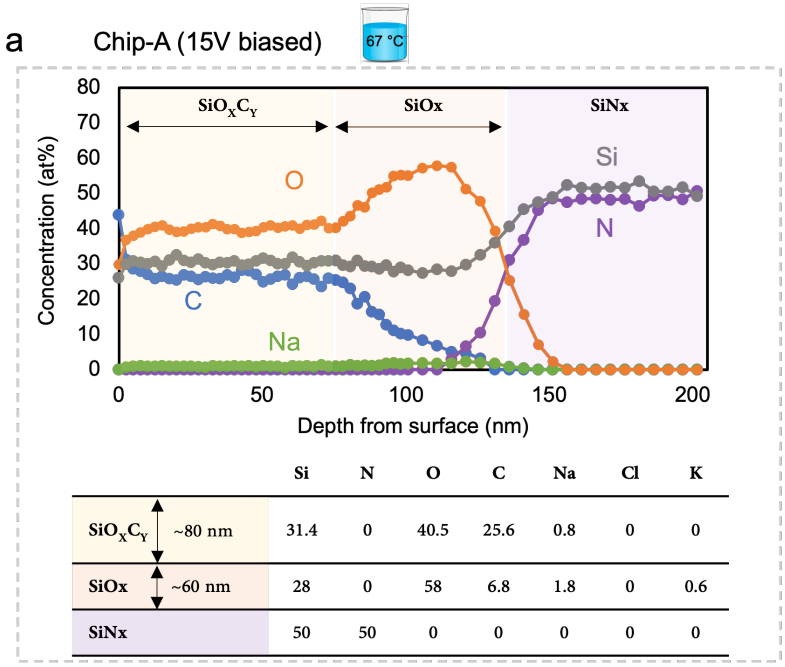
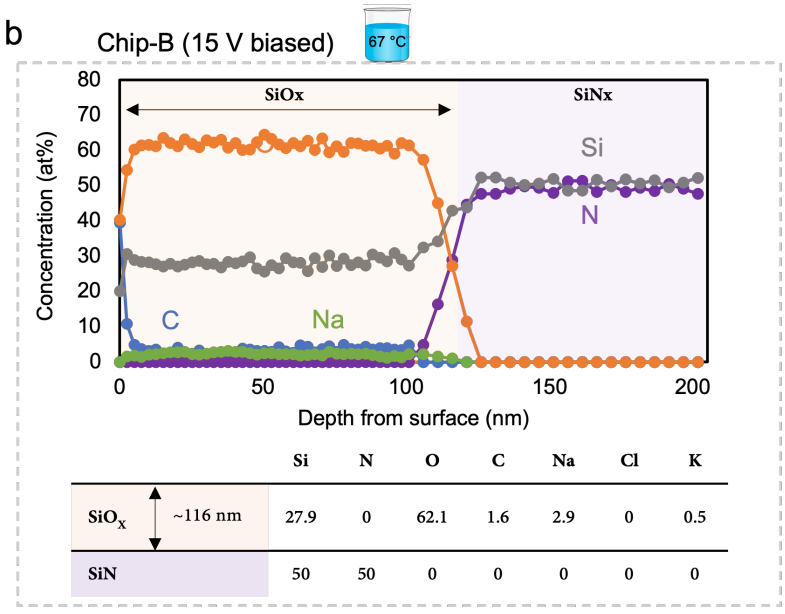


Figure 4.35: A negative mode shallow ToF-SIMS depth profiles acquired with sub-nanometer step-size (0.135 nm) from 0 - 15 nm from PDMS-coated and exposed (uncoated) regions of the 7-month explanted Chip-B ICs.



		Si	N	O	C	Na	Cl	K
SiO_XC_Y	~80 nm	31.4	0	40.5	25.6	0.8	0	0
SiOx	~60 nm	28	0	58	6.8	1.8	0	0.6
SiNx		50	50	0	0	0	0	0



		Si	N	O	C	Na	Cl	K
SiO_X	~116 nm	27.9	0	62.1	1.6	2.9	0	0.5
SiN		50	50	0	0	0	0	0

Figure 4.36: XPS depth profiles giving the chemical composition of the oxidized layer developed on the SiN_X passivation layers after 12 months of continuous electrical biasing with 15 V DC in PBS solution at 67 °C. a) Chemical composition of the developed oxidized layer on Chip-A when biased between M3-IDC (negative) and PBS (positive). b) Chemical composition of the developed oxidized layer on Chip-B when biased between M5-IDC (negative) and PBS (positive).

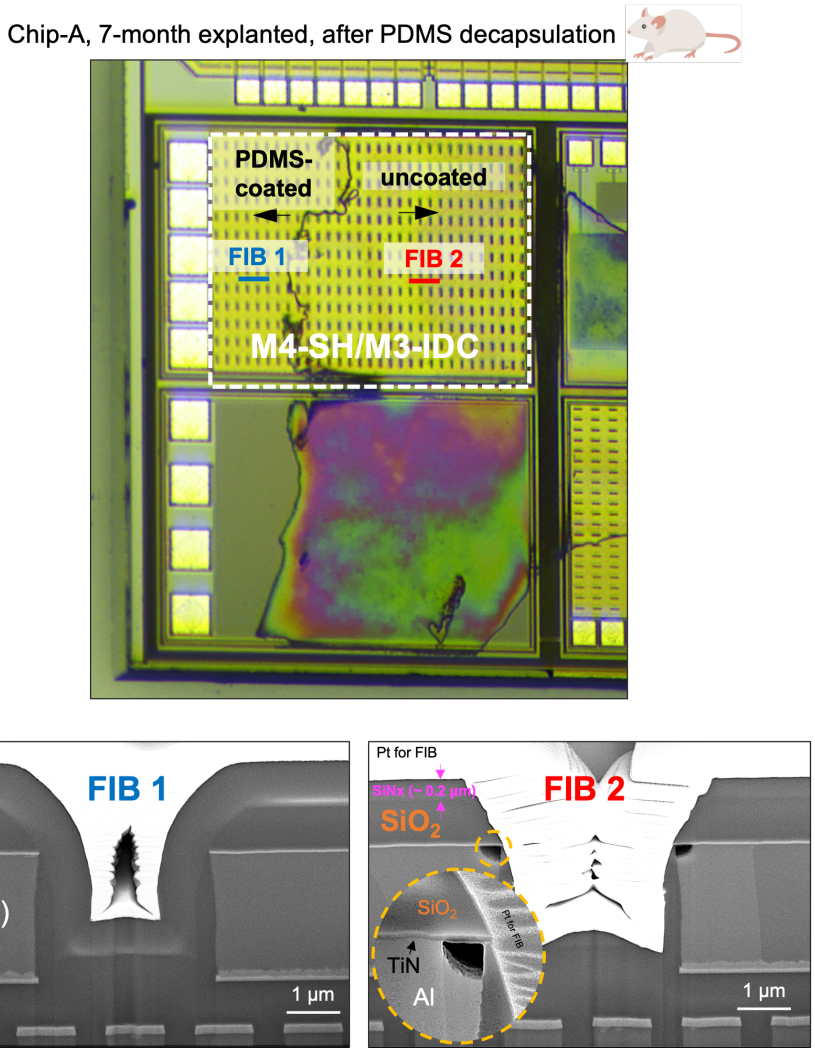


Figure 4.37: Optical micrograph and SEM cross-sectional images of a Chip-A sample explanted at month 7 and PDMS decapsulated. Blue and red lines on the M4-SH/M3-IDC structure indicate FIB cuts in the PDMS-coated and exposed (uncoated) regions, respectively. SEM cross-sectional images of the FIB cuts compare the PDMS-coated (FIB 1: bottom left) and exposed (FIB 2: bottom right) regions of the M4-SH/M3-IDC test structure. In the exposed region, corrosion of the Metal-4 (top metal) aluminum (Al) layer is visible due to the dissolution of the SiN_X passivation and the poor conformality of the SiO_2 passivation layer. Note that on top of the IC, in the flat area, a thinned SiN_X is still present. The sides, however, due to poor conformality, have a thinner SiN_X. Inset shows a high magnification of the corroded aluminum (Al) metal while the titanium nitride (TiN) layer remains intact. The poor conformality of the SiN_X and SiO_2 passivation layers is a result of using the top metallization (in this case M4).

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5

In vivo Biostability of ALD and Parylene-ALD Multilayers as Micro-Packaging Solutions for Implantable ICs

In the previous chapter, the inherent hermeticity of silicon ICs was demonstrated. However, it was found that direct exposure to biological fluids can result in IC material degradation, compromising their integrity and hermeticity. Thin-film coatings are an attractive solution for chip-scale packaging. However, their long-term in vivo biostability and performance have always been a concern when directly exposed to the body's corrosive environment. In this chapter, I investigate the long-term in vivo biostability of two different thin-film coatings: a hafnium-based atomic layer deposit (ALD) multilayer ceramic, and a hybrid ALD/Parylene-C multilayer. This chapter is a verbatim copy of the paper [1] which is in preparation for submission to a journal, and only section and figure numbers were changed to comply with the format of this thesis. In this chapter, the hafnium-based ALD was deposited by Riina Ritasalo at Picosun Oy, and the hybrid ALD/Parylene-C multilayer was deposited by Matthias Van Gompel at Comelec SA.

5.1. Introduction

Next-generation chip-embedded neural implants are emerging with the potential to revolutionize the field of neuroscience and healthcare1 [2, 3]. Packaging of these miniaturized devices, however, has been identified as one of the major challenges as biocompatibility, biostability, and effective device protection should be validated for the packaging material through long-term in vivo studies [4]. In the last years, various organic and inorganic thin-film coatings have been investigated as chip-scale packaging solutions for implantable devices [5, 6, 7]. Inorganic ceramics such as SiN_X, SiO_X, SiC, HfO_2 and

Al_2O_3 can be deposited using thermal, various plasma-enhanced chemical vapor deposition (PECVD) or atomic layer deposition (ALD) processes [8, 9]. These inorganic films can yield low water vapor transmission rates (WVTR) (as low as 10^{-6} g/cm^2/day) while having thicknesses ranging from 10 nm to 1 µm. The downside, however, is their brittleness and potential to crack in case of mechanical stress. Comparatively, organic films like parylene-C have higher WVTR (10^{-1} g/cm^2/day) but are more mechanically flexible and less susceptible to cracking [5].

Multilayered thin-film coatings have been demonstrated to have higher barrier properties compared to single layers as they create a meandering path for diffusing ions [10, 5]. Among these coatings, hybrid organic-inorganic multilayer stacks can have both superior WVTR and better flexibility [11]. These films are created by sandwiching the ceramic barrier layers (deposited using either ALD or PECVD) between organic polymer layers like parylene [5] or polyimide [12, 13]. Stacking more layers, however, does not necessarily increase the protection performance of the multilayer coating. Although at the beginning it might give a favorably low WVTR, gradually over time as the material is aged (chemically and mechanically) the intra and interlayer stresses can weaken the mechanical integrity of the coating stack, resulting in warping and delamination [5, 10]. Similarly, the surface topography of the substrate (device to be coated) can also introduce stresses in the coating stack, weakening its mechanical integrity [14]. It has also been shown that poor adhesion between the applied coating and the substrate can result in delamination and bulging of the coating [15]. Therefore, besides the WVTR, engineering and optimizing the coating stack according to the substrate is critical to ensuring successful and long-lasting protection.

As the devices are getting smaller and the coating layers thinner, the requirements for a conformal and defect-free coating are getting tighter [16]. At the same time, evaluation of these coatings is also getting more challenging, with new and more sensitive techniques being regularly proposed [17, 18, 19]. Among these techniques, magnesium and calcium tests are sensitive methods for evaluating the moisture barrier properties of thin-film coatings [20, 21, 17]. These techniques, however, are usually conducted in vitro and on non-representative material surfaces with flat features. They fall short in considering the biodegradation mechanisms experienced by biomaterials in vivo, as well as the interaction of the substrate material and topography with the coating performance.

As materials are exposed to the in vivo environment, gradual material degradation can be expected which can lower their performance and barrier properties. Previous investigations have demonstrated the degrading effect of the body environment on various ceramic and polymer biomaterials over their long-term implantation in the body [22, 23]. Understanding the in vivo behavior of these novel thin-film coatings and their possible biodegradation mechanisms can help engineer high-performance coating materials and increase the practical application of chip-scale implants.

In this work, we evaluated the long-term in vivo performance and biostability of two thin-film coatings: an organic-inorganic parylene-C ALD multilayer film, from here on referred to as ParC-ALD-ML (≈ 6 μm in thickness), and an inorganic HfO_2/Al_2O_3 ALD multilayer from here on referred to ALD-ML (≈ 100 nm in thickness) (Fig.5.1 and see Experimental Section, 4.5). To evaluate the coating films on representative surface materials, the coatings were deposited on two different microchips (n=12 chips in total) fab-

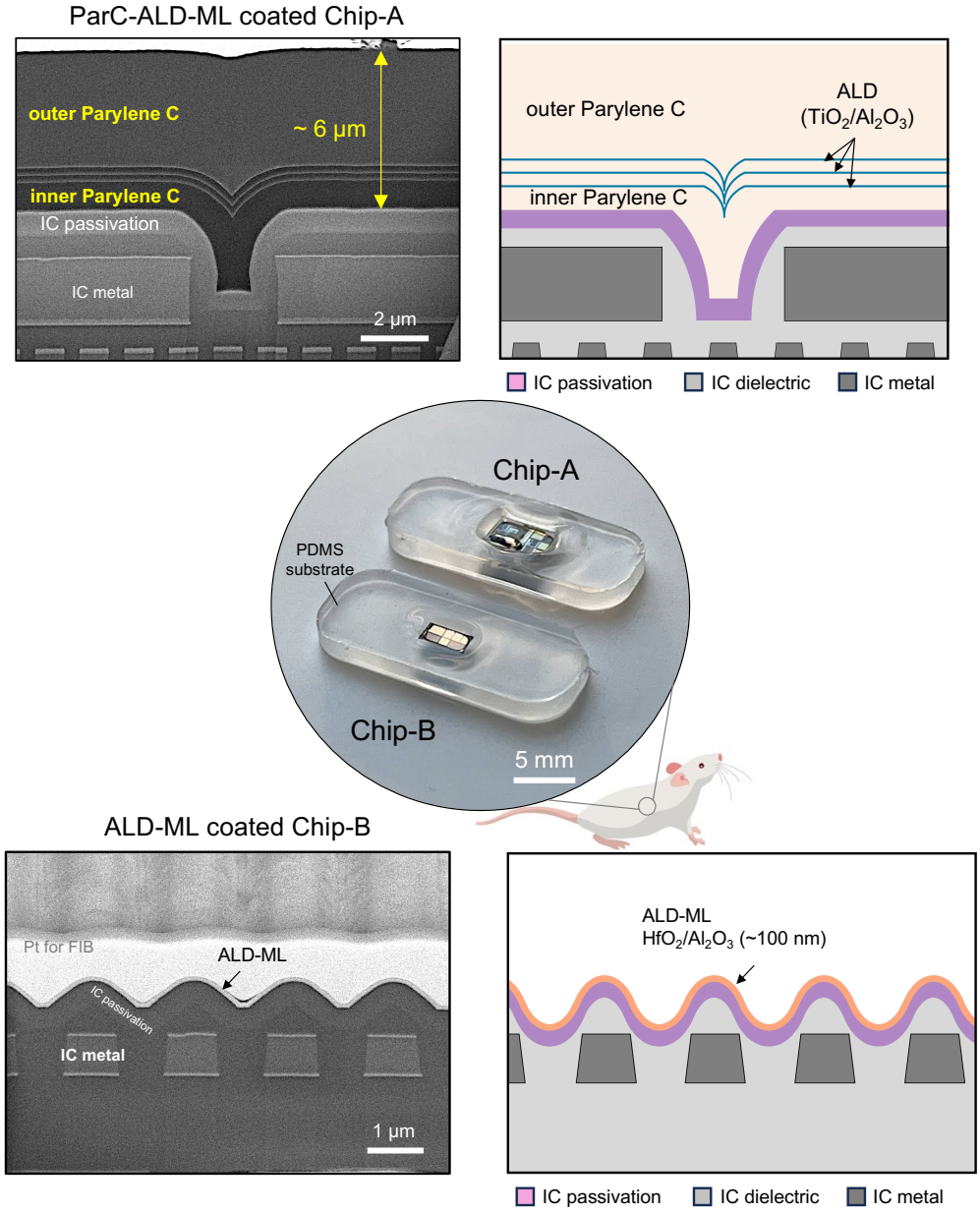


Figure 5.1: Optical and cross-sectional scanning electron microscope (SEM) images showing the multilayer coating deposited on two CMOS microchips (Chip-A and Chip-B) having different surface microtopography. Top cross-sectional SEM image and schematic of the Par-ALD-ML coating deposited on Chip-A with a total thickness of ≈ 6 μm, conformally coating the surface of the chip. Bottom cross-sectional SEM image and schematic of the ALD-ML applied on Chip-B surface with a total thickness of ≈ 100 nm. Coated chips are placed on a PDMS substrate which is used as a handling carrier. The coated top surface of all chips is directly exposed to the in vivo environment.

ricated by two different commercial CMOS foundries, from here on referred to as Chip-A and Chip-B (Fig.5.1 and see Experimental Section, 4.5). Each microchip contained different surface microtopography as a result of using the top metallization of the CMOS process. For both chips, the passivation material covering the top side of the chip was SiN_X with aluminum (Al) for the bond pad openings. In our previous investigation, we demonstrated how exposing the IC's top SiN_X passivation to the body can result in the total dissolution of the layer (see Chapter 4).

The ParC-ALD-ML stack was optimized to create a conformal coating on the microtopography of the chips (Fig.5.1a). A ≈6 μm organic-inorganic stack consisting of Parylene C and Al_2O_3-TiO_2 ALD multilayers was deposited which consisted of a 1 μm Parylene C film, three dyads (Al_2O_3/TiO_2/Parylene C), and a final top 4 μm top Parylene C layer. Depositions of the materials were done consecutively in the same vacuum vessel and without venting cycles, eliminating any contamination between the polymer and metal-oxide ALD layers. As parylene has been shown to have poor adhesion to silicon-based ceramics [24], for adhesion optimization, in situ, surface activation was performed followed by a deposition of a seed Al_2O_3 ALD layer prior to the first parylene layer.

5

For the ALD-ML, x10 layers of HfO_2 (10 nm)/Al_2O_3 (10 nm) were used. Al_2O_3 ALD layers have been reported to have one of the highest water vapor barrier properties, however, their weak chemical stability in moist environments can gradually jeopardize their barrier properties [25, 26]. For this purpose, we chose to have the HfO_2 as the final capping layer, which has shown to be highly stable when soaked in vitro in phosphate-buffered saline (PBS) solution [8, 27].

The coatings were applied on the microchips using the presented processes given in the Experimental Section (4.5). Coated chips were placed on biocompatible polydimethylsiloxane (PDMS) substrates (NuSil MED2-4213) to ease handling and implantation (Figure 5.1). The edges of the coated microchips were also covered with the soft PDMS. The top surface, however, was mainly left uncoated, directly exposing the ParC-ALD-ML and ALD-ML films to tissue. Samples were then subcutaneously implanted in rats. After 2, 4, and 7 months of in vivo aging, explanted microchips were evaluated using cross-sectional scanning electron microscopy (SEM) and atomic force microscopy (AFM), with the chemical stability and barrier properties of the coatings analyzed using time-of-flight secondary ion mass spectrometry (ToF-SIMS).

5.2. Results

5.2.1. In vivo structural stability of multilayer coatings

To evaluate the structural stability of the multilayer coatings, all explanted microchips were examined using optical and electron microscopy. Fig.5.2 shows two representative microchips encapsulated with a ParC-ALD-ML and ALD-ML coating after 7 months of implantation in rats. For these representative samples shown here, ParC-ALD-ML was used for encapsulating Chip-A (Figures 5.2 a-d), and the 100 nm ALD-ML was used for encapsulating a Chip-B IC (Figure 5.2(e-h)).

For both microchips, light microscopy (up to 100x magnification) showed no visible signs of degradation on the coating or IC across the entire surface area. Additionally, the aluminum pads coated using the thin layers showed no signs of metal corrosion.

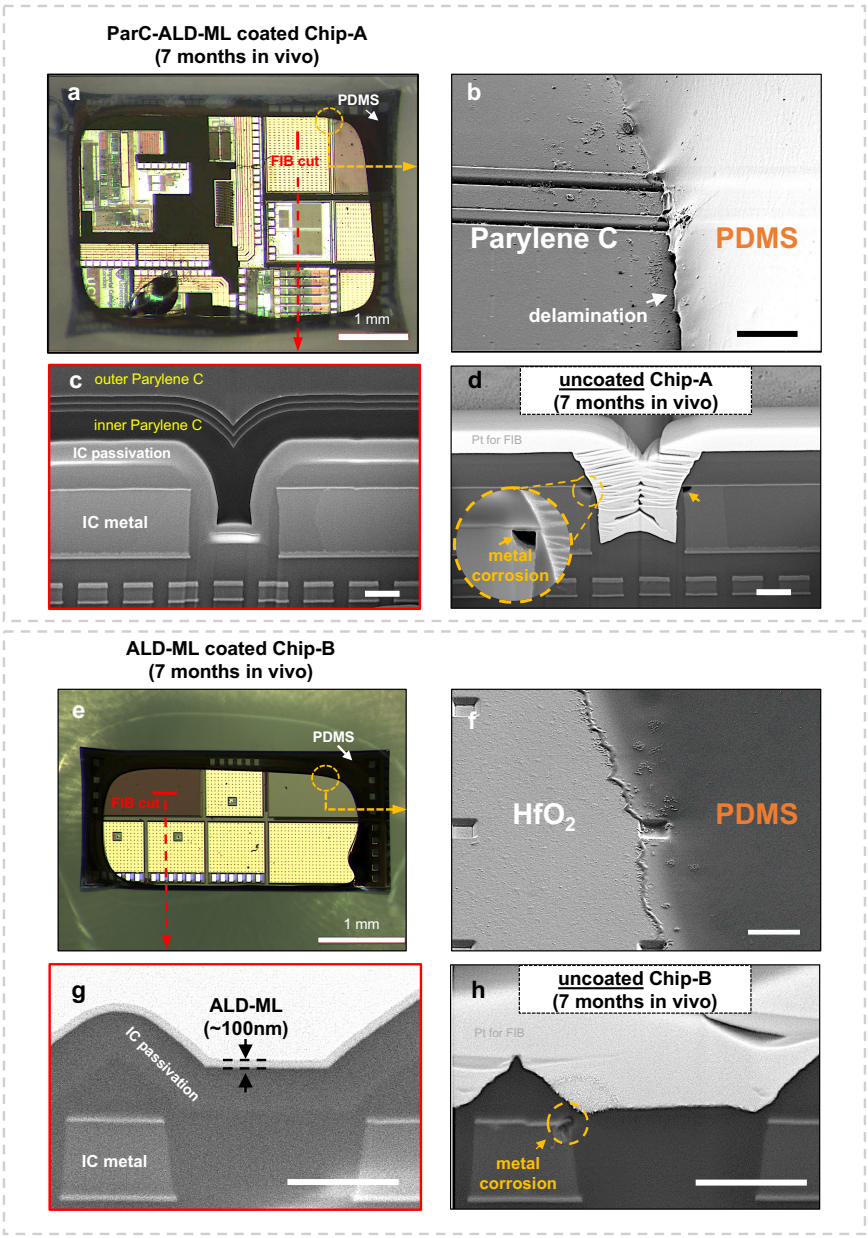


Figure 5.2: Optical micrograph and SEM images of the Par-ALD-ML and ALD-ML coatings after 7 months in vivo implantation. a) Optical micrograph showing a Chip-A coated with ParC-ALD-ML with no visible signs of degradation on the IC. b) Titled SEM image near the PDMS-coated region with interfacial delamination between PDMS and parylene. c) Cross-sectional SEM images showing the ParC-ALD-ML stack after implantation. d) Cross-sectional SEM image of a similar Chip-A with no coating showing degradation of the IC passivation and metal corrosion after 7 months of implantation. Scale bar for (c) and (d) is 100 μm. e) Optical micrograph of a representative Chip-B coated with ALD-ML with no visible signs of degradation. f) Tilted SEM image near PDMS-coated region with no signs of PDMS delamination. g) Cross-sectional SEM image showing intact ALD-ML and IC passivation and metals. Cross-sectional SEM image of a similar Chip-B with no coating showing degradation and corrosion of IC metal after 7 months of implantation. Scale bar is 1 μm.

Microscopic results, however, revealed significant delamination between the PDMS and the parylene surface, allowing lateral ingress of body fluids under the PDMS (Fig.5.2(b)). Delamination of the PDMS-to-parylene interface was noticed for the 2-month explanted microchips and was observed on all ParC-ALD-ML coated chips (n=6), indicating the poor in vivo stability of this interface. All microchips encapsulated with the ALD-ML (n=6), on the other hand, showed stability at the PDMS-HfO_2 interface with no signs of delamination when examining the PDMS-coated edges of the chips (see Fig.5.2(f)).

The structural stability of the multilayer coating stacks was analyzed using cross-sectional SEM imaging. Focused ion beam (FIB) cross-sections were made on at least three locations of each explanted microchip. Fig.5.2(c) shows a representative SEM cross-section of the ParC-ALD-ML stack on Chip-B after 7 months of implantation, demonstrating the stability of the entire multilayer stack. SEM cross-section results also indicate the adhesion stability between the ParC-ALD-ML coating and the IC's passivation surface, even on the most complex microtopography on the chip (Fig.5.2c). Fig.5.2d shows an uncoated Chip-A IC after 7 months of implantation. Comparing Fig.5.2(c) and (d) demonstrates how the ParC-ALD-ML coating protected the IC's passivation and metal from any degradation and corrosion.

Fig.5.2(e) demonstrates a cross-sectional SEM image of the ALD-ML coating on a Chip-B sample after 7 months of implantation. From the point of view of nanolaminate film thickness, no variation was observed after the in vivo study ($\approx$ 100 nm). Similar cross-section SEM investigations on other locations of the chip also showed the expected thickness of the ALD-ML and no delamination from the chip surface. Fig.5.2(h) shows an uncoated Chip-B IC after 7-month implantation in rats where degradation of the IC's passivation and metal corrosion is seen. Comparing the ALD-coated and uncoated ICs shows how a 100 nm ALD-ML coating can protect the chip from degradation.

SEM surface analysis was done on the 4 and 7-month explanted chips to detect any defects, openings, or degradation of the coating layers. Fig.5.6, Supporting Information, shows an explanted ALD-ML on Chip-B where openings or imperfections in the ALD coating are observed. The openings are detected in only one location on the chip with the size of the largest opening being $\approx$ 5 μm x 10 μm. Cross-sectional SEM evaluations in the center of the opening showed a degradation of the IC's silicon nitride (SiN_X) passivation layer. Through the opening in the ALD-ML coating, the chip's SiN_X layer was exposed to the body environment (fluids, proteins, enzymes), causing a $\approx$ 400 nm dissolution of the microchip's SiN_X layer. ParALD-ML on 4 examined microchips explanted at 4 and 7 months showed no openings or defects in the layer.

The surface stability of the coating layers was examined using AFM. Fig.5.3 presents the AFM results for representative ParC-ALD-ML and ALD-ML coated chips at 7 months in comparison to pristine un-implanted samples. Comparing the surface topography of the ParC-ALD-ML shows that exposure to the body environment results in nano-roughening of the surface parylene layer. The ALD-ML, however, showed no change in its surface topography.

5.2.2. IN VIVO CHEMICAL STABILITY AND BARRIER PROPERTIES

The chemical stability and barrier properties of both coating layers was examined using ToF-SIMS depth profile analysis. ToF-SIMS depth profiles were collected at negative and

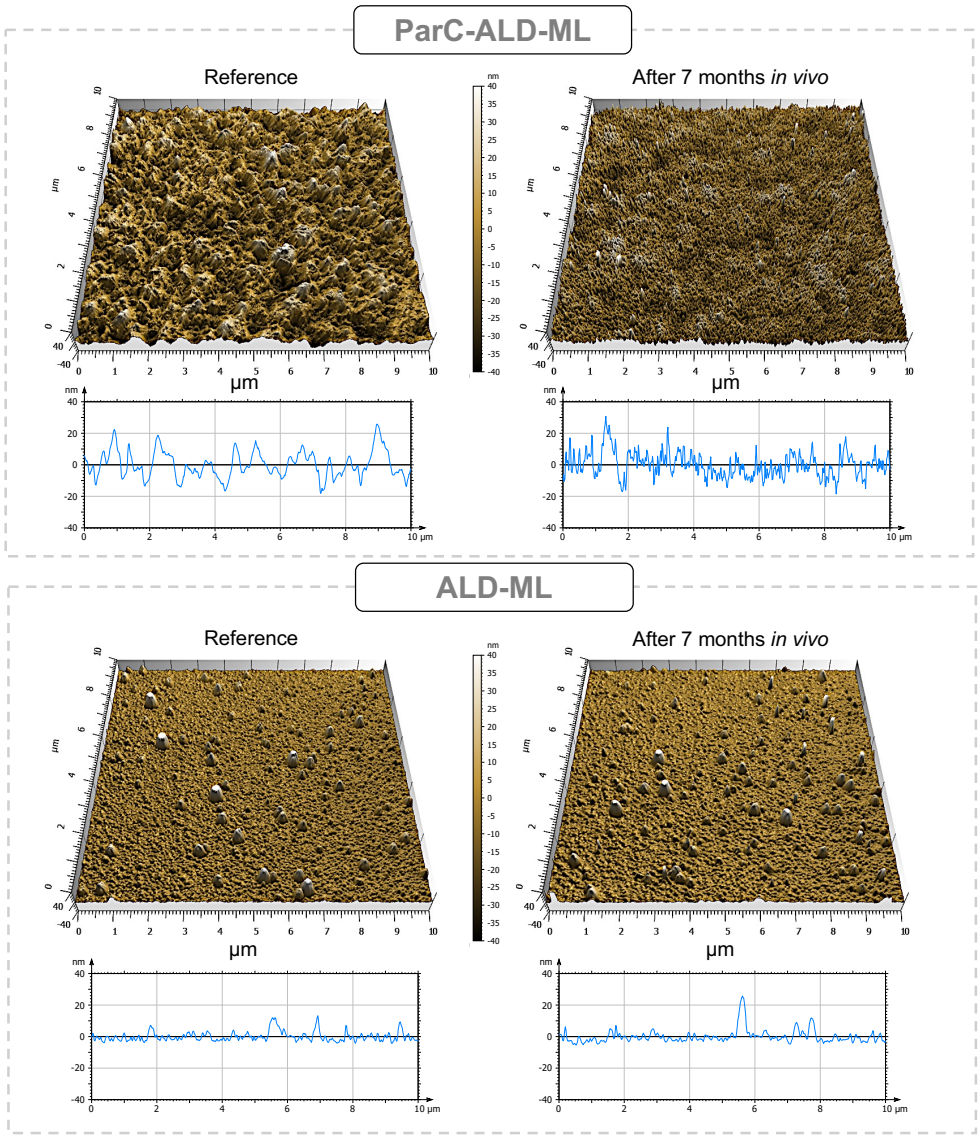


Figure 5.3: Atomic force microscopy (AFM) comparing the outer surface of the multilayer coatings after 6-month in vivo implantation with a reference non-implanted sample. Top graphs comparing the parylene surface showing nano roughening appearing on the surface after implantation. The bottom graphs show no change in surface roughness for the HfO_2 after in vivo implantation.

positive modes and analyzed on a 50 x 50 μm^2 area on two different locations on the microchips. Negative mode depth profiling was used to evaluate the oxygen and moisture ingress levels by monitoring the [O^-] and [OH^-] cluster ion in the layers. In addition, the ingress of various anions present in the body environment (Cl^-, $PO_4{}^-$, S^-) was evaluated using negative mode analysis. Positive mode depth profiling was used to detect traces of penetrating cations (Na^+, K^+, Ca^+, and Mg^+).

Fig.5.4 compares the depth profiles of reference (non-implanted) and implanted ParC-ALD-ML coatings on two separate microchips. Depth profiles were collected from the surface (0 nm) to a ≈ 150 nm depth, analyzing the outer parylene layer of the multilayer stack that is exposed to tissue. Positive mode depth profile results showed peaks of Ca^+, Na^+ and K^+ cations around a depth of about ≈20 nm, suggesting penetration of these ions. The ionic intensities decay and reach the detection level as the depth profile reaches a depth of ≈ 70 within the layer. The reference parylene sample, however, did not show any ionic impurities in the parylene layer.

To evaluate the chemical stability of the parylene layer, ToF-SIMS depth profiling was done in negative mode to monitor the carbon [C^-] intensity in the layer. In the first ≈70 nm, a drop in the carbon intensities is observed compared to bulk parylene intensities and to the reference layer. Other carbon-related cluster ions specific for parylene (such as [CCl^-]) also showed a drop in the first few 70 nm of the implanted material. The lower carbon intensity indicates possible degradation of parylene after long-term exposure to the body environment. Results in negative mode also indicated higher intensities of [OH^-] and [S^-] for the 7-month implanted parylene layer as compared to the reference layer. The higher [OH^-] could be due to the gradual moisture penetration within the parylene layer. The detected sulfur ions [S^-] could possibly originate from the tissue and body environment, gradually penetrating within the layer. The [S^-] intensity, however, decays at depths > 100 nm and reached reference levels. The lower carbon intensity and ion penetration within the first ≈70 nm of the parylene suggest concurrent surface degradation and ionic ingress in parylene upon long-term exposure to the body environment.

Negative and positive mode ToF-SIMS depth profiles of a representative ALD-ML coating after 7 months in vivo exposure appear in Fig.5.2 and are compared to a reference (non-implanted) sample. Positive mode depth profiles (Fig.5.5(a)) show no indication of cation ingress (Ca^+, Mg^+, Na^+ and K^+) in the layer. The peak observed at ≈109 nm is due to IC's surface contamination, already present before coating. Reference samples also showed a similar peak at the ALD-chip interface. The ALD-ML stacks consist of 10 HfO_2 layers and 10 Al_2O_3 layers with the HfO_2 beginning at the surface. Both positive and negative depth profiles show the presence of all 10 peaks for the 7-month implanted sample. When comparing the intensity between the reference and implanted samples (Fig.5.5(b-c)), no change in the intensity was detected, demonstrating the outstanding in vivo stability of the thin ceramic layers. Additionally, the [OH^-] signal also remains stable and similar to the reference sample indicating the high moisture barrier properties of the ALD layers.

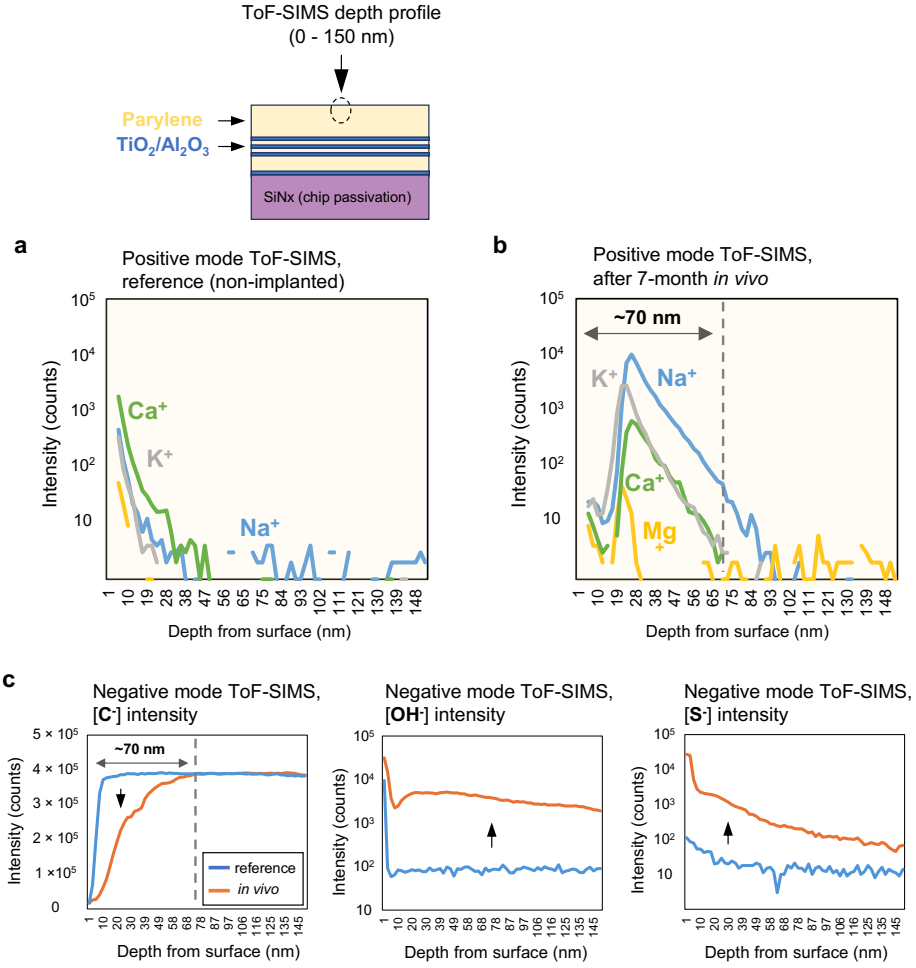


Figure 5.4: Positive and negative mode ToF-SIMS depth profiles of ParC-ALD-ML coatings, comparing reference (non-implanted) with 7-month implanted. a-b) Positive mode depth profiles from 0 - 150 nm for reference (non-implanted) (a) and implanted (b) showing ionic penetration within the ≈70 nm parylene layer. c) Negative mode depth profiles from 0 - 150 nm comparing the $[C^-]$, $[OH^-]$, and $[S^-]$ intensities on reference (non-implanted) and 7-month implanted devices. Lower carbon intensity for the first ≈ 70 nm parylene suggests degradation of the polymer.

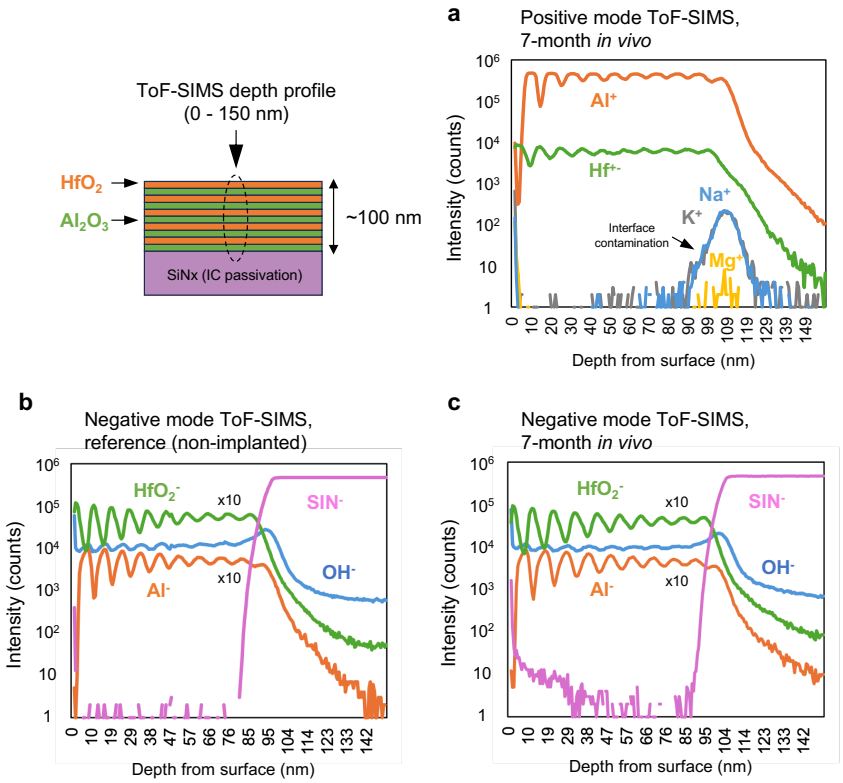


Figure 5.5: Positive and negative mode ToF-SIMS depth profiles of ALD-ML coatings, comparing reference (non-implanted) with 7-month implanted. a) Positive mode depth profile from 0 - 150 nm showing no ionic penetration in the multilayer HfO_2 - Al_2O_3 stack. b-c) Negative mode depth profiles from 0 - 150 nm comparing the $[Al^-]$, $[Hf^-]$, and $[OH^-]$ intensities on a reference (non-implanted) (b) and a 7-month implanted device (c) showing chemical stability of the entire ALD-ML stack.

5.3. DISCUSSION AND CONCLUSIONS

Table 5.1 summarizes and compares the findings for the two multilayer coatings after the 7-month in vivo study. Both films were engineered to have conformality to the chips' topography and maintain their internal structural stability through the in vivo study. The coatings were found to effectively protect the aluminum pads and SiN_X passivation on the IC from any biodegradation. Out of the tested ALD-coated ICs (n=6) no PDMS delamination was observed suggesting the excellent in vivo adhesion of PDMS to the HfO_2 layer. More significantly, the 100 nm ALD-ML showed superior biostability. The top HfO_2 showed no enhancement of oxidation which has been observed for other ceramics barriers like SiC and SiN_X [28, 29]. In combination, these insights make HfO_2 ALD a very promising bioceramic for chronic applications.

For the ParC-ALD-ML, the observed degradation and ion ingress in the exposed top parylene-C layer suggests concurrent degradation and ion penetration. To mitigate this, a biostable ALD ceramic layer can be applied to cap the parylene. Additionally, PDMS could be used as the outer tissue-contacting layer on top of the parylene. However, in this case, the poor adhesion between PDMS and parylene must be enhanced, potentially by inserting a thin ceramic layer in between which can act as an adhesion promoter [30].

Coating	Conformality	Stack Stability	IC passivation protection	PDMS adhesion	Chemical stability	Ionic barrier properties
ALD-ML (≈100 nm)	High	High	High	High	High	High
ParC-ALD-ML (≈6 μm)	High	High	High	Low	Degradation in top 70 nm	Ion ingress in top 70 nm

Table 5.1: Summary of the 7-month in vivo study.

The excellent biostability and long-term barrier properties of the HfO_2 was demonstrated. However, due to the thinness of these protective coatings, any defect or crack in the layer can allow body fluid penetration in the layer, causing gradual degradation of the IC materials. The application of a final PDMS coating may alleviate this issue as it covers imperfections and prevents the ingress of biological species. Moreover, the demonstrated in vivo adhesion of PDMS and HfO_2 makes this combination stack a suitable long-lasting packaging with PDMS acting as the compliant soft tissue contacting material. In the case of the Par-ALD-ML coated chip, no imperfections in the coating were observed when analyzing n=4 coated chips.

Stacking more layers at first might seem beneficial, but ultimately it might undermine the structural and mechanical stability of the entire stack. Especially, when combing polymers like parylene and ceramic ALD layers, any mismatch between thermal expansion between the layers might cause interlayer stresses, weakening the interfacial adhesion, and making the coating susceptible to delamination.

5.4. EXPERIMENTAL SECTION

Silicon-IC microchips: For evaluating the thin-film coating layers, two different CMOS microchips with different surface microtopography were used as test vehicles. Both chips were fabricated in a standard CMOS foundry: Chip-A was fabricated in a 4-metal,

0.35 μm process with a thick top metal (2.8 μm) and had a total area of 4 mm x 5 mm (20 mm^2). Chip-B was fabricated using a 6-metal, 0.18 μm process having a total area of 1.7 mm x 3.5 mm (5.9 mm^2).

HfO_2-based ALD multilayer (ALD-ML) coating: A 100 nm HfO_2-based ALD stack (referred to in this paper as ALD-ML), consisting of multiple HfO_2-based ALD layers was deposited at Picosun Oy using the Picosun® R-200 Advanced ALD reactor, at a pressure of about 1 mbar (N_2 atm.). The PicoHot source system (PH-300) and PicoSolution (both Picosun Oy) precursors were vaporized from stainless-steel precursor bottles at increased and room temperature, respectively. Thermal ALD processes at 125 C were applied with a build of the HfO_2-based coating. For the ALD deposition, microchips were placed on mesh grids to allow a conformal coating of the microchips.

Parylene-ALD hybrid multilayer (ParC-ALD-ML) coating: A ≈6 μm organic-inorganic stack consisting of Parylene C and Al_2O_3-TiO_2 ALD multilayers was deposited at Comelec using the C30H Parylene-ALD hybrid deposition system. The hybrid stack consists of a 1 μm Parylene C film, three dyads (Al_2O_3/TiO_2/Parylene C), and a final 4 μm top Parylene C layer. Depositions of the materials were done consecutively in the same vacuum vessel and without venting cycles. This eliminates any contamination between the polymer and metal-oxide ALD layers, usually present after handling substrates. The Parylene C layers were deposited at room temperature (23 °C). Before coating, an initial O_2 plasma treatment step followed by a silane (A174) adhesion promoter step was included in the cycle. The deposition of the metal oxide ALD layers is performed at temperatures slightly below 100 °C.

PDMS substrate and partial PDMS coating: The chips were placed on 3 mm thick, soft PDMS substrates fabricated from medical-grade silicone rubber (MED2-4213, NuSil). For manufacturing the PDMS substrates, a custom-made polytetrafluoroethylene (PTFE) mold was filled with uncured PDMS, which was then semi-cured in the oven at 100 °C for 30 minutes. At the same time, for optimal PDMS adhesion, the ICs were surface activated and cleaned using UV-ozone for 15 minutes with their top passivation facing the ozone lamp. The ICs were then placed in the center of the semi-cured PDMS substrates. After positioning, all aluminum pads and parts of the IC passivation were coated using the same medical grade PDMS (MED2-4213, NuSil). Finally, the samples were fully cured in the oven at 100 °C for two hours.

Animals, implantation, and explanation procedures: All experiments were performed per the EC Council Directive of September 22, 2010 (2010/63/EU). All procedures were reviewed and approved by the Animal Care Committee of the Research Centre for Natural Sciences and the National Food Chain Safety Office of Hungary (license number: PE/EA/1253-8/2019). The implantation procedures were carried out as follows. Wistar rats (n=6; weight, 315.5 ± 59.6 g at the initiation of the study) were anesthetized by an intraperitoneal injection of a mixture of ketamine (75mg/kg of body weight; CP-Ketamin, Produlab Pharma B. V., Raamsdonksveer, The Netherlands) and xylazine (10mg/kg of body weight; CP-Xylazin, Produlab Pharma B. V., Raamsdonksveer, The Netherlands). A body temperature of 37 °C was sustained with an electric heating pad connected to a temperature controller (Supertech, Pécs, Hungary). Before implantation, samples were sterilized by immersing them in isopropyl alcohol for at least 20 min and then washing them with a continuous stream of distilled water for 2 min. To reduce the number

of animals used, each animal was subcutaneously implanted with two microchips. The incision was closed using interrupted sutures followed by a standard combined post-operative analgesic regimen. Samples were explanted at three time points: months 2, 4, or 7. Before explantations, rats were initially anesthetized in the same way as described above. After anesthesia induction, the animals were overdosed with isoflurane (5% in 100% oxygen) until breathing stopped. Before explantations, the skin around the implants was examined for any inflammation. After long-term implantation, a tissue pocket was formed around each sample. The samples were removed from the pocket to analyze the tissue pocket. The pocket was immersed in 4% paraformaldehyde solution for 24 hours, then washed in 0.1M PBS and stored in PBS. The tissue samples were then sectioned and stained with hematoxylin and eosin stain, and photomicrographs were taken for tissue analysis. Explanted microchips were carefully rinsed with deionized (DI) water, blow-dried, and stored in a dried condition for a week before analysis.

Multilayer stack characterization using scanning electron microscopy (SEM): For realizing all cross sections and scanning electron microscopy (SEM) images, a dual-beam, focused ion beam (FIB) system (FEI Helios NanoLab600i) was used. A gallium (Ga) ion beam with nanoscale precision was used for milling and a field emission gun for high-resolution imaging. Before loading the samples into the SEM system, samples were covered in a sputter coater with a thin (≈20-50 nm) conductive layer of platinum. After selecting the area of interest in the FIB system, a 1 µm thick platinum strip was deposited with an in-situ gas injector system to protect the surface structure from ion beam-induced damage. Cross sections were prepared at a tilt angle of 52 °and a beam current between 21 and 2.5 nA at 30 kV for coarse and fine milling, respectively. The corresponding SEM images were generated with a through-the-lens detector (TLD) using back-scattered electrons (BSE).

Surface characterization using atomic force microscopy (AFM): The Bruker Icon was used in tapping and PeakForce Quantitative Nanomechanics (QNM) mode. Per sample, two areas were scanned with an area of 5 µm x 5 µm.

Chemical composition and barrier property of IC passivation layers pre- and post-aging: Time-of-flight mass spectrometry (ToF-SIMS) depth profiling: ToF-SIMS analyses were performed using an ION TOF IV instrument at Eurofins EAG Laboratories, The Netherlands. The instrument was operated in positive and negative mode using 2 keV O^{2+} and 2 keV Cs^{+} sputtering ions, respectively. At negative mode, sputtering was carried out using the 2 keV Cs+ primary ion beam to enhance the detection level of the electronegative species [O^{-}] and [OH^{-}]. The sputtered area was 250 x 250 μm^2 and the analyzed area was 50 x 50 μm^2 centered in the sputtered area. The analysis was done with a beam of 25 keV Bi+ ions. To increase the sensitivity for lighter elements all samples were stored in the instrument under ultra-high vacuum (<10^{-9} bar) for 64 hours before analysis.

5.5. SUPPLEMENTARY NOTES

Biocompatibility : Before each explanation (at 2, 4, and 7 months), careful observation of the rats' skin after shaving showed perfect healing of the implant incisions. There is no redness of the back and no scabbing or scarring. An incision was made next to the implantation incision, close to the samples. Carefully, the skin and subcutaneous mem-

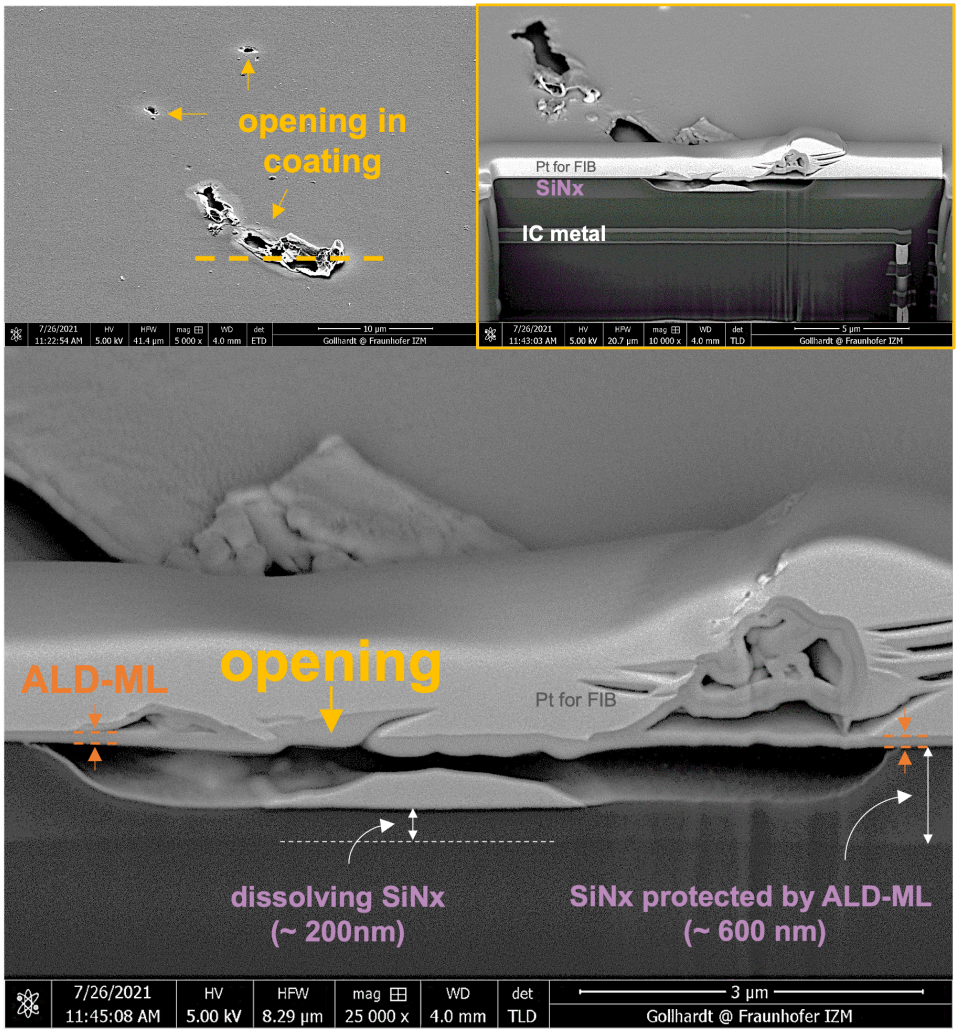


Figure 5.6: Cross-sectional SEM analyzing of openings in ALD coating. Tilted surface images of a 7-month explanted Chip-A coated the ALD-ML film showing opening and degradation. The dotted line shows the area used for the focused ion beam (FIB) for cross-sectioning. Cross-sectional SEM images showing degradation and under-etching of the microchip's silicon nitride (SiN_X) passivation due to the opening in the ALD coating. After 7 months, ≈ 400-nm of the entire 600 nm SiN_X has dissolved due to direct exposure to tissue and body fluids.

Animal	Left-side	Right-side	Explanation date	Analysis
#1	Chip-A (ALD-ML)	Chip-B (ParC-ALD-ML)	2-month	Microscopy
#2	Chip-B (ALD-ML)	Chip-A (ParC-ALD-ML)	2-month	
#3	Chip-A (ALD-ML)	Chip-B (ParC-ALD-ML)	4-month	Microscopy/SEM
#4	Chip-B (ALD-ML)	Chip-A (ParC-ALD-ML)	4-month	
#5	Chip-A (ALD-ML)	Chip-B (ParC-ALD-ML)	7-month	Microscopy/AFM /SEM/ ToF-SIMS
#6	Chip-B (ALD-ML)	Chip-A (ParC-ALD-ML)	7-month	

Figure 5.7: Implantation of coated microchips, explanation time points and analysis.

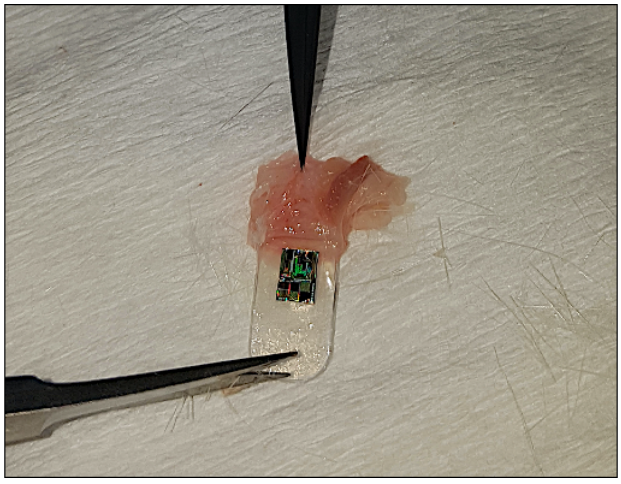


Figure 5.8: Image of an explanted ALD-ML coated Chip-A after 7 months of implantation showing easy tissue removal from the chip surface.

branes were cut. The samples were nicely integrated within the membranes. The membranes are well-vascularized. Once the tissue pocket was cut open, the sample came out without any resistance (see Fig.5.8). All samples (HfO_2-based ALD-ML and ParC-ALD-ML) had no adhering cells on the surface and came in pristine condition without additional damage to the tissue. The samples are contained within a pocket, which consists of a very thin (< 0.2 mm), flexible, well-vascularized and strong membrane.

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6

CONCLUSION AND FUTURE WORK

In this thesis, I explored strategies to improve the durability of ICs for biomedical applications. Two methods for monitoring moisture and ion ingress were developed using CMOS technology and validated through in vitro testing. Long-term accelerated aging studies demonstrated that CMOS ICs can be inherently hermetic and water-resistant even when directly exposed to physiological environments as bare dies, but are susceptible to material degradation. It was shown that PDMS, a soft but moisture-permeable coating, can effectively prevent degradations observed in the bare die regions, highlighting its potential as a biocompatible encapsulant for long-term implants. In vivo evaluations of two thin-film barrier coatings revealed the excellent stability of hafnia-based ALD and the surface degradation of a hybrid Parylene C-ALD multilayer, providing valuable insights for the design of future miniaturized single-chip implants.

6.1. CONCLUSION

CHAPTER 3

In this chapter, two concepts were proposed and verified for on-chip monitoring of moisture/ion ingress in packaged ICs. This first concept was based on a fully integrated on-chip integrity monitor array, implemented in a 0.18 μm standard CMOS process. The array utilizes novel charge/discharge-based, time-mode pixels for monitoring changes in the dielectric layers of the IC structure. In vitro verification (soaked in PBS solution) was performed on an intentionally defective IC which showed the capability of the dielectric sensor array to measure resistance changes within the array upon water/ion ingress. The second concept uses the silicon bulk of CMOS ICs to detect coating defects in thin-film packaged ICs. Off-chip in vitro measurements on a silicon IC demonstrate the feasibility of this technique.

CHAPTER 4

In this chapter, the hermeticity of IC structures was evaluated by exposing bare chips to accelerate in vitro and in vivo aging environments for 12 months. Results showed that

the ICs fabricated by the two selected CMOS foundries can be inherently hermetic and waterproof themselves, likely due to the advanced materials and processes utilized by these foundries. Exposure of the ICs to the physiological environments, however, resulted in the degradation of the IC material, with the most prominent degradation being the dissolution of the nitride passivation. PDMS coating of the ICs, on the other hand, was shown to prevent the observed degradation, making it a promising soft biocompatible encapsulant for multi-year implantations. The insights collected in this work can be useful in engineering long-lasting active neural implants.

CHAPTER 5

This chapter evaluated the long-term in vivo biostability and moisture/ion barrier properties of two thin-film coatings (hafnia-based ALD and Parylene-ALD hybrid multilayer) using various material analysis techniques. Results showed the excellent biostability of the 100 nm ALD coating with no ionic penetration within the layer. For the ParC-ALD-ML, concurrent surface degradation and ion ingress was detected within the top 70 nm on the outer parylene layer. The results and evaluation techniques presented here can enable future material selection, packaging, and testing of next-generation active neural implants.

6.2. FUTURE WORK

Throughout the long-term accelerated in vitro and in vivo investigations performed in this thesis, a number of additional research questions arose that could not be evaluated in more detail. Answers to these questions could be instrumental in realizing long-lasting implantable ICs employing polymer packaging. These questions are outlined in this section.

INTEGRITY MONITORS FOR POLYMER-PACKAGED SINGLE-CHIP IMPLANTS

The dielectric monitor (first concept) reported in Chapter 3 was originally meant to be used as an investigational tool for characterizing the ingress paths of water molecules and ions in the chip. Therefore, a sensor array was realized which occupied the majority of the chip surface. Furthermore, due to the required number of internal control signals to control the array, measurement engine internal column, and row selection logic, and required high precision and resolution measurements, the measurement engine both occupies a substantial area and is power hungry. For a practical application of the sensor, the measurement concept can be used by spreading the sensing cells on critical or sensitive areas of the chip, i.e. near the edges of the die or around sensitive connection pads. This way, the power consumption of the sensing platform could be radically reduced.

The bulk-sensing (second concept) reported in Chapter 3 used off-chip tools for measurements. The ultimate goal, however, is to have an on-chip measurement unit with the bulk being the sensing platform. This would enable an implant with autonomous in-situ hermeticity evaluation. In microelectronic design, the bulk of the chip is usually connected to the ground of the circuit, i.e. the lowest potential. Using the bulk as a sensing platform would, therefore, require novelty in the circuit design. For example, the added

circuitry should neither increase the noise nor interfere with the normal operation of the implant.

STABILITY OF SILICON-IC MATERIAL IN SMALLER TECHNOLOGY NODES

For smaller CMOS technology nodes, low-k dielectrics such as porous SiOCH are being used [1]. These dielectrics have been reported to absorb moisture, resulting in instability and reliability issues when the IC is exposed to moist environments [2]. In Chapter 4, the idea of using a top metal shield was proposed, which uses the top metallization of the CMOS process as a moisture barrier to further delay ingress. The effectiveness of this barrier could be explored for smaller CMOS nodes. Additionally, using the dielectric sensor proposed in Chapter 3, the hermeticity and robustness of smaller CMOS technology nodes could be investigated when packaged with different polymers and thin-film coatings.

EFFECT OF IC DIE THINNING ON THE BARRIER PROPERTIES OF THE PASSIVATION LAYERS

Chapter 4 evaluated the barrier properties of silicon-ICs from two commercial CMOS foundries against biofluid ingress. The chips used in this investigation had a thickness of $\approx 300\ \mu$m. Recent interest in conformable devices has resulted in new die-thinning techniques to lower the thickness of CMOS chips down to 30 μm or even lower [3]. Such thin CMOS structures ultimately have more flexibility which could therefore make their way into new applications for fully conformable implants. One key question, however, would remain which is the barrier properties of the passivation after the thinning process. Although the results in this thesis demonstrated the inherent hermeticity of the IC structure together with the excellent barrier properties of the SiN_X and SiO_X passivation layers, any microcracking could create a gross pathway for ions and moisture in the chip. Therefore, similar investigations used in Chapter 4 could be conducted to evaluate the barrier properties and hermeticity of IC structure after various thinning processes and thicknesses. Additionally, if the passivation is shown to have experienced cracks due to the thinning process, the coatings used in Chapter 4 (low viscosity silicone) and Chapter 5 (ALD and Parylene-C/ALD multilayer) could be explored as protection of the thinned chips.

THE IN VIVO VS. IN VITRO DISSOLUTION BEHAVIOR OF IC PASSIVATIONS

In Chapter 4, we evaluated the dissolution rates of CMOS passivation materials and found that in vivo dissolution rates are much higher compared to in vitro conditions, even at accelerated (67 °C) temperatures. To understand the difference in dissolution rate, more representative in vitro experiments could be conducted to better replicate the chemical environment in the body. For example, previous research has shown that the body can produce aggressive oxidizing species, such as hydrogen peroxide (H_2O_2), which can accelerate the degradation of certain biopolymers [4, 5]. For this reason, various studies have included H_2O_2 (20 mM concentration) in their aging solution during their long-term aging studies [4]. Additionally, to recreate a more organically representative environment, protein (bovine serum) could be added to the saline solution [6]. Proteins in the body have been shown to promote corrosion by inhibiting the formation of the protective passivating film on metals, making them more susceptible to corrosion [7].

FLIP-CHIP TECHNOLOGY USING BALL GRID ARRAYS AS INTERCONNECTS

Besides the stability of the silicon-IC die, ensuring interconnect reliability is crucial for developing a viable medical device. As mentioned in Chapters 2 and 4, for ICs employing PDMS packaging, moisture stability of the underlying IC die and interconnect metallization is essential. Au-Al interconnects were found to be unreliable and moisture-sensitive due to galvanic corrosion between the two dissimilar metals. Moving away from wire bonds, ball grid arrays (BGAs) offer a low form-factor interconnect solution developed for flip-chip wafer-level chip-scale packaged (WLCSP) ICs [8]. In some cases, solder balls can be directly placed on the die [9, 8]. Compared to wire-bonded pads where the gold bump only partially covers the aluminum pads, for bump-on-pad (BOP) solders, the connecting bumps cover the entirety of the aluminum pads [8]. This potentially eliminates the galvanic reaction that might occur due to moisture ingress, making BOP connections a potentially more reliable interconnect solution for PDMS-packaged ICs. As a future investigation, the moisture robustness and integrity of such BGA interconnect can be examined using accelerated in vitro testing.

MITIGATION FOR AU-AL WIRE-BOND CORROSION

In Chapter 4, the moisture instability of the Au-Al interface was demonstrated, making this die interconnect method unsuitable for PDMS-packaged ICs. To address this issue for applications utilizing wire-bonds as interconnect, two alternative solutions can be investigated:

1. Au-Plating of IC Bond Pads [8]: This technique would eliminate the Al-Au galvanic reactions by providing a consistent gold surface for bonding.

2. Aluminum Wire Bonding [10]: Using aluminum wire bonds would eliminate galvanic reactions since both the wire and the bond pads would be made of aluminum. However, the long-term stability of both solutions needs to be investigated and verified through rigorous testing.

THIN-FLIM CHIP-SCALE PACKAGING

In Chapter 5, degradation and ion ingress for the first few nanometers of the top parylene layer was observed. As future work, it could be investigated if adding a final ALD capping layer on parylene could prevent such degradations. Adding a final capping layer such as Hf_2O could also fix the poor adhesion observed between PDMS and the multilayer thin-film stack. In Chapter 4, the galvanic corrosion of the Al-Au bond pads was identified as a weak point for PDMS-packaged ICs. If switching to a more moisture-resistant wire-bond material is not feasible, it could be evaluated if using the ALD or Par-ALD multilayers, as a barrier layer underneath PDMS, could prevent the observed interconnect corrosion.

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