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Integration of power electronics into crystalline silicon solar cells

David Auke van Nijen

Integration of power electronics into crystalline silicon solar cells

Dissertation

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A journey of a thousand miles begins with a single step

Lao Zi (Chinese: 老子), 6th century BCE

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Summary

Power electronics (PE) plays a crucial role in optimizing the performance of photovoltaic (PV) systems. At present, module and sub-module level PE is increasingly being adopted in global PV installations. Typically, PE for sub-module purposes is installed in the PV junction box. However, in this dissertation another approach is investigated: integrating power electronics into or onto crystalline silicon (c-Si) PV cells. This approach has the potential to contribute to the development of shade-tolerant PV modules, increase the reliability of PV module-integrated PE, reduce the volume and weight of the PV system, and support the development of autonomous devices powered by low-power and low-current PV cells. Specifically, the aim of this dissertation is to study the integration of different PE components into c-Si solar cells, and identify the most promising approaches. The dissertation is structured in two parts.

In **Part I**, the objective is to gain a comprehensive understanding of the impedance of c-Si solar cells. To this end, **Chapter 2** reports a characterization of the impedance of eight single-cell laminates. Each laminate contains a different commercially available c-Si solar cell, featuring various cell architectures, namely Aluminium Back Surface Field (Al-BSF), Passivated Emitter and Rear Contact (PERC), Tunnel Oxide Passivated Contact (TOPCon), Interdigitated Back Contact (IBC), and Silicon Heterojunction (SHJ). It is found that the two main factors contributing to a high PN junction capacitance (C_j) at maximum power point (MPP) are (1) a low wafer dopant concentration and (2) a high MPP voltage. Furthermore, the studied cell laminates exhibit inductances between 63 and 130 nH. Following this, the impedance of PN junctions is further investigated in **Chapter 3**. Specifically, PN homojunction devices are investigated through Technology Computer-Aided Design (TCAD) simulations. This methodology allows to study the junction impedance in a detailed way, which may be difficult to do experimentally due to noise and reactance of metal contacts. Through analysis of the impedance data it is revealed that the PN junction exhibits the behaviour of a parallel resistor-capacitor circuit (RC-loop) at low frequencies, but undergoes relaxation in both PN junction resistance (R_j) and capacitance (C_j) as frequency increases. While various publications on solar-cell impedance model the low-high (LH) junction using an RC-loop, the findings presented in this chapter indicate that such a model does not accurately represent the underlying physics. Instead, this approach is likely compensating for the frequency-dependent behavior of R_j and C_j. Finally, in **Chapter 4**, the PN junction impedance of modern c-Si solar cells is studied across varying temperature and illumination conditions. In the tested conditions, the range in which the area-specific MPP R_j varies is similar for different cell architectures, despite their different properties. Conversely, the range in which the areal MPP C_j varies is significantly affected by the substrate dopant concentration and MPP voltage of the cell.

In **Part II**, the aim is to assess the feasibility of leveraging solar-cell impedance at the input of a power converter, and to explore various methods for integrating additional PE

components into solar cells. In **Chapter 5**, the feasibility of integrating different PE components into c-Si solar cells is explored. First of all, diodes exhibit high ease of integration into PV cells and successfully integrated designs have already been demonstrated in prior work. Alternatively, the integration of transistors is more complex. Since transistor fabrication processes require lithographic steps, it is necessary for cost-effective integration to combine as many processing steps as possible with PV fabrication. Regarding passive component integration, it is found that the self-capacitance of modern c-Si solar cells is sufficiently large to replace the input capacitor of an exemplary boost converter. However, for thin-film capacitor integration, it is challenging to achieve a sufficiently high areal capacitance. Moreover, the self-inductance of a solar-cell string could potentially be leveraged to replace the inductor at the input of a power converter. By analyzing this approach for an exemplary boost converter, it was found that high switching frequencies in the MHz range are required. Alternatively, the required switching frequency may be reduced through the integration of planar inductors. It was found that the area of PV cells is sufficiently large to facilitate the integration of planar coils exhibiting inductance values that are useful for power conversion. Finally, general challenges that should be considered for successful PE-PV integration are appropriate thermal management, opto-electric behaviour under illumination, and repairability. The inductor integration is further studied in **Chapter 6**. Specifically, it is explored whether large-area planar air-core inductors can yield the required inductor properties to support sub-module power conversion in PV modules. First, it is shown how the interplay between the different design parameters, such as track spacing, track width, number of turns, and middle gap size, play an important role in the inductor properties. This analysis includes changes due to high-frequency effects, which significantly impact the results. The coil geometries that are simulated yield inductance values between 0.3 and 3.2 μH. Considering the power losses, the applicability of such inductors in sub-module power converters is discussed. Finally, in **Chapter 7**, the concept of COSMOS (COmbined Solar and MOSFET) devices is introduced and a process flow is proposed in which back-contact TOPCon solar cells and lateral power MOSFETs are simultaneously fabricated on a single substrate. This process is successfully employed to manufacture both n-type solar cells with integrated p-channel MOSFETs (PMOS) and p-type solar cells with integrated n-channel MOSFETs (NMOS). Notably, efficiencies exceeding 20% are achieved for both n-type and p-type solar cells, highlighting the potential of COSMOS solar cells. Furthermore, two main integration challenges are identified. Firstly, the *off*-state leakage currents of the MOSFETs increase due to illumination. Secondly, specific topologies of monolithic integration lead to increased *off*-state leakage currents.

Samenvatting

Vermogenselektronica (VE) speelt een cruciale rol bij het optimaliseren van de prestatie van fotovoltaïsche (PV) systemen. Op dit moment wordt VE op module- en submodule-niveau steeds vaker toegepast in wereldwijde PV-installaties. Meestal wordt VE voor submodule doeleinden geïnstalleerd in de PV-aansluitdoos. In dit proefschrift wordt echter een andere benadering onderzocht: het integreren van VE in of op kristallijn silicium (k-Si) PV-cellen. Deze benadering kan bijdragen aan de ontwikkeling van schaduwtolerante PV-modules, de betrouwbaarheid van PV-module-geïntegreerde VE verhogen, het volume en gewicht van het PV-systeem verminderen, en de ontwikkeling van autonome apparaten aangedreven door PV-cellen ondersteunen. Specifiek is het doel van dit proefschrift om de integratie van verschillende VE componenten in k-Si zonnecellen te bestuderen en de meest veelbelovende benaderingen te identificeren. Het proefschrift is gestructureerd in twee delen.

In **Deel I** is het doel om een uitgebreid begrip te krijgen van de impedantie van k-Si zonnecellen. Daartoe rapporteert **Hoofdstuk 2** een karakterisering van de impedantie van acht laminaten. Elk laminaat bevat een verschillende commercieel beschikbare k-Si zonnecel, met diverse celstructuren, namelijk Aluminium Achteroppervlakteveld (Al-BSF), Gepassiveerde Emitter en Achtercontact (PERC), Tunneling Oxide Gepassiveerd Contact (TOPCon), Interdigitated Achtercontact (IBC), en Silicium Heterojunctie (SHJ). Er wordt vastgesteld dat de twee belangrijkste factoren die bijdragen aan een hoge PN-junctiecapaciteit (C_j) op het maximaal vermogenspunt (MVP) (1) een lage doteringsconcentratie van het substraat en (2) een hoge MVP-spanning zijn. Verder vertonen de bestudeerde cellaminaten inductanties tussen 63 en 130 nH. Vervolgens wordt de impedantie van PN-juncties verder onderzocht in **Hoofdstuk 3**. Specifiek worden PN-homojuncties onderzocht via Technology Computer-Aided Design (TCAD) simulaties. Deze methodologie maakt het mogelijk om de junctie-impedantie op een gedetailleerde manier te bestuderen, wat experimenteel moeilijk kan zijn vanwege ruis en reactantie van metalen contacten. De analyse onthult dat de PN-junctie zich gedraagt als een parallel geschakeld weerstand-condensatorcircuit (RC-lus) bij lage frequenties, maar ontspanning ondergaat in zowel de PN-junctieweerstand (R_j) als junctiecapaciteit (C_j) naarmate de frequentie toeneemt. In tegenstelling tot conventionele modelleringsbenaderingen, die vaak een extra RC-lus omvatten om de laag-hoog (LH) junctie te beschrijven, suggereren de bevindingen in dit hoofdstuk dat een dergelijke representatie mogelijk niet de onderliggende fysica weergeeft, met name het frequentieafhankelijke gedrag van R_j en C_j. Ten slotte wordt in **Hoofdstuk 4** de PN-junctie-impedantie van moderne k-Si zonnecellen bestudeerd onder verschillende temperatuur- en lichtomstandigheden. Onder de geteste omstandigheden is het bereik waarin de oppervlakte-specifieke MVP R_j varieert vergelijkbaar voor verschillende celarchitecturen, ondanks hun verschillende eigenschappen. Daarentegen wordt het bereik waarin de oppervlakte-specifieke MVP C_j varieert aanzienlijk beïnvloed door de doteringsconcentratie van het substraat en de

MVP-spanning van de cel.

In **Deel II** is het doel om de haalbaarheid te beoordelen van het benutten van de impedantie van zonnecellen aan de ingang van een vermogensomzetter en om verschillende methoden te verkennen voor het integreren van extra VE-componenten in zonnecellen. In **Hoofdstuk 5** wordt de haalbaarheid onderzocht van het integreren van verschillende VE-componenten in k-Si zonnecellen. Allereerst vertonen diodes een hoge mate van integratiegemak in PV-cellen en succesvolle geïntegreerde ontwerpen zijn al aangetoond in eerder werk. Daarentegen is de integratie van transistors complexer. Aangezien het fabricageproces van transistors lithografische stappen vereist, is het voor kosteneffectieve integratie noodzakelijk om zoveel mogelijk productiestappen te combineren met PV-productie. Met betrekking tot de integratie van passieve componenten wordt vastgesteld dat de eigen capaciteit van moderne k-Si zonnecellen voldoende groot is om de ingangscondensator van een voorbeeld boost-omvormer te vervangen. Voor de integratie van dunne-film condensatoren is het echter uitdagend om een voldoende hoge oppervlakte-specifieke capaciteit te bereiken. Bovendien zou de eigen inductantie van een serieschakeling van zonnecellen mogelijk kunnen worden benut om de spoel aan de ingang van een vermogensomvormer te vervangen. Bij het analyseren van deze aanpak voor een voorbeeld boost-omvormer bleek dat hoge schakelfrequenties in het MHz-bereik vereist zijn. Alternatief kan de vereiste schakelfrequentie worden verlaagd door de integratie van inductoren. Het bleek dat het oppervlak van PV-cellen voldoende groot is om de integratie van vlakke spoelen met inductantiewaarden die nuttig zijn voor vermogensconversie te faciliteren. Tot slot worden algemene uitdagingen voor succesvolle VE-PV-integratie besproken, zoals de verhitting van de componenten, opto-elektrisch gedrag onder verlichting, en repareerbaarheid. De integratie van spoelen wordt verder bestudeerd in **Hoofdstuk 6**. Specifiek wordt onderzocht of luchtkernspoelen de vereiste eigenschappen kunnen leveren om vermogensconversie op submodule-niveau in PV-modules te ondersteunen. Hierbij wordt aangenomen dat de oppervlakte van de luchtkernspoel gelijk is aan de oppervlakte van een k-Si cel. Eerst wordt aangetoond hoe de interactie tussen de verschillende ontwerpparameters, zoals de afstand tussen de sporen, spoorbreedte, aantal windingen, en de grootte van de middenopening, een belangrijke rol spelen in de spoeleigenschappen. Deze analyse neemt de invloed van operatie op hoge frequentie mee, wat een aanzienlijke invloed heeft op de resultaten. De gesimuleerde spoelgeometrieën leveren inductantiewaarden op tussen 0,3 en 3,2 μH. Rekening houdend met de vermogensverliezen, wordt de toepasbaarheid van dergelijke spoelen in submodule vermogensomzetters besproken. Ten slotte wordt in **Hoofdstuk 7** het concept van COSMOS (COmbined Solar and MOSFET) apparaten geïntroduceerd en een fabricageproces voorgesteld waarbij achtercontact-TOPCon zonnecellen en laterale vermogens-MOSFETs gelijktijdig worden gefabriceerd op een enkel substraat. Dit proces wordt met succes toegepast om zowel n-type zonnecellen met geïntegreerde p-kanaal MOSFETs (PMOS) als p-type zonnecellen met geïntegreerde n-kanaal MOSFETs (NMOS) te fabriceren. Opmerkelijk is dat voor zowel n-type als p-type zonnecellen een efficiëntie van meer dan 20% wordt behaald, wat het potentieel van COSMOS-zonnecellen bewijst. Bovendien worden twee belangrijke integratie-uitdagingen geïdentificeerd. Ten eerste nemen de lekstromen van de MOSFETs toe door belichting. Ten tweede leiden specifieke topologieën van monolithische integratie tot verhoogde lekstromen.

1

Introduction

1.1. Solar energy conversion on Earth

In the center of our solar system resides the Sun, where nuclear fusion is taking place continuously [1]. This process gives rise to the emission of solar radiation throughout space, with a fraction being trapped as heat within the Earth's atmosphere. Consequently, a climate with sufficiently stable temperatures has developed, supporting life as we know it. Sunlight plays a critical role in various processes on Earth, one fundamental example being photosynthesis. Through photosynthesis, plants use sunlight to synthesize carbohydrate molecules, a process that has been ongoing for hundreds of millions of years [2]. Over time, vast quantities of plants and microorganisms have been stored and compressed in the Earth's crust, forming what we know as fossil fuels. These fossil fuels have proven very useful to humankind due to their high energy density, meaning that burning them releases a significant amount of heat per unit of weight. This process sparked the invention of the steam engine and electric generators, enabling the conversion of the chemical energy in fossil fuels into more useful forms of energy. However, fossil fuel reserves are finite and will eventually be depleted. Moreover, the burning of fossil fuels leads to rising greenhouse gas levels in the atmosphere, contributing to global warming [3]. Consequently, there is a global effort to phase out our consumption of fossil fuels.

To proceed, it is important to distinguish between some key terms. Fossil fuels fall in the category of *primary energy sources*, meaning that they are unrefined sources of energy found in nature. However, various conversion steps typically take place before these are converted into *useful energy*, such as light produced by a lightbulb or kinetic energy of a car. The challenge that humanity faces is to maintain the same access to useful forms of energy while shifting our fossil-fuel-based primary energy sources to *renewable energy sources*, which are primary energy sources that are replenished on a human timescale. It is important to recognize that many of these renewable energy sources can be linked to the solar radiation that is incident on Earth, as illustrated in Figure 1.1. For instance, biomass is formed through photosynthesis, which we can then convert to

electricity in biomass power plants. Moreover, the primary energy source of kinetic wind energy can be converted into electricity through wind turbines. Nevertheless, the emergence of wind stems from the fact that the Sun heats the Earth's surface unevenly, leading to pressure differences in the atmosphere. Additionally, hydropower generators leverage the gravitational potential energy of water as it descends due to gravity. However, the water reaches these elevated positions initially because it evaporates into clouds under the influence of solar radiation and subsequently precipitates back down as rain. Furthermore, humankind has established two methods that facilitate a more direct conversion of solar radiation into useful forms of energy. The first is *solar thermal* conversion, where solar radiation directly heats water or another fluid. The second is *solar photovoltaic* conversion, where sunlight is directly converted into electricity. This second form is the focus of interest in this dissertation. Finally, it is worth noting that there are primary energy sources not derived from solar radiation that may still play an important role for humankind. Examples of such sources include geothermal energy within the Earth, as well as the atoms used for nuclear fission and nuclear fusion.

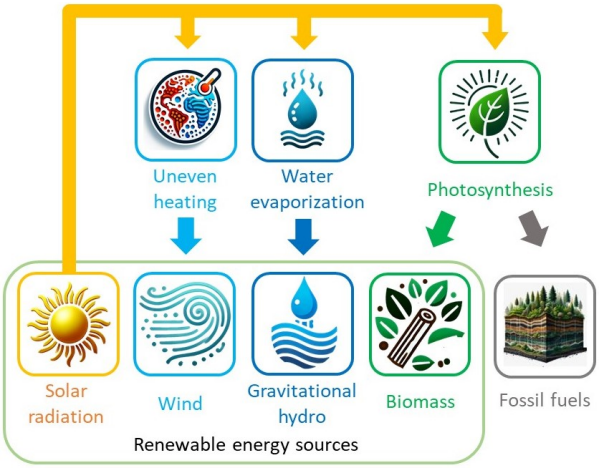


Figure 1.1: Various renewable and fossil fuel energy sources are linked to solar radiation.

1.2. Solar photovoltaic technology: from cell to system

Solar photovoltaic (PV) technology functions by directly converting solar radiation into electricity [1]. The building blocks of this technology are *photovoltaic cells*, also referred to in this thesis as *solar cells*. Solar cells are typically made of semiconductor material, which has the property of liberating electrons upon exposure to sunlight. Once an electron is liberated, it can move freely through the material, leaving behind an empty space—also called a hole—that acts as if it has a positive charge. The solar cell is designed so that, after electron-hole pairs are generated in the absorber, they are separated and directed to opposite electrodes. These electrodes serve as connection points to an external circuit, allowing the solar cell to establish an electric current. Currently, about 97% of the global solar PV market relies on solar cells made of crystalline silicon (c-Si)

absorber material [4].

Perhaps the most important figure of merit for a solar cell is its solar-to-electricity power conversion efficiency, often referred to as simply *efficiency*. The efficiency of solar cells is typically evaluated under standard test conditions (STC), which are defined by an irradiance of 1000 W/m^2, an AM1.5 spectrum, and a solar cell temperature of 25 °C [1]. At the time of writing this thesis, the record efficiency of c-Si solar cells stands at 27.4% [5]. This is remarkably close to the fundamental efficiency limit of c-Si solar cells, which is 29.4%* [6]. Additionally, the power produced by the solar cell under STC is called the *power rating*, measured in the unit watt-peak (Wp).

A typical area of modern commercial c-Si solar cells is approximately 220 cm^2 †. Assuming an efficiency of 25%, the typical power rating of such a solar cell is around 5.5 Wp. To put this in perspective, the hairdryer I have at home consumes a maximum power of 2300 W. Thus, a single solar cell will not do the job of powering household electrical appliances. Therefore, multiple solar cells are typically connected into *strings*, and laminated between glass and a backsheet, forming a so-called *PV module*. It is worth noting that a PV module usually has a somewhat lower efficiency than the individual cells it contains. While the highest efficiency of c-Si-based PV modules stands at 25.4% [7], the modern mass-production efficiency is around 22% [8–10]. Although the area of PV modules varies, most commercial PV modules have an area ranging from 1.8 m^2 to 3 m^2 [11]. Assuming 22% efficiency, their typical power rating ranges between 400 Wp and 660 Wp.

Thus, embedding multiple solar cells in a module brings solar PV technology closer to powering household electrical appliances. However, the power rating of a modern PV module is still substantially lower than the maximum power consumed by my hairdryer. Additionally, household electrical appliances are built to receive alternating current (AC) from the socket, where the electric current periodically reverses direction and continuously changes magnitude. In contrast, PV modules produce direct current (DC), which flows in only one direction. Therefore, to power my hairdryer, a *PV system* must be installed. A PV system comprises multiple electrically connected PV modules, as well as power electronics to ensure the conversion of DC power to AC. Additionally, the system includes components such as racking and wiring. Figure 1.2 illustrates the terminology from PV cell to PV system, which will be used throughout this thesis.

1.3. The rise of solar photovoltaics

Figure 1.3 shows the price development of PV technology over recent decades. It is illustrated how the module price has decreased from 126 USD/Wp in 1975 to 0.26 USD/Wp in 2022 [14]. This rapid reduction was mainly driven by technological advancements and increased economies of scale [15]. As a result, the non-modular costs of PV systems (e.g. power electronics, racking, permitting etc.) are nowadays typically higher than the PV module costs. Based on the data in Figure 1.3, the non-modular cost as a fraction of the total cost in utility-scale PV systems has increased from 55% in 2010 to 71% in 2022.

* The solar-cell efficiency limit increases to 42.8% when a cell made of another absorber material is placed on top of the c-Si solar cell, forming a so-called X-on-Si tandem cell [12]. The highest X-on-Si tandem cell efficiency reported to date is 34.6%, achieved with a perovskite top cell [13]. However, the extent to which such devices will be able to capture PV market share remains uncertain.

† Commercial solar cells vary in size. For this case, we take the approximate area of a half-cut G12 wafer [11].

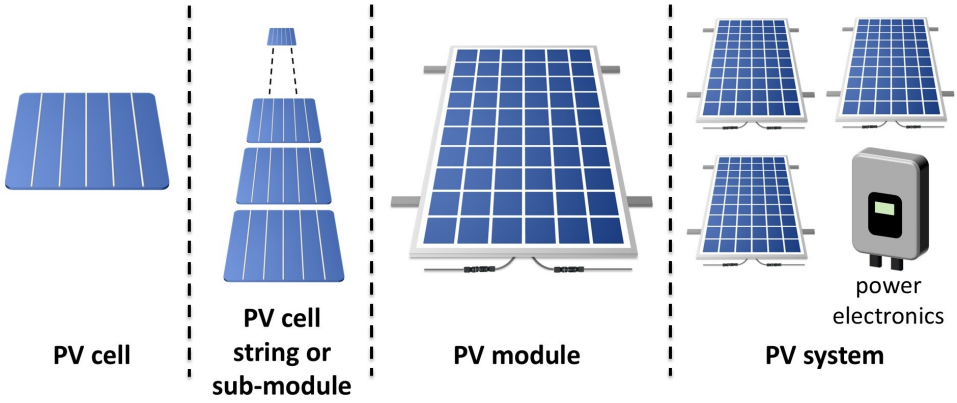


Figure 1.2: PV technology: from cell to system. The PV module figure was provided by courtesy of Patrizio Manganiello.

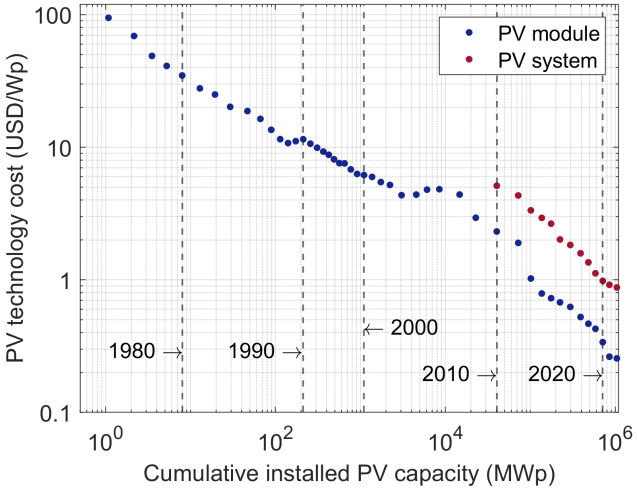


Figure 1.3: The cost of PV technology is plotted against the cumulative installed capacity, with various years highlighted to indicate specific points in time. The PV module cost data is sourced from [14]. The PV system cost data is the global capacity weighted average cost for utility-scale PV systems sourced from [16].

The cost per rated power of a PV module or system is measured in USD/Wp. However, to meaningfully compare the costs of solar PV-generated electricity with other generation technologies, we must examine the price per unit of generated electricity in USD/kWh. Unlike power, which is measured in Watts (Joules per second), kWh is a unit of energy, where one kWh equals 3.6 MJ. In the USA, the levelized cost of electricity (LCOE) for solar PV in 2022 was reported at 0.046 USD/kWh, which was 29% cheaper than the cheapest fossil fuel-fired solution*. In countries with higher solar irradiation the LCOE is even lower, such as 0.026 USD/kWh in the United Arab Emirates [16].

* A direct comparison between the LCOE of a temporally non-controllable electricity generator and that of a

As of 2023, the worldwide installed PV capacity stands at 1.58 TWp [4], accounting for 2.3% of global primary energy consumption† [17] and 5.5% of the global electricity mix [18]. Research on the future of renewable energy systems predicts that further electrification will take place across all energy sectors, and solar radiation and wind energy will emerge as the main primary energy sources [19–21]. For the optimal design of such an energy system, it is important to acknowledge that we cannot control when the sun shines and when the wind blows. In this context, promising results have been found regarding the economic viability of short-term electricity storage in batteries [22, 23] and conversion to hydrogen for industrial or long-term storage purposes [24]. However, minimizing the overall costs of such an energy system involves limiting the required storage capacity. Key approaches contributing to this include: (1) selecting an appropriate ratio between installed solar and wind capacity to ensure complementary temporal generation profiles [25]; (2) implementing continent-scale balancing of renewable fluctuations [26]; and (3) demand-side management, which involves actions that affect consumers' electricity utilization patterns [27].

1.4. The crucial role of power electronics in PV systems

Power Electronics (PE), which is based on the application of electronics to the control and conversion of electric power [29], is essential for optimizing the performance of PV systems. The fundamental elements of PE are active semiconductor devices such as diodes and power transistors, along with passive components like capacitors and inductors. Throughout this thesis, these elements are referred to as power electronic *components*. Using PE components it becomes possible to build power converters, which often serve as the building blocks of power electronic systems. The term *power converter* refers to a single power conversion stage that performs one of the following four types of power conversion: (1) AC to DC (rectifier), (2) DC to AC (inverter), (3) DC to DC, and (4) AC to AC [29]. Typically, assembling a power converter involves soldering and interconnecting PE components on a printed circuit board (PCB). Figure 1.4(a) shows a photo of an exemplary disassembled solar inverter, where important PE components for this thesis are highlighted.

A PV system typically contains one or multiple solar inverters, each of which has two main functions. The first function is maximum power point tracking (MPPT), which aims to continuously adapt the operating point of the PV modules to produce their maximum power. The second function is the DC-AC conversion to supply AC power to a household or the electricity grid. Such solar inverters may either be single-stage (e.g. only a DC-AC converter with MPPT capability) or two-stage (e.g. DC-DC converter for MPPT with a separate DC-AC converter) [31, 32]. In utility-scale multi-megawatt PV power plants, the central inverter topology is commonly used. In this setup, multiple strings of series-connected PV modules are connected in parallel to a single central inverter, which supplies power to the three-phase medium voltage grid [1, 33]. For

controllable generator is not entirely fair. Fossil fuel generators can be adjusted to meet the demand, while renewable electricity generators should be accompanied by some form of electricity storage, adding extra costs.

† To obtain this number, the substitution method was used. This method corrects non-fossil energy sources for the efficiency losses experienced by fossil fuels. Thus, primary energy generation from non-fossil sources are divided by a factor of around 0.4 [28].

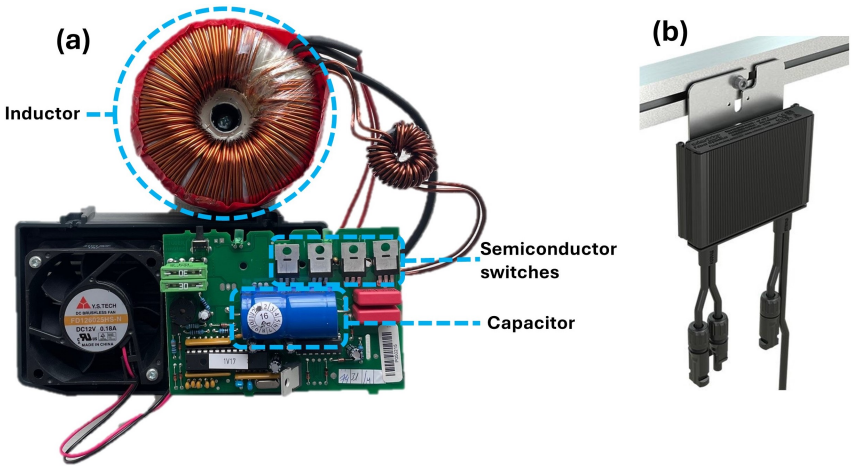


Figure 1.4: (a) The interior of an exemplary disassembled solar inverter. Highlighted are the PE components relevant to this thesis: the inductor, semiconductor switches, and capacitor. (b) The exterior of an exemplary power optimizer taken from [30], which can be mounted on the PV module frame or the racking system.

smaller PV power plants and industrial buildings, the string inverter topology is often employed. In this arrangement, each string of series-connected PV modules is connected to its own inverter, allowing the strings to be operated at their individual MPP [1, 33]. While having a low number of solar inverters per system reduces costs, this approach also has drawbacks. For instance, in a string of series-connected PV modules, the current is limited by the module with the lowest current. If a single module in the string receives less irradiance than the rest, it will limit the current of the whole string. Consequently, while central inverter and string inverter topologies are effective for large-scale PV power plants, they may be less suitable for urban integration. For instance, rooftops may have obstructions such as chimneys or trees that cast shadows on portions of the PV system. As a result, systems with module-level PE are being increasingly adopted in global PV installations. With module-level PE, the operating point of individual PV modules can be adjusted without affecting the operation of other modules in the string. Additionally, module-level PE offers improved safety capabilities and fault detection [34, 35]. The relatively low power levels associated with module-level PE facilitate the use of compact designs, as illustrated by the photo of an exemplary power optimizer in Figure 1.4(b). Module-level PE can be implemented in different ways, either replacing or working alongside traditional central PV inverters. For instance, DC-DC converters with MPPT capability (power optimizers) can be deployed at the module level, connecting to the input of a central inverter for DC-AC conversion [36]. Alternatively, the micro-inverter topology eliminates the need for a central inverter by implementing solar inverters at each module [37]. Additionally, PV module-integrated micro-inverters may faciltate the development of wireless PV modules [38–40].

Furthermore, PE plays a crucial role at the level of solar cell strings within PV modules, also called the *sub-module level*. It is well known that PV modules are affected by current mismatching between different cells, which can be caused by factors such as

inhomogeneities during production, partial shading, dirt, thermal gradients, or aging [41]. When certain cells of a PV module become shaded, they might become reverse biased, acting as loads instead of generators. This can lead to hot-spot issues, irreversibly damaging the affected cells [42]. Conventionally, this effect is mitigated by connecting bypass diodes in antiparallel to different strings of series-connected cells within the PV module [43]. Typically, the bypass diodes are placed and interconnected in the junction box at the back of the PV module, an example of which is shown in Figure 1.5(a). However, the incorporation of bypass diodes does not completely eliminate hot-spot problems [44]. Additionally, the power production of these standardized PV module designs drops substantially under non-uniform operating conditions. For instance, the power production of an entire string can be lost when only a single PV cell in the string becomes shaded [45]. Thus, to further improve the reliability and energy yield of PV systems under non-uniform operating conditions, different PV module topologies are being investigated [41, 46, 47]. Studies have shown that the energy yield in locations with partial shading can be increased by up to 25-30% when shade-resilient PV modules are used instead of conventional designs [48, 49]. For instance, one approach is to increase the number of bypass diodes [50, 51]. However, this method introduces power losses when the diodes are activated. To limit these losses, some publications suggest using transistors to perform the bypass functions, resulting in reduced power losses during bypassing [52–56]. Beyond bypass elements, various other topologies utilize more advanced sub-module PE to create shade-tolerant PV modules. One such approach is the reconfigurable module concept, where series and parallel interconnections of groups of cells can be changed during operation to optimize energy yield depending on the uniformity of illumination [57–59]. In Figure 1.5(b), a prototype of a reconfiguration matrix board is shown, which could be placed in the module's junction box. Another approach is to perform power conversion at the sub-module level, allowing for MPPT with higher granularity [60–62]. This way, the operating point of smaller groups of solar cells can be adapted without affecting the operation of the other cells in the PV module. It has been reported that module-level or sub-module-level power converters can mitigate variations in cell degradation over time, effectively increasing the system lifespan by 5–10 years compared with the nominal 25-year lifetime [41]. it is worth noting that their analysis follows a power converter failure model accounting for 5% failure rate of the converters after 25 years and 20% after 50 years.

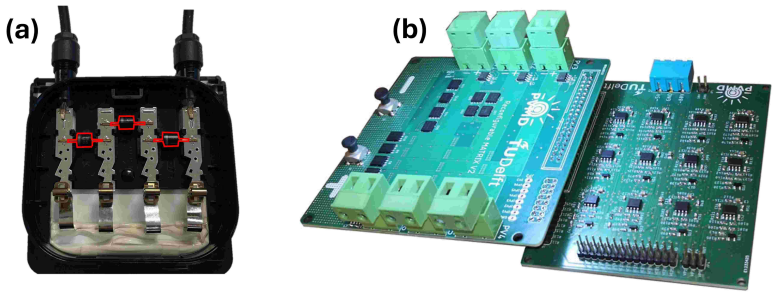


Figure 1.5: Sub-module level PE: (a) The inside of a junction box with its bypass diodes highlighted. (b) Prototype of a reconfiguration matrix board [58].

1

Furthermore, besides its role in full-sized cells and modules, PE is also important in low-power and low-current PV applications. For instance, PE increases energy yield and extends battery life in low-power autonomous devices with PV-battery combinations [63]. Another example is the Tessera module, where industrial cells are divided into smaller units and in-laminate low-current bypass diodes are employed [64].

1.5. Motivation for solar-cell-integrated power electronics

Module-level PE, such as a DC-DC power optimizer, is typically attached to the PV module frame or racking system [30]. For sub-module purposes, the PE is often installed in the PV junction box [65–67], but it can also be embedded into the PV laminate [60, 68, 69]. However, in this dissertation another approach is investigated: integrating power electronics into or onto c-Si solar cells [70], which can take various forms. For instance, one approach aims to exploit the inherent capacitive and inductive properties of solar cells [71–73]. Moreover, PE components can be integrated into or onto the solar cells during the manufacturing process [74–76]. The concept of PE-PV integration is shown schematically in Figure 1.6. The subsequent part of this section outlines the motivation and potential benefits of PE-PV integration.

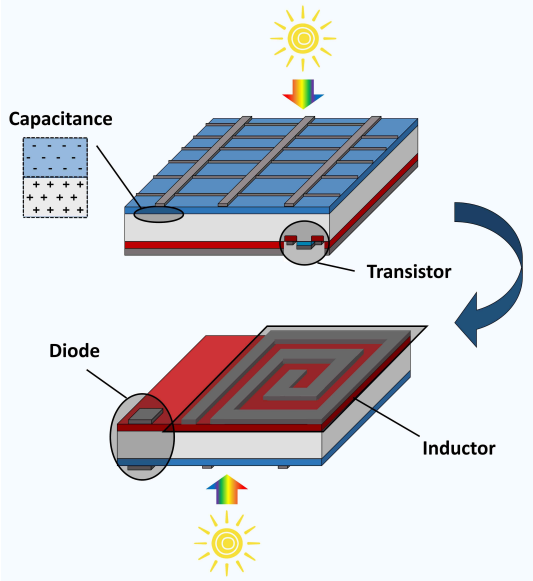


Figure 1.6: Concept of PE-PV integration. This figure was the graphical abstract of a publication that is part of this thesis [70].

As explained in the previous section, there are various ways in which sub-module PE can increase the shade tolerance of PV modules. However, implementing the PE into the junction box can result in a bulkier junction box design. Additionally, as PE become more granular and is serving smaller groups of cells—and ultimately each individual cell— the required wiring becomes increasingly complex. To address this challenge, integrating

PE directly into the laminate may emerge as a more practical solution. This could involve embedding discrete PE components into the laminate [60, 68, 69], or integrating PE components into or onto the solar cells. For example, integrating bulkier PE components onto solar cells could enable compact system-on-chip solutions that can be laminated anywhere in the PV module for granular power optimization. Taking these ideas one step further, a combination of laminated and solar-cell-integrated PE could even eliminate the need for junction boxes altogether. If most power electronics were integrated into the cells themselves, only the driving circuits of the power semiconductor switches would remain. These circuits are small enough to potentially be laminated into the gaps between PV cells. Furthermore, solar-cell-integrated PE could support highly customized designs, making it particularly suited for applications like vehicle-integrated or building-integrated photovoltaics.

In section 1.4, it was noted that the implementation of sub-module-level PE can increase the PV system lifetime. However, it has to be taken into account that each of the individual PE components that is added has a probability to fail, which could eventually affect the system reliability. Especially failure in the solder joints of discrete power transistors has been identified as one of the main failure modes of power converters in PV applications [77, 78]. This issue could potentially be mitigated by integrating transistors directly into the PV cells and connecting them monolithically, which may enhance reliability relative to conventional printed circuit board configurations. Nevertheless, since solar-cell-integrated PE could also introduce new failure modes, further investigation is required.

Furthermore, an important advantage of integrating PE into the solar cells is that the overall volume and weight of a PV system can be reduced. This can be especially advantageous for specific applications, such as space-based systems, where silicon PV technology already plays an important role [79].

Finally, there are various autonomous devices available on the market that are directly powered by PV cells. For example, many consumer or lighting products are presented in [80]. Additionally, using PV to power wireless sensors for Internet of Things (IoT) applications is gaining attention [81–84]. In such autonomous devices, PE is typically deployed to perform MPPT [85, 86]. Since in these applications the power electronics is often working with a low number of cells already, the integration of part of the PE into the cells may be more straightforward than for complete PV modules. Additionally, as these PV cells often produce small currents, the design of the PE components is simpler. If manufacturers of autonomous devices powered by PV could directly buy PV cells that can condition their power, the remaining fabrication process would be simplified significantly.

1.6. Aim and outline

The aim of this dissertation is to study the integration of different PE components into c-Si solar cells, and identify the most promising approaches. Following this introductory chapter (Chapter 1), the thesis is organized in two parts. The outline is as follows:

In **Part I**, the objective is to gain a thorough understanding of the capacitive and inductive properties of modern c-Si solar cells. These properties are analyzed by studying

the electrical impedance, which is defined as the frequency-dependent ratio between the AC voltage and AC current in a circuit. It describes both the magnitude ratio and the phase shift between the two AC signals [87]. The chapters of Part I are as follows:

- In **Chapter 2**, the impedance of eight different modern commercial c-Si solar cells is characterized in dark conditions at room temperature. By comparing their capacitive and inductive properties, further insights are gained into the relationship between impedance and solar-cell design.
- In **Chapter 3**, the impedance of PN junctions at high frequency is analyzed, and it is shown how commonly used small-signal models fail to fully capture the underlying device physics. Moreover, the impedance of low-high junctions is investigated.
- In **Chapter 4**, the variation in impedance of modern c-Si solar cells is investigated across different temperature and illumination conditions. Additionally, the range within which the capacitance of solar cells varies during practical operation is identified.

In **Part II**, the aim is to assess the feasibility of leveraging solar-cell impedance at the input of a power converter, and to explore various methods for integrating additional PE components into or onto solar cells. The chapters of Part II are as follows:

- In **Chapter 5**, the feasibility of integrating different PE components into c-Si solar cells is explored. This includes leveraging the intrinsic solar cell impedance as well as integrating additional power electronics. The analysis covers diodes, transistors, capacitors, and inductors.
- In **Chapter 6**, the integration of planar air-core inductors into PV modules is investigated. It is shown how various design parameters of a planar inductor affect its inductance and resistance. Additionally, the losses associated with implementing these coils into sub-module power converters are evaluated.
- In **Chapter 7**, the COmbined Solar cell and MOSFET (COSMOS) device is introduced. Specifically, it is reported how TOPCon back-contact solar cells with integrated power MOSFETs are fabricated. Additionally, the performance of these devices and their interactions are evaluated.

Finally, the conclusions of this dissertation are presented in **Chapter 8** together with recommendations for further research.

1.7. Main contributions to the field

The specific main contributions of this thesis to the field can be summarized as follows:

- A comprehensive impedance characterization is conducted for modern crystalline silicon solar cells, revealing the relation between cell properties and impedance.
- A deeper understanding has been achieved regarding the high-frequency impedance of the PN junction and the influence of the low-high junction.

- The dynamic resistance and capacitance of the PN junctions in solar cells are quantified at the maximum power point under varying temperature and illumination conditions.
- A comprehensive exploration is reported regarding the feasibility of integrating diodes, transistors, capacitors, and inductors into c-Si solar cells.
- A feasibility study is conducted related to the integration of planar air-core inductors onto solar cells into PV modules, with the aim of supporting sub-module power conversion.
- It is demonstrated that back-contact solar cells with integrated MOSFETs can be successfully fabricated with a relatively small number of additional processing steps compared to the reference solar-cell manufacturing.

I

Analysis of the crystalline silicon solar-cell impedance

2

Revealing the capacitive and inductive effects in modern commercial solar cells

This chapter is based on the following publication:

D. A. van Nijen, M. Muttillo, R. van Dyck, J. Poortmans, M. Zeman, O. Isabella, and P. Manganiello, "Revealing capacitive and inductive effects in modern industrial c-Si photovoltaic cells through impedance spectroscopy" in *Solar Energy Materials and Solar Cells*, vol. 260, 112486, 2023.

The data underlying this chapter was published in the 4TU Research Data Archive [*].

2.1. Introduction

In photovoltaic (PV) systems, the main purpose of solar cells is to produce a direct current (DC) upon exposure to sunlight. Much of the research and development in solar energy focuses on enhancing the efficiency of solar cells in converting light into electrical power. Nevertheless, there is also growing interest in exploring and optimizing the impedance of solar cells, which describes their response to small-signal high-frequency alternating current (AC) signals. For instance, studying the solar-cell impedance can rapidly gather large amounts of data for efficient and accurate measurements of a variety of solar cell parameters [88–90]. Additionally, the solar-cell impedance influences the performance of power electronics that perform maximum power point tracking (MPPT). To achieve a high performance in such power-conditioning circuits, it is important that

[*] D. A. van Nijen et al., "Data underlying the publication: Revealing capacitive and inductive effects in modern industrial c-Si photovoltaic cells through impedance spectroscopy." 4TU.ResearchData, Oct. 14, 2023, `https://doi.org/10.4121/0c9538d5-5930-4ae5-a3c7-0a8dbe4b94f5.v1`.

the converter is designed in accordance with the solar-cell impedance at the input [91]. Taking this one step further, it has been proposed to exploit the self-impedance of solar cells, which could lead to the development of converters that require fewer passive components at the input. For instance, in different types of power converters, an input capacitor is used to reduce the ripple voltage at the input of the converter [92]. If such a converter were used in a PV module to implement MPPT at cell or sub-module level, the self-capacitance of the solar cells could potentially fulfil the function of this input capacitor [70]. Since the capacitor is typically one of the least reliable components in power converters [93], this approach can increase reliability. It was even proposed to extend this concept to low-power applications by also exploiting the inductive effects in a PV cell string [72]. In a somewhat similar application, it has been reported that the solar cell self-capacitance can be used for power balancing among different cells [71]. Moreover, the impedance of solar cells impacts their suitability for applications beyond energy generation, such as Visible Light Communication (VLC) systems. In such systems, where solar cells can be simultaneously employed as power sources and receivers [94–96], the impedance directly influences the system's bandwidth [97]. These examples highlight the potential of solar-cell impedance analysis to reveal intrinsic device characteristics and pave the way for innovations. In contrast, it is worth noting that the capacitive effects in solar cells may also lead to unwanted effects. For example, the capacitance of c-Si solar cells is known to limit the minimal time required for current-voltage (*I-V*) measurements [98, 99].

To assess the feasibility of the above-mentioned applications, a detailed understanding of the impedance in modern industrial c-Si solar cells is crucial. Impedance spectroscopy is an established method for characterizing the impedance of nonlinear electronic devices such as solar cells [100]. Various impedance spectroscopy studies on c-Si PV cells have already been published, in which dynamic equivalent circuits of the PV cells are typically fitted to the experimental impedance data. For example, several studies have been performed for small-area c-Si PV cells up to 32 cm^2 [88, 89, 91, 101–107]. Moreover, there are several reports in the context of fault detection in which impedance spectroscopy is performed on larger cells and modules [108–111]. Furthermore, the authors of [112] have characterized capacitive effects in modern PV modules by performing direct and reverse *I-V* measurements with a pulsed solar simulator. However, their method does not take into account frequency-dependent effects and is intended to evaluate the minimum pulse time required for an accurate *I-V* measurement.

In this chapter, the impedance of single-cell laminates made with eight different commercial c-Si PV cells is characterized. Among these cells, the main available architectures, such as Aluminium Back Surface Field (Al-BSF), Passivated Emitter and Rear Contact (PERC), Tunnel Oxide Passivated Contact (TOPCon), Interdigitated Back Contact (IBC), and Silicon Heterojunction (SHJ) are included. To our best knowledge, this is the first work in which the impedance of such a broad range of large-area industrial cells is systematically compared. The measurements are carried out in dark conditions with an in-house designed impedance spectroscopy setup. Furthermore, the capacitive and inductive effects of the cell laminates are evaluated through equivalent model fitting, and the differences are explained by analyzing the underlying physics. This way, it is revealed how the dynamic behaviour of a c-Si solar cell is affected by its design.

2.2. Experimental Method

2.2.1. Cell laminates used for this study

For this study, single-cell laminates were manufactured using eight different industrial c-Si PV cells. The laminates are shown in Figure 2.1, and the exact corresponding laminated stacks are presented in Table 2.1. It is worth noting that the different cells varied in size, as well as in metallization patterns.

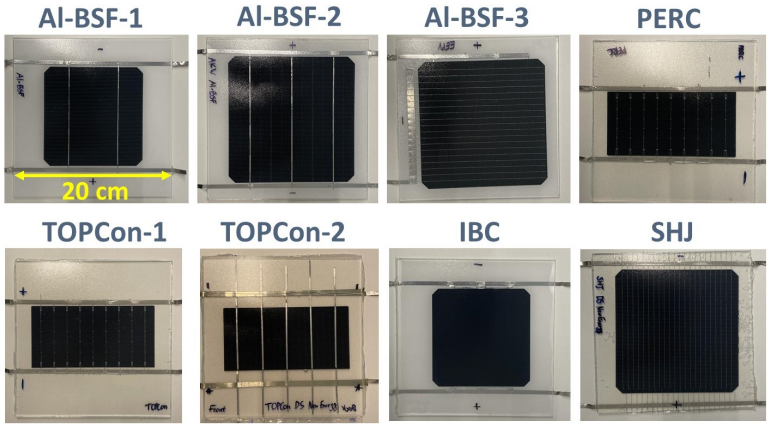


Figure 2.1: Photos of the single-cell laminates used for this study. The details of the lamination stacks are presented in Table 2.1.

Table 2.1: Overview of the materials and metallization structure that were used for the different laminates. Each row corresponds to one of the laminates in Figure 2.1. The term busbar is abbreviated by BB, SmartWire by SW, back-contacted by BC, and a white backsheet from Icosolar PPF by WBS. The SW connection uses round wires with a 200 μm core and a eutectic SnBu solder coating. The glass plates that are used are low Fe borosilicate glass without anti-reflection coating and the encapsulants are commercially available EVA and TPO. The ribbons that are used to connect the cells to external setups are commercial 0.2 mm × 0.5 cm Cu PV ribbons with a eutectic SnBi solder coating.

Laminate ID	Mono (M)/ Bifacial (B)	Cell area (cm^2)	Front	Front encapsulant	Metal front side	Active layer	Metal back side	Rear encapsulant	Back
Al-BSF-1	M	153	glass	EVA	2BB	Al-BSF	2BB	EVA	WBS
Al-BSF-2	M	244.3	glass	EVA	3BB	Al-BSF	3BB	EVA	WBS
Al-BSF-3	M	244.3	glass	EVA	SW, 19W	Al-BSF	4BB	EVA	WBS
PERC	B	126	glass	TPO	9BB	PERC	9BB	TPO	glass
TOPCon-1	B	126	glass	TPO	9BB	TOPCon	9BB	TPO	glass
TOPCon-2	B	126	glass	TPO	5BB	TOPCon	5BB	TPO	glass
IBC	M	153	glass	EVA	-	IBC	BC	EVA	WBS
SHJ	B	244.3	glass	TPO	SW, 22W	SHJ	SW, 22W	TPO	glass

For all of the laminates in Figure 2.1, *I-V* measurements were carried out in Standard Test Conditions (STC) as well as dark conditions, which are presented in Figure 2.2(a) and Figure 2.2(b), respectively. These *I-V* scans were performed using a LOANA solar cell analysis system [113]. The corresponding STC parameters are presented in Table 2.2, where the global series resistance is found from comparing the J_{sc}-V_{oc} measurement with light-IV and the double light method [113].

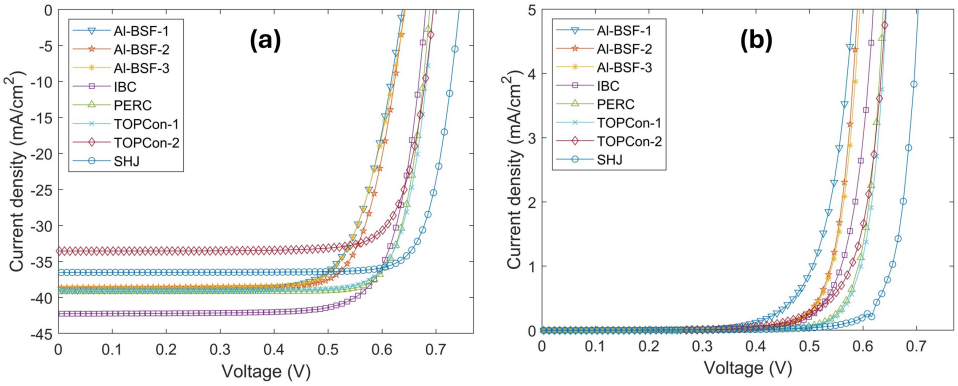


Figure 2.2: (a) *I-V* curves of the single-cell laminates in STC conditions. (b) *I-V* curves of the single-cell laminates in dark conditions. These measurements were conducted using a LOANA solar cell analysis system.

Table 2.2: STC parameters of the single-cell laminates used for this study, as characterized with a LOANA solar cell analysis system.

Laminate ID	J_{sc} **(mA/cm^2)**	V_{oc} **(mV)**	FF **(%)**	η **(%)**	V_{mpp} **(mV)**	I_{mpp} **(A)**	R_s **(Ω cm^2)**
Al-BSF-1	38.92	637.6	73.44	18.22	506.2	5.51	1.35
Al-BSF-2	38.66	641.3	76.71	19.02	521.4	8.91	1.10
Al-BSF-3	38.65	643.2	73.75	18.33	505.8	8.86	1.65
PERC	39.18	688.1	81.35	21.93	586.6	4.71	0.55
TOPCon-1	38.96	694.7	80.30	21.73	588.6	4.65	0.72
TOPCon-2	33.54	695.1	79.34	18.50	587.4	3.97	0.65
IBC	42.25	680.7	76.97	22.14	566.1	5.98	0.85
SHJ	36.52	743.0	81.52	22.12	635.8	8.50	0.94

2.2.2. Impedance spectroscopy setup

Commercial impedance spectroscopy setups are typically not suitable to characterize the laminates used in this study. For the large-area cells, DC currents higher than 0.5 A are already exceeded in dark conditions at DC bias voltages around 0.6 V. The characterization of devices at such high DC current and relatively low DC voltage levels using commercial setups is incompatible with the frequency range of interest, which extends into the kHz range (>5 kHz). To characterize the cells in a wide voltage range, an in-house impedance spectroscopy setup was designed, which is schematically represented in Figure 2.3. The DC bias and the small-signal sinusoidal waveforms are set through an Agilent 33250A function generator. The DC voltage on the PV cell is measured using a Keithley 2000 Multimeter. To increase the output current capability of the function generator, an OPA549 op-amp supplied by two EA-OS 2042-20 B power supplies is used in power buffer configuration. For accurate and high-speed analysis of these signals, the impedance data reported in this manuscript are obtained by analyzing the waveforms through lock-in amplifiers. The sinusoidal current signal $\hat{i}$ is measured using a Yokogawa 702916 current probe that is connected to a Signal Recovery 7225 DSP lock-in am-

plifier. The sinusoidal voltage signal $\hat{v}$ is recorded through an EG&G Instruments 7260 DSP lock-in amplifier, where the voltage probe of channel A is connected to the positive contact of the solar cell, and the voltage probe of channel B to the negative side. By using the A-B setting of the lock-in amplifier, the difference between the two input voltages is measured. Since the voltage and current signals are measured separately, parasitic cable influences are limited in a way that is similar to four-terminal sensing. For both lock-in amplifiers the reference channel is connected to the function generator, making it possible for both $\hat{v}$ and $\hat{i}$ to extract the root-mean-square (RMS) amplitude and the phase shift relative to the function generator waveform.

The impedance of the PV cells is characterized in a frequency range between 5 Hz and 120 kHz. This upper bound is limited by the maximum frequency of the 7260 DSP lock-in amplifier. Setting the DC bias voltage on the PV cell, performing frequency sweeps with the function generator, and recording the values from the lock-in amplifier were done through an in-house developed Labview program. This level of automation ensures repeatability of the experiments and minimizes human error.

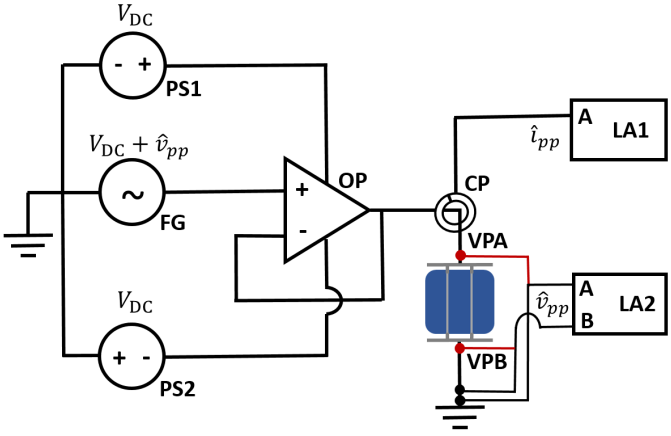


Figure 2.3: Overview of the in-house designed impedance spectroscopy setup used for this study. Power supplies 1 (PS1) and 2 (PS2) are both of the type EA-OS 2042-20 B. The function generator (FG) is an Agilent 33250A, whereas the op-amp (OP) is of the type OPA-549 and is connected in power buffer configuration. Lock-in amplifier 1 (LA1) and 2 (LA2), are a Signal Recovery 7225 DSP and a EG&G Instruments 7260 DSP, respectively. The current probe (CP) is a Yokogawa 702916, and is connected to channel A of LA1. Voltage probe VPA, which is connected to the positive contact of the PV cell, is analyzed through channel A of LA2. Voltage probe VPB, which is connected to the negative side of the PV cell, is analyzed through channel B of LA2.

Solar cells are nonlinear devices, meaning that the current generally varies nonlinearly with applied voltage. Consequently, to achieve a linear impedance response, the amplitude of the sinusoidal signal ($\hat{v}_{\mathrm{pp}}$) that is applied about a DC operating point should be sufficiently small so that the amplitude of $\hat{i}$ varies pseudolinearly with the amplitude of $\hat{v}$. If this is achieved, small changes to the amplitude of $\hat{v}$ result in linear changes in the amplitude of $\hat{i}$, but no change in the impedance [100]. In previous work, $\hat{v}_{\mathrm{pp}}$ values between 10 $\mathrm{mV_{pp}}$ and 28 $\mathrm{mV_{pp}}$ are typically chosen for impedance spectroscopy measurements on c-Si PV cells to avoid nonlinearities [88, 89, 91, 101–104].

It is worth noting that nonlinearities are most likely to affect measurements in DC bias points where the *I-V* curve exhibits the most curvature. For example, to evaluate the effect of nonlinearities on the impedance measurements performed with the setup in this work, the IBC cell is characterized at V_{DC} = 550 mV with a varying amplitude $\hat{v}_{\mathrm{pp}}$. It can be seen in Figure 2.2(b) that this operating point corresponds to a relatively strong curvature in the dark *I-V* curve. In Figure 2.4, the impedance data are presented for a frequency range between 25 Hz and 5 kHz in the form of Nyquist impedance spectra. In such a representation, the real part of the impedance is shown on the horizontal axis and its imaginary part on the vertical axis, both in Ohm (Ω). It can be seen how a too high amplitude $\hat{v}_{\mathrm{pp}}$ indeed affects the recorded impedance data. Specifically, nonlinearities at higher amplitudes lead to an underestimation of the impedance, and such underestimation becomes smaller with increasing frequency. However, for both $\hat{v}$ and $\hat{i}$, a minimum amplitude is required to maintain a good signal-to-noise ratio during a measurement. Especially around zero bias on a PV cell with a high shunt resistance, the current signal is limiting in this respect. In this work, the amplitude is minimized for each individual impedance measurement. Generally, $\hat{v}_{\mathrm{pp}}$ is limited to a maximum value of 6 $\mathrm{mV_{pp}}$ for V_{DC} values of 400 mV and higher.

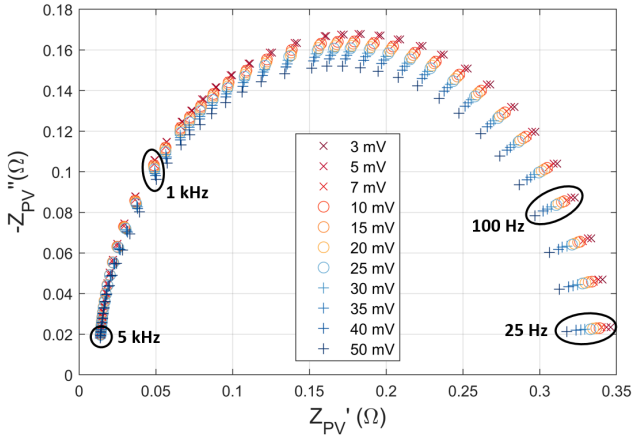


Figure 2.4: Experimentally recorded Nyquist spectra for the IBC cell at a DC bias voltage of V_{DC} = 550 mV. The spectra were characterized at a varying peak-to-peak amplitude $\hat{v}_{\mathrm{pp}}$ of the small sinusoidal signal, as indicated in the legend.

2.3. Theory

2.3.1. PN junction impedance

The dominant physical mechanisms that drive the PN junction current vary with the bias voltage [114]. At reverse bias, the generation current —arising from an imbalance between generation and recombination within the depletion region—plays an important role. At low forward bias, the current is typically dominated by recombination of charge carriers within the depletion region. At high forward bias, the current is governed by the flow of majority carriers across the depletion region, where they are subsequently in-

jected as minority carriers into the opposing quasi-neutral regions. In the quasi-neutral regions, the transport of these minority carriers is diffusion-driven due to the absence of a significant electric field. In this high forward-bias regime, the current-voltage characteristic of the PN junction can be described by the ideal diode equation [114]:

$$I_d = Aqn_i^2 \left[\frac{1}{N_a}\sqrt{\frac{D_n}{\tau_{n0}}} + \frac{1}{N_d}\sqrt{\frac{D_p}{\tau_{p0}}} \right] \left[\exp\left(\frac{qV_F}{kT}\right) - 1 \right] \tag{2.1}$$

where A is the cross-sectional area of the PN junction, q is the elementary charge constant, n_i is the intrinsic carrier concentration, and N_a and N_d are the acceptor and donor concentrations. Additionally, D_p and D_n are the diffusion constants of minority carrier holes in n-type material and minority carrier electrons in p-type material, respectively. Moreover, τ_{p0} and τ_{n0} are the effective minority charge carrier lifetimes. Finally, V_F is the applied forward-bias voltage, k is the Boltzmann constant, and T is the temperature. It is worth noting some assumptions that were used in deriving Equation 2.1 [114]:

- The PN junction consists of homogeneously doped regions.
- The abrupt junction approximation is applied, which assumes that there is an abrupt discontinuity in space charge density between the space charge region and the neutral semiconductor region.
- The Maxwell-Boltzmann approximation is applied to the Fermi-Dirac distribution function.
- Low-level injection conditions are valid, where the excess minority carrier concentrations are much smaller than the thermal-equilibrium majority carrier concentrations.
- The quasi-neutral p-type and n-type regions are long compared to the minority carrier diffusion length.

A complete discussion on the applicability of these assumptions to modern solar cells is out of the scope of this thesis. However, it is important to understand that there are limitations in applying Equation 2.1 to PN junctions in solar cells. For instance, in solar cells the diffusion length is typically much greater than the length of the quasi-neutral regions to facilitate the collection of photogenerated carriers. An alternative derivation uses the short diode approximation, which assumes a much larger diffusion length relative to the quasi-neutral region length, leading to a pseudolinear variation of the minority carrier concentration with distance. However, this approximation is also not directly applicable to solar cells, which typically incorporate low-high junctions that oppose minority carrier motion towards that electrode [115, 116]. Indeed, a well-performing low-high junction is characterized by a low surface recombination velocity or contact recombination rate [117, 118]. Considering these complexities, τ_{p0} and τ_{n0} in Equation 2.1 may be interpreted as *effective* lifetimes. Similarly, the concept of effective diffusion length is commonly used in publications that describe the current-voltage characteristics of silicon solar cells [118–121].

In a more general current-voltage expression, I_d varies with V_F following the relationship $I_d = I_s \exp\big((qV_F)/(nkT)\big)$, where I_s is the saturation current and n is the diode ideality factor. While the values of I_s and n give useful insights into the solar-cell characteristics, a single constant value for these parameters is typically not sufficient to represent the physical reality [122]. For instance, their values often vary with the voltage. At low forward-bias voltages, where I_d is dominated by Shockley-Read-Hall recombination within the depletion region, n may take values between 1.5 and 2 [114]. At higher forward-bias voltages n may assumes a value closer to 1 [123], which in the ideal case leads to Equation 2.1. Additionally, the values of I_s and n may vary depending on the dominant recombination mechanisms, doping density, and injection level [124–126].

While Equation 2.1 describes the DC characteristics of the PN junction, this chapter focuses on the investigation of its AC characteristics. To do this, we assume a small-signal sinusoidal voltage superimposed on a DC voltage. At low frequencies, the ratio between $\hat{v}_{\text{pp}}$ and $\hat{i}_{\text{pp}}$ is determined by the slope of Equation 2.1, and is referred to as the diffusion resistance. The diffusion resistance of the PN junction in forward bias can be expressed by the following relationship [114]:

$$R_{\text{dif}} = \frac{kT}{qI_d} \tag{2.2}$$

where both R_{dif} and I_d vary with the applied bias voltage. Furthermore, the PN junction exhibits capacitive effects. As the capacitive behaviour of c-Si solar cells originates in their junctions, it is worth reviewing the two main capacitive components of which any PN junction is constituted. The depletion capacitance is the capacitance that is associated with the ionized donor and acceptor atoms in the depletion region of a PN junction. It is influenced by the dopant concentrations and the applied voltage, since these factors affect the depletion region width and charge density. For a PN junction with homogeneously doped regions, the depletion capacitance can be expressed by the following equation [114]:

$$C_{\text{dep}} = A\sqrt{\frac{q\epsilon_s N_a N_d}{2\,(V_{bi}+V_R)\,(N_a+N_d)}} \tag{2.3}$$

where ϵ_s is the permittivity of the semiconductor, V_{bi} the built-in potential, and V_R is the applied reverse-bias voltage.

The diffusion capacitance is the capacitance that is associated with the build-up of minority carrier charge in the quasi-neutral regions. The diffusion current has an exponential dependence on the applied forward-bias voltage. The diffusion capacitance can be expressed by the following equation [114]:

$$C_{\text{dif}} = \frac{q^2 n_i^2 A}{2kT}\left(\frac{\sqrt{D_p\tau_{p0}}}{N_d}+\frac{\sqrt{D_n\tau_{n0}}}{N_a}\right)\exp\left(\frac{qV_F}{kT}\right) \tag{2.4}$$

It is worth noting that this expression for the diffusion capacitance only holds when the assumptions $\omega\tau_{p0} \ll 1$ and $\omega\tau_{n0} \ll 1$ are valid [114], where ω is the radian frequency of the small signal. Above this characteristic frequency, the minority carrier excess densities are no longer able to follow the AC signal and the C_{dif} contribution to the total capacitance relaxes [127].

As can be deduced from Equations 2.3 and 2.4, the total capacitance exhibited by PN junctions is dominated by the depletion capacitance at low applied forward-bias voltages. At higher voltages, the total capacitance becomes dominated by the exponentially increasing diffusion capacitance, although also the depletion capacitance increases because of the term $V_{bi}+V_R$ in the denominator.

2.3.2. Dynamic equivalent solar cell model

There are typically two junctions present in c-Si solar cells, which are the PN junction and the low-high (LH) junction. In the context of small-signal analysis, the PN junction is often represented by a circuit consisting of a resistor and a capacitor in parallel (*RC*-loop) [114]. The resistor in this model is determined by the diffusion resistance described by Equation 2.2. It is worth noting that at low bias voltages, the practical resistance of the PN junction often becomes limited by the shunt resistance [128]. The capacitance of the *RC*-loop is related to Equation 2.3 and Equation 2.4. Regarding the LH junction, it is important to highlight some differences with the PN junction. The LH junction establishes a built-in potential that repels minority carriers from the contacts that collect majority carriers. Specifically, the LH junction is composed of an accumulation layer on the lowly doped side and a depletion layer on the highly doped side. Generally, the depletion layer is much thinner than the accumulation layer and the built-in potential across the depletion layer never exceeds the thermal voltage [129]. Additionally, an important difference between PN junctions and LH junctions is that the LH junction does not exhibit a high diffusion resistance in reverse bias [130]. Consequently, the equations from the previous section are not applicable to LH junctions. Nonetheless, it is common in solar-cell impedance literature to model the impedance of the LH junction using an *RC*-loop [73, 89, 91, 110, 131, 132]. This modeling approach has been adopted in the study reported in this chapter*.

Using the concepts described above, a dynamic equivalent solar cell model can be defined. In this chapter, the equivalent circuit in Figure 2.5(a) is used to fit the experimental impedance data recorded for the different laminates. The circuit contains two parallel *RC*-loops (R_j-C_j and R_{LH}-C_{LH}), a series resistance R_s, and an inductor L_s. To relate the components in Figure 2.5(a) to the physics in the PV cell, Figure 2.5(b) is included. When comparing these circuits, it can be observed that R_j denotes the parallel of the diffusion resistance R_{dif} and the shunt resistance R_{sh}. Additionally, C_j represents the net capacitance of C_{dep} and C_{dif}. Moreover, the inductor L_s in Figure 2.5 accounts for the inductive reactance in the laminate, which is mostly a result of the current travelling through the interconnection and cell metallization and is most prominent in the high frequency end of the impedance spectrum.

Furthermore, it is important to discuss the various types of junctions and contacts found in modern c-Si solar cells. Traditional c-Si solar cell architectures, such as Al-BSF and PERC designs, feature PN homojunctions. While some assumptions like the abrupt junction approximation may not apply to diffused junctions, much of the existing the-

* It should be noted that modeling the LH junction with an *RC*-loop was later found to be inaccurate in representing the underlying physics. A detailed discussion on this matter is provided in Chapter 3. Nevertheless, the results and discussion in Chapter 2 focus predominantly on the PN junction results. Since the PN junction dominates the impedance, the discussion and conclusions in this chapter remain valid.

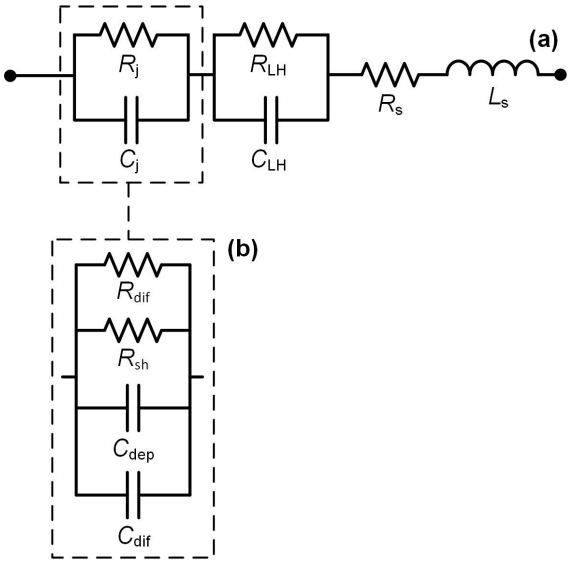


Figure 2.5: (a) Electrical equivalent model used in this study to fit the experimentally recorded impedance data of the single-cell laminates. The R_j-C_j and R_{LH}-C_{LH} loops represent the impedance of the junctions in the PV cell. R_s and L_s denote the series resistance and inductance, respectively. (b) A more detailed equivalent circuit that clarifies how the R_j-C_j loop corresponds to the cell physics. It is shown that R_j represents the parallel of the diffusion resistance R_{dif} and shunt resistance R_{sh}, whereas C_j is constituted of the parallel of C_{dep} and C_{dif}.

ory on impedance in PN junctions remains relevant. However, modern solar cells are increasingly adopting passivating contacts [117]. The TOPCon architecture features a thin SiO_x layer adjacent to a doped poly-Si layer, while the SHJ contact consists of a thin intrinsic amorphous silicon layer coupled with a doped amorphous or nanocrystalline layer. Additionally, there have even been demonstrations of dopant-free selective contacts with a MoO_x hole collector [133]. This raises the question of how closely these modern junctions resemble the behavior of traditional PN homojunctions. First, despite their differing structures, both passivating and non-passivating carrier-selective contacts generally adhere to the same current-voltage characteristic as described by Equation 2.1 [134]. Furthermore, in the present study it was found that the circuit illustrated in Figure 2.5 accurately describes the impedance of the IBC, TOPCon, and SHJ solar cell laminates, similarly to those with Al-BSF and PERC architectures. As it will be shown later in this chapter, the C_j values of the various cells exhibit a trend that appears to be more influenced by substrate properties than by the distinctions between homojunctions and passivating contact architectures. However, this does not imply that the impedance of passivating contacts is entirely similar to that of homojunction architectures, as some differences have been reported in the literature [107, 135, 136].

2.3.3. Equivalent model fitting

The impedance of the circuit in Figure 2.5(a) is described by the following equation:

$$Z_{\mathrm{PV}} = i\omega L_s + R_s + \left[R_j \parallel \frac{1}{i\omega C_j} \right] + \left[R_{LH} \parallel \frac{1}{i\omega C_{LH}} \right] \tag{2.5}$$

where i denotes the imaginary unit, R_j is the PN junction resistance, and C_j is the PN junction capacitance. Equation 2.5 can be rewritten into the form $Z_{\mathrm{PV}} = Z'_{\mathrm{PV}} + iZ''_{\mathrm{PV}}$ with the resistance Z'_{PV} and the reactance Z''_{PV} being defined as follows:

$$Z'_{\mathrm{PV}} = R_s + \frac{R_j}{1 + R_j^2\omega^2 C_j^2} + \frac{R_{LH}}{1 + R_{LH}^2\omega^2 C_{LH}^2} \tag{2.6}$$

$$Z''_{\mathrm{PV}} = \omega L_s - \frac{R_j^2\omega C_j}{1 + R_j^2\omega^2 C_j^2} - \frac{R_{LH}^2\omega C_{LH}}{1 + R_{LH}^2\omega^2 C_{LH}^2} \tag{2.7}$$

In Equation 2.7, the occurrence of negative or positive signs can be attributed to the distinct behavior of current and voltage in capacitors and inductors. Specifically, in a capacitor, the current leads the voltage, resulting in a negative sign, whereas in an inductor, the current lags behind the voltage, leading to a positive sign. To determine the values of the circuit parameters in Figure 2.5(a) at any DC operating voltage V_{DC}, Equations 2.6 and 2.7 are simultaneously fitted to the recorded impedance data through complex nonlinear least-squares (CNLS) analysis [137]. For the fitting procedure, the MATLAB *lsqcurvefit* solver is used, with the fitting parameters being C_j, R_j, C_{LH}, R_{LH}, L_s, and R_s. It is worth noting that at low V_{DC} values, the Nyquist spectra of the different laminates closely resemble semi-circles, which implies that the R_j-C_j loop dominates the total PV impedance. At higher bias voltages, the Nyquist spectra can deviate somewhat from the semi-circular shape. For the CNLS analysis in this work, a PV model consisting of only the R_j-C_j loop is used at low V_{DC} values, whereas the full model from Figure 2.5(a) is used at higher V_{DC} values. To determine from which V_{DC} value it becomes necessary to use the full impedance model, it is checked whether the fitting quality with only the R_j-C_j loop exceeds certain error thresholds. This methodology, along with the error metrics definitions, is explained in further detail in Appendix A.

2.4. Results and Discussion

The impedance of each cell laminate was characterized from short-circuit to well above V_{mpp} in steps of maximum 0.1 V. In Figure 2.6, the experimentally recorded impedance data for the IBC laminate, as well as the CNLS fits to the data are presented. This same procedure was followed for the other seven laminates. In the remainder of this section, the most important findings are summarized. The focus is on the best-fit values for the R_j-C_j loop and L_s of the dynamic equivalent circuit in Figure 2.5(a). Since these circuit elements constitute the main fraction of the total PV impedance, they are the most physically relevant and can be fitted with the highest accuracy.

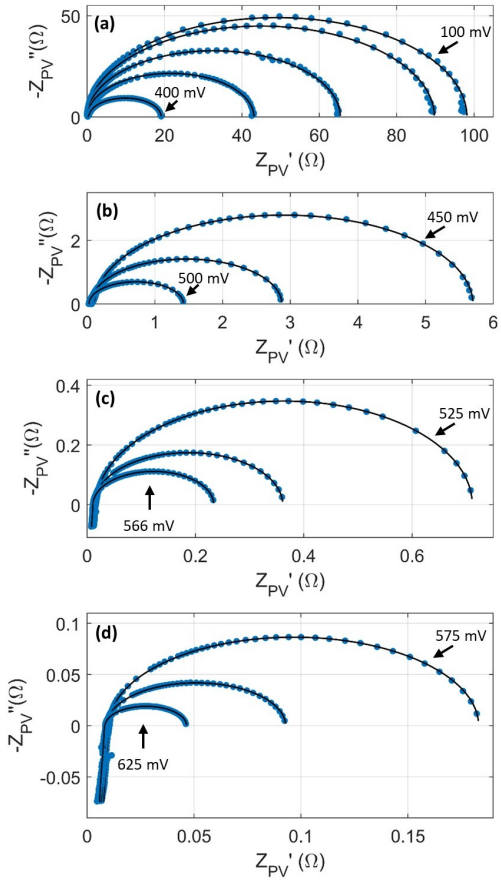


Figure 2.6: Nyquist spectra for the IBC cell recorded at various DC voltages. The symbols represent experimental data and the lines are CNLS fits to the data using the circuit model of Figure 2.5(a). In 2.6(a), the plots of successively decreasing radii were collected at gradually increasing applied DC bias voltages in the following order: V_{DC} = 100, 200, 300, 350, and 400 mV. In 2.6(b), the plots of large to small radii correspond to 450, 475, and 500 mV. The plots of successively decreasing radii in 2.6(c) were recorded at 525, 550, and 566 mV (V_{mpp}). In 2.6(d), the plots of large to small radii correspond to 575, 600, and 625 mV.

2.4.1. PN junction capacitance

Since the R_j-C_j loop dominates the total impedance of the different cells that were tested, C_j has a strong impact on the total impedance. Figure 2.7 illustrates C_j as a function of the applied V_{DC}. In this context, C_j refers to the *areal* PN junction capacitance, indicating that C_j is normalized to the PV cell area. As expected from Equation 2.4, an exponentially increasing capacitance as a function of applied V_{DC} is observed in the high forward-bias region. The slight deviations from this exponential trend can most likely be explained by the fact that the effective voltage over the R_j-C_j loop is slightly lower than the applied voltage [89]. For instance, a small fraction of the applied voltage drops over R_s, and this fraction increases for increasing V_{DC}.

It is shown in Equation 2.4 that the minority carrier lifetime τ_{min} is one of the param-

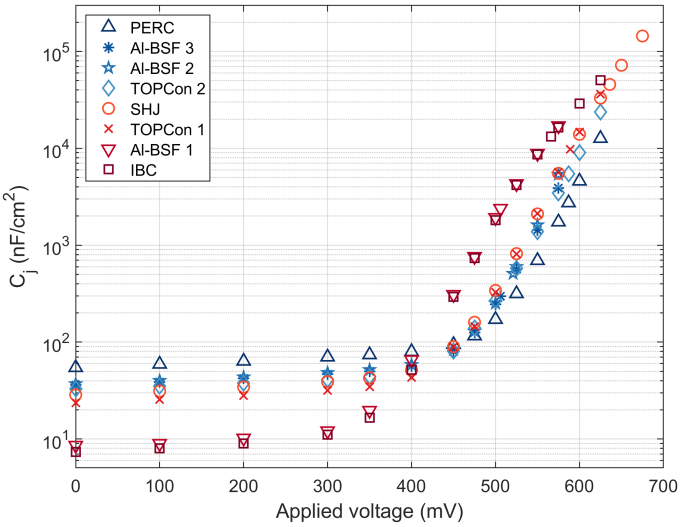


Figure 2.7: The areal C_j of the cell laminates as a function of applied DC bias voltage, which is obtained by fitting the circuit in Figure 2.5(a) to the experimentally recorded impedance data through CNLS analysis.

eters affecting the diffusion capacitance. Indeed, a high τ_{min} is typically mentioned in literature as an important reason for high diffusion capacitances in high-efficiency cells [112]. To cross-check this with our results in Figure 2.7, it is important to realize that a change in τ_{min} does not affect the slope of the capacitance-voltage (C_j-V) curve, but only shifts the curve horizontally in the high forward-bias region. Taking into account that the V_{oc} is a good indicator of the minority carrier lifetime [1], it could be expected that the curves shifted the most to the left correspond to the cells with the highest V_{oc}. However, when comparing the results in Figure 2.7 to the V_{oc} values in Table 2.2, no such trend is observed. On the contrary, for the cell with the lowest V_{oc} (Al-BSF 1), the C_j-V curve in the high forward-bias region is among the two cells for which the curve is shifted the furthest to the left. These results suggest that τ_{min} is not the most important factor affecting the shape of the C_j-V curve of c-Si solar cells.

For interpreting Figure 2.7, a more useful starting point is the low-voltage region, where C_j is dominated by the depletion capacitance C_{dep}. As described in Equation 2.3, the C_{dep} is governed by the dopant concentrations around the PN junction. To further analyze C_j in the low-voltage region, it is worth noting that c-Si PV cells typically exhibit two characteristics that facilitate a simplified analysis. Firstly, the depletion region of the PN junction usually extends into the bulk of the wafer. Indeed, in simulated band diagrams of PV cells based on TOPCon [138] and SHJ technology [139, 140], it is shown that the band bending extends into the bulk of the wafer. Secondly, the substrate doping density N_{sub} - also known as wafer dopant concentration - is typically much lower than that of the charge-carrier selective layer on the other side of the PN junction. When these two conditions are satisfied, the PN junction can be treated like a one-sided junction, which is defined as a PN junction where one side is much more heavily doped than the adjacent side [114]. In that case, the expression for the depletion capacitance from

Equation 2.3 simplifies to:

$$C_{\text{dep}} \approx A\sqrt{\frac{q\epsilon_s N_{\text{sub}}}{2\,(V_{bi}+V_R)}} \tag{2.8}$$

which implies that the depletion capacitance in a c-Si PV cell is primarily determined by N_{sub} and V_{bi}. In fact, both these parameters can be extracted from the $1/C_j^2$ versus V_{DC} relationship in the bias voltage region where the depletion capacitance is dominant. Specifically, N_{sub} can be obtained from the slope of this curve, while V_{bi} can be determined from the voltage at which a linear fit to the $1/C^2$ data crosses zero [114, 141]. To extract these values from the different laminates, capacitance-voltage (C-V) measurements are conducted at 10 kHz between V_R = 2.0 V and V_F = 0.3 V. The resulting N_{sub} and V_{bi} values are presented in Table 2.3.

It appears that among the different laminates, N_{sub} exhibits a much wider spread than V_{bi}. Whereas N_{sub} can vary by as much as a factor 62, the V_{bi} variation is limited to a factor 1.4. Therefore, it can be concluded that the depletion capacitance in a c-Si PV cell is mainly determined by N_{sub}. In Figure 2.7, the marker color transition from blue to red (transition from △ to □) visualizes a decreasing areal depletion capacitance.

Table 2.3: Substrate dopant density N_{sub} and built-in potential V_{bi} of all laminates as extracted from C-V measurements at 10 kHz between V_R = 2.0 V and V_F = 0.3 V. The measurements were carried out using an HP 4284A precision LCR meter.

Laminate ID	N_{sub} **(atoms × cm^{-3})**	V_{bi} **(V)**
Al-BSF-1	4.2×10^{14}	0.57
Al-BSF-2	1.1×10^{16}	0.63
Al-BSF-3	1.0×10^{16}	0.64
PERC	2.6×10^{16}	0.74
TOPCon-1	4.5×10^{15}	0.65
TOPCon-2	1.0×10^{16}	0.77
IBC*	4.5×10^{14}	0.64
SHJ	5.6×10^{15}	0.56

* Only C-V data between V_R = 0.5 V and V_F = 0.3 V was used. In the case of an IBC structure, a too high reverse bias voltage may lead to interaction between neighbouring fingers.

Furthermore, upon closer examination of Figure 2.7, a consistent trend can be observed: the lower C_j is in the low-voltage region, the more the curve is shifted to the left in the high-voltage region. This trend suggests that N_{sub} does not only govern the depletion capacitance in the low-voltage region, but also the diffusion capacitance in the high-voltage region. Indeed, Equation 2.4 shows that the diffusion capacitance is directly dependent on the dopant concentrations outside the depletion region. The results in this work show that the substrate doping density affects the shape of the C_j-V curve of a c-Si PV cell much more than the V_{oc}.

Since a low N_{sub} shifts the C_j-V relationship in the high-voltage region to the left in Figure 2.7, a low N_{sub} contributes to reaching a high diffusion capacitance at V_{mpp}. However, when comparing the capacitance of the different cells, it is important to realize

that in practice they will operate at different voltages due to their different V_{mpp} values. The lowest and highest C_j values in this work for an applied voltage equal to the V_{mpp} in STC conditions, are 0.30 μF/cm^2 for the Al-BSF-3 cell and 45.6 μF/cm^2 for the SHJ cell. It is worth pointing out that in Figure 2.7 the C_j-V curve of the SHJ cell is shifted to the right compared to the IBC cell in the high voltage region. Nevertheless, the reason that the SHJ cell still has the highest C_j value for operation around maximum power point is its high V_{mpp} of 636 mV in STC conditions.

2.4.2. Outlook for capacitive effects in PV cells

Since the results in this work show that the capacitive effects in solar cells are mostly governed by the substrate doping density, it is worth to discuss how N_{sub} affects the performance of c-Si PV cells, and to analyze the latest trends in industry.

Traditionally, in Al-BSF cells, recombination at the full-area metal rear contact limits the total minority charge carrier lifetime τ_{min} [142]. Even for industrial n-type TOPCon cells with efficiencies over 23%, it has been reported that recombination at the front and back sides is still limiting τ_{min} [143]. Nevertheless, it is crucial to select the wafers with the right properties to ensure that the V_{oc} is limited by recombination near the contacts. The V_{oc} is determined by the extent of splitting between the quasi-Fermi levels [1]. In the past, when the quality of silicon wafers was not as high as it is today, there were more Shockley-Read-Hall (SRH) defects present in the bulk. If a wafer exhibits a relatively low bulk lifetime (< 500 μs), it is preferable for maximizing the quasi-Fermi level splitting to have a relatively high N_{sub}, as this shifts the Fermi level closer to the band edge [142, 144, 145]. Consequently, manufacturers typically selected wafers with a relatively high N_{sub} [143]. However, using wafers with a lower N_{sub} can increase the short-circuit current I_{sc}. It is worth noting that it varies for the different c-Si cell technologies how strongly I_{sc} is affected by N_{sub}, and which physical processes govern this effect [142–144]. Furthermore, it is worth noting that N_{sub} has an impact on the *FF*, which varies for different PV cell technologies and geometries [142]. Thus, the optimum N_{sub} in mass-produced silicon wafers for industrial c-Si PV cells is influenced by various factors. Recent improvements in the Czochralski (Cz) process have ensured that the major share of the PV wafer market is now based on monocrystalline ingots grown via the Cz method [146]. As the quality of these wafers improves, the optimum N_{sub} is nowadays shifting to lower values [143].

Furthermore, due to the progress in surface passivation technology and wafer pretreatment [147, 148], we are nearing the point where surface recombination is suppressed to such a level that recombination in the bulk starts to limit τ_{min} in industrial c-Si PV cells. For the Cz wafers that are nowadays used in industrial PV cells, τ_{bulk} is usually still limited by SRH recombination [144]. Nevertheless, for SHJ PV cell precursors based on n-type Cz wafers, implied V_{oc} values have already been achieved that are only 9 mV away from the intrinsic limit [149]. Furthermore, these previously predicted intrinsic limits are even being exceeded by recent reports on monocrystalline silicon float zone wafers passivated with TOPCon contact stacks [147, 150]. If the τ_{bulk} in modern wafers becomes limited by Auger recombination, it becomes relevant to mention that the efficiency limit for c-Si PV cells is the highest for a wafer bulk made of undoped silicon [6, 151]. This is related to the fact that the intrinsic Auger recombination rate

R_{intr} in the bulk of the wafer reduces for a lower N_{sub} [152, 153], leading to a higher limit for the V_{oc}. It is worth noting that R_{intr} particularly increases for an N_{sub} above ~10^{15} cm^{-3} for n-type Si and above ~10^{16} cm^{-3} for p-type Si [6].

Concluding, in high-efficiency c-Si PV cells, increased use of wafers with a low substrate doping density is likely to happen in the future. Furthermore, these cells will likely operate at higher V_{mpp} values. As such, the MPP capacitance of industrial c-Si PV cells will likely increase over the coming years. It is important to note that the cell capacitance exhibits a linear dependency on the solar cell area. Additionally, the equivalent capacitance of a string of cells varies inversely with the number of series-connected cells in that particular string. Consequently, the prevailing industry trends concerning wafer size and the number of cells within a module will directly influence the capacitance observed at module-level.

2.4.3. Inductive effects

Research has been emerging on exploiting inductive effects in PV cell strings [70, 72], and to the best of our knowledge, there have been no previous reports on inductive effects in full-sized industrial cells. The found inductance values of the cell laminates suggest that the inductance is independent of V_{DC}. This is within expectation, since most of the inductive effects presumably originate in the wiring and metal interconnections of the PV cells. Since the inductive reactance makes up a larger share of the impedance at higher V_{DC}, the CNLS fitted values at the highest bias voltages give the best indication of the inductance of the laminate. Thus, the inductances obtained by fitting the impedance data at the seven highest bias points for each laminate are used for a statistical analysis, which is presented in Figure 2.8. The corresponding details concerning the cell metallization and wirings in the laminates are presented in Table 2.1.

Regarding the interpretation of the inductances in Figure 2.8, it is important to take into account that part of the inductance in the laminates does not originate in the PV cells themselves, but rather in the metal ribbons within the laminates. Thus, when it comes to inductance, in this manuscript the terminology *laminate* is used instead of *cell*. First of all, it is worth noting that the cells in the laminates have different areas, implying different lengths of their metal contacts. It is expected that longer wires result in larger inductances [154]. However, in Figure 9 it is shown that the 5-inch cell laminates Al-BSF-1 and IBC have higher inductances than those of the 6-inch cells Al-BSF-2 and Al-BSF-3. This suggests that there are other factors in the cell design that have a larger effect on the resulting inductance. It seems that cell laminates with a similar metallization structure, such as the bifacial 5BB/9BB laminates (PERC, TOPCon 1, TOPCon 2) have a similar inductance between 63-70 nH. When considering all the cells with a busbar metallization, namely Al-BSF-1, Al-BSF-2, PERC, TOPCon-1, and TOPCon-2, it seems that an increase in the number of busbars decreases the inductance. This is in accordance with theory, for which the equivalent inductance scales inversely with the number of inductors connected in parallel. For an increase in the number of busbars from 5 (TOPCon 2) to 9 (PERC, TOPCon 1) the decrease in L_s is marginal, suggesting that most of the inductive effects are originating in the ribbons that are externally connected to the cells.

However, in Figure 2.8 it is shown that the IBC and SHJ cell laminates have a relatively high inductance, in spite of their high number of parallel metal lines in the metallization.

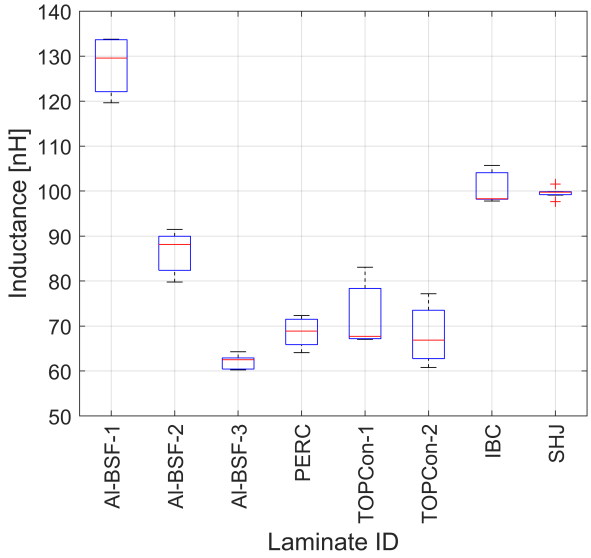


Figure 2.8: Statistical analysis regarding the inductance of the cell laminates. The values for the inductance are obtained by fitting the circuit in Figure 2.5(a) to the experimentally recorded impedance data through CNLS analysis. The values used to generate this figure correspond to the seven highest DC bias voltages that were recorded for each laminate. On each box, the red central line indicates the median, and the bottom and top edges of the box indicate the 25^{th} and 75^{th} percentiles, respectively. The whiskers extend to the most extreme data points not considered outliers, and the outliers are plotted individually as red crosses.

It is known that for a straight wire both the shape and the cross-sectional area A_{cross} affect the self-inductance, and a smaller A_{cross} typically yields a larger inductance [154]. Thus, the relatively high inductances in the IBC and SHJ laminates could be due to the difference in shape and cross-section of the metal patterns compared to the cells with a more classical busbar metallization. Furthermore, it is worth noting that there is a relatively small space between the metal contacts in the case of the IBC cell, which could cause magnetic interaction between neighbouring metal fingers. Finally, it is worth commenting on the Al-BSF-3 laminate, which has SW front metallization. In spite of this, the current collection at the rear of this cell is still happening through 4 busbars. Therefore, the equivalent inductance is a combination of the effect of the many smart wires and the busbars.

2.4.4. Validity of the impedance model

In general, the CNLS analysis performed in this work yields high-quality fits to the experimental data. Nevertheless, it was observed that the fits become less accurate when the applied DC bias voltage approaches V_{oc}, and these deviations are mostly occurring in the high-frequency region. Several factors could be contributing to these deviations, among which the following three. Firstly, since the impedance of the PV cells is lowest at high frequency and at high V_{DC} values, measurement errors could become more apparent. Secondly, high-frequency electromagnetic effects such as skin effect could play a role. Thirdly, the conditions $\omega\tau_{\text{p0}} \ll 1$ and $\omega\tau_{\text{n0}} \ll 1$ may no longer be valid, meaning

that the diffusion capacitance is no longer frequency-independent. This third factor is further discussed in Chapter 3.

2.5. Conclusions

In this chapter, the impedance of eight single-cell laminates based on different industrial c-Si PV cells was characterized. The capacitive and inductive effects in the laminates were evaluated by fitting a dynamic PV equivalent circuit to the experimentally recorded impedance data through complex nonlinear least-squares analysis.

The experiments show that the PN junction capacitance at maximum power point varies for the different cells between 0.30 and 45.6 μF/cm^2. The two main factors contributing to a high PV cell capacitance at maximum power point are (1) a low wafer dopant concentration and (2) a high maximum power point voltage. Upon analyzing the trends in upcoming high-efficiency c-Si PV cells, increasing capacitances are expected in the future. Furthermore, the studied cell laminates exhibit inductances between 63 and 130 nH. When comparing the inductive effects between the different laminates, it appears that the inductance decreases when the metallization structure consists of a higher number of busbars. Furthermore, the geometry of the metal contacts affects the inductance.

The findings in this chapter have some practical consequences. For instance, the minimum time that is required for accurate *I*-*V* measurements, which is limited by the cell capacitance, must be set accordingly. Additionally, the insights into the variations in capacitive and inductive effects between different cell architectures can be useful for optimizing the design of power converters that perform maximum power point tracking. Finally, the increasing capacitance in modern solar cells will also offer opportunities, as the first publications where the impedance of PV cell strings is exploited have already been emerging.

3

The nature of silicon PN junction impedance at high frequency

This chapter is based on the following publication:

D. A. van Nijen, P. Procel, R. A. C. M. M. van Swaaij, M. Zeman, O. Isabella and P. Manganiello, "The nature of silicon PN junction impedance at high frequency", accepted for publication in *Solar Energy Materials and Solar Cells*, 2025.

The data underlying this chapter was published in the 4TU Research Data Archive *.

3.1. Introduction

In the context of small-signal analysis, it is well known that the PN junction impedance cannot be fully represented by any linear, lumped, finite, passive, or bilateral network [114]. Nevertheless, when the frequency is sufficiently low, the PN junction impedance can be approximated by a parallel resistor-capacitor circuit (*RC*-loop), a common simplification found in literature. At these lower frequencies, the minority carrier distribution can effectively "follow" the frequency of the AC signal. Yet, as the frequency increases beyond a certain threshold, violating this condition, the *RC*-loop approximation loses its validity. However, it is important to mention that solar cells consist of more than just a PN junction. For example, direct metal contact to the lightly doped substrate is not appropriate, as it would lead to the formation of a Schottky barrier and/or Fermi level pinning [117]. Hence, practical devices often possess a so-called low-high (LH) junction, which reduces the contact resistance by facilitating tunneling and reduces surface recombination. However, this poses a challenge when the impedance of such a device no longer behaves like a single *RC*-loop beyond a certain frequency. Is this because the *RC*-loop approximation of the PN junction is no longer valid, or is it due to

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separate impedance effects in the LH junction? In solar-cell literature, various high-frequency effects are attributed to this LH junction. For instance, an additional *RC*-loop is frequently incorporated into the impedance model to account for the LH junction impedance [73, 89, 91, 110, 131, 132]. Moreover, sometimes a constant phase element (CPE) or a third *RC*-loop is even introduced to solar-cell impedance models to address various non-ideal effects in devices with passivating contacts [107, 135]. While these adjustments often improve fitting accuracy, the underlying physics may not be accurately captured.

In this chapter, the impedance of crystalline silicon (c-Si) PN junction devices is investigated through Technology Computer Aided Design (TCAD) simulations. The TCAD simulation methodology enables the isolation of the PN junction impedance, since ideal contacts can be positioned on a bulk material without the inclusion of a LH junction. Moreover, the almost noise-free simulation data facilitate a thorough examination of subtle shortcomings of equivalent model fits. While much of the theory in this paper also applies to devices with passivating contacts, this study exclusively focuses on homojunction architectures. It is crucial for the field to understand the limitations of modeling PN homojunction impedance across different frequency ranges with a resistor-capacitor circuit. Without this knowledge, non-idealities may be incorrectly attributed to other parts of the device. For instance, one outcome of this paper is that certain impedance behaviour that is often attributed to capacitive effects in the LH junction, is in fact due to non-ideal high-frequency effects in the PN junction. First, the chapter demonstrates the frequency range within which the PN junction can be accurately represented by an *RC*-loop, and it explores the consequences of exceeding this frequency threshold. Subsequently, it is demonstrated how the silicon bulk properties influence these results. Finally, it is discussed how the impedance changes when a LH junction is added to the device structure.

3.2. Theory

In section 3.2.1, the theory of PN junction admittance related to minority carrier diffusion is summarized. Subsequently, section 3.2.2 outlines a more comprehensive small-signal impedance model of a PN junction, and provides equations describing the circuit element values.

3.2.1. PN junction small-signal admittance

When a PN junction diode is forward biased, diffusion mechanisms play an important role in the admittance. In a PN junction, the electron diffusion current is given by [114]:

$$I_{n0} = \frac{AqD_n n_{p0}}{L_n} \exp\left(\frac{qV_F}{kT}\right) \tag{3.1}$$

where A is the cross-sectional area of the PN junction, q is the elementary charge constant, D_n is the diffusion constant of electrons, n_{p0} is the minority carrier electron concentration on the p side of the junction, L_n is the effective electron diffusion length, and V_F is the applied forward-bias voltage. Finally, k and T are the Boltzmann constant and temperature, respectively. Similarly, the hole diffusion current in a PN junction is given

by [114]:

$$I_{p0} = \frac{AqD_p p_{n0}}{L_p} \exp\left(\frac{qV_F}{kT}\right) \tag{3.2}$$

where D_p is the diffusion constant of holes, p_{n0} is the minority carrier hole concentration on the n side of the junction, and L_p is the effective hole diffusion length. Using these diffusion current expressions, the PN junction admittance can be defined as [114]:

$$Y = \frac{1}{V_t}\left[I_{p0}\sqrt{1+i\omega\tau_{p0}} + I_{n0}\sqrt{1+i\omega\tau_{n0}}\right] \tag{3.3}$$

where the thermal voltage V_t is kT/q, i denotes the imaginary unit, τ_{p0} and τ_{n0} are the minority charge carrier lifetimes, and ω is the radian frequency of the small signal. It is worth noting that the real and imaginary terms in Equation 3.3 can be separated using the following equation:

$$\sqrt{1+i\omega\tau_0} = \pm\left[\sqrt{\frac{\sqrt{1+\omega^2\tau_0^2}+1}{2}} + i\sqrt{\frac{\sqrt{1+\omega^2\tau_0^2}-1}{2}}\right] \tag{3.4}$$

No linear, lumped, finite, passive, bilateral network exists that can be synthesized to give the admittance function of Equation 3.3 [114]. However, assuming that the frequency is low enough that the minority carrier distribution in the quasi-neutral regions of the junction can follow the AC voltage ($\omega\tau_0 \ll 1$), the approximation $\sqrt{1+i\omega\tau_0} \approx 1 + i\omega\tau_0/2$ can be made. Substituting this into Equation 3.3 yields the following expression for the low-frequency admittance:

$$Y = \frac{1}{V_t}\left[I_{p0}\left(1+\frac{i\omega\tau_{p0}}{2}\right) + I_{n0}\left(1+\frac{i\omega\tau_{n0}}{2}\right)\right] \tag{3.5}$$

As opposed to the admittance in Equation 3.3, the low-frequency admittance in Equation 3.5 can be described by a lumped passive circuit. Indeed, Equation 3.5 can be written in the form:

$$Y = g_{\text{dif}} + i\omega C_{\text{dif}} \tag{3.6}$$

with the diffusion conductance g_{dif} and diffusion capacitance C_{dif} both being frequency-independent. However, Equations 3.3 and 3.4 dictate that as a certain frequency threshold is exceeded, both the real and imaginary part of the admittance are expected to increase with frequency. In the high-frequency limit, the admittance of Equation 3.3 simplifies to semi-infinite Warburg admittance [88]. Here, the admittance magnitude increases proportionally to $\sqrt{\omega}$, with equal real and imaginary parts. Physically, Warburg admittance behavior arises whenever a reaction is under partial or complete mass-transport control by diffusion [155].

3.2.2. Small-signal model

In the previous subsection it was shown that the small-signal equivalent circuit of a PN junction should include a diffusion resistance R_{dif} and a diffusion capacitance C_{dif} to

account for the dynamics involved in the diffusion of minority carriers. Additionally, to create a more comprehensive small-signal equivalent circuit of a PN junction, other elements are incorporated. These are a shunt resistance R_{sh} (whose ideal value is very high) and a series resistance R_s. Furthermore, a depletion layer capacitance C_{dep} is introduced to account for the capacitance related to the ionized atoms in the depletion region. The value of C_{dep} is expected to remain independent of frequency up to at least 1 MHz [127, 156]. The complete small-signal equivalent circuit incorporating all these components is presented in Figure 3.1(a). For further analysis, this model can be simplified to the one in Figure 3.1(b), in which R_j is the parallel of R_{dif} and R_{sh}, and C_j is the parallel of C_{dep} and C_{dif}.

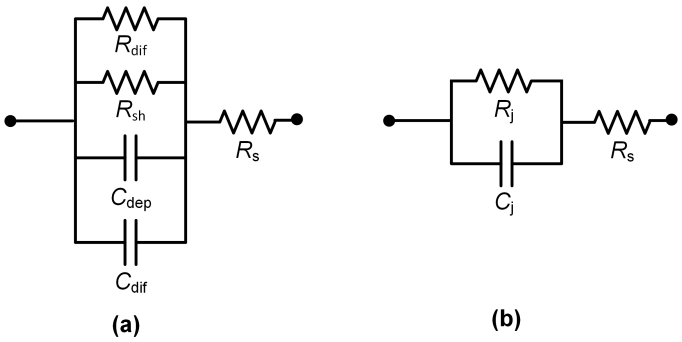


Figure 3.1: PN junction equivalent circuits: (a) full circuit, (b) simplified circuit used for the analysis in this work.

As shown in Chapter 2, the depletion layer capacitance (C_{dep}) typically dominates C_j at reverse bias and at low forward bias voltage. Moreover, the low-frequency diffusion capacitance (C_{dif}) typically dominates C_j at high forward bias voltage. The impedance of the circuit in Figure 3.1(b) is given by the following equation:

$$Z = R_s + \left[R_j \parallel \frac{1}{i\omega C_j} \right] \tag{3.7}$$

Equation 3.7 can be rewritten into the form $Z = Z' + iZ''$ with the real part Z' and the imaginary part Z'' being defined as follows:

$$Z' = R_s + \frac{R_j}{1 + R_j^2 \omega^2 C_j^2} \tag{3.8}$$

$$Z'' = -\frac{R_j^2 \omega C_j}{1 + R_j^2 \omega^2 C_j^2} \tag{3.9}$$

In Equation 3.9, the negative sign can be attributed to the behavior of current and voltage in capacitors. Specifically, in a capacitor, the current leads the voltage, resulting in a negative sign. The impedance of Equation 3.7 would ideally produce a semicircle in a Nyquist plot. However, as discussed in section 3.2.1, R_{dif} and C_{dif} can be expected to

maintain their constant values only below a certain threshold frequency. At frequencies well beyond this threshold, the impedance associated with the diffusion process may begin to resemble a Warburg element, resulting in a -45° feature in the high-frequency part of the Nyquist plot [100, 156, 157].

3.3. Simulation approach

In section 3.3.1 the model used to generate impedance data is introduced. Subsequently, in section 3.3.2 it is explained how these impedance data are analyzed.

3.3.1. TCAD Sentaurus model

In this study, electrical simulations of the semiconductor devices are performed using the finite element simulator TCAD Sentaurus [158]. The two-dimensional device structures simulated in this work are illustrated in Figure 3.2. The structure depicted in Figure 3.2(a) consists of an n-type bulk and two ideal contacts with no resistance situated at the opposite side of the bulk. The top contact is from now on referred to as the positive contact, with the bottom contact being the negative contact. In this study different variations were investigated, but the results presented are primarily for a contact width of W_c = 50 μm, a bulk width of W_{bulk} = 500 μm, a thickness of t_{bulk} = 200 μm, and a substrate/bulk n-type dopant concentration of N_{sub} = 1 × 10^{15} cm^{-3}. The PN structure in Figure 3.2(b) is obtained from the former by including a p^+-doped emitter directly underneath the positive contact. Alternatively, the LH structure in Figure 3.2(c) includes an n^+-doped layer above the negative contact. The interface between this doped region and the bulk is also referred to as the low-high (LH) junction or the back surface field (BSF). It is worth noting that both the p^+-layer from Figure 3.2(b) and the n^+- layer from Figure 3.2(c) have Gaussian doping profiles with a peak concentration of 1 × 10^{19} cm^{-3} at the surface, which drops to 10% of the peak value at half of their respective junction depths t_{E} and t_{BSF}, both set at 10 μm. Finally, the PN/LH structure in Figure 3.2(d) includes both an emitter and LH junction. Since it is expected from Equation 3.3 that the minority carrier lifetime plays an important role in the admittance, the trap density in the bulk is an important parameter that can impact both C_j and R_j. In this study, the bulk trap density of the different structures in Figure 3.2 is adjusted using a parameter called the Shockley-Read-Hall (SRH) lifetime τ_{SRH}.

The small-signal AC analysis is conducted using the *ACCoupled* solve section of TCAD Sentaurus, assuming dark conditions and a temperature of 25 °C. This simulation generates a frequency-dependent impedance matrix, comprising the real and imaginary parts of the impedance at each frequency examined during the AC analysis. In this study, the frequency range of interest spans from 10 μHz to 1 GHz. It is worth noting that in experimental devices, the inductance of the metal contacts dominates the reactance at high frequencies [73], whereas there is no such inductance in the simulation approach utilized here. Additionally, the use of ideal contacts in the simulation excludes any high-frequency effects that may alter the impedance of metal contacts. Moreover, the simulation data is characterized by low noise levels. Consequently, the simulation data enables the identification of subtle trends strictly related to the impedance of the junctions themselves, which may be more challenging to extract from experimental

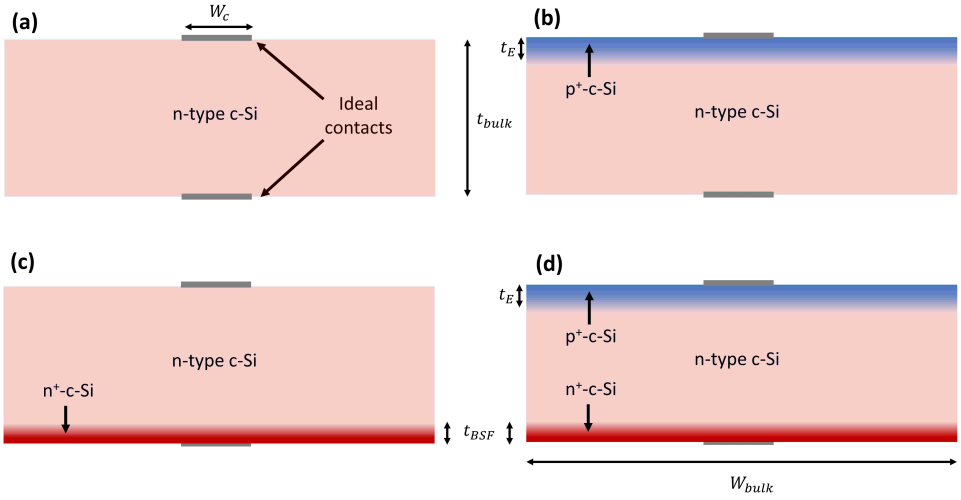


Figure 3.2: Simulated structures. Structure (a) consists of only an n-type bulk with two ideal contacts. Unless otherwise specified, in this study the bulk has a thickness t_{bulk} of 200 μm, a width W_{bulk} of 500 μm, and a bulk n-type dopant concentration N_{sub} of 1×10^{15} cm^{-3}. The ideal contacts have a width W_{C} of 50 μm. Structure (b) includes a p$^+$ doped layer near the positive contact, called the emitter. Structure (c) includes an n$^+$ doped layer near the negative contact, forming a so-called LH junction or BSF. Both the emitter and the BSF are composed of highly doped p$^+$ and n$^+$ regions, respectively, with Gaussian doping profiles. Each profile has a peak concentration of 1×10^{19} cm^{-3} at the surface, and drops to 10% of the peak value at half of their respective junction depths t_{E} and t_{BSF}, both set at 10 μm. Finally, structure (d) includes both a PN and LH junction.

data.

3.3.2. Equivalent circuit analysis

The next step involves interpreting the impedance data using the electrical circuit depicted in Figure 3.1(b). To extract the values of the different circuit elements, two different methods are employed:

1. CNLS fitting: Complex nonlinear least-squares (CNLS) analysis is utilized to simultaneously fit Equations 3.8 and 3.9 to the impedance data. This approach, widely applied in the analysis of c-Si solar cells, assumes fixed element values for R_j, C_j, and R_s. However, as explained in section 3.2.1, this assumption holds true only up to a certain frequency limit. This study further elaborates on the frequency limitations of this fixed circuit element assumption.

2. Analytic approach: In the simulated device structures, R_s is primarily influenced by the series resistance of the semiconductor bulk. It is generally assumed that R_s is mostly independent of frequency [89], and later in this work it is shown that this is also a valid approximation for the simulated device structures. Moreover, at high frequencies nearing 1 GHz, the real part of the impedance is primarily governed by R_s. Thus, one possible strategy is to extract the R_s value directly from the high-frequency real part of the impedance. If the value of R_s is known, R_j and C_j

remain as the two unknowns in Equations 3.8 and 3.9. Their values can then be analytically computed from the impedance data at each individual frequency value. As such, this method facilitates the analysis of how R_j and C_j vary with frequency. It is worth noting that this analytic approach cannot be used for more complex equivalent circuits with more than two unknowns.

As further elaborated in section 3.4, throughout this study the low-frequency values of R_j and C_j from these two different methods closely align. However, differences between the methods emerge as the frequency exceeds a certain threshold.

3.4. Results

In section 3.4.1 the validity of the CNLS and analytic approach are compared over the whole tested frequency range. Subsequently, in section 3.4.2 it is demonstrated how the silicon bulk properties influence these results. Finally, section 3.4.3 discusses how the impedance changes when a LH junction is added to the device structure. These three sections represent the main findings from this work. Design factors that have a more subtle influence on the impedance, such as variations in the dopant concentration and/or junction depth (t_E and t_{BSF}) of the emitter and BSF, are not reported in this study.

3.4.1. PN junction impedance at high frequency

In this section, the evolution of the PN junction impedance is discussed as the frequency reaches a level where the minority carrier concentration profile can no longer follow the AC signal. Previous literature suggests that the diffusion capacitance "contributes a frequency-dependent diffusion capacitance to the total capacitance" [159]. Additionally, it has been observed that the diffusion capacitance "relaxes" at high frequencies, meaning that its value reduces with frequency [127]. While discussions often focus on the frequency-dependent behavior of C_j, the frequency-dependence of R_j is typically not discussed, potentially leading readers to assume that R_j remains frequency-independent while C_j decreases with frequency. In some works where a CPE is used in the equivalent model to address the capacitance variations, the resistive elements are typically fixed [107, 135]. However, it is worth pointing out that from Equations 3.3 and 3.4 it can be deduced that once the frequency exceeds a threshold where the condition $\omega\tau_0 \ll 1$ no longer holds, both the real and imaginary parts of the admittance become frequency-dependent. Specifically, both the real and imaginary parts of the admittance start to increase with frequency, indicating a relaxation of both R_j and C_j. This theoretical prediction aligns with the TCAD simulation results from this study. Figures 3.3(a) and 3.3(b) depict the impedance data of the PN junction structure from Figure 3.2(b) at 0 mV and 500 mV DC bias voltage, respectively. Moreover, these plots include the best CNLS and analytic fits. As expected, the fits from the analytic approach perfectly overlap with the data, since a point-by-point fitting is performed. Additionally, in the bottom two plots in Figures 3.3(a) and 3.3(b), the C_j and R_j values extracted from both the CNLS and analytic methods are plotted as a function of frequency.

Figure 3.3(a) at 0 mV bias shows that the CNLS method offers a high-quality fit across the entire frequency range. Consequently, it might appear reasonable to conclude that

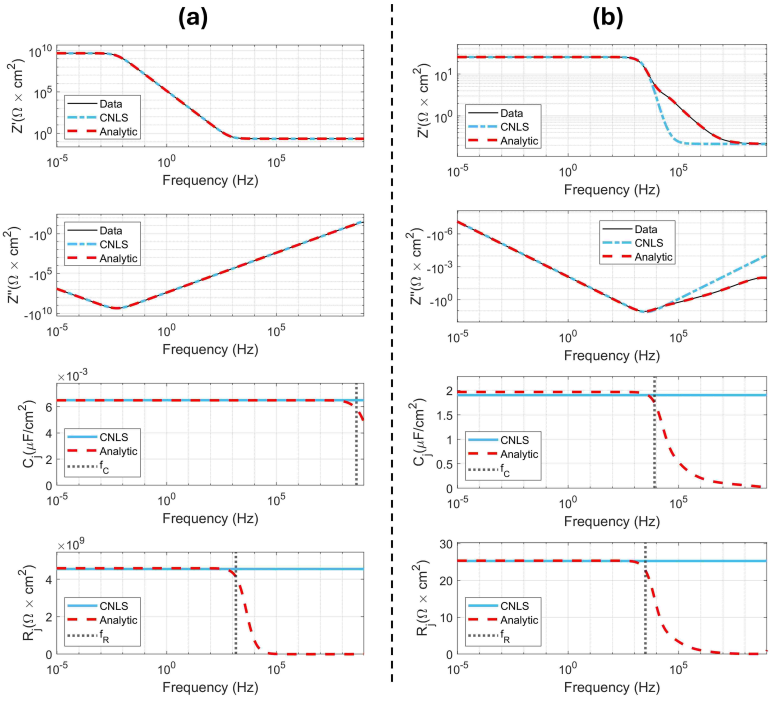


Figure 3.3: (a) Impedance analysis of the PN structure shown in Figure 3.2(b) at 0 mV bias voltage and τ_{SRH} = 10 ms. From top to bottom, the real part of the impedance, the imaginary part of the impedance, C_j and R_j are shown as functions of frequency. In the bottom two plots, f_C = 444 MHz and f_R = 1.4 kHz represent the frequencies where C_j and R_j, respectively, drop below 90% of their low-frequency value. (b) Impedance analysis of the same PN structure under a forward bias voltage of 500 mV, with τ_{SRH} = 10 ms. The plots follow the same order as in (a), with f_C = 8.1 kHz and f_R = 3.1 kHz.

R_j and C_j maintain fixed values throughout the frequency spectrum. Indeed, within the low-frequency range, the analytic approach yields identical values for R_j and C_j as the CNLS approach. However, at higher frequencies, the analytic approach indicates that R_j and C_j begin to relax within the tested frequency range. Here, f_C and f_R denote the frequencies where C_j and R_j, respectively, have dropped below 90% of their low-frequency value. In Figure 3.3(a), f_C and f_R are 444 MHz and 1.4 kHz, respectively. While the high value of f_C can be attributed to the dominance of the depletion capacitance, the relatively low value of f_R may seem unexpected, considering the high-quality CNLS fit. However, closer inspection reveals slight deviations between the CNLS fit and the impedance data, although these deviations are relatively minor and may not conclusively demonstrate that R_j has indeed become variable.

Nevertheless, Figure 3.3(b) at 500 mV forward bias provides deeper insights. Here, the deviations between the best CNLS fit and the impedance data clearly highlight the shortcomings of fixed circuit elements in accurately describing PN junction physics. The analytic approach suggests that f_R remains similar to the 0 mV bias case, at 3.1 kHz. Moreover, at 500 mV bias, the anticipated variability of C_j becomes noticeable from f_C =

8.1 kHz and higher. The lower value of f_C at 500 mV compared to 0 mV can be attributed to the dominance of the diffusion capacitance over C_j in this case. In this study it was confirmed that no good fit can be achieved over the whole frequency range when R_j is held fixed and C_j is calculated at each individual frequency. Instead, the only plausible explanation is that both R_j and C_j relax with increasing frequency when f_R and f_C are exceeded, respectively. Finally, it is worth noting that in Figure 3.3(b), the low-frequency value of C_j differs slightly between the CNLS and the analytic method. This difference arises because the CNLS fit is performed over the entire frequency range, also optimizing the fit beyond the frequency where C_j and R_j start to relax.

3.4.2. Bulk properties influence on PN junction impedance

In PN junctions where one side has a much higher dopant concentration than the other, the impedance is mainly affected by the properties of the lowly doped side of the junction. In the context of solar cells, it is thus important to mention that the substrate dopant concentration has a strong impact on the impedance [73]. However, since this effect is already well-known, the focus in this section shifts toward another bulk property, which is the bulk trap density. Specifically, the influence of bulk trap density is investigated by varying τ_{SRH} in the PN junction structure depicted in Figure 3.2(b). Figure 3.4(a) illustrates how the low-frequency C_j (determined using the analytic approach) varies as a function of τ_{SRH} for various applied DC bias voltages. At low bias voltage between 0 mV and 200 mV, where the depletion capacitance dominates, C_j does not depend on τ_{SRH}. This observation aligns with Equation 2.3, which states that C_{dep} is independent of the minority carrier lifetime. However, at higher bias voltages, a different trend emerges. Specifically, in the range where τ_{SRH} is lower than 10^{-4} s, C_j exhibits a strong increase with τ_{SRH}. It is worth noting that the simulated C_j-τ_{SRH} relationship deviates from the square root dependency predicted by Equation 2.4. This deviation arises because, in the simulated device structure with a bulk thickness of 200 μm, a small fraction of carriers recombines at the ideal contacts rather than in the bulk. A reference simulation with a bulk thickness of 1000 μm and a τ_{SRH} variation between 10^{-7} s and 10^{-4} s (not shown in this paper) confirms this, as it exhibits the square root dependency predicted by Equation 2.4. Moreover, above $\tau_{SRH} = 10^{-4}$ s, the dependency of C_j on τ_{SRH} diminishes. Presumably, this trend is attributed to the decreasing dominance of SRH recombination. As the hole diffusion length approaches or exceeds the bulk thickness, the effective lifetime in the bulk becomes dominated by minority carrier recombination at the ideal contacts. Indeed, as the effective hole lifetime increases from 10^{-5} s to 10^{-4} s, the theoretical relationship for the diffusion length ($L_p = \sqrt{D_p \tau_{p0}}$) predicts that L_p increases from 110 μm to 349 μm, hereby exceeding the bulk thickness. In cases where the bulk thickness is much smaller than the minority carrier diffusion length, commonly observed in solar cells, the diode is referred to as a *short diode*. The short diode explanation was further supported by confirming that for low τ_{SRH}, C_j does not depend on the bulk thickness, whereas for high τ_{SRH}, C_j does vary with the bulk thickness. However, these additional results are not included in this article. Furthermore, Figure 3.4(b) demonstrates the variation of R_j with τ_{SRH}. As expected, an increase in τ_{SRH} corresponds to higher R_j values since the spatial distribution of minority carrier holes in the n-type bulk becomes less steep. Similar to the behavior observed for C_j in Figure 3.4(a), stabilization occurs as

τ_{SRH} approaches levels where the short diode approximation applies. It is worth noting that this stabilization is not observed around 0 mV bias, presumably due to the dominance of generation and recombination currents at low voltages, unlike the diffusion current observed in forward bias [114].

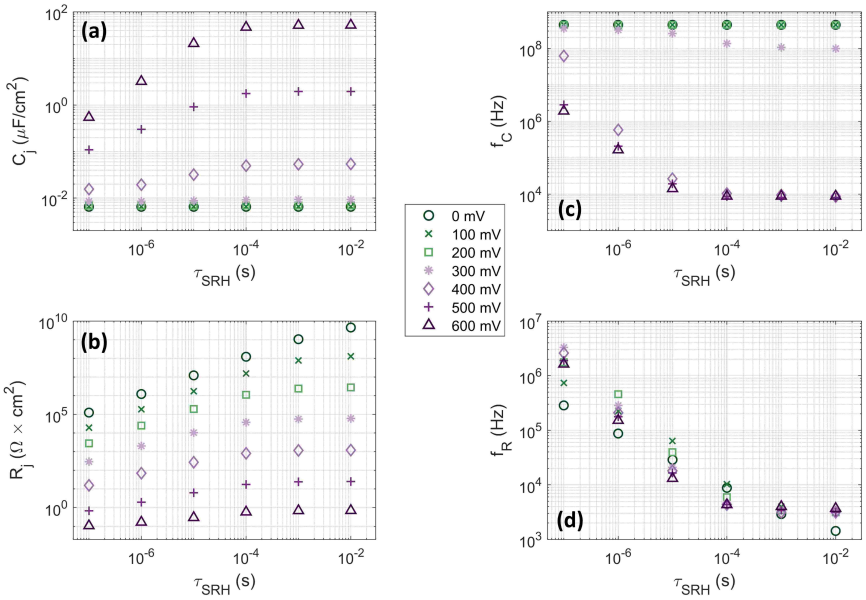


Figure 3.4: Equivalent circuit element analysis of the PN structure of Figure 3.2(b). In (a) and (b), the low-frequency C_j and R_j, which are determined using the analytic method, are presented as a function of τ_{SRH} for various DC bias voltages, respectively. Moreover, in (c) and (d), f_C and f_R are plotted as functions of τ_{SRH} for various DC bias voltages. f_C and f_R denote the frequencies where C_j and R_j, respectively, have dropped below 90% of their low-frequency value.

In Figure 3.4(c), f_C is plotted as functions of τ_{SRH}. In the low-voltage region, where C_{dep} dominates, f_C remains relatively high and independent of τ_{SRH}. However, in forward bias it can be observed that f_C decreases with increasing τ_{SRH}, with a stabilization occurring towards high τ_{SRH}. Similarly, Figure 3.4(d) demonstrates that f_R varies with τ_{SRH}, exhibiting a stabilization trend towards high τ_{SRH}. This stabilization aligns with the earlier explanation that the impedance becomes less influenced by the bulk trap density as τ_{SRH} reaches a value where the short diode approximation becomes valid.

In Figure 3.5, the Nyquist spectra of the PN junction devices at 500 mV forward bias are presented for varying τ_{SRH} values ranging from 10^{-7} s to 10^{-2} s. In each plot, f_R and f_C are highlighted. Notably, f_R and f_C decrease as τ_{SRH} becomes higher. However, since the values of R_j and C_j change as well, f_R and f_C consistently fall within the frequency regime where the Nyquist spectra are near the top of the semi-circle. Consequently, all plots visibly deviate from the semi-circular shape expected of an RC-loop, indicating the frequency-dependence of R_j and C_j. However, it must be noted that the shape of the Nyquist spectra may change when a LH junction is added at the negative contact. Further discussion on this topic is provided in the next section.

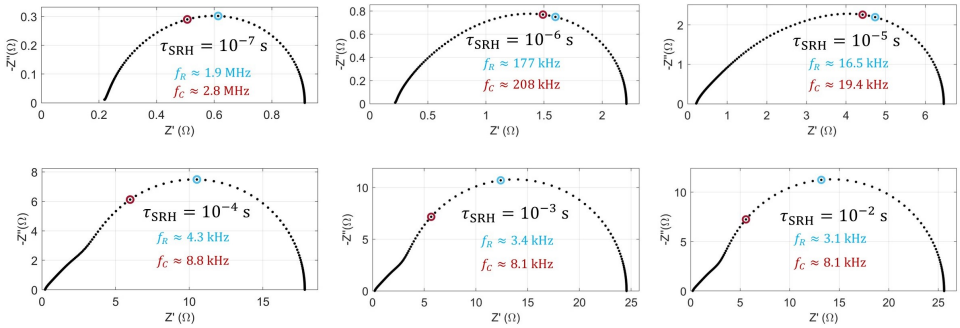


Figure 3.5: Nyquist spectra of the PN structure of Figure 3.2(b) at 500 mV forward bias for varying τ_{SRH}. f_C and f_R are highlighted in each plot.

3.4.3. Low-high junction influence

In this section, the influence of a highly doped n^+-layer on the impedance is examined. As previously mentioned, practical c-Si solar cells commonly incorporate such a LH junction, also known as a back surface field (BSF). In addition to facilitating tunneling, the BSF serves as a barrier that prevents minority holes in the n-region from diffusing to the defective metal-semiconductor interface [1]. Consequently, SRH recombination is reduced and the open-circuit voltage (V_{oc}) is enhanced. In literature on impedance spectroscopy for c-Si solar cells, the LH junction is often accounted for by incorporating an additional *RC*-loop into the equivalent circuit of the device [73, 89, 91, 110, 131, 132]. However, there is limited discussion on comparing the impedance of PN junction devices with and without a BSF. Presumably, this is because practical devices inherently contain such a junction, making it challenging to experimentally test a device without it. With the simulation approach utilized in this study, further insights can be obtained about the impedance of the LH junction. Comparing an n-type bulk structure (Figure 3.2(a)) with a similar structure incorporating a LH junction at the negative contact (Figure 3.2(c)), the impedance spectra are plotted in Figure 3.6.

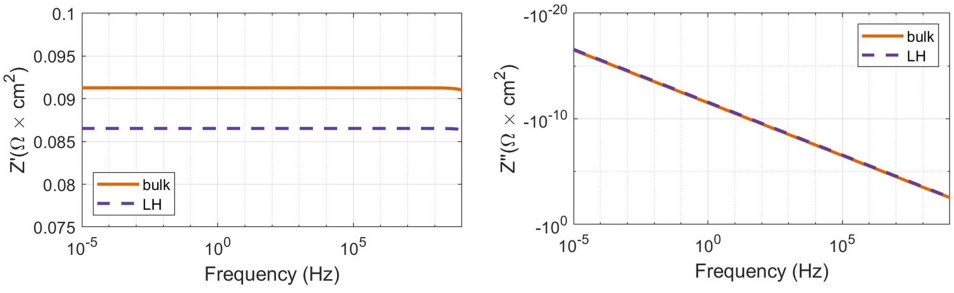


Figure 3.6: Impedance of the n-type bulk structure of Figure 3.2(a) and the n-type bulk with n^+-doped LH structure of Figure 3.2(c). τ_{SRH} = 10 ms and W_c and W_{bulk} are both equal to 500 μm. The plots are for 0 mV bias, but the results are nearly identical when a positive bias voltage is applied to the bulk contact with respect to the BSF contact.

In Figure 3.6 it is evident that the Z' of the LH structure is slightly lower than that of the bulk structure, which is due to the higher conductivity in the n^+ layer. Moreover, it can be observed from Figure 3.6 that both impedance spectra exhibit predominantly resistive behavior, with Z' remaining constant and Z'' negligibly small across most frequencies. Hence, it is worth noting that this result confirms the validity of assuming a constant R_s value in the analytic approach employed in this study. Only at the upper-frequency limit does Z'' become measurably large compared to Z', leading to a -1.7° phase shift at 1 GHz. The evolution of Z'' with frequency in Figure 3.6 appears in both the bulk structure with and without the LH junction. This effect is presumably due to the device's geometric capacitance, with the silicon bulk acting as the dielectric and the contacts as plates. However, in real-world devices this effect would likely be obscured, as inductance tends to dominate Z'' at high frequencies. Consequently, two key observations emerge. Firstly, the LH junction device structure exhibits lower Z' compared to the bulk, meaning that the LH junction only lowers the series resistance and does not introduce additional resistive effects. Secondly, the LH junction itself does not seem to introduce dynamic effects within the frequency range of interest.

In spite of the previous observations, the presence of a LH junction can significantly affect the impedance of a full PN junction device. To illustrate this, the impedance of (1) a PN device structure and (2) a PN/LH device structure are depicted in Figure 3.7. In the simulations it was observed that for both bias voltages, the electrostatic potential across the PN junction remains virtually unchanged between the device structures with and without the LH junction. This is related to the fact that the applied voltage mainly drops across the PN junction, rather than over the LH junction. Therefore, the differences in the impedance spectra due to addition of a LH junction are not related to changes in the bias voltage across the PN junction.

In the case of the 0 mV bias voltage depicted in Figure 3.7(a-b), there is a noticeable difference in the overall impedance between the two structures. Using the analytic approach, the differences in R_s and the low-frequency values of R_j and C_j upon addition of the LH junction are compared. The low-frequency R_j increases from 4.54×10^9 Ωcm^2 to 1.25×10^{10} Ωcm^2, while R_s decreases from 0.22 Ωcm^2 to 0.088 Ωcm^2. The increase in R_j can primarily be attributed to the fact that the BSF repels minority carriers from the negative contact. Consequently, the distribution of minority carriers throughout the bulk becomes less steep, resulting in an increase in R_j. Conversely, the decreased R_s can be attributed to the enhanced lateral charge carrier transport within the highly doped region of the LH junction. It is worth noting that the low-frequency C_j remains unchanged at 6.50 nF/cm^2 between the two device structures. This consistency can be attributed to the fact that the depletion capacitance solely relies on the ionized atoms within the depletion region of the PN junction.

For the 500 mV case in Figure 3.7(c-d), the addition of the LH junction increases the low-frequency R_j from 25.3 Ωcm^2 to 801 Ωcm^2. R_s is again decreased from 0.22 Ωcm^2 to 0.088 Ωcm^2. The explanations are similar to the 0 mV case. However, opposed to the 0 mV case, the addition of the LH junction at 500 mV increases the low-frequency C_j from 1.97 $\mu F/cm^2$ to 2.72 $\mu F/cm^2$. This increase can be attributed to the fact that the BSF repels the minority carrier holes from the negative contact, increasing the effective lifetime of holes stored in the silicon bulk. Furthermore, it is worth reflecting how the

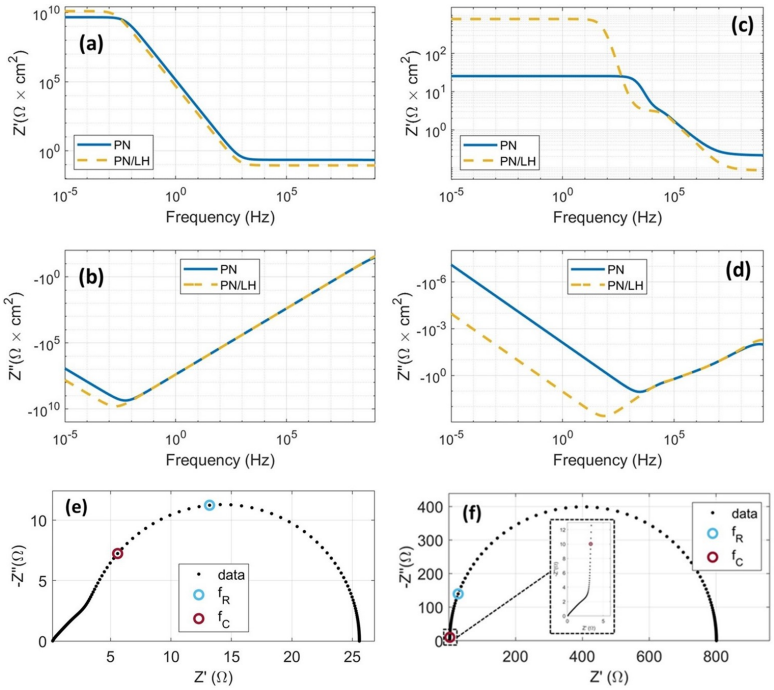


Figure 3.7: Comparison between the impedance of the PN structure of Figure 3.2(b) and the PN/LH structure of Figure 3.2(d) for τ_{SRH} = 10 ms. (a) and (b) present the impedance at 0 mV bias, whereas (c) and (d) are at 500 mV forward bias. Finally, (e) and (f) show the Nyquist spectra at 500 mV forward bias of the PN and PN/LH structure, respectively. For the PN structure at 500 mV bias, f_R and f_C are 3.1 kHz and 8.1 kHz, respectively. In contrast, for the PN/LH structure, f_R and f_C decrease to 0.40 kHz and 5.9 kHz, respectively.

addition of the LH junction affects the Nyquist plots. The Nyquist spectra at 500 mV bias are presented in Figure 3.7(e) for the PN device, and in Figure 3.7(f) for the PN/LH device. At first glance, the Nyquist spectrum of the device with the PN/LH junction seems to closely resemble a semi-circular shape, as opposed to the PN structure. However, the zoomed-in view in Figure 3.7(f) shows that the high-frequency variations of R_j and C_j still occur and create distortions to the high-frequency tail of the Nyquist spectrum.

In this section, it was demonstrated that the LH junction exhibits no significant impedance characteristics by itself. This finding contrasts with existing literature, where the LH junction is often represented as an additional RC-loop in series with the R_j-C_j loop [73, 89, 91, 110, 131, 132]. Indeed, particular combinations of parameters in devices with a PN/LH structure can result in a Nyquist plot resembling that of two RC-loops in series. For instance, Figure 3.8 illustrates how the Nyquist spectra of a PN/LH device changes when the bulk dopant concentration is changed between N_{sub}=1 × 10^{15} and N_{sub}=5 × 10^{16} cm^{-3}. While one resembles a single semicircle, the other might be mistaken for two superimposed semicircles. However, this study suggests that the inclusion of an R_{LH}-C_{LH} loop to the model does not accurately represent the underlying physics. Instead, its inclusion in the model appears to account for the frequency-dependent

variations in R_j and C_j. Throughout our investigation, instances were observed where the two RC-loop model falls short in explaining the impedance spectra adequately, indicating that the relaxation of R_j and C_j is a more plausible explanation. Moreover, such relaxation phenomena cannot always be easily detected through Nyquist plots on linear scales. Therefore, Bode plots or real and imaginary impedance plots on a logarithmic scale often provide better insights.

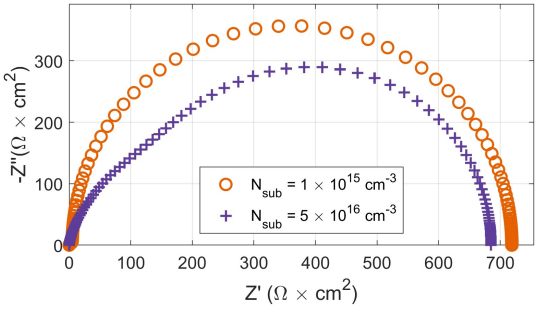


Figure 3.8: Nyquist spectra of the PN/LH structure of Figure 3.2(d) for wafer dopant concentration values of N_{sub}=1 × 10^{15} cm^{-3} and N_{sub}=5 × 10^{16} cm^{-3}. The impedance data are recorded at 500 mV forward bias with the bulk properties set at τ_{SRH} = 10 ms and t_{bulk} = 300 μm.

3.5. Conclusion

The impedance characteristics of PN homojunction devices were investigated, particularly focusing on the effects of frequency, applied bias voltage, bulk trap density, and the presence of a low-high (LH) junction or back surface field (BSF). The employed TCAD simulation method allows to detect subtle trends that may be difficult to identify experimentally due to noise and reactance of metal contacts. Through analysis of the impedance data it was revealed that the PN junction exhibits a fixed RC-loop behavior at low frequencies, but undergoes relaxation in both resistance R_j and capacitance C_j as frequency increases. Additionally, it was found that when the bulk defect density decreases below a certain threshold, the effective minority carrier lifetime in the bulk becomes limited by recombination at the contacts. In this regime, the short diode approximation effectively explains various observed impedance trends and factors such as wafer thickness and the presence of a BSF strongly affect the impedance. Notably, it was shown that the addition of a LH junction repels minority carriers from this contact, hereby impacting the impedance by altering R_j, C_j, and R_s. While various publications on solar-cell impedance model the low-high (LH) junction using an RC-loop, the findings presented in this chapter indicate that such a model does not accurately represent the underlying physics. Instead, this approach is likely compensating for the frequency-dependent behavior of R_j and C_j. The insights from this chapter are important for solar-cell applications that require a thorough understanding of the small-signal response. Moreover, this work serves as a basis for fully understanding the impedance of solar cells with passivating contacts.

4

Solar-cell impedance across varied temperature and illumination conditions

This chapter is based on the following publication:

D. A. van Nijen, S. Naoom, M. Muttillo, P. Procel, M. Zeman, O. Isabella and P. Manganiello, "Analyzing the PN junction impedance of crystalline silicon solar cells across varied illumination and temperature conditions", in *Solar Energy Materials and Solar Cells*, vol. 279, 113255, 2025.

The data underlying this chapter was published in the 4TU Research Data Archive [*].

4.1. Introduction

In the pursuit of exploiting the solar-cells impedance in these applications, it is important to mention that the impedance of a solar cell can vary. For instance, when solar cells are deployed in real-world conditions, they are subjected to varying levels of irradiance and temperature. To compensate for these environmental changes, MPPT is employed, which continually adjusts the operating voltage of the solar cell. This dynamic interaction of multiple factors leads to fluctuations in the impedance during practical operation. It is expected that there may be some variation in series resistance during operation [89, 131, 160], whereas the changes in the inductance would be limited [161, 162]. However, the PN junction impedance dominates the overall impedance at low frequency and is anticipated to show the highest variability with changes in bias voltage, irradiance, and

[*] D. A. van Nijen et al., "Data underlying the publication: Analyzing the PN junction impedance of crystalline silicon solar cells across varied illumination and temperature conditions", 4TU.ResearchData, 2024, `https://doi.org/10.4121/5b387cd1-9b99-4042-a7b5-e92f5ad198a4`.

temperature. Additionally, the greatest knowledge gap relates to a quantification of the variability of the PN junction impedance.

Consequently, the primary objective of this study is to understand how the PN junction impedance of modern crystalline silicon (c-Si) solar cells varies under real-world operating conditions. Impedance data are gathered through both experimental impedance spectroscopy and Technology Computer-Aided Design (TCAD) simulations. The experimental part of the study is performed using single-cell laminates based on commercial Passivated Emitter and Rear Contact (PERC) and interdigitated-back-contact (IBC) solar cells. The TCAD part is conducted using a Tunnel Oxide Passivated Contact (TOPCon) solar cell architecture with efficiency approaching the performance limit of c-Si cells. It is worth noting that the architecture of a solar cell (e.g., aluminium back surface field, PERC, silicon heterojunction, TOPCon, IBC) has little influence on the capacitance-voltage (C-V) relationship. Instead, the C-V relationship is primarily affected by the substrate dopant concentration (N_{sub}), also known as the wafer or bulk dopant concentration [73]. Specifically, a low N_{sub} leads to high capacitance in forward bias. Moreover, a highly efficient cell likely has a high maximum power point voltage (V_{mpp}), which in turn leads to an increased capacitance during operation. By experimentally examining the impedance of cells with different values of N_{sub} and V_{mpp}, we gain insights into the variations among modern commercial c-Si solar cells. Moreover, the TCAD simulations provide insights into the behavior of solar cells approaching the efficiency limit.

The paper is structured as follows: The method is detailed in section 4.2; In section 4.3, the small-signal equivalent modeling of solar-cell impedance is discussed, along with discussions on the limitations of the employed model; Section 4.4 presents the results and discussion; Finally, the conclusions are given in section 4.5.

4.2. Method

4.2.1. Experimental impedance characterization

For the experimental part of this study, two single-cell laminates based on commercial c-Si solar cells were fabricated. The first laminate was based on an interdigitated-back-contact (IBC) solar cell laminated in a stack consisting of glass - EVA (ethylene vinyl acetate) - cell - EVA - backsheet. The second laminate was based on a PERC solar cell laminated in a stack consisting of glass - TPO (thermoplastic polyolefin) - cell - TPO - backsheet. For both laminates, the cell area, substrate dopant concentration (N_{sub}), built-in potential (V_{bi}), and standard test conditions (STC) parameters are presented in Table 4.1. These specific cells were selected because the PERC cell has a high N_{sub} and low V_{mpp}, whereas the IBC cell has a low N_{sub} and high V_{mpp}. Therefore, the operational capacitance of these cells is expected to be around the lower and upper limits that can be anticipated from modern commercial c-Si solar cells.

For the experimental impedance characterization of this study, an in-house developed impedance spectroscopy setup is employed. During the impedance recordings, the cell is biased at a certain direct current (DC) operating point, after which a small-signal alternating current (AC) voltage is superimposed. The resulting AC waveforms of the voltage and current signals are analyzed using lock-in amplifiers. The employed setup is

Table 4.1: Properties of the single-cell laminates employed in this study. N_{sub} and V_{bi} are extracted in dark conditions according to the methodology presented in a previous publication [73]. Moreover, the efficiency, the open-circuit voltage (V_{oc}), the short-circuit current density (J_{sc}), the fill factor (FF), and the maximum power point voltage (V_{mpp}) are all obtained in STC conditions using a LOANA solar cell analysis system [113].

	IBC	**PERC**
Cell area (cm^2)	153	122.15
N_{sub} (atoms × cm^{-3})	1.0×10^{14}	8.0×10^{15}
V_{bi} (mV)	0.58	0.63
Efficiency (%)	23.75	18.46
V_{oc} (V)	725.0	649.6
J_{sc} (mA/cm^2)	40.49	36.47
FF (-)	0.809	0.779
V_{mpp} (V)	622	534

similar to one reported in a previous publication [73], but includes some modifications:

- A controllable LED-based light source with an AM1.5-like spectrum in the visible range is fixed above the solar laminate, allowing to set the irradiance.
- During the measurements, the laminate is placed on an 80 cm × 80 cm temperature-controlled plate, enabling temperature regulation. The laminate temperature is monitored using a thermocouple and a Pico logger. In the case of the PERC laminate, the thermocouple is directly attached to the back of the solar cell and included in the lamination stack. In the case of the IBC laminate, the thermocouple is attached to the backsheet of the laminate.
- Similar to previous work [73], the output of an OPA-549 op-amp, configured as a non-inverting summing amplifier, is connected at the positive contact of the solar cell. However, unlike the direct connection of the negative contact of the solar cell to the ground in prior work, in this study, we connect the negative contact to the negative terminal of a second OPA-549 op-amp. This configuration ensures compatibility with the utilized unidirectional power supply when a photocurrent arises in the solar cell.

A schematic representation of the employed impedance spectroscopy setup is shown in Figure B.1 of Appendix B.1. Throughout this study, all reported experimental impedance measurements are conducted once the solar-cell temperature stabilizes at the desired level. The temperature is varied from 30 °C to 60 °C, while the irradiance ranges from dark conditions to 0.5 sun. The reported frequency range for the experimental impedance data spans from 5 Hz to 10 kHz.

4.2.2. TCAD impedance simulations

Furthermore, as solar cells get closer to the performance limit in the coming years, their impedance may change. To investigate this, a performance-limit c-Si device is studied by using the finite element simulator TCAD Sentaurus [158]. A TOPCon architecture was selected, as this is predicted to become the dominant cell concept in terms of market

share by 2024 [11]. Specifically, the simulated cell structure is a specific type of TOPCon architecture known as the PeRFeCT (Passivated Rear and Front ConTacts) solar cell [163]. This device architecture features: (i) a highly transparent lightly P-doped homojunction as front surface field (FSF); (ii) a P-doped TOPCon layer formed only underneath the front metal grid; (iii) a rear emitter with a B-doped poly-Si layer deposited on thin SiO_x. While utilizing the PeRFeCT device architecture, the device parameters are adjusted to approach the performance limit of c-Si devices, similar to a previous publication [164]. Regarding the structure, the wafer thickness is 200 μm and the front side metallization coverage is 0.833% with a finger width of 5.0 μm. At $N_{sub} = 3.2 \times 10^{15}$ cm^{-3}, the simulated efficiency under STC reaches 26.9%, with an open-circuit voltage of 739 mV, a short-circuit current density 43.4 mA/cm^2, a fill factor of 0.841, and a maximum power point voltage of 649 mV.

The small-signal AC analysis is conducted using the *ACCoupled* solve section of TCAD Sentaurus. This simulation generates a frequency-dependent impedance matrix, comprising the real and imaginary parts of the impedance at each frequency examined during the AC analysis. In this study, the reported frequency range spans from 1 nHz to 1 MHz. The temperature is varied from 15 °C to 75 °C, while the irradiance ranges from dark conditions to 1.2 suns.

4.2.3. Small-signal equivalent circuit fitting

Figure 4.1 shows the small-signal equivalent circuit that is used in this study to model the solar-cell impedance. The parallel resistor-capacitor circuit (RC-loop) represents the PN junction impedance, with R_j being the PN junction resistance and C_j the PN junction capacitance. Moreover, the circuit in Figure 4.1 includes a series resistance R_s and an inductance L_s. Notably, due to the findings in Chapter 3, the circuit does not include an RC-loop to represent the low-high junction. While the model in Figure 4.1 generally gives an effective representation of the solar-cell impedance, it is worth noting that it does not account for certain high-frequency phenomena related to the minority carrier diffusion. These limitations are further discussed in section 4.3.

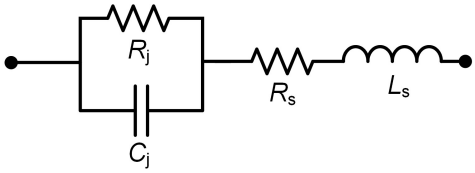


Figure 4.1: Solar cell small-signal circuit that is employed in this study for equivalent model fitting.

The impedance of the circuit in Figure 4.1 is given by the following equation:

$$Z = i\omega L_s + R_s + \left[R_j \parallel \frac{1}{i\omega C_j} \right] \tag{4.1}$$

where i denotes the imaginary unit. Equation 4.1 can be rewritten into the form $Z = Z' + iZ''$ with the real part Z' and the imaginary part Z'' being defined as follows:

$$Z^{'} = R_s + \frac{R_j}{1 + R_j^2 \omega^2 C_j^2} \tag{4.2}$$

$$Z^{''} = \omega L_s - \frac{R_j^2 \omega C_j}{1 + R_j^2 \omega^2 C_j^2} \tag{4.3}$$

To determine the values of the circuit parameters in Figure 4.1 at any bias voltage V_{DC}, Equations 4.2 and 4.3 are simultaneously fitted to the recorded impedance data through complex nonlinear least-squares (CNLS) analysis [137]. For the fitting procedure, the MATLAB *lsqcurvefit* solver is used, with the fitting parameters being C_j, R_j, L_s, and R_s.

4.3. Impedance modeling considerations

4.3.1. High-frequency R_j and C_j relaxation

There are typically two junctions present in c-Si solar cells, which are the PN junction and the low-high (LH) junction. It is widely acknowledged that the impedance of a PN junction can be modeled using a parallel resistor-capacitor circuit (*RC*-loop) [114]. Additionally, in studies on solar-cell impedance, the LH junction is often accounted for by incorporating into the equivalent circuit an additional *RC*-loop in series with the PN-junction *RC*-loop [73, 89, 91, 110, 131, 132]. In recent publications on TOPCon and silicon heterojunction cells, a constant phase element (CPE) or a third *RC*-loop is even introduced to solar-cell impedance models to address various non-ideal effects in such devices [107, 135]. While good fitting quality can be achieved, linking the elements in these advanced equivalent circuits to the underlying physics remains challenging. For instance, in Chapter 3 of this thesis it was demonstrated that this approach of modeling the LH junction with an *RC*-circuit does not accurately represent the underlying physics [165]. Instead, it was shown that the inclusion of a second *RC*-loop accounts for the relaxation of R_j and C_j with frequency. It is worth noting that the relaxing behavior of R_j and C_j sometimes manifests in the impedance in a manner closely resembling the impedance of two *RC*-loops. Depending on the solar cell under study and its operating conditions, this modeling approach based on two series-connected *RC*-loops may still yield accurate fitting results

4.3.2. Model accuracy at different bias voltages

This section elaborates on when and how the relaxation of R_j and C_j manifests in the impedance of a solar cell. Figure 4.2 illustrates TCAD-generated impedance spectra of the TOPCon solar cell with an area of 153 cm^2 at different bias voltages (0 mV, 400 mV, 650 mV). For each voltage, the real part (Z'), imaginary part (Z''), magnitude, and phase of the impedance are depicted as functions of frequency. Additionally, each plot includes the optimal CNLS fit using the circuit from Figure 4.1. It is important to note that a series resistance of $R_s = 5$ mΩ and an inductance of $L_s = 60$ nH, which are realistic values for the metal contacts in commercial solar cells [73], have been added to the TCAD-generated impedance data in Figure 4.2. This adjustment ensures that the analysis does not overly emphasize impedance trends that would not be detectable in real-world devices.

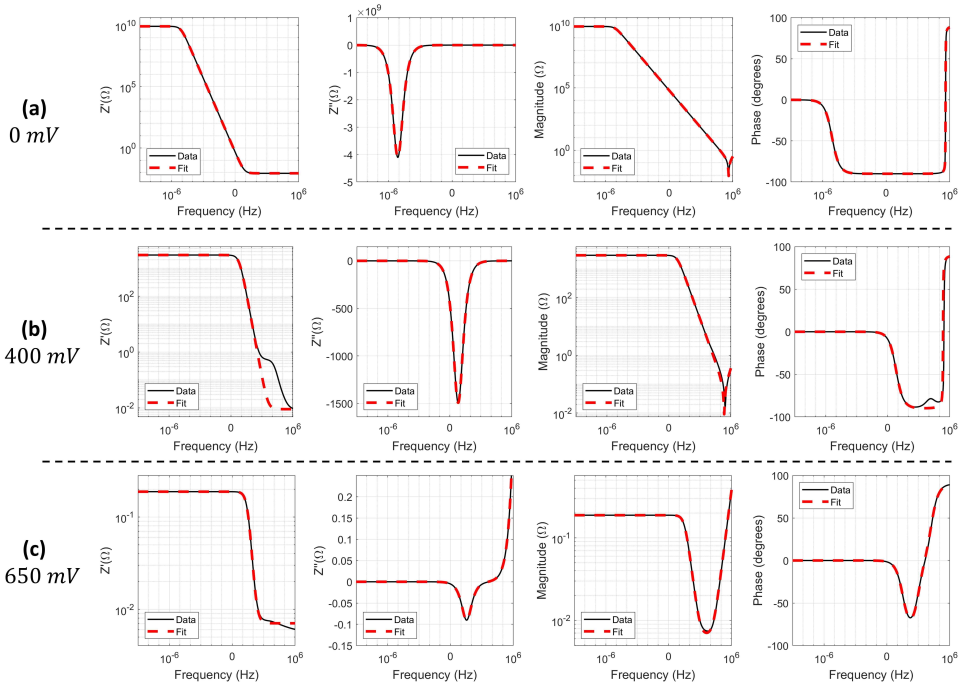


Figure 4.2: TCAD-generated impedance data of TOPCon solar cell with best CNLS fits at (a) 0 mV bias, (b) 400 mV bias, and (c) 650 mV bias. For each bias voltage, the plots display (from left to right) the real part (Z'), imaginary part (Z''), magnitude, and phase of the impedance. All impedance data are simulated under dark conditions at a temperature of 25 °C.

In Figure 4.2(a) at a bias voltage of V_{DC} = 0 mV, it is evident that the model gives an accurate fit, which is consistent with previous research [73]. However, as depicted in Figure 4.2(b) at V_{DC} = 400 mV, it is apparent that the employed small-signal equivalent circuit fails to fully capture the impedance. While the fitting quality is high in the low-frequency range up to about 100 Hz, a deviation becomes noticeable for Z' at higher frequencies. This discrepancy is likely related to the relaxation of R_j and C_j [165]. At V_{DC} = 650 mV, as shown in Figure 4.2(c), the same relaxation phenomenon occurs. However, in this case it occurs at a frequency where Z' is already dominated by the series resistance (R_s). Consequently, the overall fit is considerably improved at 650 mV compared to 400 mV. In general, if the frequency at which Z' starts to be dominated by R_s is low enough, as seen in Figure 4.2(a) and 4.2(c), the model yields accurate fits. However, if the relaxation of R_j and C_j occurs at a frequency lower than the point where Z' becomes dominated by R_s, as shown in Figure 4.2(b), a deviation may occur between the fit and the actual impedance. Finally, it is worth mentioning that the data presented in Figure 4.2 has little to no noise, since it is generated through TCAD simulations. When some noise is present during an experimental measurement, it can become more challenging to detect the relaxation of R_j and C_j.

4.3.3. Impedance modeling in practice

In the previous section, it was shown that in the bias voltage range above 0 mV and below the MPP voltage (V_{mpp}), the fit can deviate somewhat at high frequencies. However, since the fitting accuracy is high at low frequencies, the low-frequency values of R_j and C_j are still well identified by the employed procedure. Furthermore, when the tested solar cells are biased around their V_{mpp}, the small-signal equivalent circuit of Figure 4.1 yields satisfactory fitting quality. To illustrate this, the impedance data of the different solar cells from this study are presented along with the CNLS fits in Figure 4.3. Specifically, the impedance data are recorded at the V_{mpp} of each cell at 0.5 sun irradiance and a temperature of 30 °C. Figure 4.3(a) includes TCAD-generated impedance data of the TOPCon solar cell with an area of 153 cm^2 and an added series resistance of R_s = 5 mΩ and inductance of L_s = 60 nH. Additionally, Figure 4.3(b) and 4.3(c) present experimentally recorded impedance data of the IBC and PERC solar cell, respectively. The achieved fitting accuracy in Figure 4.3 confirms the validity of the employed small-signal equivalent circuit at MPP. Finally, it is worth noting that while the impedance of the TOPCon and IBC devices at 10 kHz is dominated by inductive behavior, as indicated by a positive phase shift, the impedance of the PERC device remains dominated by the PN junction capacitance, resulting in a negative phase shift. Such differences between solar cells can be important for optimizing the design of power converters that perform maximum power point tracking.

4.4. Results and discussion

4.4.1. Effect of illumination

This section analyzes the effect of illumination on the PN junction impedance in solar cells. Before presenting the results obtained in this study, it is useful to briefly review the state of the art on this topic. It is known that the additional majority carriers generated due to illumination affect the depletion region width [88]. In previous publications it is described how the depletion region width in short-circuit condition approximately changes due to illumination [166, 167]. For instance, for the p-side of a given PN junction, this change is described by the following relationship [166]:

$$W_{sc,p} \approx \frac{W_{d,p}}{1+\delta/2} \tag{4.4}$$

with $\delta = \Delta n / N_a$. Here, $W_{sc,p}$ represents the illuminated p-side depletion region width, $W_{d,p}$ denotes the dark p-side depletion region width, Δn is the additional electron density generated due to the illumination, and N_a signifies the acceptor concentration on the p-side of the junction. Since the value of δ is inversely related to N_a, illumination leads to a more pronounced reduction in the depletion region width for lower dopant concentrations. Additionally, it is important to consider that a change in irradiance alters the DC current flowing through the device. Consequently, the effective voltage drop over the series resistance changes when the irradiance level is adjusted. Thus, even if the applied bias voltage at the outer device terminals remains unchanged, the irradiance level affects the effective voltage drop over the PN junction. In fact, it has been suggested that the change in effective voltage drop is the only effect that illumination has on the PN junction impedance in solar cells [89]. To verify this, a useful feature of the TCAD

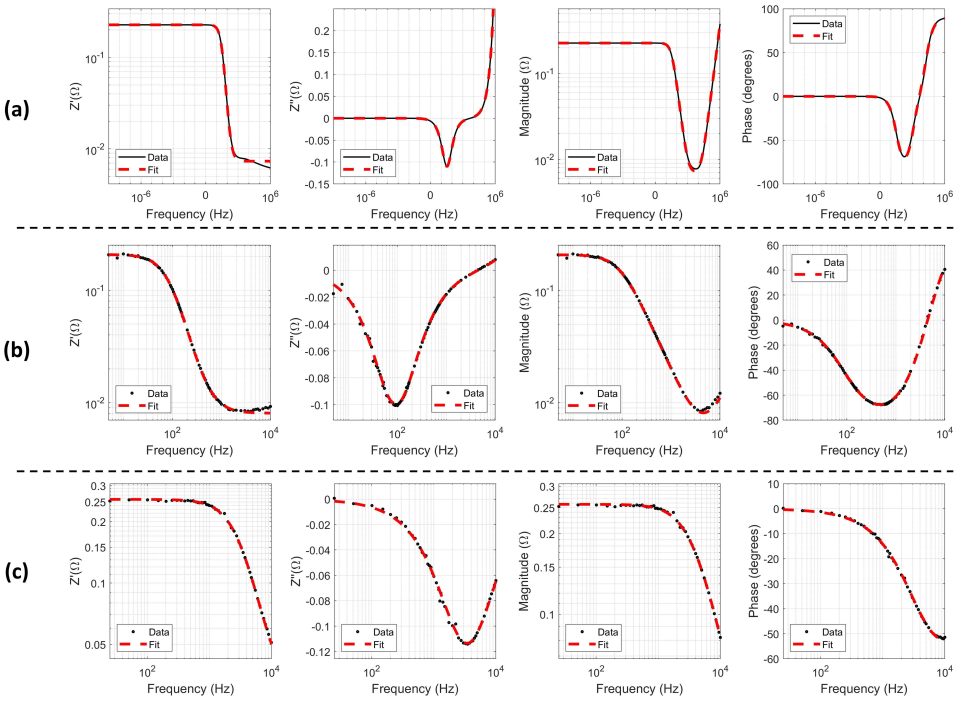


Figure 4.3: Impedance at the maximum power point voltage with best CNLS fits for (a) the TCAD-generated impedance data of the TOPCon device, (b) the experimentally recorded impedance data of the IBC solar cell laminate, and (c) the experimentally recorded impedance data of the PERC solar cell laminate. The plots display (from left to right) the real part (Z'), imaginary part (Z''), magnitude, and phase of the impedance. In all cases, the irradiance is 0.5 suns and the temperature is 30 °C.

approach can be utilized: the effective electrostatic potential across the PN junction (V_j) can be directly extracted. Therefore, the R_j and C_j values can be plotted as functions of the applied voltage on the outer terminals, as well as functions of the V_j.

In Figure 4.4, the CNLS-fitted values of R_j and C_j are analyzed for the TCAD-simulated TOPCon device, across varying irradiance levels between dark conditions and 1.2 suns. Specifically, in Figure 4.4(a) and Figure 4.4(b), the R_j and C_j values are plotted as functions of the applied forward bias voltage, respectively. Moreover, the same R_j and C_j values are presented as functions of electrostatic PN junction potential (V_j) in Figure 4.4(c) and Figure 4.4(d), respectively. Furthermore, the corresponding results from the experimental part of this study are shown in Figure B.2 of Appendix B.2.

In Figure 4.4(a), it is evident that at a given applied voltage, an increase in irradiance level lowers R_j. Comparing this to Figure 4.4(c), it becomes apparent to what extent this effect is caused by an illumination-induced change in V_j. At low forward bias in Figure 4.4(c), R_j decreases with increasing irradiance for a given V_j value. This is likely due to two main effects. Firstly, photogenerated charge carriers in the space charge region are swept out by the electric field, giving rise to a drift current. Secondly, at low forward bias, the forward-bias recombination current is often larger than the diffusion current

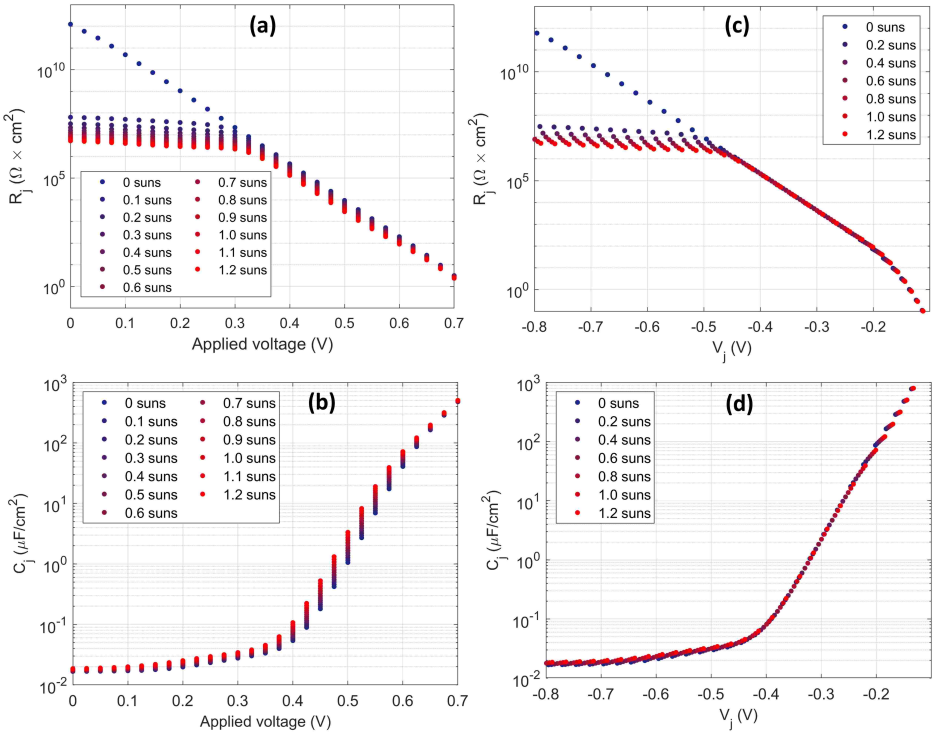


Figure 4.4: Effect of illumination on R_j and C_j, as extracted from TCAD-generated impedance data of a TOPCon solar cell. The irradiance is varied between dark conditions and 1.2 suns in steps of 0.1 sun. (a) shows R_j and (b) shows C_j, both obtained through CNLS analysis and plotted as functions of applied forward bias voltage. Additionally, the same R_j and C_j values are presented as functions of V_j in (c) and (d). The bulk dopant concentration of the simulated solar cell is $N_{\text{sub}} = 3.2 \times 10^{15}$ cm^{-3} and the impedance data is simulated at a temperature of $T = 25\,^{\circ}$C.

[114]. The higher number of excess carriers in the space charge region under illumination increases the likelihood of recombination. Both these factors may be contributing to a reduction of R_j by increasing illumination at low forward bias. It is worth noting that these effects are much less, if at all, visible for the R_j values extracted from the experimental data presented in Figure B.2. In practical devices, the shunt resistance limits R_j around zero bias voltage. Consequently, the change in R_j at low bias voltage caused by illumination is less detectable from the experimental results. Furthermore, at forward bias (e.g., for V_j > -0.45 V), the R_j-V_j relationship of Figure 4.4(c) remains nearly unaffected by illumination. This indicates that the effect that illumination has at high forward bias in Figure 4.4(a) is mostly caused by a change in V_j. Furthermore, in deep forward bias (e.g., for V_j > -0.2 V), the slope of the R_j-V_j relationship in Figure 4.4(c) changes. This changing slope may be caused by two effects. First, it may be related to high-level injection effects. Second, in this range a significant portion of the incremental forward-bias voltage drops across the low-high junction. This reduction in potential barrier height could increase the surface recombination velocity.

In Figure 4.4(b), it is evident that for a given applied voltage, an increase in irradiance does increase C_j. This effect is most pronounced at a forward bias voltage between 0.4 V and 0.6 V. However, in Figure 4.4(d), C_j is plotted as a function of V_j for different irradiance levels. Here, the relationship remains nearly unaffected by illumination, indicating that the earlier changes in C_j due to illumination in Figure 4.4(b) are mostly explained by a shift in V_j. This result is consistent with prior work [89]. Moreover, it is worth noting that the slope of the C_j-V relationship in Figure 4.4(b) reduces at high forward bias (e.g., for V > 0.6 V), whereas the slope remains relatively constant for the C_j-V_j relationship in Figure 4.4(d). This shows that the diminishing slope in Figure 4.4(b) is predominantly caused by the applied voltage dropping across other parts of the device, such as the low-high junction and series resistance, rather than the PN junction. Finally, it is important to mention that at low bias voltage, the extent to which illumination affects C_j for a given applied voltage is strongly affected by the substrate dopant concentration. Indeed, from the experimental results presented in Figure B.2, it is evident that at low bias voltage, the C_j of the IBC device increases more strongly with illumination than that of the PERC device. This is presumably related to its significantly lower substrate dopant concentration, and consistent with the prediction from Equation 4.4.

4.4.2. Effect of temperature

This section analyzes the effect of temperature on the PN junction impedance in solar cells. Before presenting the results, it is useful to briefly review the relevant physics. An increase in semiconductor temperature raises the intrinsic carrier concentration in the material [114], which in turn increases the reverse saturation current density of the PN junction. Consequently, higher temperatures enhance diffusion across the depletion region. Moreover, similar to the previously discussed effect under illumination, the increased intrinsic carrier concentration at higher temperatures can reduce the depletion region width and hence the electrostatic junction potential V_j. Therefore, in the temperature analysis, it is useful to analyze the R_j and C_j values both as functions of the applied voltage on the outer terminals and as functions of V_j.

In Figure 4.5, the CNLS-fitted values of R_j and C_j are analyzed for the TCAD-simulated TOPCon device, across varying temperature levels between 15 °C and 75 °C and under a fixed illumination of 0.5 sun. Specifically, in Figure 4.5(a) and Figure 4.5(b), the R_j and C_j values are plotted as functions of the applied forward bias voltage, respectively. Moreover, the same R_j and C_j values are presented as functions of V_j in Figure 4.5(c) and Figure 4.5(d), respectively. Furthermore, the corresponding results from the experimental part of this study are shown in Figure B.3 of Appendix B.2.

From Figure 4.5(a), it is evident that a higher temperature leads to a lower R_j. However, the change is more prominent at high forward bias than at low forward bias. At low forward bias, the R_j of the TCAD-simulated device is primarily influenced by the forward-bias recombination current, which is at a relatively high level due to the presence of photogenerated charge carriers. Consequently, the changing temperature has a limited effect. At high forward bias, the R_j of the TCAD-simulated device is primarily influenced by the diffusion of minority carriers. Here, the higher temperature leads to enhanced diffusion, and in turn, a lower R_j. In Figure 4.5(b), it can be seen that for low bias voltages, temperature has little effect on C_j. This is according to expectation,

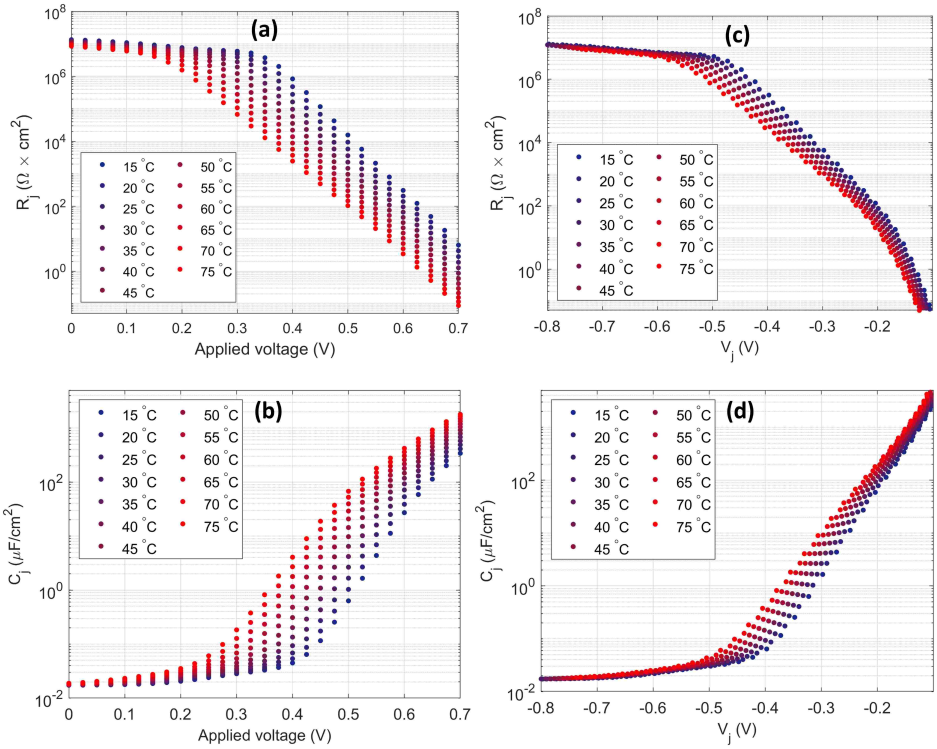


Figure 4.5: Effect of temperature on R_j and C_j, as extracted from TCAD-generated impedance data of a TOPCon solar cell.The temperature is varied between 15 °C and 75 °C in steps of 5 °C. (a) shows R_j and (b) shows C_j, both obtained through CNLS analysis and plotted as functions of applied forward bias voltage. Additionally, the same R_j and C_j values are presented as functions of V_j in (c) and (d). The bulk dopant concentration of the solar cell is N_{sub}=3.2 × 10^{15} cm^{-3} and the impedance data is simulated under an irradiance of 0.5 sun.

since the depletion capacitance dominates C_j in this regime. Conversely, in forward bias, a higher temperature clearly leads to a higher C_j at a given applied voltage. This is attributed to the enhanced diffusion capacitance. The TCAD results from Figure 4.5(a) and Figure 4.5(b) align with the experimental results shown in Figure B.3 of Appendix B.2, confirming these observations.

Additionally, when comparing Figure 4.5(a) and Figure 4.5(b) to Figure 4.5(c) and Figure 4.5(d), there are some subtle changes in the trends of R_j and C_j. Notably, the extent to which the temperature affects R_j and C_j for a fixed V_j value is somewhat less pronounced than for a fixed applied voltage. This indicates that part of the temperature effect observed in Figure 4.5(a) and Figure 4.5(b) is due to the narrowing of the depletion region width at higher temperatures. Moreover, when R_j and C_j are plotted as a function of V_j, it becomes apparent that the slopes become less steep as the temperature increases. This observation is consistent with theoretical expectations [114].

4.4.3. Impedance variations during MPPT

Now that the effects of illumination and temperature on the PN junction impedance have been thoroughly discussed, our focus shifts to impedance variations during practical operation. Here, one important factor must be included: the operating voltage is not constant. Fluctuations in irradiance and temperature affect the current-voltage ($I-V$) relationship. Thus, in practical PV systems, the maximum power point tracker (MPPT) continually adjusts the DC operating voltage to generate the maximum power. When irradiance increases, the maximum power point voltage (V_{mpp}) of the solar cell will increase as well. Thus, although the direct effect of illumination on the C_j-V relationship is limited, an increase in irradiance in real-world conditions will increase the operating voltage, in turn leading to a decreased R_j and an increased C_j. When it comes to temperature, the dynamics are different. As discussed in section 4.4.2, a rising temperature will decrease R_j and increase C_j at a given voltage. However, an increase in temperature is known to lower the V_{mpp}. In turn, the lower operating voltage leads to a counterbalancing increase in R_j and decrease in C_j. In this section, the combined effects of the factors discussed above on the impedance variations are quantified.

First, the TCAD approach is used to study the variations in operating impedance of the TOPCon solar cell. For this experiment, the irradiance was varied between 0.1 sun and 1.2 suns, in steps of 0.1 sun. For each of these illumination intensities, the temperature was varied between 15 °C and 75 °C in steps of 5 °C. For each irradiance-temperature combination, the $I-V$ curve is simulated and the V_{mpp} is determined. Subsequently, the impedance data is generated in each condition for a DC bias voltage equal to the V_{mpp}. Finally, the R_j and C_j values are obtained through CNLS analysis and are presented in Figure 4.6. This is done for substrate dopant densities of 1×10^{14} cm^{-3}, 1×10^{15} cm^{-3}, and 1×10^{16} cm^{-3}.

The results in Figure 4.6 show a consistent trend for all the different dopant concentration values: variations in irradiance strongly affect the maximum power point (MPP) value of both R_j and C_j, whereas the effect of temperature is limited. This outcome highlights the important role that MPPT plays in determining the operating impedance of solar cells. Whereas it was previously found that temperature has a stronger impact on the R_j-V and C_j-V relationships than illumination, the values of R_j and C_j during MPPT are more strongly affected by illumination. When the temperature increases, the reduction of the V_{mpp} approximately cancels out the enhanced diffusion effect, resulting in rather stable values of R_j and C_j. Looking at R_j specifically, the minimum and maximum MPP R_j values vary approximately between 12.9-14.4 $\Omega \times$ cm^2 (1.2 suns, 75 °C) and 149-156 $\Omega \times$ cm^2 (0.1 sun, 15 °C). Thus, the ranges that can be expected during practical operation are fairly similar for different bulk dopant concentrations. Shifting focus to C_j, its minimum and maximum areal MPP values show higher variability when the bulk dopant concentration is changed. For $N_{\text{sub}} = 1 \times 10^{16}$ cm^{-3}, the minimum and maximum MPP C_j values vary between 13.5 μF/cm^2 (0.1 sun, 15 °C) and 118 μF/cm^2 (1.2 suns, 75 °C). For $N_{\text{sub}} = 1 \times 10^{14}$ cm^{-3}, the variation is between 89.0 μF/cm^2 and 245 μF/cm^2. This difference confirms the important role of N_{sub} for the PN junction capacitance of solar cells. However, the MPP C_j range of $N_{\text{sub}} = 1 \times 10^{14}$ cm^{-3} and $N_{\text{sub}} = 1 \times 10^{15}$ cm^{-3} are fairly similar. This suggests that some stabilization can occur in the MPP C_j towards low dopant concentrations below 1×10^{15} cm^{-3}.

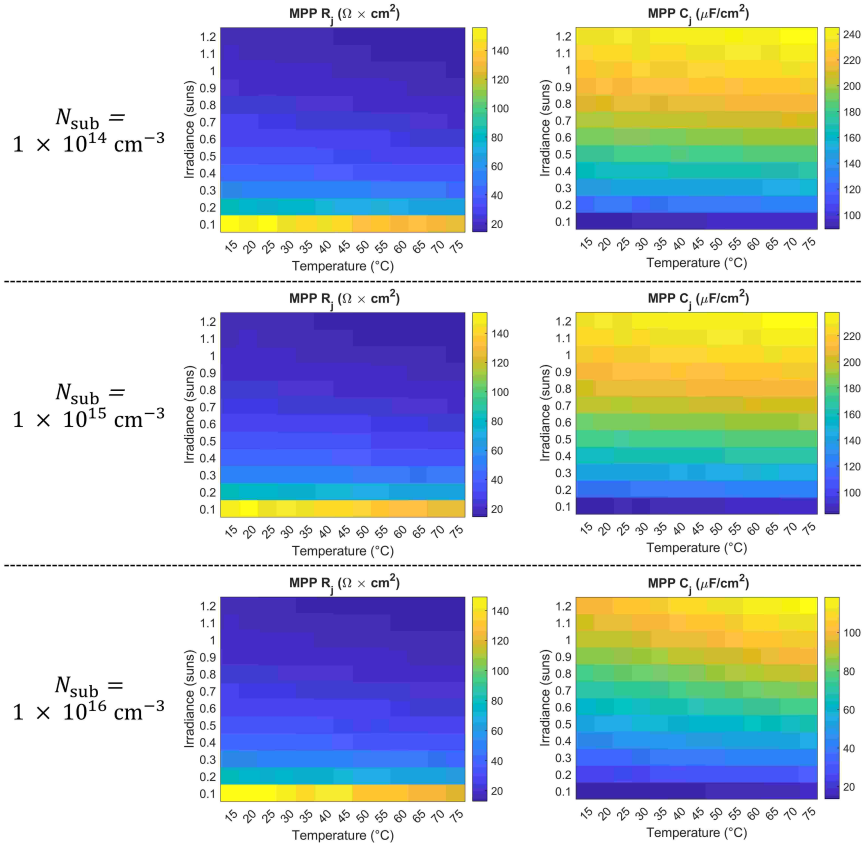


Figure 4.6: Variation of R_j and C_j across varied irradiance and temperature conditions, with the DC bias voltage adjusted to the V_{mpp} corresponding to each condition. The values are obtained through CNLS fitting of TCAD-generated impedance data of TOPCon solar cells with different bulk dopant concentrations (N_{sub}).

A similar analysis was conducted experimentally using the impedance spectroscopy setup. In this case, the IBC and PERC solar cell laminates were subjected to irradiance conditions between 0.1 sun and 0.5 sun in steps of 0.1 sun, whereas the temperature of the laminates was varied between 30 °C and 60 °C in steps of 10 °C. The resulting CNLS-fitted R_j and C_j values at MPP are presented in Figure 4.7. The experimental results from Figure 4.7 mostly confirm the observed trends from the TCAD simulations. Here too, the irradiance has stronger impact on the MPP impedance than the temperature. Notably, the experimentally observed MPP R_j ranges of the IBC and PERC laminates are highly similar to each other, as well as to that of the TCAD-simulated TOPCon device. Specifically, the MPP R_j values of the IBC cell vary between 27.8 Ω × cm^2 and 157 Ω × cm^2, whereas those of the PERC cell vary between 27.1 Ω × cm^2 and 153 Ω × cm^2. This suggests that the slope of the IV-curve at V_{mpp} depends significantly more on the irradiance than on the cell architecture. Conversely, the experimental results show that the MPP C_j range can be highly variable for different solar cells. As mentioned in the

introduction, the MPP C_j ranges of these PERC and IBC laminates are expected to be around the lower and upper limits that can be anticipated from modern commercial c-Si solar cells, respectively. Specifically, the MPP C_j values of the IBC cell vary between 20.2 μF/cm^2 and 61.6 μF/cm^2, whereas those of the PERC cell vary between 0.283 and 1.98 μF/cm^2. Remarkably, the minimum MPP C_j value of the IBC cell is a factor ~10.2 higher than the maximum value of the PERC cell. Additionally, the maximum MPP C_j value of the IBC cell is a factor ~218 higher than the minimum value of the PERC cell.

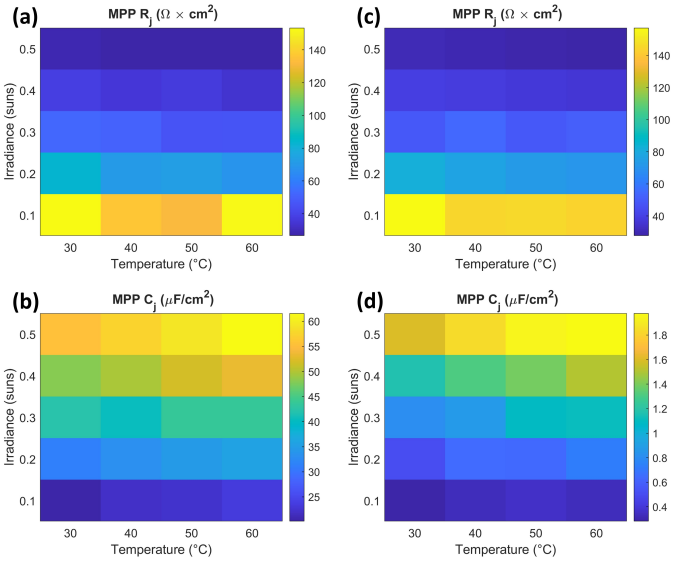


Figure 4.7: Variation of R_j and C_j across varied irradiance and temperature conditions, with the DC bias voltage adjusted to the V_{mpp} corresponding to each condition. The values are obtained through CNLS fitting of experimentally recorded impedance data for the (a-b) IBC and (c-d) PERC solar cell laminates.

4.5. Conclusion

Various publications have emerged where the impedance of solar cells is exploited to realize innovative applications. However, for the continued advancement of such applications, it is crucial to understand how the impedance of modern solar cells varies during operation. In this chapter it was shown how the PN junction impedance of modern solar cells varies across different bias voltages and under varying illumination and temperature conditions.

For a given solar cell bias voltage, variations in temperature have a notably stronger impact on the PN junction impedance than changes in irradiance. Considering that the impedance of a PN junction can be represented by a parallel resistor-capacitor (R_j-C_j) circuit, higher temperatures enhance the diffusion of minority carriers, thereby reducing R_j and increasing C_j at a given voltage, especially under high forward bias. However, during maximum power point (MPP) tracking, variations in irradiance have a greater impact on the PN junction impedance than temperature variations. This is related to

the fact that increased irradiance intensity raises the MPP voltage. In contrast, when the temperature is varied, the change in the diffusion process is approximately compensated by a changing MPP voltage. In the tested conditions, the range in which the MPP R_j varies was similar for different cell architectures, despite their different properties. Specifically, the MPP R_j values of the IBC cell vary between 27.8 $\Omega \times cm^2$ and 157 $\Omega \times cm^2$, whereas those of the PERC cell vary between 27.1 $\Omega \times cm^2$ and 153 $\Omega \times cm^2$. A similar range was observed for the TCAD-simulated TOPCon devices. Conversely, the range in which the MPP C_j varies is significantly affected by the substrate dopant concentration (N_{sub}) and maximum power point voltage. For the performed experiment under irradiance levels between 0.1 sun and 0.5 sun and operating temperature between 30 °C and 60 °C, the areal MPP C_j values of the IBC cell with N_{sub} = 1.0 × 10^{14} cm^{-3} varied between 20.2 $\mu F/cm^2$ and 61.6 $\mu F/cm^2$, whereas those of the PERC cell with N_{sub} = 8.0 × 10^{15} cm^{-3}varied between 0.283 and 1.98 $\mu F/cm^2$. Moreover, TCAD simulations of a performance-limit TOPCon cell with N_{sub} = 1.0 × 10^{14} cm^{-3}, where the irradiance level was varied between 0.1 sun and 1.2 suns and the operating temperature between 15 °C and 75 °C, show that the areal MPP C_j can increase to a range between 89.0 $\mu F/cm^2$ and 245 $\mu F/cm^2$. The findings in this chapter are relevant for applications such as the design of MPPT circuits, visible light communication, and leveraging solar cell self-capacitance for voltage balancing in converters or power balancing among cells.

II

Integration of power electronics

5

Exploring the feasibility of different integration concepts

This chapter is based on the following publication:

D. A. van Nijen, P. Manganiello, M. Zeman, and O. Isabella, "Exploring the benefits, challenges, and feasibility of integrating power electronics into c-Si solar cells" in *Cell Reports Physical Science*, vol. 3, 100944, 2022.

5.1. Introduction

The integration of power electronics (PE) into crystalline silicon (c-Si) solar cells includes a wide range of possibilities. This chapter describes the feasibility of various integration concepts, encompassing both an overview of existing research and lesser-explored approaches. It is important to distinguish between two different methods of integration. Firstly, when it comes to passive components like capacitors and inductors, a possibility is aim at leveraging the capacitive and inductive effects that solar cells inherently exhibit. In such instances, where the cell's design remains unaltered, the feasibility primarily revolves around technical considerations, with no associated increase in production costs. In this chapter it is mainly investigated to which extent these passive solar cell properties can be exploited at the input of power converters. Secondly, integration may entail adding PE components to the c-Si solar cells. Here, the feasibility depends on how the PE components can be designed to achieve the desired properties. It is important to assess not only technical feasibility but also keep in mind the economic viability of these concepts, as modifications to cell design can incur additional costs compared to conventional production methods. The feasibility analysis regarding this second method includes the viability of integrating diodes, transistors, capacitors, and inductors, since they are the basic power electronic components relevant to PV modules.

When exploring the integration of PE components into c-Si solar cells, one of the most important factors that need to be considered is the *ease of integration*, which can be captured in two main points. Firstly, to create a c-Si solar cell with integrated power

electronic components, it may be necessary to adjust the fabrication processes used for regular cells. As the standard fabrication processes are thoroughly optimized to make high-efficiency cells, the changes must have as limited an impact as possible on the performance of the solar cell device itself. The processing steps needed to integrate the power electronics should not harm the solar cell and vice versa. For example, plasma etching is often used for transistor fabrication, since it allows for high-resolution pattern transfer to the underlying layer with less undercutting than for wet etching steps [168]. However, plasma etching steps can be detrimental to the passivation of a solar cell [169]. Thus, the first factor determining the ease of integration of a power electronic component into a solar cell is the extent to which the fabrication process is compatible with the manufacturing process of a solar cell. Secondly, the integrated power electronic components may compete with the PV cell area used for the collection of charge carriers. For example, this is the case for integrated semiconductor devices like diodes and transistors, which should thus occupy as little area as possible to maintain a high PV conversion efficiency. When these PE components are fabricated in industry, the maximum number of devices that fit on the wafer is processed simultaneously. This scalable nature of the process facilitates cheap manufacturing [170]. However, in the integrated approach, we postulate that these devices should only occupy a relatively small wafer area. Thus, for this approach to become cost-effective compared to discrete power electronics from industry, it is crucial that only a limited amount of additional processing steps are introduced compared to standard solar cell manufacturing. Combining some of the processing steps required for the fabrication of power electronics components with similar processing steps that are already used for the fabrication of the solar cell would be the smartest way to reduce the total processing time and cost. Several examples of designs where fabrication steps can be combined will be given later in this section. Thus, the second factor determining the ease of integration of a power electronic component into a solar cell is the extent to which its fabrication steps can be combined with fabrication steps that are already used to create PV cells.

Furthermore, it should be mentioned that the optimal design of integrated power electronic components depends on the PV cell structure that is considered. Thus, it is important to distinguish between front-back contacted (FBC) and interdigitated-back-contacted (IBC) PV cells. Both types of structures are presented in Figure 5.1. Whereas the contacts responsible for collecting charge carriers are located on opposite sides of the wafer in FBC designs, all contacts are located on the back of the cell in IBC designs [1]. The different power electronic components that are considered for integration can also have either vertical (contacts on opposite sides of the wafer) or lateral structures (contacts on the same side of the wafer). As a result, there are many design options available for the integration of power electronics into PV cells. In this chapter, we consider lateral and vertical power electronic components as well as FBC and IBC PV cell structures. Finally, it is worth noting that in the case of bifacial cell designs, additional optimization is required for some of the proposed concepts.

The *ease of integration* is an important factor determining the costs that are involved in integrating PE compared to regular cell production. Whether the different concepts are cost-competitive depends on the application. For instance, in the case of shade-resilient modules, the incremental costs for adding PE should be compensated by the

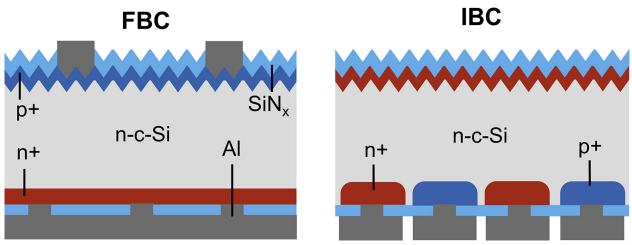


Figure 5.1: Front-back contacted (FBC, left) and interdigitated back contacted (IBC, right) PV cell structures. The legend of colors applies to all the figures in this chapter.

additional energy that is generated due to the increased shade resilience of PV modules. At this stage, quantifying the capital expenditures (CAPEX) of cell-integrated PE is challenging. The various concepts that are described in this dissertation do not necessarily need to be applied simultaneously on the same cell. Moreover, when several cells are combined in a module, it may be possible that only a part of them contain integrated PE. Consequently, costs vary depending on the specific integration concepts and module topologies employed. Nevertheless, for PV module designs incorporating either a reconfiguration strategy or sub-module DC-DC power optimizers with PE implemented in the junction box, cost-benefit analyses have demonstrated profitability in regions with frequent partial shading [59, 65]. Furthermore, it is important to mention that the market adoption of solar-cell-integrated PE components is influenced by more than just economic factors. For instance, the added value of integrating PE into c-Si solar cells can also lie in reduced volume and weight, or customizability.

5.2. Feasibility

5.2.1. Diodes

Standard c-Si based PV module designs include several bypass diodes in the junction box. There are two main types of diodes being used nowadays, which are the pn junction diode and the Schottky barrier diode. Both devices can be fabricated in lateral and vertical designs, as presented in the example structures in Figure 5.2. Note that the n-c-Si region in the figures is a lowly doped drift region that is present to increase the reverse breakdown voltage. In low-power diodes which do not require a large blocking voltage capability, such a drift region is not required [29].

Since diodes consist of metal-semiconductor contacts and pn-junctions, there are some clear similarities with various c-Si solar cell designs. These similarities were already noticed by Green et al. in 1981, who reported the development of solar cells with integrated bypass diodes [74]. When these devices were used in a PV module prototype, improved shade resilience was demonstrated [171]. A few decades later in 2012, a new study about a PV module with cell-integrated bypass diodes was published [75]. In this work, the leakage currents of the diode in reverse bias conditions were reduced by isolating the device from the solar cell substrate by laser isolation.

In all the studies that were just mentioned, a pn junction diode with a vertical structure was integrated into an FBC solar cell. Indeed, if we compare the vertical diode struc-

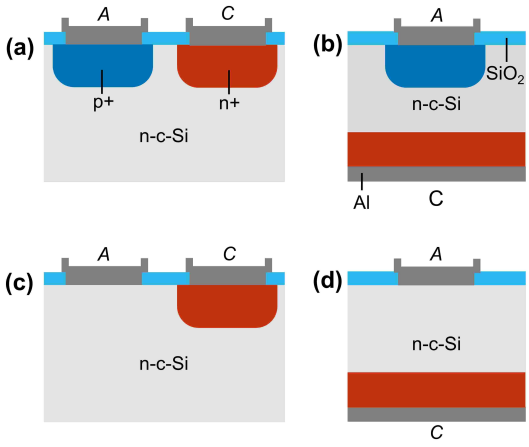


Figure 5.2: Basic diode structures of: (a) Lateral pn junction diode. The anode and cathode are represented by *A* and *C*, respectively. (b) Vertical pn junction diode. (c) Lateral Schottky barrier diode. (d) Vertical Schottky barrier diode.

ture of Figure 5.2(b) with the FBC solar cell structure of Figure 5.1, the clear similarities between the two allow for high ease of integration. However, there are some inherent drawbacks to this approach, which can be explained by reviewing some theory about breakdown in pn junctions. The breakdown voltage of a pn junction is the reverse-biased voltage at which the current rapidly increases. Two mechanisms that can cause breakdown in pn junctions are the Zener effect and the avalanche effect [114]. Zener breakdown occurs in highly doped pn junctions through a tunneling mechanism. Avalanche breakdown occurs when charge carriers moving across the space charge region acquire sufficient energy from the electric field to create new electron-hole pairs by colliding with atomic electrons within the depletion region. In diodes, the breakdown voltage due to Zener and avalanche effects can be increased by lowering the doping concentration of the lowly doped drift region [168]. However, lowering this doping concentration implies that the depletion region of the pn junction extends further into the lowly doped region. This can induce a third breakdown mechanism, called punch-through breakdown, where the depletion region extends all the way across the drift region under influence of a reverse-bias voltage [114]. The lowest diode on-resistance per unit area of the wafer can be achieved when the drift region length is minimized while still preventing punch-through breakdown. Thus, for diodes fabricated in industry, the doping concentration and length of the drift region are carefully optimized to minimize the on-resistance of the device while achieving the desired blocking voltage capability [29]. Considering the above, it becomes clear that the major drawback of integrating a vertical pn junction diode into an FBC solar cell is that there is little flexibility to tune the length and doping concentration of the drift region. Most solar cells produced in the photovoltaic industry nowadays are based on gallium-doped p-type wafers or phosphorus-doped n-type wafers with a thickness of around 100-150 μm [11]. At the pn junction doping levels that are typically used in c-Si PV cells, a combination of Zener and avalanche effects is typically causing breakdown [172–174]. Depending on the illumination conditions and

temperature, the breakdown voltage of pn junctions in c-Si PV cells was reported in the range of 10-25 V. However, as the PV wafer thickness is usually 100 μm or higher, the drift region length of a vertically integrated diode is unnecessarily long with respect to such blocking voltages [29]. As a result, the on-resistance per unit area of the wafer of a vertically integrated diode is sub-optimal. Despite this drawback, the on-resistance of vertical diodes can be lowered by increasing the cross-sectional area of the diode. This way, the dissipation losses can be reduced, which ensures that the diode temperature does not rise dangerously above that of the rest of the cell [175]. However, as already explained earlier, it is crucial for integrated power electronics that their surface area is as limited as possible to maintain a high PV conversion efficiency. In the I-V curves of the vertically integrated bypass diode in [75], it can indeed be seen that the trade-off between a low diode on-resistance and a high PV conversion efficiency resulted in a device with a larger on-resistance than is achieved for state-of-the-art bypass diodes. Thus, to make vertically integrated diodes a success, further research to adequately handle this trade-off is required. Furthermore, if we consider the role that vertically integrated pn junction diodes can play on a system-level, we have to take into account that blocking voltages in the range of 10-25 V can be expected. Although the devices would thus not be able to block the voltage of 60 cells, they could play a role in PV module designs with a high bypass diode granularity.

An alternative method, that has not been reported thus far, would be to integrate a pn junction diode with a lateral structure into a c-Si solar cell. As the lateral design has highly doped p^+ and n^+ regions on the same side of the wafer, the ease of integration might be higher for IBC than for FBC PV cell structures. An important advantage of the lateral diode design is that the length of the drift region can be controlled. Thus, the bias voltage at which avalanche or Zener effects cause junction breakdown can be chosen as the aimed breakdown voltage of the device, and the drift region length can be adjusted accordingly to prevent punch-through effects. However, a drawback of these lateral structures is that the width of the device needs to be large enough to accommodate for a sufficiently low on-resistance in forward bias. As the resistive effects in the metal contacts start to play a role in devices with a large width [176], designs where separate diodes are connected in parallel might be most efficient. Furthermore, also for integrated lateral diode designs, the total area of the device must be as limited as possible.

Most arguments that are thus far made for vertical and lateral pn junction diode structure are also true for Schottky diodes. However, Schottky barrier diodes can offer some important advantages over pn junction diodes. Most notably, the on-state voltage drop over the Schottky diode is lower and it has faster switching capabilities due to it being a unipolar device [114]. Whereas a low Schottky barrier height facilitates a low on-state voltage drop, a minimum barrier height is necessary to achieve sufficient blocking voltage capability and suppress leakage currents in reverse bias. Schottky power devices are typically designed with a barrier height of around 0.7 eV [177]. To achieve a sufficiently high Schottky barrier for n-type silicon, high work function metals such as Cr, W, Mo, and Pt are typically deployed. These materials are rarely used as metal contacts of solar cells, which poses a challenge to the ease of integration. When considering metals that are more commonly used in PV cells, such as Al and Ag, these are known to result

in relatively low Schottky barrier heights below 0.6 eV for both n-type and p-type wafers [178]. However, in the case of Al/p-Si, it has been shown that the diode performance can be improved if the metal deposition is preceded by a certain wet etching, dry etching, or implantation step. Using these fabrication methods has resulted in devices with a Schottky barrier height between 0.75 eV - 0.83 eV and good ideality factors between 1.05-1.25 [179–181]. As such, integration of Al/p-Si Schottky diodes into p-type PV cells could result in well-performing devices with high ease of integration.

5.2.2. Transistors

Optimal operation of PV is not possible without transistors. These devices are necessary for power optimizers and inverters that are already commonly used in PV systems nowadays. In this article, we argue that power conversion at sub-module or even cell level can be facilitated by including transistors into c-Si solar cells. When it comes to power converters, high switching frequencies are considered beneficial since they allow for smaller passive components [182]. Therefore, solar-cell-integrated transistors should ideally be able to switch at high frequencies when they are part of a submodule power converter. Another application of cell-integrated transistors is to facilitate the reconfigurable module concept. A straightforward design of reconfigurable modules is to implement the so-called reconfiguration matrix on a printed circuit board, that is installed into the junction box. However, the potential benefits of solar cell-integrated transistors to support reconfigurable module concepts have already been mentioned in previous research [183, 184]. The transistors used in reconfigurable modules must either conduct or divert the current generated by (groups of) PV cells, but they do not work at a high switching frequency. Therefore, compared to the transistors used in power converters, it is more crucial to reduce on-resistance to limit conduction losses than to focus on high-speed designs.

First, it must be noted that for the fabrication of transistors, photolithographic patterning steps are used [168]. Although photolithography is known to work well in supporting high-efficiency PV cell concepts such as IBC designs, it is a relatively costly process that the photovoltaic industry is trying to move away from [185–187]. As such, the need for lithography poses a challenge to the cost-effectiveness of transistor integration into PV cells. However, as was explained earlier, combining fabrication steps can increase the cost-effectiveness of processing steps, which is also true for lithographic steps. For example, it is interesting to highlight the option of integrating transistors with lateral structures onto IBC solar cells. As this allows all contacts to be located on the backside of the PV cell, monolithic integration between the components and the cell contacts can be achieved. As was explained earlier, monolithic integration of power electronics can have a positive effect on the reliability of power converters.

Furthermore, it is worth mentioning that the worldwide market share of c-Si PV cell technology has shifted from predominantly multi-c-Si to mono-c-Si material, the latter now having an 84% market share of total c-Si production [188]. Since mono-c-Si is more suitable for the fabrication of high-quality semiconductor devices than multi-c-Si [189], this recent market trend can make the integration of transistors into c-Si PV cells more viable. However, it must be noted that transistors should preferably be fabricated on flat wafer surfaces, instead of the pyramidal surface texture used in solar cells. Although the

processing of industrial FBC cells typically starts with creating a double-sided texture on both sides of the wafer, for most cell types the rear side of the wafer is flattened by a subsequent etching step [146]. Since single-side wafer texturing does not prohibit subsequent photolithographic steps [190], the texturing process does not prohibit transistor integration. Furthermore, in the case of IBC cell fabrication, the rear side of the wafer is often flat throughout the full process and the front side texturing takes place towards the end of the process [190–192].

Another factor that must be considered is the compatibility in thermal budget between transistors and PV cells. In the case of solar cells, the thermal budgets vary for different cell designs [146]. However, there is only a limited thermal budget available for the fabrication of transistors [193]. Although combined designs could be achieved by performing part of the process flows consecutively instead of simultaneously, this approach poses a challenge to the cost-effectiveness. Thus, to be able to combine as much of the process flows as possible, similar thermal budgets for the different devices are beneficial. As such, depending on the transistor design, a low thermal budget silicon heterojunction process could be preferred over PV cell processes with higher thermal budgets.

Finally, in industry, transistors are typically fabricated into layers that are epitaxially grown on semiconductor substrates. By accurately controlling the desired doping profile through the growth of an epitaxial layer, the desired transistor properties can be achieved [168]. However, preceding the transistor integration by the growth of an epitaxial layer would pose a challenge to the cost-effectiveness and ease of integration [194]. Thus, it could be more favourable to integrate the device directly into the bulk of the c-Si solar cell wafer. On the other hand, this approach would leave less flexibility to control the doping profile of the substrate. The substrate doping concentration influences important properties of the transistors, such as the breakdown voltage [114]. Furthermore, the doping concentration across the wafer might be too heterogeneous for reproducible transistor fabrication. P-doped wafers have the advantage that boron or gallium doping is typically more homogeneously distributed across the wafer than phosphorus doping in n-type wafers [1, 195]. Thus, the potential to leave out the epitaxial layer from the fabrication process might be higher for p-type than for n-type wafers.

When considering transistor integration into a c-Si solar cell, a wide range of devices can be considered. In this work, we will limit ourselves to the most used ones, which are bipolar junction transistors (BJTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs). The insulated-gate bipolar transistor (IGBTs) is out of the scope of this article, as this device would be relatively complex to integrate into a solar cell and is typically designed for a higher blocking voltage capability than what is necessary for sub-module PV applications. When comparing the BJT and MOSFET, the latter is usually the preferred type of device for high-frequency switching applications in the range from a few watts to a few kilowatts due to its fast switching characteristics [196]. On the other hand, both BJTs and MOSFETs are suitable to serve as switches in reconfigurable modules, where fast switching characteristics are less crucial.

When comparing the ease of integration of these two types of transistors into a c-Si solar cell, each has its advantages and drawbacks. In Figures 5.3(a) and 5.3(b), the standard structures of the BJT and the MOSFET, respectively, are presented. For the BJT,

a double-diffused structure is present beneath the emitter and the base contacts. Such a double-diffused structure is usually not present in c-Si solar cells, which implies that integration of a BJT into a solar cell would necessarily require additional processing steps to create this structure. On the other hand, the source and drain in the MOSFET structure as presented in Figure 5.3(b) can be fabricated in one single implantation step. As an implantation step with a similar dose and implantation energy is typically used to form the source and drain of a MOSFET and carrier-selective contacts of a solar cell [168, 191], this step can potentially be combined. However, the main challenge for the integration of a MOSFET into a solar cell is the fabrication of the gate oxide, which has the purpose to isolate the substrate from the gate contact. To create the gate oxide, a high-quality SiO_2 layer up to a thickness of 10's of nm is typically grown using thermal oxidation [114]. As such, integration of the MOSFET structure as presented in Figure 5.3(b) would require additional processing steps to fabricate a gate oxide. There are a few publications in which the integration of MOSFETs and thin-film capacitors with front-back contacted PV cells is investigated [76, 197, 198]. Although they made some innovative steps towards cell-embedded PE, the PV cell structure has some intrinsic limitations to reaching a high efficiency, which are for instance the non-textured front side and an aluminium plate covering the full back-side of the device.

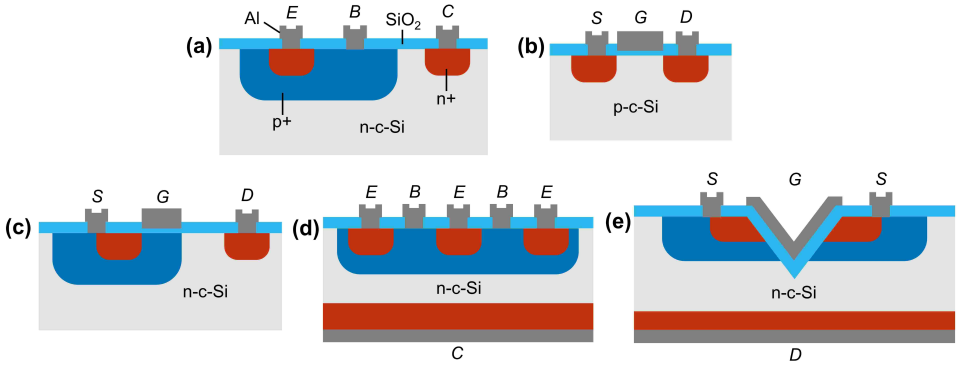


Figure 5.3: Basic transistor structures: (a) Bipolar junction transistor (BJT) structure. The emitter, base, and collector are represented by E, B, and C, respectively. (b) Metal-oxide-semiconductor field-effect transistor (MOSFET) structure. The source, gate, and drain are represented by S, G, and D, respectively. (c) Lateral double-diffused metal-oxide-semiconductor (LDMOS) structure. (d) Power BJT structure. (e) V-groove double-diffused metal-oxide-semiconductor (VDMOS) structure.

A transistor must be designed such that it is capable of handling the desired voltage and current. To achieve the desired blocking voltage, the design considerations are similar to those of the diode. Thus, the substrate doping concentration can be lowered to prevent avalanche and Zener effects, while punch-through effects can be avoided by giving the depletion regions sufficient space to extend. In the BJT, this implies that the width of the base region needs to be sufficiently large. However, a relatively large base width is known to cause a smaller current gain, thus increasing the losses in the device [114]. In the MOSFET, a similar trade-off is present. The source-drain spacing needs to be increased to prevent punch-through effects [170], but for the regular MOSFET de-

sign, this implies that the channel length increases. This is unfavourable, as the channel length should be as short as possible to minimize the on-resistance and to maximize the switching speed [114, 199]. An additional downside of the regular MOSFET design is that the voltage at which avalanche breakdown effects occur is known to decrease if the gate overlaps with the drain region [200]. Thus, the MOSFET design from Figure 5.3(b) is generally not considered to be well suited for power applications [201].

There exists an alternative lateral MOSFET design that is more suitable for power applications, often called the lateral double-diffused MOS transistor (LDMOS), as presented in Figure 5.3(c) [202]. It is worth noting that such lateral power MOSFETs are mainly used in power integrated circuits, but are rarely used as discrete devices [170]. In the LDMOS design in Figure 5.3(c), the gate oxide no longer covers the full distance between the source and drain. This means that enlarging the source-drain spacing to prevent punch-through effects does no longer imply that the channel length increases as well. Thus, if blocking voltages are required where the standard MOSFET structure would need a relatively large channel length, the LDMOS structure can be used instead to achieve a smaller on-resistance and higher switching speed. Furthermore, in the LDMOS design, the gate plate does not overlap with the drain region, hereby mitigating the enhanced avalanche effect mentioned earlier [200]. Although the LDMOS design has some clear advantages over the regular MOSFET design for power applications, the ease of integration into a solar cell is challenging. The LDMOS design combines the difficulties that were mentioned earlier for integration of the BJT (double-diffused structures) and the MOSFET (gate oxide fabrication).

Neither of the previously mentioned lateral transistor structures is commonly used in industry for the fabrication of discrete power devices [170]. Examples of power transistors preferred in industry are presented in Figures 5.3(d) and 5.3(e). Both these structures consist of vertical designs, which dominate the market of power transistors. The main motivation to use these vertical structures is that lateral structures for power devices typically take up more surface area of the silicon as the required blocking voltage capability increases. Since this is not the case for vertical designs, a higher packing density of transistors on a wafer can be achieved [170]. Furthermore, in vertical devices, the desired current carrying capability can be achieved by using a sufficiently large cross-sectional area of the wafer. As such, the cross-sectional area through which current is flowing through the device is maximized [114]. Although vertical structures are preferred in industry for the fabrication of power transistors, these structures are less suitable for solar cell integration. Compared to the more simple structures from Figures 5.3(a) and 5.3(b), numerous additional processing steps are required for the fabrication. Another drawback of these vertical transistor structures is that monolithic integration of these devices with other components in the IBC solar cell would be a challenge, as the contacts are located on opposite sides of the wafer. Integration of vertical power transistors into ICs is also known to be a challenge [203]. Furthermore, as was presented earlier in the section on diodes, the breakdown voltages of pn junctions in solar cells typically lie in the range between 10 V and 25 V. If the bulk region of the PV wafer serves as the drift region, similar breakdown voltages can be expected for a vertically integrated MOSFET. As was the case for the integration of a vertical diode, the drift region would in this case be unnecessarily long with respect to these blocking voltages.

Having reviewed the design adaptations that are typically deployed in industry to make the transistors more suitable for power applications, we found that these adaptations are less favourable for transistor integration into a solar cell. Thus, it is worth considering what roles the standard designs from Figures 5.3(a) and 5.3(b) might play when they are integrated into a solar cell. If the device were directly integrated into the bulk of the wafer, the drain-source breakdown voltage that can be achieved would be similar to the case of the integrated diode (10-25 V). Assuming that the V_{oc} value of typical c-Si solar cells lies in the range of 0.5-0.75 V, the most simple transistor structures from Figures 5.3(a) and 5.3(b) would be perfectly capable of blocking the voltage of a single cell or several series-connected cells [204]. Thus, these cell-integrated transistors are not limited by their blocking voltage capability to play a role in sub-module power conversion. However, the main challenge for the lateral MOSFET structures might be to design them such that they have sufficient current carrying capability. For solar cells that are typically used in industrial PV modules, the I_{mpp} typically lies in the range of 5-10A at STC conditions [205]. To enable such current levels in the transistor structures from Figures 5.3(a) and 5.3(b), the device width should be orders of magnitude higher than their counterparts used in integrated circuits. Designs with large widths are not straightforward to make, as the power dissipation in the metal fingers and interconnections become more dominant, also referred to as the *scaling issue* [176]. To this end, a similar design to the one that is used in the LDMOS design in [202] could be adapted to increase the current carrying capability. Here, several devices are effectively connected in parallel while sharing a common gate. Furthermore, an additional challenge for MOSFET structures with a large width is that the switching speed becomes lower due to the switching process not occurring uniformly over the whole device [206].

5.2.3. Capacitors

A capacitor is a device that stores electrical energy by accumulating electric charge on two conductors separated by an insulator. Typically, capacitors consists of two electrical conductors separated by a dielectric medium. For a parallel-plate capacitor, the capacitance is given by:

$$C = \frac{\epsilon_0 \epsilon_r A}{d} \tag{5.1}$$

where $\epsilon_0 = 8.854 \cdot 10^{-14}$ F/cm is the permittivity of vacuum, ϵ_r (≥ 1) is the relative permittivity of the dielectric, A the area of the plates, and d the distance between the plates. To realize a high capacitance per unit area, the dielectric layer thickness d should be as small as possible. On the other hand, a minimum thickness d is necessary to avoid dielectric breakdown [114]. For example, a commonly used insulator such as thermally grown SiO_2 has a dielectric strength of 10 MV/cm [168]. Therefore, such a layer requires a thickness of at least 10 nm to prevent dielectric breakdown at a voltage of 10 V between the plates. In the remainder of this section, several possibilities to integrate a capacitor in c-Si solar cells are explored.

First, we consider the possibility to exploit the capacitive behaviour that solar cells naturally exhibit. Taking the depletion capacitance and the diffusion capacitance of c-Si solar cells into account, the two diode equivalent model can be expanded with the self-capacitance, as presented in Figure 5.4(a). It should be noted that the total capacitance

of a string of series-connected cells scales inversely with the number of cells, which implies that the capacitive effects that can be observed at a module level are smaller than at cell level.

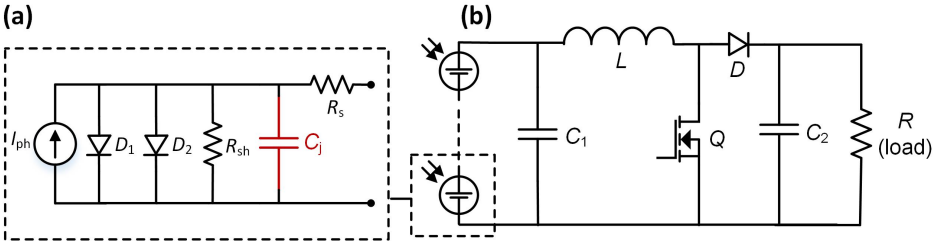


Figure 5.4: (a) Equivalent solar cell circuit with a current source, two diodes (D_1 and D_2), a shunt resistance (R_{sh}), and a series resistance (R_s). Moreover, the circuit is expanded with the PN junction capacitance (C_j). (b) Example circuit of a DC-DC boost converter with a string of series-connected solar cells at the input. The capacitors, inductor, MOSFET, diode, and resistor are represented by C, L, Q, D, and R, respectively.

In different types of power converters, such as the DC-DC boost converter shown in Figure 5.4(b), an input capacitor C_1 is used to reduce the ripple voltage at the input of the converter [92]. If such a converter were used in a PV module at cell or sub-module level, the self-capacitance of the solar cells could potentially fulfil the function of this input capacitor. The main advantage of exploiting the self-capacitance in this manner is that it removes the need to add a physical input capacitor to the power converter. However, a challenge to tackle would be that in this application the capacitance of the input capacitor depends on the operating conditions of the solar cell. Furthermore, it is important to comment on whether the self-capacitance of PV cells is large enough to fulfil the function of an input capacitor and keep the voltage ripple sufficiently low. When Equations (12) and (21) from [92] are combined, the minimum required input capacitance of a DC-DC boost converter for MPPT application can be approximated by:

$$C = \frac{I_{mpp}\gamma_{I_L}}{8V_{mpp}\gamma_{V_{mpp}}f} \tag{5.2}$$

where I_{mpp} is the maximum power point current, γ_{I_L} the inductor current ripple factor, V_{mpp} the maximum power point voltage, $\gamma_{V_{mpp}}$ the maximum power point voltage ripple factor, and f the switching frequency. Given that the required input capacitance depends on the V_{mpp} and I_{mpp} of the solar-cell string, factors such as the cell type, cell area, and the number of series-connected cells play an important role. Moreover, the switching frequency f significantly affects the capacitance requirements. Generally, increasing the switching frequency reduces the size of the required passive elements, thereby decreasing the overall cost and size of the converter [207]. However, the switching frequency must remain within a certain upper limit to avoid excessive switching losses. While switching frequencies are typically not listed in power converter datasheets, modern commercial module-level DC-DC power optimizers may operate around 200 kHz*. Similarly, in a 2013 research publication on sub-module-level DC-DC

* This is based on measurements conducted in the lab of Prof. Dr. F. P. Baumgartner. They characterized the

power optimizers a switching frequency of 250 kHz was reported [65]. This publication noted that operating at low voltage at the sub-module level permits the use of power transistors with faster switching dynamics, enabling relatively high switching frequencies. Moreover, advancements in transistor technology are expected to further increase feasible switching frequencies in the future. It is worth noting that the upper limit of switching frequency can also be extended by considering different converter topologies. Furthermore, a design choice needs to be made for the maximum allowed voltage ripple, which is typically chosen below 1% [92]. If some typical numbers for cell-level power conversion are considered (γ_{I_L} of 20%, $\gamma_{V_{mpp}}$ of 1% an I_{mpp} of 6 A, a V_{mpp} of 0.63 V, and a conservative f of 100 kHz), Equation 5.2 gives a minimum required input capacitance of 238 μF. This can be compared to the lowest operational MPP capacitance values found in Chapter 4. The lowest values in that chapter were found for an irradiance of 0.1 sun and a temperature of 30 °C: 0.283 μF/cm^2 for the PERC cell and 20.2 μF/cm^2 for the IBC cell. Whereas the MPP capacitance of the PERC is relatively low, that of the IBC is easily high enough to reach the required input capacitance. Thus, the self-capacitance of industrial c-Si PV cells can be sufficiently large to fulfil the role of input capacitor at cell or sub-module level power conversion. However, two key factors must be considered for such applications. First, the impedance measurements presented in Part I of this thesis were obtained using signals with an amplitude well below the thermal voltage kT/q, which corresponds to approximately 25.7 mV at room temperature. Therefore, these findings are only applicable for potential applications such as utilizing the capacitance at the input of a power converter if the voltage ripple across the PN junction remains minimal. Second, at high operating frequencies, the dynamic resistance and capacitance of the PN junction exhibit relaxation effects. Further research is needed to determine how this frequency-dependent behavior influences the voltage and current ripples and their potential impact on losses.

Since the so far discussed self-capacitance is a result of the physical processes taking place in solar cells, the capacitor cannot be connected in a place of choice. For example, it is unlikely that the self-capacitance can fulfil the function of C_2 in Figure 5.4(b), as it is not naturally in the right place in the equivalent solar cell circuit. As such, it is worth considering a *decoupled* approach, where one or both of the electrodes of the PV-integrated capacitor are decoupled from the PV device.

First, we consider the integration of so-called *thin film capacitors*, which are commonly used in integrated circuits. The most used types of these thin film capacitors are the metal-insulator-metal (MIM) capacitor, the metal-oxide-semiconductor (MOS) capacitor, and the pn junction capacitor, all presented in Figure 5.5. When thin film capacitor structures as in Figure 5.5 are integrated into c-Si PV cells, the surface area that the devices occupy competes with the area used for charge carrier collection in the PV cells. Thus, for the feasibility of this approach, a sufficiently high capacitance density must be achieved. However, it is worth noting that a high capacitance density is often counterbalanced by a low maximum voltage rating. This can be explained by the fact that dielectric breakdown occurs at a lower voltage as the dielectric layer gets thinner, as was explained earlier in this section. When reviewing literature, it appears that reported den-

operation of a modern commercial buck-boost power optimizer with a rated DC input power of 370 W and a maximum DC input voltage of 60 V, where the switching frequency was determined to be 200 kHz.

sities of planar CMOS compatible thin film capacitors are currently lower than 1 μF/cm^2 [208]. In [209], the development of a CMOS compatible capacitor is reported with a capacitance density of 0.8 μF/cm^2 and a maximum voltage rating of 3 V. The highest capacitance densities are achieved for designs with advanced 3D-structures, resulting in capacitance densities of 28 μF/cm^2 and 1.15 μF/cm^2 for MIM and pn-junction capacitors, respectively [210, 211]. However, the relatively complex fabrication steps required for the fabrication of such devices deteriorate the ease of integration into PV cells. Thus, a planar thin film capacitor that is integrated into a PV cell is unlikely to exceed a capacitance density of 1 μF/cm^2. As explained earlier in this section, the input capacitor of a cell or sub-module level DC-DC boost power converter typically requires a capacitance in the order of tens of μF. Although the required capacitance might differ for other applications and power converter configurations, it can be concluded that it is challenging to achieve PV-integrated thin film capacitors with a high enough capacitance to be applied in PV power converters.

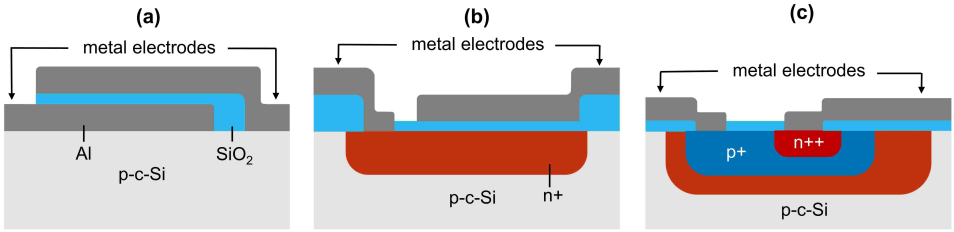


Figure 5.5: Basic thin film capacitor structures: (a) Metal-insulator-metal (MIM) capacitor, where two metal layers are separated by a dielectric. (b) Metal-oxide-semiconductor (MOS) capacitor, where a dielectric is separated by a metal layer and a highly doped region. (c) Pn junction capacitor structure, where the junction capacitance creates the capacitive effects.

An alternative approach is presented in [212], where a photosupercapacitor is added to the back of a perovskite solar cell. Here, a three-electrode interconnection scheme is used and the PV cell and capacitor share a common electrode to realize a hybrid solar-storage device. In Figure 5.6, a similar structure is presented for a c-Si PV cell. The main advantage of this approach is that the capacitor does not compete with the PV cell area used for charge carrier collection. Since this allows for the integration of capacitors with a larger area, it becomes simpler to create integrated devices with sufficiently high capacitance. However, a drawback of this three-electrode interconnection approach is that the application is restricted to configurations where the capacitor is directly connected to the PV cell. As such, the flexibility to apply this capacitor integration method in different power converter topologies is limited.

5.2.4. Inductors

An inductor is a device that stores energy in the form of a magnetic field when electric current flows through it. Inductors are based on the principle of Lenz's law, which states that a change in current in all electrical conductors creates a magnetic flux that tends to cancel the change, an effect referred to as inductance [213]. To achieve a high inductance, most inductors consist of an electrical conductor that is wound around a

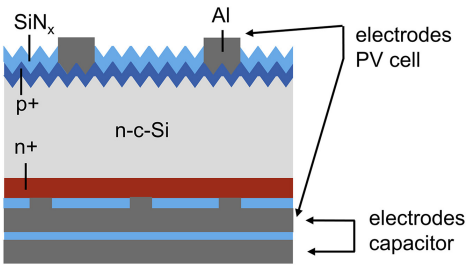


Figure 5.6: Three-electrode interconnection scheme, where the PV cell and capacitor share a common electrode

ferromagnetic core. As such, inductors are often the bulkiest and most expensive components in power converters [214–217].

However, like all conductors, regular c-Si PV cells themselves exhibit inductive effects. Similar to the approach in the previous section, we consider first the possibility to exploit the inductive behaviour that solar cells naturally exhibit. In Chapter 2, the inductive behaviour in modern solar cells was reported. There, it was found that the studied single-cell laminates exhibited inductances between 63 and 130 nH. It is important to note that the inductance of only the cell is lower than that of the full laminate, although its exact value is unknown. When considering a string of series-connected cells, the total inductance scales linearly with the number of cells. This self-inductance can be compared the properties of an inductor that is positioned at the input of a power converter. For instance, the minimal inductance of the inductor in a DC-DC boost converter can be calculated by [92]:

$$L_{min} = \frac{V_{mpp} D}{I_{mpp} \gamma_{I_L} f}, \tag{5.3}$$

where L_{min} is the minimum required inductance, V_{mpp} is the maximum power point voltage of the solar cell string, D is the duty cycle of the converter, I_{mpp} is the maximum power point current of the string, γ_{I_L} is the inductor ripple current factor. Hence, the product of I_{mpp} and γ_{I_L} is the peak-to-peak value of the ripple current. Moreover, f is the converter switching frequency. From Equation 5.3 it can be deduced that in the boost converter, the inductance required to achieve a certain ripple current scales linearly with the number of series-connected cells. As such, it can be calculated irrespective of the string length from which frequency it becomes possible to replace the input inductor of a boost converter with the self-inductance of a solar cell string. Here, it is assumed that the self-capacitance of the solar cell string sufficiently reduces the voltage ripple [70]. When considering typical values (V_{mp} = 0.63V, D=0.5, I_{mp}=6A, γ_{I_L}=0.2 and L=65 nH), the minimum required frequency is approximately 4 MHz. For a switch-mode converter, this switching frequency is relatively high. In general, it must be acknowledged that a high switching frequency in the converter comes with the disadvantages of (1) higher switching power losses, (2) increased inductor core losses, and (3) heightened electromagnetic interference.

Another approach would be to integrate the inductor onto the solar cell, which could facilitate a lower switching frequency than when only the solar cell self-inductance is

used. To further explore the integration of inductors onto PV cells, we can review related research from the fields of integrated circuits (ICs) and wireless power transfer (WPT). In integrated circuits, *thin film inductors* are formed by creating spiral-like metallization patterns on top of silicon wafers [168]. It has been demonstrated experimentally that thin film inductors can be used for DC-DC power conversion [218–220]. It is worth noting that screen printing, which is commonly used for the fabrication of solar cells, can be used as well to fabricate planar inductors [221]. Thin film inductors can be fabricated in various layouts, such as square, hexagonal, circular, and octagonal patterns [222]. Although more background on analytical expressions for the self-inductances of these different spiral metal patterns can be found in [223], the dependence of the inductance on the number of turns is usually quadratic [224]. The main drawback of increasing the number of turns on a given area is that this causes the series resistance of the conductor to increase as well. An important figure of merit for inductors that quantifies the trade-off between inductance and resistance is the quality factor $Q = \omega L/R$. It is worth noting that both the Q and the inductance density can be increased by enclosing the conductor with magnetic material [225]. On the other hand, magnetic materials bring along fundamental loss mechanisms, such as hysteresis and Eddy-currents [226]. The core losses become increasingly dominant for operation at higher frequencies [227], and can have a significant effect on the watt-hour efficiency of DC-DC power converters [228]. Thus, air-core inductors are more suitable for very high frequency (VHF) applications (30-300 MHZ) [229]. Apart from the intended operating frequency, the optimal design of an inductor depends on the power level that the device should be able to support. Since the power levels in WPT are usually higher than those in ICs, the planar inductors in WPT applications typically require a higher Q and a lower parasitic resistance. As such, the planar coils reported in the field of WPT give a better indication of which inductances can be achieved on PV cells. In [230], a planar coil structure with an outer diameter of 10 cm for application in WPT was reported to exhibit a self-inductance of 3.13 μH and a Q of 185. In [231], a self-inductance of 12.52 μH and a Q of 63 were reported for a planar coil with an outer diameter of 13 cm. For diameters up to 20 cm, it has been demonstrated that inductance values from several tens of μH up to 80 μH can be achieved, corresponding to Q values between 50 and 120 [231–235]. Such inductance values are in the same order of magnitude as inductors that are used in module-level power optimizers in PV applications. For example, the inductor of the module-level power optimizer in [236] has an inductance of 22 μH. It is worth mentioning that the inductance of several solar cells connected in series adds up. This means that the inductance of a string of cells can be increased in a relatively simple manner by increasing the number of series-connected cells. Thus, we can conclude that the area of c-Si PV cells is sufficiently large to facilitate the integration of planar inductors exhibiting inductance values and quality factors that are useful for power conversion and wireless power transfer. Moreover, when considering the performance at system level, it could also be a possibility to design the interconnections between cells such that the self-inductance is increased. However, it is out of the scope of this thesis to further describe this option. Next, we investigate how planar coils can be integrated onto c-Si PV cells.

Firstly, we consider re-designing the metallization patterns that are already present in common PV cell designs. This approach offers ease of integration, since it might be

realized without any additional fabrication steps compared to standard c-Si cell process flows. For FBC solar cell designs, there are metal front- and back contacts present. Since the classic metal grid pattern on the front surface involves a careful optimization in the trade-off between resistive and shading losses [1], there is little room to create spiral-like metallization patterns here. There might be more potential to create such patterns on the backside, where the absence of shading losses (at least in non-bifacial cells) gives more room to make alterations to the metallization pattern. On the backside of an FBC solar cell, the metal contacts with underlying point contacts can be re-designed into a spiral-like shape, as presented in Figure 5.7(b). A similar approach could be used for IBC solar cells, as presented in Figure 5.7(d). It is worth mentioning that the latter solution only shows a possible geometrical re-design option for the IBC fingers and metal contacts. However, the interaction between the two coils must be properly studied to verify whether this topology can be effectively used as an integrated inductor within a power converter. The two-diode equivalent circuit of a solar cell with increased self-inductance is presented in Figure 5.7(e).

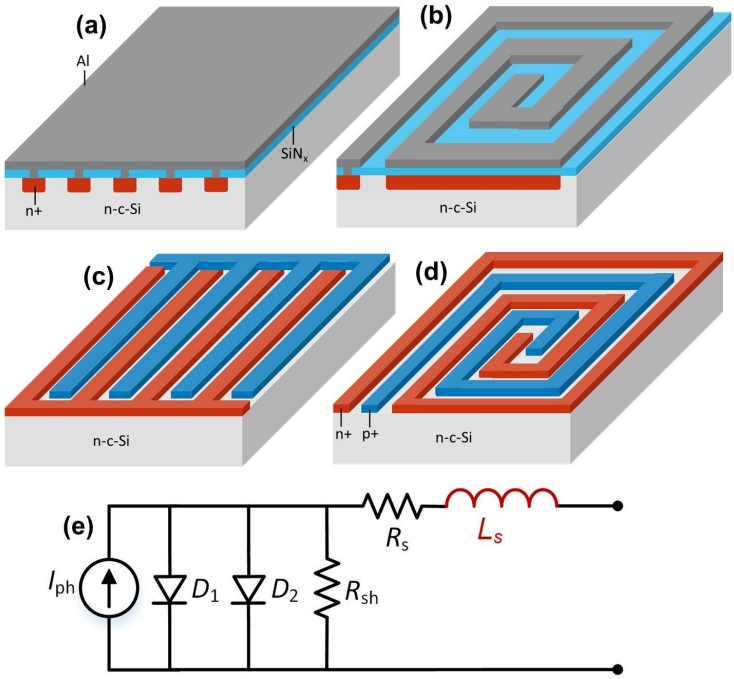


Figure 5.7: Enhancing PV self-inductance by re-designing metal contacts into spiral-like patterns. (a) Rear side of an FBC cell structure with point contacts. (b) Possible re-design of the FBC cell structure, aimed at an increased self-inductance. (c) Rear side of an IBC solar cell structure, where highly doped layers are used for collection of charge carriers. In an IBC cell, metal contacts are placed on top of these doped layers. (d) Possible re-design of the IBC cell structure, aimed at an increased self-inductance. (e) Two-diode equivalent solar cell model expanded with self-inductance (red).

It should be taken into consideration that the analytical formulas developed for inductors are not directly applicable for this solar cell-integrated approach, as the current

through the metal layer will increase towards the outer side of the spiral. Thus, quantifying the exact inductances that the proposed structures will exhibit requires further research. Furthermore, these spiral-like metallization patterns on the back of solar cells will affect the series resistance and thus the fill factor with respect to standard c-Si solar cell designs. Future research will need to verify whether it is possible to create a c-Si solar cell with a good fill factor and a high self-inductance at the same time. Finally, it is worth noting that the addition of a magnetic material can also be considered to increase the self-inductance without increasing the number of turns. The deposition of magnetic material on one side of the inductor can increase the inductance up to 100% [237]. However, including such magnetic materials would increase fabrication costs and require additional processing steps using materials that have not been studied in combination with solar cells, such as Ni-Fe, Co-Zr-Ta, and Fe-Al-O [238, 239].

Furthermore, it is worth considering a *decoupled* approach, where the inductor is separated from the charge carrier collection layers by an insulator, as presented in Figure 5.8. This method offers more flexibility in the inductor design, as it allows the charge carrier collection layers and the planar coil to be optimized separately. Thus, the process of increasing the self-inductance without causing a too large loss in fill factor is simplified. Furthermore, the decoupled approach allows configurations where the cell is transformed into a 4-terminal device. As such, it would enable integrated designs where the inductor is not directly connected to the PV generator, such as the buck converter. A final advantage of this approach is the reduced probability that the addition of magnetic materials will affect the solar cell, as it is separated by an insulating layer. The structure would also allow for designs where the magnetic material is present on both sides of the inductor, also known as the sandwich structure [240]. However, the decoupled approach will require additional processing steps compared to regular PV cell fabrication processes. Every step from the deposition of the insulating layer onwards needs to be performed specifically to create the inductor. Thus, it would be more challenging to achieve cost-effective designs for this decoupled approach. A feasibility study for inductor integration with the decoupled approach is described in Chapter 6.

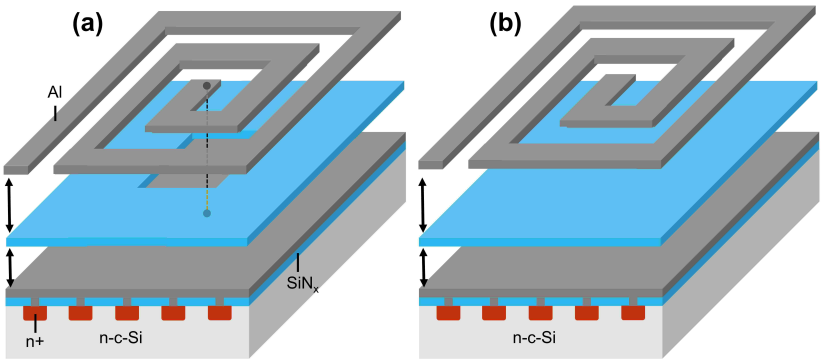


Figure 5.8: Decoupled inductor integration, where a planar inductor is spatially separated from the PV cell by an insulating layer: (a) The inductor is electrically connected to one of the PV cell contacts, but spatially separated from the PV cell by an insulating layer. (b) In the decoupled approach, the design can be adapted in a relatively simple way to create a 4-terminal configuration.

5.2.5. Combining the different solutions

Whereas integration of each power electronic component was treated separately in the previous sections, the main potential lies in combining the different approaches. For example, the integration of power transistors and the exploitation of PV self-capacitance and self-inductance were discussed in the previous sections. For successful implementation of these three concepts into one PV cell, the equivalent circuit of the cell can be expanded as in Figure 5.9.

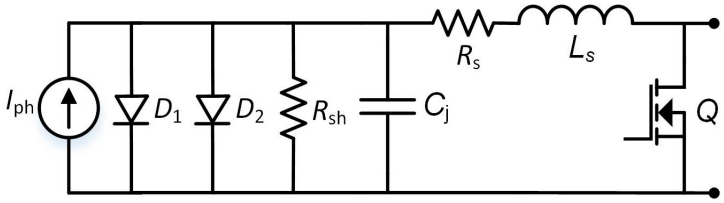


Figure 5.9: Equivalent circuit of a solar cell
, expanded with the self-capacitance, self-inductance, and an integrated MOSFET.

If we refer back to the equivalent circuit of a DC-DC boost converter from Figure 5.4(b), a large part of the boost converter would already naturally be included in the solar cell. Solar cell integration of a DC-DC boost converter is particularly promising because the self-capacitance and self-inductance of the solar cell are naturally complementary to the boost converter topology. Nevertheless, when power electronics can be successfully integrated into solar cells, numerous new topologies for power converters and reconfigurable modules will become possible.

5.3. Challenges

In the previous section about feasibility, the importance of ease of integration has already been stressed. Moreover, several specific challenges of the different power electronic components were treated. In this section, we describe some more general challenges related to successful integration of power electronic components into c-Si PV cells.

5.3.1. Thermal management

Thermal management will be a challenge for successful integration of power electronics, as power dissipation due to the parasitic resistance of the devices might cause the PV cells to heat up. It is well known that the efficiency of solar cells decreases with increasing temperatures. This is caused by the diminishing of the V_{oc} and FF, even though the J_{sc} increases slightly [241, 242]. Non-uniformities in the temperature distribution across a cell lead to further losses. For instance, in [243] it was shown that non-uniformities in the temperature distribution of a solar cell are amplified during exposure to sunlight. In the case of 1000 W/m^2, a specific pre-heated part of the cell heats up 14.2% faster than the surrounding cell area. As such, an initial temperature mismatch of 5.9K leads to an 8.6% reduction in I_{sc} and a 10.8% reduction in V_{oc} compared to a uniformly illuminated device. Thus, especially in the case of integrated power electronic components that only

occupy part of the wafer surface, the heat dissipation in the devices must be limited by ensuring that the parasitic resistance of the integrated power electronics is sufficiently low. For successful industry adoption, additional measures might be required to improve thermal management, either at cell- or module-level.

5.3.2. Opto-electrical challenges

Moreover, there are opto-electrical challenges involved in successful integration of power electronics into the bulk of c-Si solar cells. For discrete semiconductor power devices from industry, packaging protects the silicon from sunlight and other external influences. However, in the integrated approach, the power electronics and solar cell share a common bulk. Firstly, this means that the integrated power electronics will be exposed to photogenerated charge carriers that are generated in the bulk of the wafer. In the case of a diode or a pn junction capacitor, it is possible that the device would start acting like a solar cell itself, which means an undesired current would be generated from inside the device. There might be differences between pn junction diodes and Schottky barrier diodes in how sensitive the devices are to such an effect. However, the previous works about integrated bypass diodes into solar cells did not report any effect of photogenerated carriers, which can presumably be explained by the effect being minor due to the small area of the device on the wafer. In the case of transistors, the photogenerated charge carriers could pose a challenge to their performance and controllability. Here, there might be differences between current controlled transistors (BJT) and voltage controlled transistors (MOSFET) in their sensitivity to such an effect. Furthermore, electrical interactions in the bulk of the wafer could lead to undesired effects. For example, the potential differences that are generated during PV operations might affect the operation of integrated transistors. It is worth mentioning that there have been reports of transistors and PV cells sharing a common bulk [244–248]. These reports describe low-power chips (μW-mW) that are powered by an on-chip PV cell, and demonstrate the technical feasibility of transistors and PV cells sharing a common bulk. However, these publications often involve simple PV architectures with relatively low solar cell efficiencies, and the extent of opto-electrical interaction between the chip and the solar cell is highly dependent on the specific design. Thus, further research is required on the opto-electrical challenges related to device integration into PV cells to fully understand and properly describe them. If these challenges turn out to be too detrimental, alternative integration approaches can be considered. For example, the power electronics can be separated from the bulk of the PV wafer by an insulating layer. Nonetheless, such an approach would require additional processing steps.

5.3.3. Repairability and long-term reliability

When a failure occurs in a single PV component nowadays, the complete module is often decommissioned and directed towards disposal [249]. Nevertheless, interest in on- or off-site repairability has been increasing. For example, it has been reported that special PV module designs with higher repairability can become cost-effective [250]. However, the integration of power electronics into solar cells poses a challenge to the repairability when a single component fails. In such cases, the only possibility would be to replace the complete cell with a new one. It is worth mentioning that there are developments

towards PV modules in which the cells are not laminated [251], making it more feasible to replace individual cells in the module.

For successful industry adoption, it is thus important that the lifespan of the integrated power electronics is similar to that of PV modules. Typical lifetimes of PV systems are in the range of 25 years. However, most system-level inverters come only with a 10-year warranty, which means that owners of PV installations should account for a replacement of the inverter during the lifetime of the PV system. Nevertheless, manufacturers of module-level converters typically provide higher warranties of 25 years. Taking these typical PV module and power converter lifespans into account, the analysis in [41] shows that adding sub-module level power electronics can improve the lifetime of PV systems by 5-10 years. Furthermore, as explained earlier, monolithically integrated components into PV cells hold the promise of higher reliability, potentially increasing the converter lifetime further.

5.4. Discussion

Integration of power electronics into c-Si PV cells has the potential to (partly) replace module-level power electronics and enable highly granular sub-module-level power optimization for higher energy yield. Furthermore, cell-integrated power electronics might simplify designs of autonomous devices powered by PV cells. Eventually, cell-integrated power electronics could even facilitate innovative PV module designs that are capable of wireless power transmission.

The feasibility of integrating various designs of diodes, transistors, capacitors, and inductors into c-Si solar cells was discussed. First of all, diodes exhibit high ease of integration into PV cells and successfully integrated designs have already been demonstrated. On the other hand, the integration of transistors is more complex. Since transistor fabrication processes require lithographic steps, it is necessary for cost-effective integration to combine as many processing steps as possible with PV fabrication. It was found that there is limited flexibility to combine processing steps of standard vertical power transistor designs with PV fabrication. As such, possibilities were suggested to combine certain aspects of small-signal and power transistors to end up with transistor designs that have appropriate properties and could be integrated in a relatively simple way. Regarding passive component integration, it was found that the self-capacitance of modern crystalline silicon solar cells is sufficiently large for to replace the input capacitor of a boost converter. However, for thin-film capacitor integration, it is challenging to achieve a sufficiently high capacitance. For this approach, the capacitor area competes with the cell area that is used for charge carrier collection, and reported capacitance densities are typically lower than 1 μF/cm^2. Thus, to achieve the desired capacitance with an integrated capacitor, a more promising configuration is a three-electrode interconnection scheme on the backside of an FBC cell. However, this approach has thus far only been used to realize a hybrid solar-storage device and allows for limited flexibility to be applied in different power converter topologies. Finally, the integration of inductors onto solar cells was explored. As a starting point, the self-inductance of a solar cell string could potentially be leveraged to replace the inductor at the input of a power converter. Using this approach for an exemplary boost converter, it was found that high switching frequencies in the MHz range are required. Alternatively, the required switch-

ing frequency may be reduced through the integration of inductors. It was found that the area of PV cells is sufficiently large to facilitate the integration of planar coils exhibiting inductance values that are useful for power conversion. In WPT applications, planar coil inductances of 3-80 μH have been demonstrated on areas similar to those of industrial PV cells. Moreover, several design options were proposed to integrate spiral-like metallization patterns and planar coils on the backside of FBC and IBC PV cells.

Generally, it is a challenge to realize integrated power electronics designs that have high ease of integration and are at the same time competitive with discrete power devices that can be bought on the market. Future research will prove whether the trade-offs that need to be overcome can be adequately handled. Finally, general challenges that should be considered for successful integration of power electronics are appropriate thermal management, opto-electric behaviour under illumination, and repairability.

6

Feasibility study on photovoltaic module-integrated planar air-core inductors

This chapter is based on the following publication:

D. A. van Nijen, S. Chakravarty, J. Voorn, M. Zeman, O. Isabella and P. Manganiello, "Feasibility study on photovoltaic module-integrated planar air-core inductors to facilitate embedded power electronics", in *Energy Reports*, vol. 13, 82-89, 2025.

The data underlying this chapter was published in the 4TU Research Data Archive [*].

6.1. Introduction

The option to remove the inductor from the power converter and directly integrate it onto the solar cells is relatively unexplored. Inductors play an important role in power converters by reducing the ripple current [92], but they often emerge as the largest and most expensive components [214–217]. Nevertheless, increasing the switching frequency can reduce the required inductance value, hereby reducing the costs and volume of the inductor [207]. Here, it is worth noting that every conductor exhibits at least some inductance. Thus, pushing this concept to its limit involves exploiting the natural inductance exhibited by solar cells at the input of a converter to the point where a physical inductor becomes unnecessary [72]. Switch-mode converters that normally have their inductor at the input of the converter could be suitable candidates for this concept. However, to achieve a sufficiently low current ripple with this approach, a switching frequency of at least several MHz may be required (the calculation for an

[*] D. A. van Nijen et al., "Data underlying the publication: Feasibility study on photovoltaic module-integrated air-core inductors to facilitate embedded power electronics", 4TU.ResearchData, 2024, https://doi.org/10.4121/b7267f87-15b1-4c97-b9b2-e3aeb95393ac.

exemplary boost converter was shown in section 5.2.4). For a switch-mode converter, this switching frequency can lead to high losses. In general, it must be acknowledged that increasing the switching frequency also comes with the disadvantages of (1) higher switching power losses, (2) increased inductor core losses, and (3) heightened electromagnetic interference.

An intermediate approach in between conventional sub-module converters and high-frequency converters that leverage the solar-cell self-inductance could be to integrate inductors at a sub-module level. By selecting a planar inductor structure, they could potentially be embedded within the PV laminate. For instance, this integration could be done by directly integrating the inductor on the back of a PV cell [70]. Alternatively, other module-integration methods, such as combinations with three-dimensional-woven interconnection fabrics [252] or conductive interconnection foils [253], could be worth exploring. Successfully integrating inductors in such a way can enhance the inductance of a solar-cell string when connected in series. Subsequently, this can be leveraged in combination with converter topologies that incorporate an inductor at the input. Additionally, the planar inductors offer flexibility in their connection configurations, allowing the inductance to be used in converter topologies with inductors located in other parts of the circuit. However, to assess the integration feasibility, it is crucial to understand the design requirements of the inductor itself. A common approach to enhance the inductance of an inductor involves using a ferromagnetic core made of material with large magnetic permeability. This study, however, investigates planar inductors without such a core. Since the common PV-module materials such as silicon, encapsulants, glass, copper, aluminum etc., all have a relative magnetic permeability close to one - similar to the magnetic permeability of vacuum and air - this design is referred to as *air-core* inductors. Specifically, we explore how the planar air-core inductor design can be adjusted to achieve the desired inductor performance and evaluate the feasibility of integrating these inductors into a sub-module-level power converter. All inductors in this study use copper as their conductor material, which their area fixed at 12.5 cm × 12.5 cm, which is the maximum available area for a 5-inch solar cell [254]. On the one hand, air-core inductors offer simple manufacturing and eliminate core losses during operation. On the other hand, achieving sufficiently high inductance can be challenging. This necessitates operation at relatively high switching frequency, which can adversely affect inductor performance. While high-frequency effects could be partly mitigated by using litz wires [255], this contradicts the goal of simplified manufacturing. Therefore, this study evaluates the potential of the more simple planar inductor designs, despite the high-frequency effects.

This study employs a finite element model, which is introduced in section 6.2. This is followed by an analysis of how various inductor design parameters affect the performance in section 6.3. The feasibility for integration into sub-module power converters is discussed in section 6.4, followed by the conclusions in section 6.5.

6.2. Simulation method

Figure 6.1(a) shows an example of how the inductor can be integrated at a sub-module level [70]. In this configuration, the inner terminal of the planar inductor is connected to the metal back-side of a PV cell, while the outer terminal can be connected to an external

circuit. Apart from this internal connection, the inductor is separated from the PV cell by an electrically insulating layer, which could be either encapsulant material or a dielectric layer. The inductance of a planar inductor is the sum of the self-inductances of the individual metal segments and the mutual inductances between them [256, 257]. Although analytic expressions for calculating inductance of planar inductors have been reported [224], it is important to note that these expressions are only valid for specific ranges of coil geometries and frequency ranges. For instance, in practical applications such as power converters, the inductor is subjected to a ripple current at a certain frequency. At sufficiently high frequencies, this introduces phenomena such as the skin effect and proximity effect. Skin effect is the phenomenon where alternating current tends to concentrate near the surface of the conductor at high frequencies [258]. This occurs due to the eddy currents that are induced by the time-varying magnetic field. Additionally, the proximity effect is caused by magnetic interaction between different segments of the inductor track. The time-varying magnetic fields generated by neighboring segments further modify the current distribution, leading to a higher current density at the edges of the track [259]. Due to these high-frequency effects, the resistance and inductance values may differ under direct current (DC) and alternating current (AC) conditions, both of which are often relevant for implementation in a power converter. To analyze the inductance and resistance for planar inductor structures such as the one in Figure 6.1(a) while accounting for high-frequency effects, the planar inductors in this study are analyzed using the finite element method simulator COMSOL [260]. Specifically, a three-dimensional inductor geometry, as depicted in Figure 6.1b, is investigated. The analysis is performed using the magnetic fields interface, which solves Maxwell's equations. This solution is computed in the frequency domain, meaning it is based on a sinusoidal current excitation at a fixed frequency. By calculating the magnetic field and induced current distributions within the inductor, the simulation provides both an inductance value and a resistance value for each tested geometry. The details and equations supporting these computations are outlined in the AC/DC module user's guide of COMSOL [261]. In the simulated geometries, the inner and outer terminals of the inductor are connected to form a closed-loop design to comply with the current conservation inherent in Ampère's law. While not shown in Figure 6.1b, the inductor geometry is positioned within a spherical air domain, with an infinite element domain at the outer boundary to emulate a domain of infinite extent. This configuration ensures accurate simulation of the magnetic field lines, resulting in precise inductance values. The inductor itself is made of copper with a conductivity of 5.998×10^7 S/m and the temperature is set at 20 °C. It is important to mention that since the coil is surrounded by air, parasitic phenomena that may occur between the coil and substrate in the eventual application are not considered in this analysis. Various coil design parameters, as indicated in Figure 6.1b, are examined in this study. These parameters include the internal diameter or middle gap (g), track spacing (s), track width (w), and thickness (t). The outer diameter (d) is fixed at 12.5 cm to optimize the inductor design while ensuring it fits within the area of an industrial solar cell.

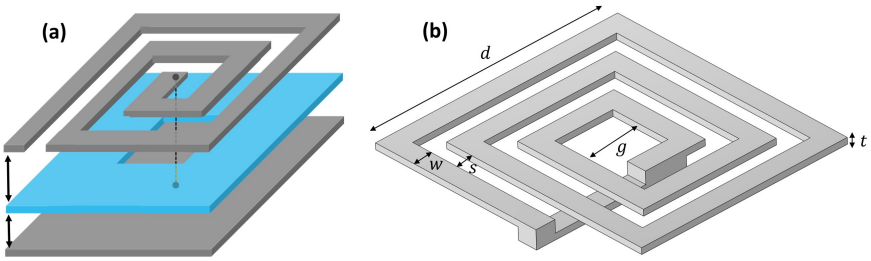


Figure 6.1: (a) Example configuration of how a planar inductor could be integrated at a sub-module level. Whereas the inner terminal of the inductor is connected to the back-side of a PV cell, the rest is separated by an electrically insulating layer. Moreover, (b) shows the geometry of an example three-turn inductor structure as modeled in this study. Various design parameters are indicated; the outer diameter (d), internal diameter or middle gap (g), track spacing (s), track width (w), and thickness (t).

6.3. Inductor design results

This section describes how the inductor properties change with design and frequency variations, focusing primarily on AC inductance (L_{AC}) and AC resistance (R_{AC}). At relatively low frequencies below 1 kHz, the high-frequency effects in the studied inductor geometries diminish, causing the 1 Hz values to converge to the DC inductance (L_{DC}) and DC resistance (R_{DC}). As a reference for interpreting the inductor resistance values, it is useful to revisit Table 2.2 in Chapter 2, where the area-specific series resistance of the different solar cell laminates ranges between 0.55 Ωcm^2 and 1.35 Ωcm^2. For a solar-cell area of 156 cm^2, this would correspond to a series resistance between 3.5 mΩ and 8.7 mΩ.

6.3.1. Spacing/width variation

The effect of track spacing (s) on inductor performance, with d and g held constant, is illustrated in Figure 6.2. Notably, an increase in track spacing corresponds to a decrease in w. The results are for a 4-turn coil with a gap of 4 cm and a thickness of 0.5 mm. Figure 6.2(a) demonstrates that at low frequencies, minimizing s while maximizing w leads to the lowest R_{AC} values. This is as expected, since a high w maximizes the cross-section of the track. However, maximizing w and minimizing s does not necessarily yield the lowest R_{AC} values at high frequencies. For air-core inductors, it is known that the resistance may increase at high frequency due to the skin effect and the proximity effect [262]. Which of these two mechanisms dominates the increase in resistance depends on the inductor geometry. For instance, at frequencies of 50 kHz and higher, Figure 6.2(a) shows that there is significant increase in R_{AC} when s decreases below 2 mm. This shows that a minimum spacing is required to limit the proximity effect. Conversely, increasing s beyond approximately 6 mm also leads to a higher R_{AC}, attributed to the increase in DC wire resistance due to reduced w. Thus, for frequencies above 50 kHz, R_{AC} reaches its minimum around a spacing of 4-6 mm. However, even at this spacing, there is still a notable increase in R_{AC} with increasing frequency, which can presumably be mostly attributed to the skin effect in the inductor's track. The occurrence of the skin effect at high frequencies is an inherent limitation of the chosen design. While out of the scope

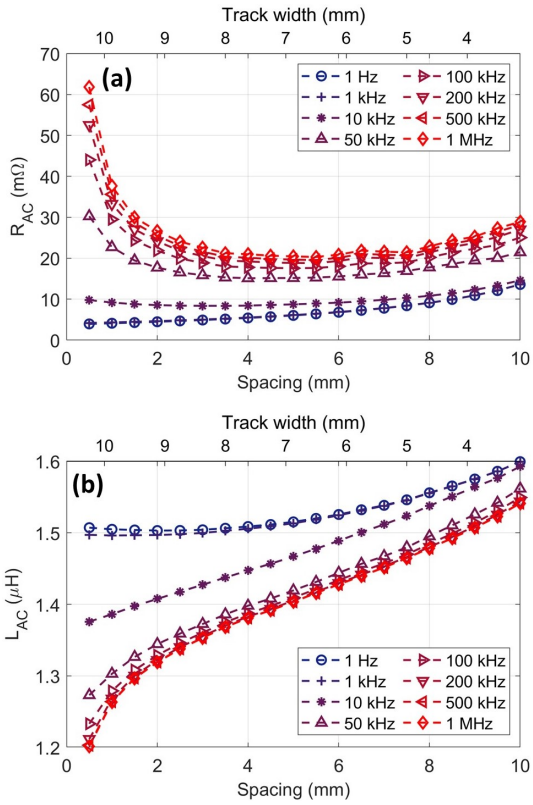


Figure 6.2: The (a) R_{AC} and (b) L_{AC} of a planar inductor are plotted as a function of spacing (primary horizontal axis) and width (secondary horizontal axis). The inductor structure consists of 4 turns, with an outer diameter d of 12.5 cm, a middle gap g of 4 cm, and a thickness t of 0.5 mm.

of this thesis, a discussion on the use of alternative track structures such as multitrack, in-layer twisted, or Litz structures is reported in [262].

In Figure 6.2(b), it is evident that for both low and high frequency, an increase in s is accompanied by an increase in L_{AC}. At low frequencies, this is mostly related to the fact that an increase in s corresponds to a decrease in w. Previous work has shown that structures with smaller cross-sections tend to exhibit higher inductance values [262]. The reason behind this phenomenon is that the magnetic field becomes more concentrated around the conductor, resulting in higher self-inductance [154]. Indeed, through additional COMSOL simulations for a straight wire it was confirmed that the relative increase in L_{AC} as w decreases is similar (not shown). Furthermore, Figure 6.2(b) shows that higher frequencies reduce L_{AC} for all tested geometries. This is related to the well-established phenomenon that the self-inductance of wires decreases as the current distribution over their cross-section changes with increasing frequencies [263]. It is important to note that the decrease in L_{AC} with frequency is more pronounced for low s values than for high s values. At higher s values, the change is primarily due to the skin

effect, while at lower s values, both the skin effect and proximity effect contribute to the alteration in current distribution.

The interplay between s and w significantly influences the quality factor of the inductor. The quality factor Q is defined as $Q = 2\pi f L_{AC}/R_{AC}$, with f representing the frequency. For frequencies between 10 kHz and 1 MHz, the highest Q value is observed within the spacing range of 4 mm to 6 mm. However, it must be noted that the highest Q does not necessarily correspond to the optimal coil for integration into a power converter, as R_{DC} can also play an important role.

6.3.2. Gap/width variation

The effect of the middle gap (g) on the inductor performance is shown in Figure 6.3. The results are for a 4-turn coil with a spacing of 5 mm and a thickness of 0.5 mm. Since d and s are held constant, an increase in g results in a decrease in w. Additionally, a larger g results in an increase in the total track length.

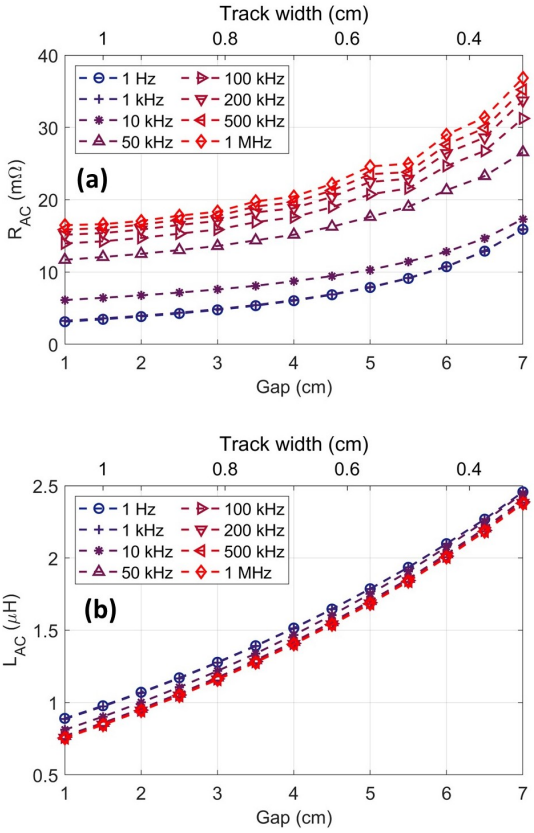


Figure 6.3: The (a) R_{AC} and (b) L_{AC} of a planar inductor are plotted as a function of gap size (primary horizontal axis) and width (secondary horizontal axis). The inductor structure consists of 4 turns, with an outer diameter d of 12.5 cm, a spacing s of 5 mm, and a thickness t of 0.5 mm.

Figure 6.3(a) illustrates that a higher g correlates with an increase in R_{AC} across all tested frequencies. At low frequencies, this effect is due to both the smaller cross-section of the track and the increased total track length. However, at higher frequencies, the relative increase in R_{AC} due to an increase in g becomes smaller. For instance, at 1 Hz the R_{AC} increases a factor ~5.1 when g is increased from 1 cm to 7 cm, whereas this is only a factor ~2.2 for 1 MHz. This difference is mainly attributed to the skin effect, which causes the current to concentrate at the edges of the wire at high frequencies. Consequently, a reduction in w has a diminished impact on the R_{AC} at high frequency.

In Figure 6.3(b), it is evident that increasing g significantly increases the L_{AC} across all tested frequencies, which aligns with expectations [262]. This behavior can be understood by considering that mutual inductance is positive when currents in two parallel segments flow in the same direction and negative when they flow in opposite directions. In planar inductors, the total inductance is determined by the sum of the self-inductance and the cumulative mutual inductances between all track segments. When g increases, the contributions of positive mutual inductances between turns increase, while the contributions of negative mutual inductances decrease [224]. More theoretical background on the positive and negative mutual inductances within different segments of a planar inductor has been reported by Greenhouse [256]. Additionally, the increase in L_{AC} with higher g is partly attributed to the longer track length and the reduced w.

For low frequencies of 1 Hz and 1 kHz, the quality factor Q reaches its peak when the gap is minimized to 1 cm. However, as the frequency increases to 50 kHz and beyond, the optimal range for Q shifts to a range where the g value lies between 4 cm and 7 cm. A slightly declining trend in Q is observed beyond 5.5 cm.

6.3.3. Number of turns vs gap/width variation

In the preceding section, it was demonstrated that increasing the middle gap (g) significantly contributes to enhancing inductance. However, another viable method for boosting inductance is by increasing the number of turns (N). Indeed, it is expected from literature that the inductance increases quadratically with the number of turns when d and g are held constant [224]. This raises the question of whether a high g or a high N yields the best inductor performance, characterized by a high inductance and low resistance. Figure 6.4 presents L_{AC} at 500 kHz plotted as a function of (a) R_{DC} and (b) of R_{AC}. The data in Figure 6.4 are obtained for coils with varying number of turns and gap sizes. Optimal performance would position the data in the top left quadrant of these figures. However, it is evident from both Figure 6.4(a) and Figure 6.4(b) that a trade-off exists in the design. While L_{AC} can be increased by raising either N or g, this inevitably leads to higher R_{DC} and R_{AC} values. The changes in R_{DC} and R_{AC} result from the combined effects of variations in the total track length and the track's width. Such trade-offs between inductance and resistance are commonly encountered in inductor design [257]. It is worth noting that the inductor thickness (t) is a parameter that can still be varied, exerting limited influence on the inductance but affecting the resistance. This means that by varying t, the data in Figure 6.4 can be shifted horizontally, to a certain extent allowing for the adjustment of the resistance to the desired value. However, in this work a maximum t of 1 mm is used, since coils with higher t consume more material, are more difficult to manufacture, and can pose practical challenges for integration into a

PV module.

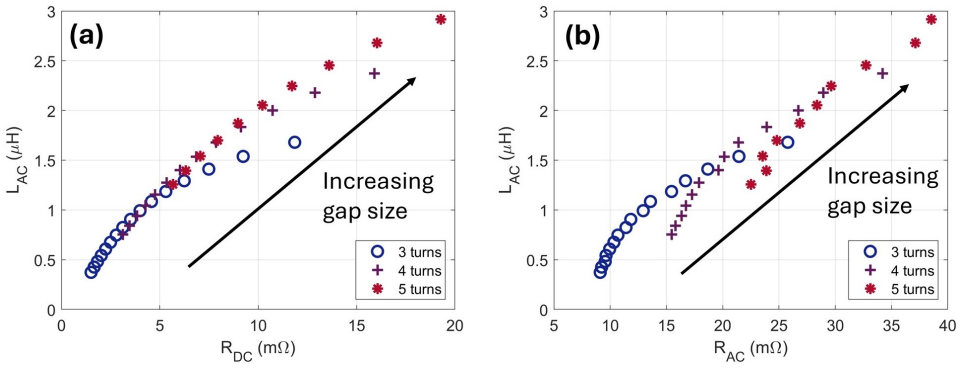


Figure 6.4: L_{AC} at 500 kHz plotted as a function of (a) R_{DC} and (b) of R_{AC}. The data are obtained from inductor geometries with varying number of turns and varying gap size, all with d = 12.5 cm, s = 5 mm, and t = 0.5 mm. For 3 turns, g is varied in steps of 0.5 cm between 1 cm and 8.5 cm. For 4 turns, g is varied in steps of 0.5 cm between 1 cm and 7 cm. For 5 turns, g is varied in steps of 0.5 cm between 1 cm and 5.5 cm.

6.4. PV module integration feasibility

Now that the inductor design considerations have been investigated, the next step is to assess whether these coils possess the desired properties for integration into a sub-module power converter. For this analysis, we assume that a string of series-connected solar cells is connected at the input of a DC-DC boost converter, which is a basic converter topology employed for MPPT in PV applications [92]. The schematic of this approach, with the inductor to be replaced by a planar inductor highlighted, is presented in Figure 6.5.

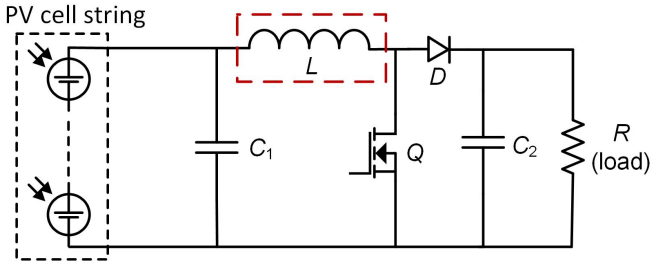


Figure 6.5: String of series-connected solar cells at the input of a DC-DC boost converter. The inductor to be replaced by a planar inductor is highlighted. The capacitors, inductor, MOSFET, diode, and resistive load are represented by C, L, Q, D, and R, respectively.

In the DC-DC boost converter from Figure 6.5, the input capacitor C_1 and the inductor L ensure that the PV cell string operates near its maximum power point. The inductor L reduces current ripple, while the capacitor C_1 minimizes voltage ripple. It is important to note that these components can partially compensate for each other; for instance, a lower capacitance may be offset by a higher inductance, and vice versa [92]. However, for

the feasibility analysis in this section, certain assumptions are made. Specifically, it is assumed that the inductor must suppress the ripple current to a peak-to-peak value lower than 20% of the DC input current at the maximum power point (MPP) under Standard Test Conditions (STC), with a duty cycle of 0.5. Additionally, it is assumed that the input capacitor C_1 minimizes the voltage ripple to the desired level. This may be achieved by leveraging the solar-cell self-capacitance [38, 70, 73], or through the integration of a capacitor within the PV module [69]. It was shown in section 5.2.4 that under these conditions, a switching frequency of approximately 4 MHz is required when only the self-inductance of a PV cell string is leveraged. In the present section, we investigate the feasibility of lowering this switching frequency to 250 kHz and 500 kHz by implementing planar air-core inductors. It is important to note that the number of solar cells in the string at the converter's input can vary, ranging from a single-cell string to a string with multiple cells. The length of the string has important implications for the required inductor properties. On the one hand, in short strings where the voltage is relatively low, the inductor only requires limited inductance to reduce the ripple current to the desired level. This is advantageous for the feasibility, as it was explained in section 6.3.3 that a lower ohmic resistance can be achieved in inductors that require a lower inductance. On the other hand, for longer strings the inductor can be permitted to have a higher resistance. This is because the power losses in the inductor depend solely on the current and do not depend on the voltage. Consequently, to achieve low power losses in the inductor as a fraction of the power generated by the string, a higher ohmic resistance is acceptable when the inductor is used with a longer solar cell string. Considering these factors, the feasibility analysis is performed for different string lengths by following these steps:

1. A range of different inductor geometries is simulated in COMSOL at 1 Hz (representing DC conditions), 250 kHz, and 500 kHz. The inductor variations comprise different numbers of turns (3, 4, 5), gap sizes (1 cm - 8 cm), spacings (1 mm, 3 mm, 5 mm) and thicknesses (0.25 mm, 0.5 mm, 1 mm). For the different combinations of these parameters, we obtain the R_{DC}, L_{DC}, R_{AC}, and L_{AC}. The resulting L_{AC} values from these different inductor geometries range between 0.3 μH and 3.2 μH.

2. The solar cell MPP parameters under STC are set at a V_{mpp} of 0.63 V and an I_{mpp} of 6 A. Using equation 5.3, we can evaluate for different solar cell string lengths and frequencies what minimum inductance is required to suppress the ripple current below 20%. Using these results, we categorize the inductors based on their L_{AC} values for implementation into different string lengths at both 250 kHz and 500 kHz. Here, the self-inductance of the solar cell string is not included in this analysis and we assume one inductor per string. Moreover, it is assumed that the inductor is implemented with the highest possible solar cell string length, as long as it is able to suppress the ripple current below 20% at STC.

3. For each combination of an inductor and a given solar cell string, we can calculate the ohmic losses in the inductor. The ohmic losses are based on the DC current, as well as on the AC ripple current. The method for calculating power losses in the inductor is described in Appendix D. Finally, we express the inductor ohmic losses as a fraction of power generated in the solar cell string.

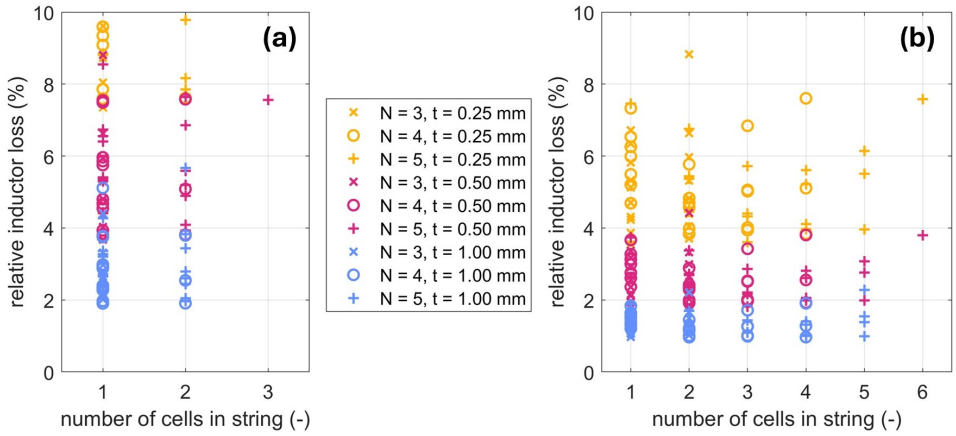


Figure 6.6: Feasibility for inductor integration at (a) 250 kHz and (b) 500 kHz. All inductors have d = 12.5 cm, but comprise different numbers of turns (3, 4, 5), gap sizes (1 cm - 8 cm), spacings (1 mm, 3 mm, 5 mm) and thicknesses (0.25 mm, 0.50 mm, 1.0 mm). The losses are calculated under the assumption that the solar cell (string) is operating at the maximum power point in STC.

Figure 6.6 presents the results of the feasibility analysis, showing the relative ohmic inductor losses as a fraction of the power generated in the solar cell string for various string lengths. Figure 6.6(a) shows the analysis at 250 kHz, whereas 6.6(b) illustrates the analysis at 500 kHz.

First of all, it follows from Figure 6.6 that there is potential to integrate planar air-core inductors at the sub-module level to facilitate embedded power electronics. However, when comparing Figure 6.6(a) and 6.6(b), it is evident that the lowest relative losses in the inductor are around 2% at 250 kHz, whereas they decrease to around 1% at 500 kHz. This occurs because as the frequency increases, a given inductor geometry compatible with a higher string length, thereby reducing the relative losses in the inductor. This shows the importance of switching frequency as well as the number of series-connected cells for the feasibility assessment. It is worth noting that in both Figure 6.6(a) and 6.6(b), the strings with the highest number of cells have only a few data points. This is because only a few of the simulated geometries have sufficient inductance to suppress the ripple to the desired level at these combinations of frequency and input voltage.

Moreover, the scattered data throughout the plots indicate that optimizing inductor parameters, such as the number of turns, spacing, and gap size, plays a crucial role in achieving the optimal design. Generally, it appears that inductors with a relatively low spacing of 1 mm achieve the lowest relative losses. This is because the DC losses are higher than the AC ohmic losses; typically, the AC losses only constitute a few percent of the total ohmic losses in the inductor. Additionally, the thickness t is a key factor in achieving the desired level of ohmic losses. For instance, at 500 kHz the lowest relative losses are approximately 4% at 0.25 mm thickness, 2% at 0.50 mm thickness, and 1% at 1.0 mm thickness. It is also worth noting that for both 250 kHz and 500 kHz, the lowest relative inductor loss remains fairly constant across different string lengths.

However, no conclusive statements can be made about whether these loss factors

are 'good enough.' Adjustments to certain assumptions can significantly alter the data in Figure 6.6. For instance, operating at higher frequencies or allowing a higher ripple current level would permit a lower minimum inductance. This would enable the use of an inductor with fewer turns and lower thickness, or the same inductor for a longer string length. Moreover, it is ultimately up to the power electronics designer to determine the desired converter efficiency, size, and cost. Nevertheless, this feasibility analysis provides a general indication of the potential role that planar air-core inductors can play in sub-module power converters. Overall, this study demonstrates that planar air-core inductors have the potential to be implemented into PV modules, enabling the removal of the inductor from the power converter. However, it is important to acknowledge that in most cases this requires that (1) the converter has a high switching frequency of multiple hundreds of kHz and (2) the inductor thickness is at least multiple hundreds of micrometer. Although the focus of this study is not on manufacturing, it must be noted that the required inductor thickness range surpasses the capabilities of screen printing, the primary technique employed by the PV industry for solar cell metallization [264]. Hence, alternative manufacturing methods should be explored for the planar inductor, such as cutting or etching copper foil [265], or utilizing a form of additive manufacturing [266, 267]. These conditions present significant challenges for this solution to be widely adopted in the PV market. Nevertheless, this study can serve as a foundation for further research. For instance, it could be worthwhile to study the implementation of planar inductors in combination with leveraging the self-inductance of solar cells, thereby reducing the minimum inductance requirements from the inductor. Additionally, the high-frequency properties of the inductor could be enhanced by using alternative track structures, such as multitrack or Litz wire designs [262]. Moreover, multiple inductors per string could be considered. Another approach could involve increasing inductance by utilizing planar inductors with ferromagnetic core material, potentially reducing the required number of turns and thickness. Furthermore, practical issues must be addressed if feasible combinations are identified. For example, thermal management and electromagnetic interference will need to be carefully considered in real-world applications.

6.5. Conclusion

In this chapter, it was investigated whether copper planar air-core inductors with an area of 12.5 cm × 12.5 cm can yield the required inductor properties to support sub-module power conversion in PV modules. First, it was shown how the interplay between the different design parameters, such as track spacing, track width, number of turns, and middle gap size, play an important role in the inductor properties. This analysis includes changes due to high-frequency effects, which significantly impact the results. Specifically, it was shown that a minimum track spacing of a few millimeters is necessary to limit the proximity effect at frequencies of 50 kHz and above. Additionally, it was observed that increasing the middle gap size or the number of turns can enhance the inductance, though both approaches come with the drawback of increased inductor resistance.

The coil geometries that were simulated yield inductance values between 0.3 μH and 3.2 μH. The feasibility of implementing these inductors into an exemplary DC-DC boost converter was evaluated. To adequately reduce the current ripple from a solar cell string

with such inductance values, a significant switching frequency of at least several hundred kHz is required. Moreover, at 500 kHz, an inductor thickness of around 0.5 mm is necessary to keep the ohmic losses in the inductor below 2% of the total generated power in standard test conditions. While demonstrating feasible combinations, these findings also present significant challenges for the sub-module integration of air-core planar inductors. For future research, several proposals were made to improve the inductor properties. These include incorporating ferromagnetic core materials or leveraging the self-inductance of the solar-cell string. Additionally, practical issues such as thermal management and electromagnetic interference will need to be carefully addressed in real-world applications.

7

COmbined Solar cell and MOSFET (COSMOS) devices

This chapter is based on the following publication:

D. A. van Nijen, T. Stevens, Y. Mercimek, G. Yang, R. A. C. M. M. van Swaaij, M. Zeman, O. Isabella, and P. Manganiello, "Combined Fabrication and Performance Evaluation of TOPCon Back-Contact Solar Cells with Lateral Power Metal-Oxide-Semiconductor Field-Effect Transistors on a Single Substrate", in *Solar RRL*, vol. 8, 2300829, 2024.

7.1. Introduction

This chapter focuses on the integration of transistors into PV cells. Transistors are crucial for power converters as well as reconfigurable modules, and can act as bypass elements with low parasitic power dissipation. Previously, researchers proposed a fabrication process integrating MOSFETs and capacitors with front-back contacted PV cells [76, 197, 198]. Although they made some innovative steps towards cell-embedded power converters, the PV cell structure has some intrinsic limitations to reaching a high efficiency, which are for instance the non-textured front side and an aluminium plate covering the full back-side of the device. In this current work, we introduce the COSMOS device, denoting COmbined Solar and MOSFET. Specifically, we report the simultaneous manufacturing of lateral power MOSFETs and interdigitated back contact (IBC) c-Si solar cells with ion-implanted poly-Si passivating contacts on a single c-Si substrate. The adoption of the Tunnel Oxide Passivated Contact (TOPCon) cell architecture ensures that the solar cell can attain state-of-the-art efficiencies. Moreover, a substantial number of processing steps are common to both devices, promoting cost-effective integration of the MOSFET. It is worth highlighting that the proposed device structure places all contacts of both the solar cell and the MOSFET on the back side of the wafer. This offers design flexibility in terms of the number of transistors and the series or parallel interconnection schemes that may be required for different applications. The devices are characterized in both dark and illuminated conditions, and based on these results

we reflect on the remaining challenges for real-world implementation. Additionally, we investigate how the performance of the MOSFET is influenced when its drain or source has a direct monolithic connection to the solar cell.

7.2. Process flow description

First, a reference process flow for solar manufacturing is outlined in section 7.2.1, drawing from prior research. Building upon this, section 7.2.2 introduces a process flow for COSMOS devices, which unifies MOSFET fabrication with the aforementioned solar cell manufacturing in a single combined process. For reference, labels ranging from P1 to P6 are used in both sections to designate every lithographic step. In this work, the photolithographic patterning steps are performed using the soft contact method with a SUSS MicroTec MA/BA8 mask aligner. Although this method allows for UV patterning at once for the full area of the wafer, it offers limited resolution, typically above 1 μm, as compared to image-projection photolithography [268, 269]. Furthermore, it is worth noting that a *standard cleaning procedure* is performed between various steps of the process flows to prevent cross-contamination between processing tools. Although the cleaning procedure is not always mentioned explicitly, it plays an important role in ensuring the quality of the fabricated devices. The cleaning procedure consists of (i) HNO_3 (99%, room temperature) dip for 10 minutes, followed by rinsing in DI water for 5 minutes, then (ii) HNO_3 (69%, 110 °C) dip for 10 minutes followed by rinsing in DI water for 5 minutes. Finally, in section 7.2.3 some manufacturing limitations are discussed along with some trade-offs inherent to the combined manufacturing. In this work both n-type and p-type double-polished float-zone wafers are used with a thickness of 285 μm, and having <100> orientation and resistivity of 1-5 Ωcm.

7.2.1. Reference Solar Cell Manufacturing

Figure 7.1 illustrates the reference solar cell manufacturing process, serving as the foundation for this study. Please note that this flowchart was not executed in the current work and therefore does not provide as much detail as the process described in the next section (Section 7.2.2). More comprehensive insights into the processing of these IBC solar cells are available in previous publications [191, 192, 270]. In brief, the fabrication procedure involves the following key steps:

I After the formation of alignment markers (P1), the native oxide is removed by an HF dip. This is directly followed by the formation of a tunneling oxide. Subsequently, a 250-nm thick intrinsic amorphous silicon (i-a-Si) layer is deposited using low-pressure chemical vapor deposition (LPCVD).

II Using two separate photolithographic patterning steps (P2 & P3), phosphorus and boron are locally implanted into the i-a-Si layer to create the emitter and back-surface field (BSF) regions.

III A trench is etched between the BSF and emitter regions by wet-etching a photolithography-patterned protective layer on top of both BSF and emitter (P4). Furthermore, the etching step removes the i-a-Si layer on the front side.

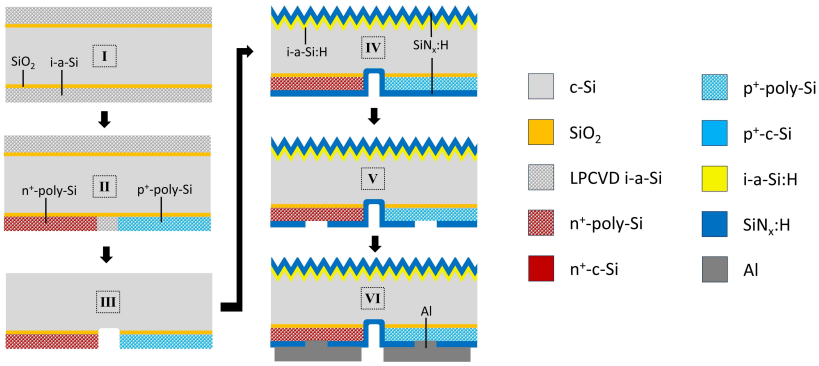


Figure 7.1: Reference process flow for IBC solar cells based on an etch-back process [192]. The back-side structure consists of ion-implanted poly-Si passivating contacts.

IV The front side of the wafer is textured. Subsequently, a lightly-doped front surface field (FSF) implantation may be performed (not sketched in Figure 7.1), followed by a high temperature annealing step to activate and drive-in the dopants. Next, using plasma-enhanced chemical vapour deposition (PECVD), an i-a-Si:H / SiN_x:H stack is deposited for passivation and anti-reflection purposes. Furthermore, a PECVD SiN_x:H layer is added on the back side.

V Backside openings are etched in the SiN_x:H layer using BHF etching (P5).

VI Finally, a metallization step is performed using lift-off (P6), which may be followed by a hotplate annealing step.

Using the above process, an IBC solar cell efficiency of 23.0% has been demonstrated [192]. Beyond this particular process flow, TOPCon technology in front/back-contacted architectures has yielded state-of-the art solar cell efficiencies of 26.4% on n-type wafers and 26.0% on p-type wafers [271, 272]. Furthermore, a 26.1% efficiency has been demonstrated in an IBC structure [273]. Although the term TOPCon is commonly used, tunneling through the oxide is not the only current transport mechanism [274]. Thus, the same structure is regularly referred to with the term polycrystalline silicon on oxide (POLO).

7.2.2. COSMOS process flow and wafer layout

The process flow used for the fabrication of the COSMOS device is schematically represented in Figure 7.2. This figure shows the fabrication process using a p-type wafer, resulting in p-TOPCon devices and n-channel MOSFETs. The same process can be dually applied to n-type wafers, resulting in the creation of n-TOPCon devices and p-channel MOSFETs. Both options were fabricated in this study. The different steps involved in the COSMOS process are as follows:

I The first step is to form a 54-nm thick SiO_2 layer through thermal oxidation at 1000 °C. This layer will eventually become the gate oxide, meaning that it must be sufficiently thick to insulate the substrate from the gate metal. Subsequently, using a

patterning step (P1) and a 1:7 buffered HF solution (BHF), this oxide is selectively removed in the area where the solar cell will be located.

II The native oxide is removed by a dip in 0.55% HF for four minutes, where it is worth noting that this also slightly etches the gate oxide, which reaches a thickness of ~40 nm. Directly after, a ~1.5-nm thick SiO_2 layer is formed by the method of Nitric Acid Oxidation of Silicon (NAOS) [270]. A NAOS procedure follows the same steps as described for the *standard cleaning*, only both HNO_3 dips are performed for 15 minutes to ensure uniformity of the oxide.

III A 250-nm thick intrinsic amorphous silicon (i-a-Si) layer is deposited using LPCVD, which is done in a Tempress LPCVD tube furnace at a temperature of 580 °C, a SiH_4 gas flow of 45 sccm, a pressure of 150 mTorr, and a deposition rate of 2.2 nm/min. After the deposition, an annealing step at 600 °C for 1 hour is performed.

IV The back side of the wafer is protected by a temporary PECVD SiO_x layer. Then, the poly-Si on the front side is removed by a wet poly-etch solution, which consists of 48% HNO_3 and 0.75% HF, resulting in an etching rate of 200-300 nm/min. Subsequently, the front side of the wafer is textured in 4% TMAH with a 2% Alkatex 8 additive at 80 °C for 12 minutes. Afterwards, the SiO_x layer on the back side is removed using BHF.

V Now the textured front side is protected by a PECVD SiO_x layer. Using a patterning step (P2), the poly-Si on the back side is selectively removed. This has a double purpose. First, a trench is created in the PV area between the emitter and BSF region. Second, in the MOSFET area the gate structure is created. It is worth noting that this etching step has been done in two different ways, namely (i) a wet poly-etch using PECVD SiO_2 as a mask, and (ii) reactive ion etching using photoresist as a mask. Subsequently, for both these methods a BHF etching step removes the oxide that remains in the MOSFET region underneath the etched poly-Si as well as the SiO_x layer on the front side.

VI Using photoresist as a mask (P3), an implantation is performed to simultaneously create (i) the emitter region of the solar cell and (ii) the gate, source and drain region of the MOSFET. All implantations are carried out with a consistent tilt angle of 7° and a rotation of 22°. For the phosphorous implantation, the parameters are set at an energy of 20 keV and a dose of 6×10^{15} ions·cm^{-2}. In the case of boron implantation, the energy and dose are configured at 15 keV and 5×10^{15} ions·cm^{-2}, respectively [191].

VII Using photoresist as a mask (P4), an implantation is performed to simultaneously create (i) the BSF region of the solar cell and (ii) the doped region underneath the grounding contact of the MOSFET. Subsequently, a 5-minute thermal anneal is performed at 950 °C to drive-in and activate the dopants. This is done in a Tempress tube furnace in an N_2 and O_2 environment at a gas flow rate of 6000 sccm and 100 sccm, respectively. The ramping rate for heating or cooling is 10 °C/min.

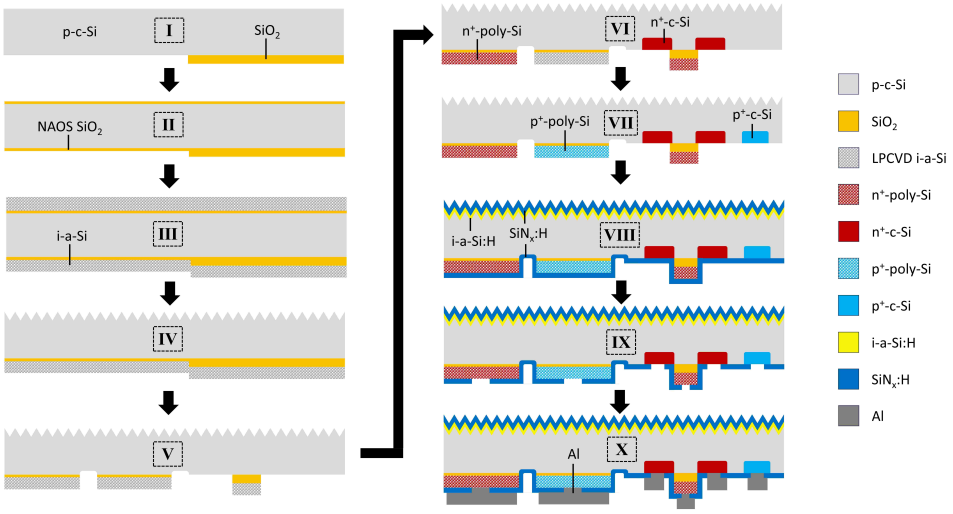


Figure 7.2: Combined Solar cell and MOSFET (COSMOS) process flow.

VIII An HF dip is performed to remove the native oxide. Subsequently, a 5-nm thick i-a-Si:H / 60 nm-thick SiN_x:H stack is deposited through PECVD on the front side for passivation and anti-reflection. Furthermore, a 100 nm-thick SiN_x:H PECVD layer is deposited on the back side.

IX Using photoresist as a mask (P5), openings are created in the SiN_x:H layer on the backside through wet etching in BHF.

X Lift-off is used to form the back side metal pattern with a 2-μm thick evaporated Al layer (P6). This may be followed by a hotplate annealing step at 350 °C for 5 minutes.

Step I of the COSMOS process requires the formation of a local gate oxide to successfully manufacture the MOSFETs. This is the main step that applies uniquely to the MOSFET and does not benefit the solar cell. However, it is worth noting that the corresponding lithographic step can directly be used to create alignment markers on the wafer. Thus, when comparing the combined process flow in this section to the solar cell manufacturing from section 7.2.1, they exhibit an equal number of photolithographic patterning steps. As such, compared to the solar-cell manufacturing, the COSMOS process requires only a very limited number of additional fabrication steps, allowing for cost-effective integration of the MOSFET.

Furthermore, it is worth discussing some aspects related to the MOSFET manufacturing. The employed COSMOS fabrication method consists of a so-called *gate-first* process, in which the gate structure is crafted before the source/drain regions. This is in contrast to the *gate-last* process, which follows the opposite sequence. One notable advantage of the *gate-first* approach is its self-aligned nature, which means that the entire poly-Si gate region, including the source and drain regions, is implanted simultaneously. As poly-Si is being doped, the SiO_2-poly-Si structure simultaneously serves as a natural

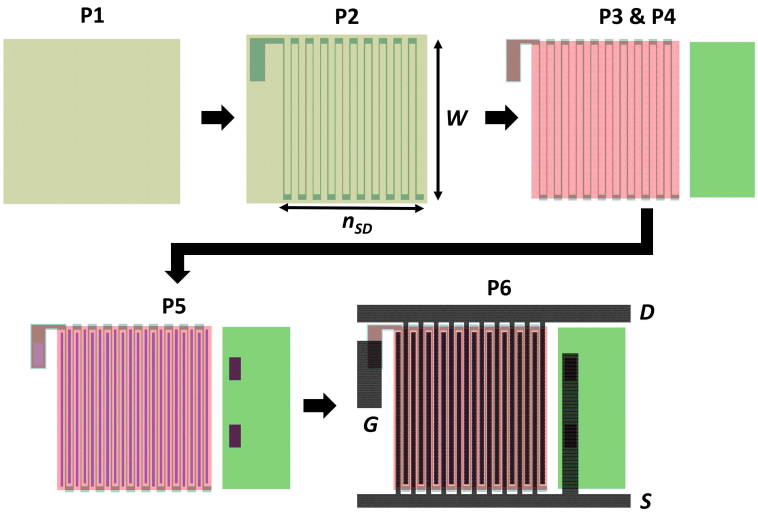


Figure 7.3: MOSFET fabrication patterning. P1: gate-oxide formation; P2: channel definition; P3&P4: implantations; P5 contact openings; P6: metallization. The MOSFET in this figure contains ten parallel source/drain couples (n_{SD}), a channel legnth (L) of 4 μm, and has a width (W) of 0.7 mm. For the devices that were manufactured in this study, n_{SD} was varied between 1 and 10, the W between 1 and 5 mm, and L was fixed at 4 μm. The MOSFET source/drain fingers have a breadth of 20 μm, and are placed over 10 μm-wide contact openings.

mask to protect the channel region during implantation. Consequently, this allows for only a small overlap between the source and drain regions with the gate structure compared to the *gate-last* method, where mask design misalignment tolerances necessitate greater overlap. Additionally, it is worth noting that the *gate-last* method might not be easily compatible with solar-cell manufacturing. In the *gate-last* method, the formation of the thermal gate oxide occurs towards the end of the process, which could potentially affect the passivation of the solar cell.

A close-up of the photomasks used in the COSMOS process is depicted in Figure 7.3 for the MOSFET fabrication part and in Figure 7.4 for PV manufacturing part. It is important to note that these figures are intended to illustrate the device structures, so the dimensions may be slightly modified compared to the actual masks. Furthermore, the labels P1-P6 in both figures correspond to the lithographic steps detailed earlier in this section. The final wafer layout is depicted in Figure 7.5. This wafer contains ten solar cells, with four of them being monolithically integrated with a MOSFET. This monolithic integration implies that either the source or drain contact of the MOSFET has a direct connection to one of the solar cell contacts. Additionally, on the bottom two rows of the wafer, there are fourteen MOSFETs present with varying geometries.

7.2.3. Manufacturing limitations and trade-offs

For achieving optimum MOSFET performance, utilizing a MOSFET with a small gate length is advantageous. For instance, a small gate length leads to a lower channel re-

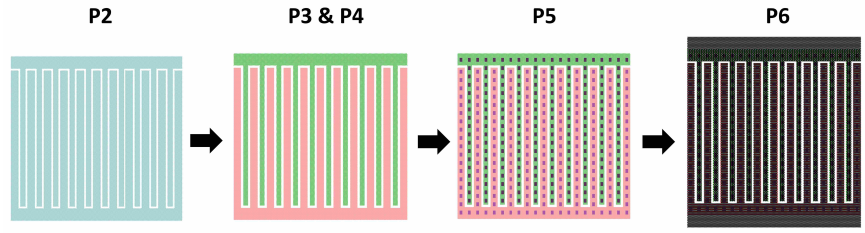


Figure 7.4: PV fabrication patterning. P2: IBC pattern definition; P3&P4: implantations; P5 contact openings; P6: metallization. The cells have a pitch size of 520 μm, consisting of an emitter finger width of 290 μm, a BSF finger width of 190 μm, and trenches of 20 μm between the p- and n-type fingers. The contact openings underneath the metal fingers have a dimension of 100 μm × 50 μm.

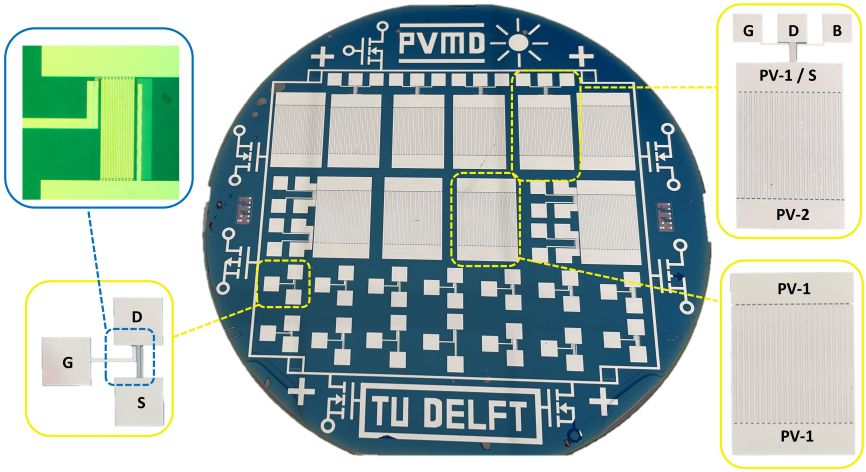


Figure 7.5: Final wafer layout. The Source, Drain, Body, and Gate contact pads of the MOSFETs are labeled as S, D, B, and G, respectively. For the individual MOSFET structures on the bottom two rows, there is no separate body contact, since the body is shorted to the source. Additionally, the contact pads for the IBC solar cells are marked as PV-1 and PV-2. In the top right, a structure is highlighted where the solar cell and MOSFET are monolithically integrated. For the MOSFETs with such monolithic interconnections, the source has a direct connection to the PV contact. Additionally, the body has an independent contact pad (B) and is not shorted to the source. This configuration allows for the interchange of source and drain contacts.

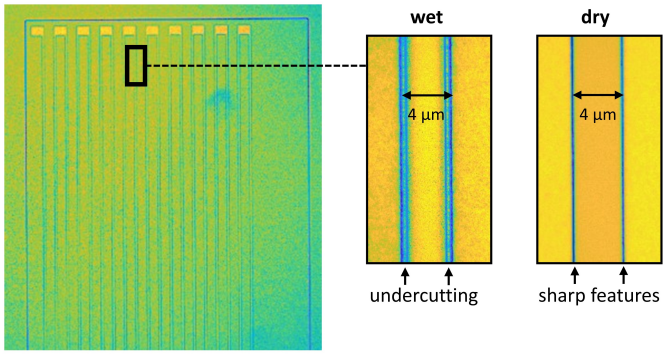


Figure 7.6: Microscope picture of the SiO_2-poly-Si gate structure after two minutes of wet etching and after dry etching, which is at the end of step V in Figure 7.2. The poly-Si wet etchant has an etching rate of 200-300 nm/min, resulting in up to ~500 nm of undercutting on both sides of the gate structure after two minutes of etching. This figure demonstrates that dry etching produces sharper features with less undercutting.

sistance in the *on*-state, as will be explained further in section 7.3.3. During fabrication performed preliminary to this work, it was observed that with the employed contact photolithography method, gate lengths as small as 4 μm could be reliably transferred onto the photoresist while maintaining the desired pattern. For masks with even smaller gate lengths, instances were noted where portions of the gate structure were not accurately transferred. This occurrence is likely attributed to diffraction effects at the edges of the mask features during the exposure process [168]. As a result, all MOSFETs presented in this study maintain a consistent gate length of 4 μm. Nevertheless, it is important to highlight that a substantial reduction in gate length could be realized through the utilization of the more advanced method of image projection photolithography, using an optical lens between the mask and the wafer [268]. However, such a reduction would bring its own challenges. For instance, an obstacle could arise in patterning the SiO_2-poly-Si gate structure during step P2, where different wafers are subjected to either wet or dry etching of poly-Si. In Figure 7.6 a microscope picture is presented of the MOSFET structure after the etching step. It becomes apparent that in the case of wet etching there is significant undercutting of the mask, effectively reducing the gate length. Since in this work a rather large gate length of 4 μm is employed, the wet etching's undercutting impact was tolerable. On the one hand, for gate length downscaling, the enhanced control of dry etching might be essential. Indeed, low-temperature dry etching is the preferred method for transistor fabrication, since it allows for high-resolution pattern transfer to the underlying layer with less undercutting than for wet etching steps [168]. On the other hand, reactive ion etching (RIE) has been reported to lead to reduced passivation quality in solar cells [169, 275]. For solar cells, etching methods such as wet etching and atmospheric pressure etching are preferred [169, 276]. Thus, the choice between wet and dry etching of the poly-Si is a trade-off that is studied in this work. Specifically, the wafers in this work are split up between different etching method and times. For the COSMOS devices manufactured in this study, the variations in the poly-Si etching process are presented in Table 7.1.

Table 7.1: Poly-Si etching details used for the different wafers in this study. N-D and N-W represent n-type wafers subjected to dry and wet poly-Si etching, respectively. P-D and P-W denote p-type wafers undergoing dry and wet poly-Si etching, respectively.

	n-type wafer dry etching (N-D)			n-type wafer dry etching (N-D)					p-type wafer dry etching (P-D)	p-type wafer dry etching (P-D)		
ID	1	2	3	1	2	3	4	5	1	2	3	5
etching time	-	-	-	1m 20s	1m 40s	2m	2m 30s	3m	-	1m 40s	2m	3m

Another challenging factor linked to the pursuit of gate length reduction is the high-temperature thermal annealing during step VII of the COSMOS process, as detailed in section 7.2.2. This step serves to drive-in and activate the dopants, meaning that the implanted atoms diffuse through the lattice. However, maintaining adequate spacing between the source and drain regions on either side of the channel becomes crucial. Limited spacing risks source-drain shorting or punch-through effects, discussed further in section 7.3.2. While this specific annealing step did not induce these effects in this study, extensive gate length downscaling could necessitate re-optimization of the annealing process to align with the thermal budget of the MOSFET.

Furthermore, a notable trade-off was observed during the fabrication process of COSMOS devices. In the final step, specifically during step X outlined in section 7.2.2, a hotplate annealing procedure can be conducted. This step proved vital for stable MOSFET performance, as elaborated in section 7.4.1. Interestingly, it slightly improved the STC efficiencies for n-type solar cells, but had a detrimental effect on p-type cells. This example highlights a trade-off where a specific step enhances MOSFET performance but diminishes PV performance. Though optimization was not pursued within the scope of this work, such steps would ideally require a refined fabrication approach that carefully manages this trade-off.

7.3. Theoretical Background

This section describes some fundamental MOSFET parameters. Furthermore, it is discussed how the desired parameters are achieved, and the inherent limitations that arise from the chosen design are explained. Further theoretical explanations and equations underlying this section are provided in Appendix C.1.

7.3.1. Threshold voltage

The threshold voltage V_T is an important characteristic of a MOSFET, representing the gate-to-source voltage V_{GS} at which a conductive channel forms beneath the gate. Through deliberate design, a particular V_T can be achieved for a given device. It is important to realize that in the case of an n-channel MOSFET (NMOS) on a p-type substrate, the device is off when $V_{GS} < V_{TN}$, and the device is on when $V_{GS} > V_{TN}$. In the case of a p-channel MOSFET (PMOS) on an n-type substrate, the device is off when $V_{GS} > V_{TP}$, and the device is on when $V_{GS} < V_{TP}$. The threshold voltage of a MOSFET is primarily influenced by parameters such as the substrate dopant density, charge trapped around the oxide-semiconductor interface, oxide thickness, and the specific

choice of gate metal, resulting in a particular metal-semiconductor work function difference. While MOSFETs are typically engineered to possess specific threshold voltages, our approach in this study diverges from convention. The central focus here is the integration of the MOSFET with minimal processing steps. The devices fabricated in this study are placed directly onto the wafer bulk, allowing for simple integration with PV cells. This encompasses both NMOS devices on p-type substrates and PMOS devices on n-type substrates. While in solar cells there is a certain flexibility in the choice of substrate dopant density [73], it is important to acknowledge that for COSMOS devices the choice of substrate has an important effect on certain transistor characteristics, such as the threshold voltage. To achieve better control over the MOSFET characteristics, techniques like epitaxial layer growth or localized doping adjustments through implantation could be considered. However, at this stage of the study such steps were not included.

7.3.2. Blocking capability

Another important characteristic of a power MOSFET is the blocking capability, which is the extent to which the MOSFET is able to block the voltage between drain and source. This characteristic comprises two primary aspects.

Firstly, during the device's *off*-state, it is crucial for the MOSFET to exhibit low drain leakage current or subthreshold conduction. Lower leakage currents lead to reduced losses, increasing overall efficiency. An important mechanism that can be responsible for drain leakage current in the *off*-state is band-to-band tunneling in the gate-to-drain overlap region [277, 278]. In addition to this, it has been reported that traps around the Si-SiO_2 interface induce further leakage currents [279].

Secondly, any MOSFET is susceptible to a drain-to-source breakdown beyond a specific applied drain-to-source voltage V_{DS}. The voltage at which this occurs is called the breakdown voltage V_B, and has a direct impact on its prospective applications within a PV panel. Given that the voltage of a PV cell string scales linearly with the quantity of series-connected cells, the MOSFET breakdown voltage imposes a restriction on the number of series-connected cells that the device can effectively manage. There are various mechanisms that can cause breakdown in a MOSFET once a certain V_B is exceeded, among which are dielectric breakdown, avalanche breakdown, or punch-through breakdown. Which mechanism is limiting depends on the specific device design. It is important to acknowledge that the chosen MOSFET design in the COSMOS devices has limitations in achieving a high breakdown voltage. Firstly, there is an overlap between the gate plate and drain region, which means that the onset of avalanche breakdown happens at a lower voltage [200]. Morover, to avoid the occurrence of avalanche breakdown, it becomes imperative to utilize a substrate dopant density that is sufficiently low. Nonetheless, within the context of the utilized MOSFET design, such an approach can give rise to punch-through breakdown, necessitating the imposition of a minimum channel length. In contrast, specific power MOSFET designs do not have overlap between the gate plate and drain region and they manage to circumvent the trade-off between V_B and channel length [202]. However, this comes at the cost of an increase in the number of fabrication steps, which is not aligned with the objectives of this work. Nevertheless, the limited maximum V_B of the MOSFETs does not prohibit usage in applications with constrained

voltage requirements. For example, integration into PV modules at the sub-module level could remain a viable option, particularly when controlling only a limited number of series-connected cells.

7.3.3. *On*-resistance

An important characteristic of a power transistor is its resistance in the *on*-state, commonly referred to as the *on*-resistance R_{on}. Presence of any parasitic resistance in the *on*-state leads to ohmic losses during operation, meaning that the R_{on} should be as low as possible for maximum efficiency. The primary contributor to R_{on} is often the channel resistance. In the linear operational region, the channel resistance R_{CH} of an NMOS can be expressed as shown in [114]:

$$R_{\text{CH}} = \frac{L}{W \mu_n C_{\text{ox}} (V_{GS} - V_{TN})} \tag{7.1}$$

where L denotes the channel length, W is the channel width, and μ_n represents the electron channel mobility. In contrast to the threshold voltage and blocking capability, the control over R_{on} is achieved through mask design within the scope of this work. Furthermore, it is worth mentioning that the mobility in silicon is almost three times higher for electrons than for holes [114]. Consequently, an NMOS with equal geometry when compared to a PMOS will yield a lower R_{CH}, which often makes NMOS devices the preferred choice for power applications.

Although Equation 7.1 shows an inverse relationship between the device width and R_{CH}, it is important to acknowledge that there can be non-ideal effects at play in power MOSFETs. One notable effect is the increasing prominence of power dissipation within metal fingers and interconnections as device width increases, which is an aspect referred to as the *scaling issue* [176]. To reduce losses due to the scaling issue, lateral power MOSFETs often employ a design that incorporates multiple source-drain couples in parallel, sharing a common gate [76, 202]. In the context of the current study, devices are fabricated with varying widths and different numbers of parallel source-drain couples (n_{SD}), allowing for an analysis and quantification of the scaling effect. Specifically, for the devices manufactured in this study, n_{SD} was varied between 1 and 10, the W between 1 and 5 mm, and L was fixed at 4 μm. This approach allows to find the most efficient way to reduce R_{on} in the COSMOS devices.

7.4. Results and Discussion

This section presents the results that were obtained for the manufactured COSMOS devices. Initially, section 7.4.1 exhibits the outcomes of the fabricated MOSFETs. The transistors are characterized using a Cascade Summit 12000 probe station connected to a Keysight B1500A Semiconductor Parameter Analyzer. Subsequently, in section 7.4.2, the solar cell results are detailed. The current-density voltage (J-V) characteristics of the solar cells are measured using a continuous solar simulator (Wacom WXS-156S AAA). The solar cells, which have areas varying between 1.22 cm^2 and 1.29 cm^2, are exposed through masks that feature 1cm × 1cm apertures in the solar cell regions. Finally, in section 7.4.3, the challenges related to achieving effective device performance for successful integration are explored.

7.4.1. MOSFETs

An annealing step after the metallization is known to lead to the alteration of the localized states near the Si-SiO_2 interface [280, 281]. In the manufactured NMOS and PMOS devices, such a step resulted in more stable threshold voltages and enhanced charge carrier mobility within the channel. Thus, all MOSFET results presented in this study are for wafers that underwent a hotplate annealing step at 350 °C for 5 minutes. More information on the performed hotplate annealing experiments and its effect on the charge trapped at the oxide-semiconductor interface are given in Appendix C.2.

The leakage currents of the manufactured MOSFETs was tested, and the $I_D - V_{GS}$ characteristics of selected NMOS and PMOS devices are presented in Figure 7.7. Since the vertical axis shows I_D on a logarithmic scale, it allows for a detailed analysis of the leakage currents. First, it is important to analyze the shape of the curves in the *off*-state, which is for V_{GS} below V_{TN} of the NMOS devices in Figure 7.7(a), and for V_{GS} above V_{TP} of the PMOS devices in Figure 7.7(b). For all devices it is evident that as the device is biased deeper into the *off*-state, the leakage increases. This phenomenon has been reported in literature and is attributed to tunneling effects at the Si-SiO_2 interface in the gate-to-drain overlap region, which are sensitive to the electric field created by the applied V_{GS} [277]. Furthermore, Figure 7.7 illustrates that there can be variations in drain leakage current among devices placed on the same wafer. These differences cannot be attributed to the varying n_{SD}. Instead, they might be caused by variations in traps near the Si-SiO_2 interface between different devices. Indeed, publications suggest that that traps near the Si-SiO_2 interface significantly contribute to leakage, caused by effects such as interface trap-assisted tunneling and thermal generation current described by Shockley-Read-Hall theory [279, 282]. In general, upon analysing the drain leakage current of the devices across the different wafers, it can be concluded that the *off*-state drain leakage currents for the manufactured PMOS devices are notably lower than those for the NMOS devices. In this study, relatively well-performing NMOS devices have a leakage current of approximately $\sim 2 \times 10^{-5}$ A at $V_{DS} = 0.1$ V, whereas the PMOS devices display leakage currents of around $\sim 1 \times 10^{-10}$ A at $V_{DS} = -0.1$ V, which is a remarkable factor of 2×10^5 lower. This disparity between NMOS and PMOS leakage current is not yet fully understood and can have different reasons. For instance, it could be related to the more graded boron doping concentration of PMOS devices near the drain-to-substrate junction compared to phosphorus doping concentration in NMOS devices, which may reduce band-to-band tunneling effects [283]. Additionally, variations in trap concentration at the Si-SiO_2 interface between n-type and p-type wafers might contribute to the observed difference. Although not further explored in this work, it is expected that optimization of the implantation and thermal annealing steps during the fabrication process could lead to more stable leakage currents across different devices on the same wafer and reduce the NMOS leakage currents to levels comparable to those of the manufactured PMOS devices.

Regarding breakdown voltage V_B, an analysis was conducted to determine the maximum V_{DS} voltage that NMOS and PMOS devices could withstand before reaching the point of breakdown. A stepwise increase in V_{DS} was executed to identify the specific V_B value at which I_D began to rise sharply. Frequently, the devices experienced irreversible breakdown when pushed to their limits. Figure 7.8 illustrates $I_D - V_{DS}$ curves for different

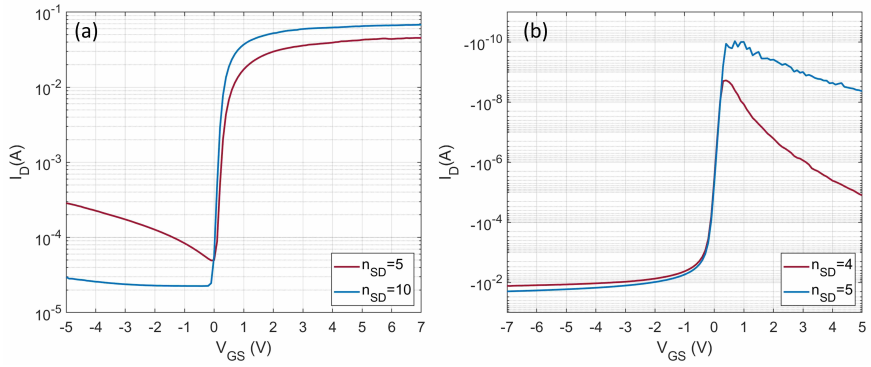


Figure 7.7: (a) $I_D - V_{GS}$ curves of two NMOS devices on wafer P-W-2 with $W = 2$ mm recorded at $V_{DS} = 0.1$ V. (b) $I_D - V_{GS}$ curves of two PMOS devices on wafer N-W-1 with $W = 2$ mm recorded at $V_{DS} = -0.1$ V.

V_{GS} values both before and after breakdown. It is evident that the NMOS device can tolerate V_{DS} up to 9 V, while the PMOS can endure a V_{DS} of 6 V prior to breakdown. Following the catastrophic breakdown, the V_B values of both devices are compromised, dropping to -1 V and -5 V, respectively. The irreversible nature of the observed breakdown makes it plausible that a form of dielectric breakdown occurred. Typically, the V_B value was observed in the range of an applied V_{DS} between 5 V and 10 V. It is worth noting that in several of the manufactured MOSFETs, the breakdown behavior was already apparent immediately after the manufacturing process, suggesting the possibility of defects that might have developed within the oxide during fabrication. The breakdown voltage V_B of COSMOS MOSFETs could potentially be elevated by adopting a higher quality or thicker gate oxide, until a point where punch-through or avalanche effects set a constraint on the breakdown effect.

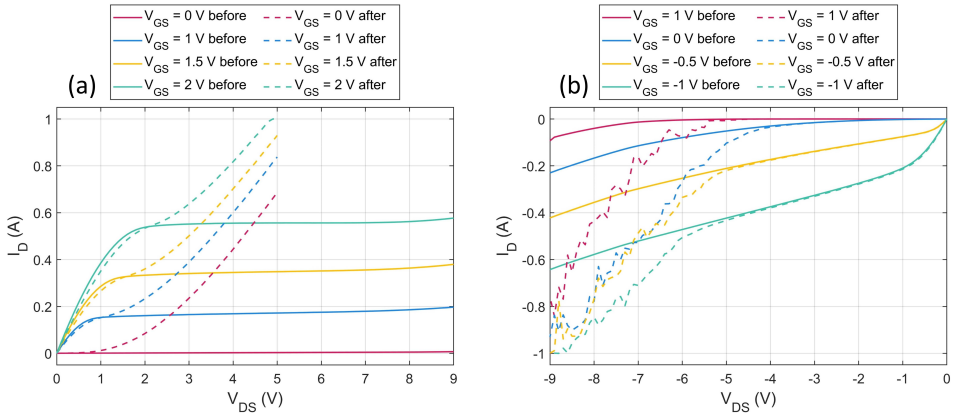


Figure 7.8: $I_D - V_{DS}$ curves for varying V_{GS} values before and after irreversible breakdown. In (a) an NMOS device from wafer P-D-1 is presented, whereas the PMOS device shown in (b) is from wafer N-W-5. Both the NMOS and PMOS have an $n_{SD} = 10$ and $W = 2$ mm device structure.

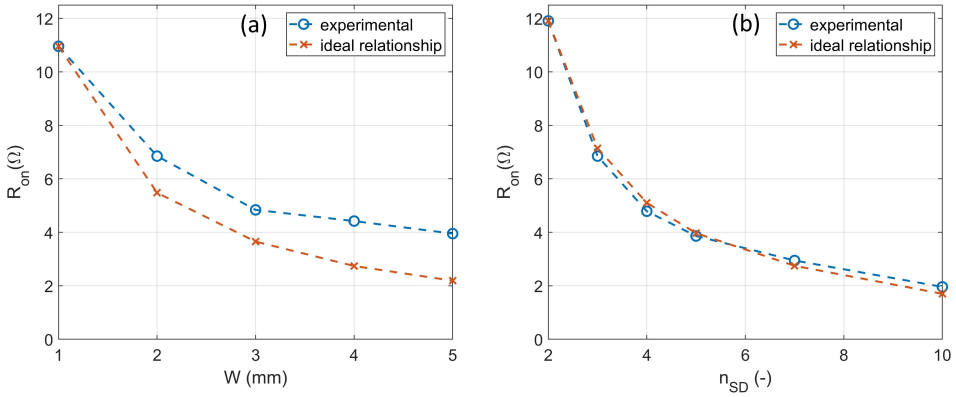


Figure 7.9: *On*-resistance for PMOS devices on a wet-etched wafer (N-W-3). The experimental R_{on} values are calculated from the slope of the $I_D - V_{DS}$ measurement between 0 V and 0.1 V at V_{GS} = -8 V. For (a), all devices have an $n_{SD} = 3$, while W is varied. The ideal relationship is based on the assumption that from $W = 1$ mm, R_{on} follows a W^{-1} relationship based on Equation 7.1. For (b), all devices have a $W = 2$ mm, while n_{SD} is varied. The ideal relationship is based on the assumption that R_{on} scales inversely with the number of parallel channels in the device, with $n_{SD} = 2$ as a starting point.

Furthermore, as previously discussed in section 7.3.3, the *on*-resistance R_{on} can be manipulated through various design-oriented MOSFET parameters. This has been examined by comparing the R_{on} of manufactured PMOS devices with different geometries, as depicted in Figure 7.9. To quantify R_{on}, we calculate its values based on the slope of the $I_D - V_{DS}$ curve, specifically within the voltage range of 0 V to 0.1 V at a fixed V_{GS} of -8 V. It is important to note that all the data points in this figure pertain to the same wafer, namely N-W-3 from Table 7.1. In Figure 7.9(a), the impact of width (W) on R_{on} is presented. According to the theoretical relationship defined by Equation 7.1, R_{on} is expected to exhibit an inverse relationship with W. However, the experimentally obtained R_{on} values deviate somewhat from this ideal relationship. Thus, the experimental results are compared with an ideal curve that assumes R_{on} follows a W^{-1} relationship starting from $W = 1$ mm. This comparison highlights that as W increases, the experimental R_{on} values decrease at a rate that is less steep than the ideal prediction. This implies that there is an increase in *on*-resistance per unit of added width. This phenomenon is likely attributed to the presence of non-zero resistance within the metal contacts of the source and drain, a concept described earlier in this study as the *scaling issue*. Another strategy for reducing the R_{on} involves manufacturing MOSFETs with a common gate, but with multiple source/drain couples in parallel (n_{SD}). Figure 7.9(b) illustrates the effect of n_{SD} on R_{on}. In addition, an ideal relationship is provided based on the assumption that R_{on} decreases linearly with the number of parallel channels in the device, using n_{SD}=2 as the starting point. In this case, the experimental results closely align with the expectations derived from this ideal relationship, particularly when compared to Figure 7.9(a). This shows that increasing the number of source-drain couples can be a more effective strategy for reducing R_{on} than increasing W. Furthermore, there appears to be room for further reduction in R_{on} by elevating n_{SD}. By employing devices with $n_{SD} = 10$ and $W = 2000$ μm, this study achieved *on*-resistances of 1.01 Ω for an NMOS device at

V_{GS} = 10 V, and 1.29 Ω for a PMOS device at V_{GS} = −10 V. The lower R_{on} values in NMOS devices compared to PMOS devices can be attributed to the higher electron mobility compared to hole mobility. This characteristic often makes NMOS devices the preferred choice for power applications.

7.4.2. Solar cells

The outcomes of the COSMOS solar cells are depicted in Figure 7.10. Different colors are allocated for p-type and n-type cells, as well as for wet and dry etching of poly-Si. Each wafer is identified on the horizontal axis using labels that correspond to those in Table 7.1. The outcomes for n-type cells are presented post hotplate annealing, while the results for p-type cells are shown prior to annealing. This distinction is due to the negative impact of hotplate annealing on the V_{oc} of p-type cells that was observed. Notably, the figure's boxplots only include functional cells on the wafer, excluding non-operational cells from the analysis. Additionally, it is important to acknowledge that the *J-V* curves of the fabricated cells often displayed unexpected irregularities or kinks in the low forward bias voltage region. This can be observed in the *J-V* curves presented in Figure 7.11. The exact cause of these kinks remains unclear. They might be associated with capacitive effects that somehow influence the measurements, shunting between n- and p-type fingers, or it is possible that the current distribution within the solar cell varies with the operating voltage.

In Figure 7.10 it can be seen that the COSMOS solar cells manufactured in this study yield STC efficiencies ranging between approximately 16% and 20%. It is shown that for both p-type and n-type cells, wet etching yields superior efficiencies compared to dry etching. This enhanced efficiency mainly stems from improvements in V_{oc} and J_{sc}. Prior research has also highlighted that reactive ion etching (RIE) can compromise passivation quality [169, 275], aligning with our findings. Although our results underscore the preference for wet etching to achieve optimal solar cell performance, it is important to consider some nuances. Firstly, the utilized dry etching equipment is a shared tool employed for various processes unrelated to solar-cell manufacturing. Hence, the observed drop in passivation quality might not be inherent to the dry etching process itself, but rather a consequence of the specific tool employed. Secondly, it is important to note that strategies exist for re-passivation after RIE [284]. However, within the scope of this study, no such re-passivation techniques were explored.

Furthermore, it is worth comparing between the outcomes of n-type and p-type solar cells. The results unveil that n-type wafers exhibit lower V_{oc} values than their p-type counterparts. Conversely, n-type solar cells show higher FF values compared to p-type counterparts. Although there is variation in efficiencies across different wafers, the achieved efficiencies for both n-type and p-type solar cells are within a similar range. The best *J-V* curves for n-type and p-type solar cells within this study are illustrated in Figure 7.11, having efficiencies of 20.29% and 20.66% respectively. Increasing the V_{oc} values by further optimization in passivation holds the potential to push the efficiency of the COSMOS solar cells closer to that of state-of-the-art TOPCon solar cells. Nevertheless, the achieved efficiencies exceeding 20% demonstrate the potential of the COSMOS process for fabricating high-efficiency solar cells.

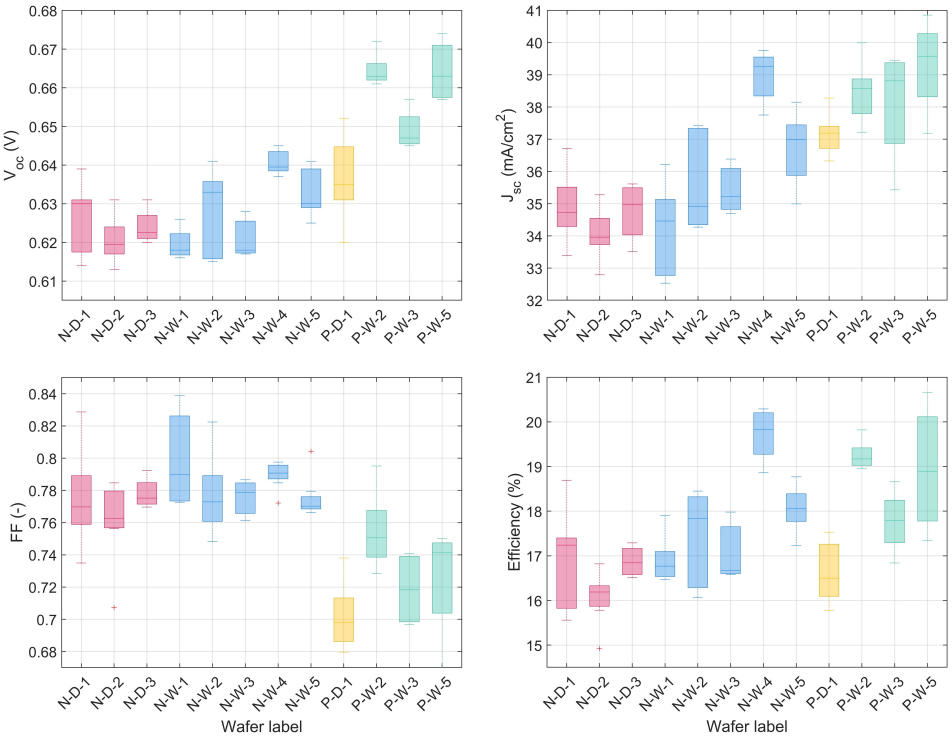


Figure 7.10: Overview of the solar cell performance in STC conditions across the various wafers. Included in the analysis are the open circuit voltage (V_{oc}), the short-circuit current (J_{sc}), the fill factor (FF), and the conversion efficiency. The results for the n-type solar cells are recorded after hotplate annealing, whereas the results for the p-type solar cells do not include this step. On each box, the central line within the box indicates the median, and the bottom and top edges of the box indicate the 25$^{\text{th}}$ and 75$^{\text{th}}$ percentiles, respectively. The whiskers extend to the most extreme data points not considered outliers, and the outliers are plotted individually as red crosses.

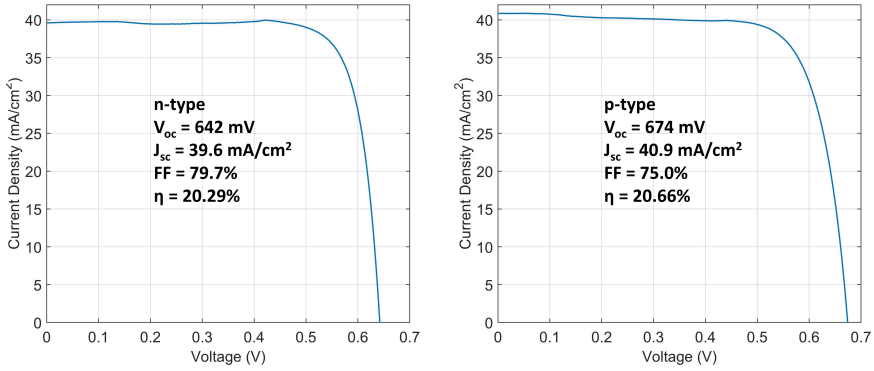


Figure 7.11: J-V curves of the cells with the highest recorded efficiency for both the n-type and p-type devices. The n-type cell is from wafer N-W-4, whereas the p-type cell is located on wafer P-W-5.

7.4.3. Integration challenges

The preceding sections examined the individual performance of MOSFETs and solar cells, each under different conditions — MOSFETs under dark conditions and solar cells under illuminated conditions. Nonetheless, given that the COSMOS approach integrates these devices onto a single substrate, additional complexities emerge. This section identifies and describes the two major integration challenges that arise from this combined approach.

For successful integration of MOSFETs into solar cells, it is important to understand how the devices respond to illumination. To this end, a comparison is made between the dark performance of the MOSFET and its behavior under illumination, with the wafer being exposed to light from the textured front side, featuring a spectrum closely resembling AM1.5 at 1000 W/m^2. This analysis is carried out using the Wacom WXS-156S AAA solar simulator. The impact of illumination on the $I_D - V_{GS}$ curves is shown in Figure 7.12. Analysis of both NMOS and PMOS devices reveals that in the *on*-state of the MOSFET, there is negligible difference between the dark and illuminated curves. However, a significant increase in drain leakage currents during the *off*-state of the device is observed for both cases when exposed to light. This increase is likely attributed to the photogeneration of free charge carriers near the channel area. Such behavior under illuminated conditions presents a challenge to the MOSFET-PV integration concept. While the most straightforward solution could involve local optical shading of the relatively small MOSFET area, this approach would result in a loss of active area on the wafer. Alternatively, more sophisticated strategies might include the creation of a local electrical barrier to prevent charge carriers from the bulk reaching the channel region of the MOSFET, thereby mitigating these photogenerated leakage currents. For instance, this could be done by introducing an inversely doped well underneath the MOSFET area, creating a different doping profile compared to the bulk of the wafer.

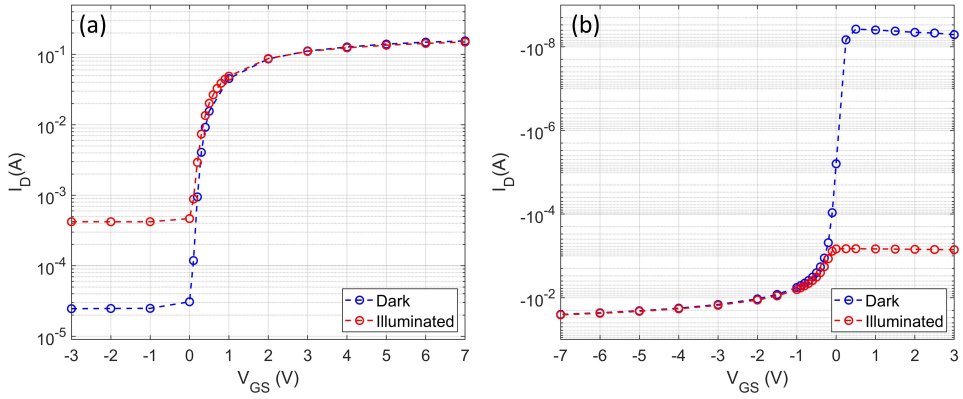


Figure 7.12: $I_D - V_{GS}$ curves in both dark and illuminated conditions, all obtained using the Wacom WXS-156S AAA solar simulator. (a) shows an NMOS device with $n_{SD} = 10$ and $W = 2$ mm on wafer P-W-2, recorded at $V_{DS} = 0.1$ V. (b) shows a PMOS device with $n_{SD} = 5$ and $W = 2$ mm on wafer N-W-4 recorded at $V_{DS} = -0.1$ V.

Additionally, it should be noted that while the COSMOS approach offers the potential advantage of monolithic integration between solar cells and MOSFETs, there is an important consideration to take into account. The bulk of the wafer can facilitate leakage currents, meaning that the establishment of monolithic interconnections requires additional considerations compared to configurations where separate discrete devices are interconnected. As depicted in Figure 7.5, the wafer layout in this study features multiple solar cells monolithically integrated with MOSFETs. In these particular MOSFETs with monolithic interconnections, the body has an independent contact pad and is not shorted to the source contact. This configuration allows for the interchange of source and drain contacts. Hence, the manufactured structures enable a direct exploration of how a MOSFET's performance is influenced by whether its drain or source has a monolithic connection to the solar cell. The study encompasses all possible connections: NMOS with source/drain connected to p^+ solar cell contact (BSF), NMOS with source/drain connected to n^+ solar cell contact (emitter), PMOS with source/drain connected to p^+ solar cell contact (emitter), and PMOS with source/drain connected to n^+ solar cell contact (BSF). The $I_D - V_{GS}$ curves for these various configurations are illustrated in Figure 7.13. Each subfigure depicts the two curves for the same MOSFET, with only the drain and source contacts swapped during the measurement. These data are obtained in dark conditions using the using the Cascade Summit 12000 probe station connected to a Keysight B1500A Semiconductor Parameter Analyzer. Furthermore, the monolithic interconnection configuration is presented next to each plot.

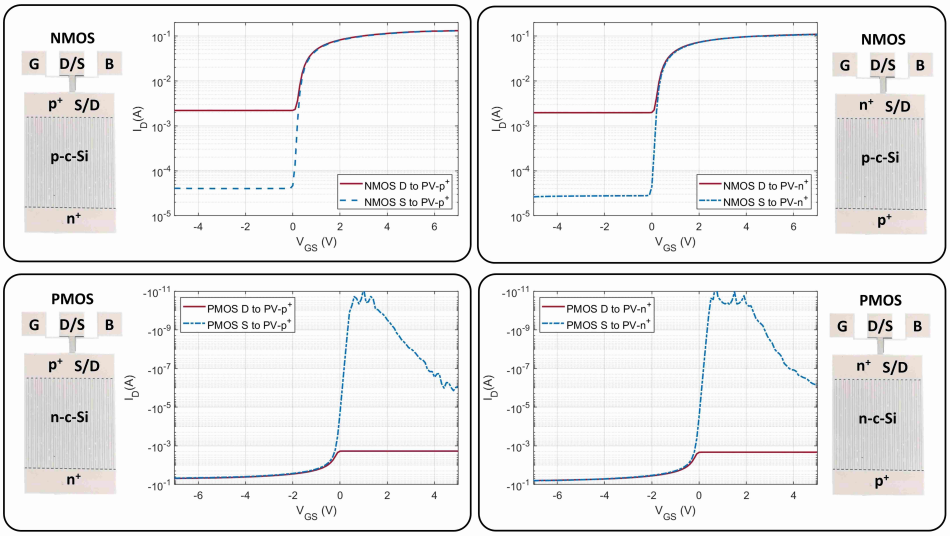


Figure 7.13: Effect of different monolithic interconnections on $I_D - V_{GS}$ curves. These curves were all measured under dark conditions, at $V_{DS} = 0.1$ V for NMOS devices, and at $V_{DS} = -0.1$ V for PMOS devices. Since the body contact is separated from the source, two $I_D - V_{GS}$ curves were recorded for each configuration: one with the source contact connected to the solar cell and the other with the drain contact connected to the solar cell.

In Figure 7.13, the performance in the *on*-state remains relatively consistent regardless of the interconnection topology. However, distinctions in leakage currents during the *off*-state are apparent among different interconnection schemes. Notably, for all topologies, the leakage currents are remarkably lower when the source is monolithically connected to the PV cell in comparison to the drain connection. This observation suggests that a monolithic connection between the drain and solar cell can introduce an unintended leakage path. Typically, a MOSFET exhibits low drain leakage in the *off*-state because the drain-substrate junction is in reverse bias. However, when the drain contact is monolithically interconnected with a solar cell contact, this introduces an additional path for the current into the substrate. Consequently, it is desirable for the device structure employed in this study to solely feature monolithic interconnections between the source and solar cell, while avoiding such connections between the drain and solar cell. To still accommodate integration topologies where the drain is connected to the solar cell, modifications to the device structure should be explored. For example, this could involve creating an inversely doped well underneath the MOSFET. This well could be biased independently of the substrate, potentially offering enhanced control over MOSFET behavior.

7.5. Conclusions

In this study, the concept of COSMOS devices was introduced and a process flow was proposed in which IBC TOPCon solar cells and lateral power MOSFETs are simultaneously fabricated on a single substrate. This process was successfully employed to manufacture both n-type solar cells with integrated p-channel MOSFETs (PMOS) and p-type solar cells with integrated n-channel MOSFETs (NMOS). Important trade-offs related to fabrication, such as the choice between dry or wet etching and the impact of hotplate annealing at the end of the process, were discussed. Notably, remarkable efficiencies exceeding 20% were achieved for both n-type and p-type solar cells, highlighting the potential of COSMOS solar cells. In addition, both NMOS and PMOS devices were successfully manufactured. In the *off*-state, NMOS devices exhibited leakage currents of approximately $\sim 2 \times 10^{-5}$ A at $V_{DS} = 0.1$ V, while PMOS devices displayed leakage currents of around $\sim 1 \times 10^{-10}$ A at $V_{DS} = -0.1$ V, a remarkable factor of 2×10^5 lower. Optimizations in the fabrication process are expected to reduce NMOS leakage currents to levels comparable to those of the manufactured PMOS devices. Moreover, the study demonstrated how the *on*-resistance of the MOSFET in a COSMOS device can be controlled by varying its geometry. Expanding the channel width is effective up to a certain point, beyond which increasing the number of source-drain couples connected in parallel becomes a more efficient strategy. The NMOS devices outperformed PMOS devices in achieving a low *on*-resistance per unit area due to the higher electron mobility compared to holes.

Furthermore, this study identified several integration challenges. Characterizing the MOSFET under illuminated conditions revealed that *off*-state leakage currents increase due to illumination. Consequently, for real-world applications of PV-integrated transistors, it is important to develop strategies to mitigate these effects. Additionally, various configurations of monolithic integration between the MOSFETs and solar cells were explored. This analysis revealed that the presence of a monolithic connection between the MOSFET drain and the PV contact leads to a higher drain leakage current as compared

to a configuration where the source is connected to the PV contact. This difference can presumably be attributed to the unintended current path introduced through the PV contact and the bulk of the wafer in the former case. Thus, the monolithic integration must be approached with care. In summary, the COSMOS approach presents promising results for advancing the smart integration of transistors in PV applications with high-efficiency cells.

8

Conclusions and outlook

8.1. Conclusions

This thesis, structured in two parts, presented findings regarding the integration of power electronic (PE) components into crystalline silicon (c-Si) solar cells.

In **Part I**, the objective was to gain a comprehensive understanding of the impedance of c-Si solar cells. To this end, **Chapter 2** reported a characterization of the impedance of eight single-cell laminates. Each laminate contained a different commercially available c-Si solar cell, featuring various cell architectures, namely Aluminium Back Surface Field (Al-BSF), Passivated Emitter and Rear Contact (PERC), Tunnel Oxide Passivated Contact (TOPCon), Interdigitated Back Contact (IBC), and Silicon Heterojunction (SHJ). It was found that the two main factors contributing to a high PN junction capacitance (C_j) at maximum power point (MPP) are (1) a low wafer dopant concentration (N_{sub}) and (2) a high MPP voltage. Furthermore, the studied cell laminates exhibit inductances between 63 and 130 nH. When comparing the inductive effects between the different laminates, it appears that the inductance decreases when the metallization structure consists of a higher number of busbars. Additionally, the geometry of the metal contacts affects the inductance. These insights into the variations in capacitive and inductive effects between different cell architectures can be useful for optimizing the design of power conditioning circuits. However, during the analysis subtle deviations were found while fitting the model to the experimental impedance data. This suggested that the employed small-signal circuit did not fully capture the underlying physics. As such, the impedance of PN junctions was further investigated in **Chapter 3**. Specifically, PN homojunction devices were investigated through Technology Computer-Aided Design (TCAD) simulations. This methodology allowed to study the junction impedance in a detailed way, which may be difficult to do experimentally due to noise and reactance of metal contacts. Through analysis of the impedance data it was revealed that the PN junction exhibits the behaviour of a parallel resistor-capacitor circuit (RC-loop) at low frequencies, but undergoes relaxation in both PN junction resistance (R_j) and C_j as frequency increases. While various publications on solar-cell impedance model the low-high (LH) junction

using an *RC*-loop, the findings presented in this chapter indicate that such a model does not accurately represent the underlying physics. Instead, this approach is likely compensating for the frequency-dependent behavior of R_j and C_j. Finally, in **Chapter 4**, the PN junction impedance of modern c-Si solar cells was studied across varying temperature and illumination conditions. In the tested conditions, the range in which the area-specific MPP R_j (in $\Omega \times \text{cm}^2$) varied was similar for different cell architectures, despite their different properties. Conversely, the range in which the areal MPP C_j varied was significantly affected by the wafer dopant concentration and MPP voltage. For the performed experiment under irradiance levels between 0.1 sun and 0.5 sun and operating temperature between 30 °C and 60 °C, the areal MPP C_j values of the IBC cell with $N_{\text{sub}} = 1.0 \times 10^{14}$ cm^{-3} varied between 20.2 μF/cm^2 and 61.6 μF/cm^2, whereas those of the PERC cell with $N_{\text{sub}} = 8.0 \times 10^{15}$ cm^{-3}varied between 0.283 and 1.98 μF/cm^2. Moreover, TCAD simulations of a performance-limit TOPCon cell with $N_{\text{sub}} = 1.0 \times 10^{14}$ cm^{-3}, where the irradiance level was varied between 0.1 sun and 1.2 suns and the operating temperature between 15 °C and 75 °C, show that the areal MPP C_j can increase to a range between 89.0 μF/cm^2 and 245 μF/cm^2. The results of this chapter can serve as a guideline for researchers and power electronics designers to understand how the PN junction impedance changes across varied environmental conditions.

In **Part II**, the aim was to assess the feasibility of leveraging solar-cell impedance at the input of a power converter, and to explore various methods for integrating additional PE components into solar cells. In **Chapter 5**, the feasibility of integrating different PE components into c-Si solar cells is explored. First of all, diodes exhibit high ease of integration into PV cells and successfully integrated designs have already been demonstrated in prior work. Alternatively, the integration of transistors is more complex. Since transistor fabrication processes require lithographic steps, it is necessary for cost-effective integration to combine as many processing steps as possible with PV fabrication. Regarding passive component integration, it was found that the MPP self-capacitance of modern c-Si solar cells is sufficiently large to replace the input capacitor of an exemplary boost converter. Conversely, for thin-film capacitor integration, it is challenging to achieve a sufficiently high areal capacitance. Moreover, the self-inductance of a solar cell string could potentially be leveraged to replace the inductor at the input of a power converter. By exploring this approach for an exemplary boost converter, it was found that high switching frequencies in the MHz range are required. Alternatively, the required switching frequency may be reduced through the integration of planar inductors. It was found that the area of PV cells is sufficiently large to facilitate the integration of planar coils exhibiting inductance values that are useful for power conversion. Finally, general challenges that should be considered for successful PE-PV integration are appropriate thermal management, opto-electric behaviour under illumination, and repairability. The inductor integration feasibility was further studied in **Chapter 6**. Specifically, it was explored whether planar air-core inductors with an area of 12.5 cm × 12.5 cm can yield the required inductor properties to support sub-module power conversion in PV modules. First, it is shown how the interplay between the different design parameters, such as track spacing, track width, number of turns, and middle gap size, play an important role in the inductor properties. This analysis includes changes due to high-frequency effects, which significantly impact the results. The coil

geometries that are simulated yield inductance values between 0.3 and 3.2 μH. The feasibility of implementing these inductors into an exemplary DC-DC boost converter was evaluated. To adequately reduce the ripple current from a solar cell string with such inductance values, a significant switching frequency of at least several hundred kHz is required. Moreover, at 500 kHz, an inductor thickness of around 0.5 mm is necessary to keep the ohmic losses in the inductor below 2% of the total generated power in standard test conditions. Finally, in **Chapter 7**, the concept of COSMOS (COmbined Solar and MOSFET) devices was introduced and a process flow was proposed in which back-contact TOPCon solar cells and lateral power MOSFETs are simultaneously fabricated on a single substrate. This process was successfully employed to manufacture both n-type solar cells with integrated p-channel MOSFETs (PMOS) and p-type solar cells with integrated n-channel MOSFETs (NMOS). Important trade-offs related to fabrication, such as the choice between dry or wet etching and the impact of hotplate annealing at the end of the process, were discussed. Notably, efficiencies exceeding 20% were achieved for both n-type and p-type solar cells, highlighting the potential of COSMOS solar cells. Furthermore, two main integration challenges were identified. Firstly, the *off*-state leakage currents of the MOSFETs increase due to illumination. Secondly, specific topologies of monolithic integration lead to increased *off*-state leakage currents.

8.2. Outlook

In the short term, the following recommendations are offered for further research:

- This thesis presents a comprehensive analysis of solar-cell impedance. Building on these findings, preliminary electrical circuit simulations were conducted to explore the potential of leveraging the capacitive properties of solar cells at the input of a DC-DC boost converter. The results suggest that the solar-cell capacitance can replace the physical input capacitor while maintaining minimal voltage ripple across the PN junction. In further research it could be experimentally confirmed whether the capacitive and inductive properties of solar cells can be leveraged at the input of power converters. For such applications, two important factors need to be considered. First, the impact of high-frequency relaxation of the PN junction resistance and capacitance on performance should be investigated. Second, the voltage ripple across the PN junction must remain sufficiently small to preserve a pseudolinear solar-cell impedance. If this condition cannot be met for a specific solar-cell string and power electronics configuration, the influence of the non-linear impedance behavior must be evaluated.

- As a next step, the simulated findings on planar air-core inductors presented in this thesis could be validated through experiments. Additionally, modifications to inductor design, such as incorporating ferromagnetic core materials, could be studied. Furthermore, the exploration could be expanded to include the integration of solar cells and planar inductors with other areas.

- The mitigation of light-induced leakage currents in the MOSFETs could be further investigated. For instance, this could potentially be achieved by placing the MOSFET in an inversely doped well compared to the bulk doping. Another ap-

proach could be to implement optical shading on a small fraction of front side of the COSMOS device. Moreover, the current leakage paths through the monolithic interconnection with solar cells could be further studied.

- To enhance the compatibility of COSMOS processing with the PV industry, it could be studied whether the number of photolithographic steps can be reduced. For instance, the feasibility of incorporating processing techniques such as laser doping, laser contact opening and/or laser ablation into the process flow could be explored.

Looking further ahead, the following recommendations are offered fur future research:

- In this thesis, the focus was on the integration of individual power electronic components into solar cells. Building on these findings, future research could explore the optimal utilization of these components in PV applications. The possibilities are diverse; for instance, solar-cell-integrated MOSFETs could be employed as bypass elements or to enable reconfiguration strategies. Alternatively, various solar-cell-integrated PE components could be combined to form part of a power converter for maximum power point tracking. To identify optimal topologies, it must be considered that the cell-level integrated PE can be combined with PE components that are embedded in the PV laminate. For instance, these embedded components could be thin-film capacitors, planar inductors, or small-area wafers dedicated to power conditioning functionality. These wafers could house PE components or driving circuits. This application-focused research could pave the way for more targeted optimization of solar-cell-integrated PE components.

- A cost estimation study could be conducted for the various designs of solar-cell-integrated PE. This could reveal the markets that are potentially suited for the different approaches explored in this thesis. For instance, if a fabrication process involves lithographic steps, it is unlikely to be adopted for commercial PV modules in the short term. However, such an approach might still find application in niche markets, such as PV-powered sensors or electronics.

- A solar-cell topology gaining interest is the three-terminal (3T) tandem architecture, as it does not require current matching between the two subcells [285]. A common 3T configuration features an IBC c-Si bottom cell connected to the top cell through a recombination junction [286, 287]. It would be valuable to investigate whether employing COSMOS devices as bottom cells can enhance the PE design of modules composed of 3T tandem cells.

A

Fitting quality assessment

In Chapter 2, two metrics are used to quantitatively assess the fitting quality. The first metric is the Root-Mean-Square Error (RMSE), which is calculated as follows:

$$\mathrm{RMSE} = \sqrt{\frac{\sum_{i=1}^{n} \left(X_{\mathrm{exp}} - X_{\mathrm{model}}\right)^2}{n}} \tag{A.1}$$

where X_{exp} is the experimentally recorded data, X_{model} is the value that is predicted by the model with the best-fit circuit element values, and n represents the number of data points. Furthermore, to calculate the Normalized Root Mean Square Error (NRMSE), the RMSE is normalized to the range of observed data as follows:

$$\mathrm{NRMSE} = \frac{\mathrm{RMSE}}{X_{\mathrm{exp,max}} - X_{\mathrm{exp,min}}} \tag{A.2}$$

where $X_{\mathrm{exp,max}}$ and $X_{\mathrm{exp,min}}$ are the highest and lowest value of the experimentally recorded dataset, respectively.

In Chapter 2, the NRMSE is used to assess the fitting quality for the magnitude ($\mathrm{NRMSE_M}$), the real part of the impedance ($\mathrm{NRMSE_R}$), and the complex part of the impedance ($\mathrm{NRMSE_X}$). The normalization is done to obtain a fair comparison between impedance measurements at different DC bias voltages. For instance, the magnitude of the impedance is significantly higher at low bias voltages than at high bias voltages. Whereas the magnitude, resistance and reactance are represented on linear scales, the phase is represented on a periodic scale (which repeats after a certain value). Thus, in this work the choice was made to directly use the RMSE_θ without normalization to assess the phase fitting quality for the phase. To determine whether the model consisting of only the R_j-C_j loop is satisfactory, it is chosen that $\mathrm{NRMSE_M}$, $\mathrm{NRMSE_R}$ and $\mathrm{NRMSE_X}$ must be smaller than 0.015. Furthermore, RMSE_θ must be smaller than 2.5. If these thresholds are exceeded, the full model from Figure 2.5 is used.

B

Impedance Addendum

B.1. Impedance spectroscopy setup

The impedance spectroscopy setup employed in Chapter 4 is shown in Figure B.1.

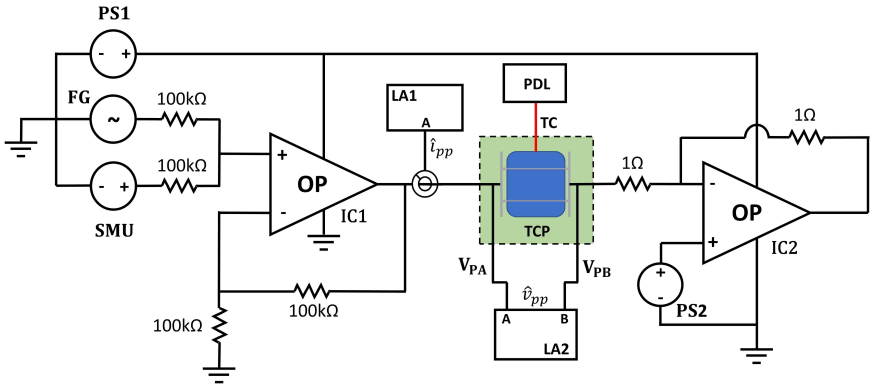


Figure B.1: Schematic representation of the employed impedance spectroscopy setup. The function generator (FG) is an Agilent 33250A. Moreover, the opamps (OP) are of the type OPA-549 and are connected in a non-inverting summing configuration (IC1) and inverting current to voltage (transimpedance amplifier) configuration (IC2). The power supply 1 (PS1) is of the type EA-OS 2042-20. Alternatively, the power supply 2 (PS2) is a voltage divider circuit located on a printed circuit board, supplying half the voltage of PS1. This approach enables the use of a single physical power supply and prevents a high forward current to the power supply. The source measurement unit (SMU) is used to set the bias voltage. The current probe (CP) is an Yokogawa 702916 connected to channel A of the EG&G Instruments 7260 DSP lock-in amplifier (LA1). Furthermore, the voltage probes (VPA) and (VPB) are connected to the positive and negative contacts of the PV cell, repectively. On the other side, VPA and VPB are connected to channel A and B of the Signal Recovery 7225 DSP lock-in amplifier (LA2). The temperature-controlled plate (TCP) is of the type Thermo Scientific Polar Series Accel 500 LC. Finally, the temperature is monitored using a type RS pro type T thermocouple (TC) and a Pico TC-08 Data Logger (PDL). Setting the DC bias voltage on the PV cell, performing frequency sweeps with the function generator, and recording the values from the lock-in amplifier were done through an in-house developed Labview program.

B.2. Experimental results

The effect of illumination on the PN junction impedance of the single-cell laminates is shown in Figure B.2.

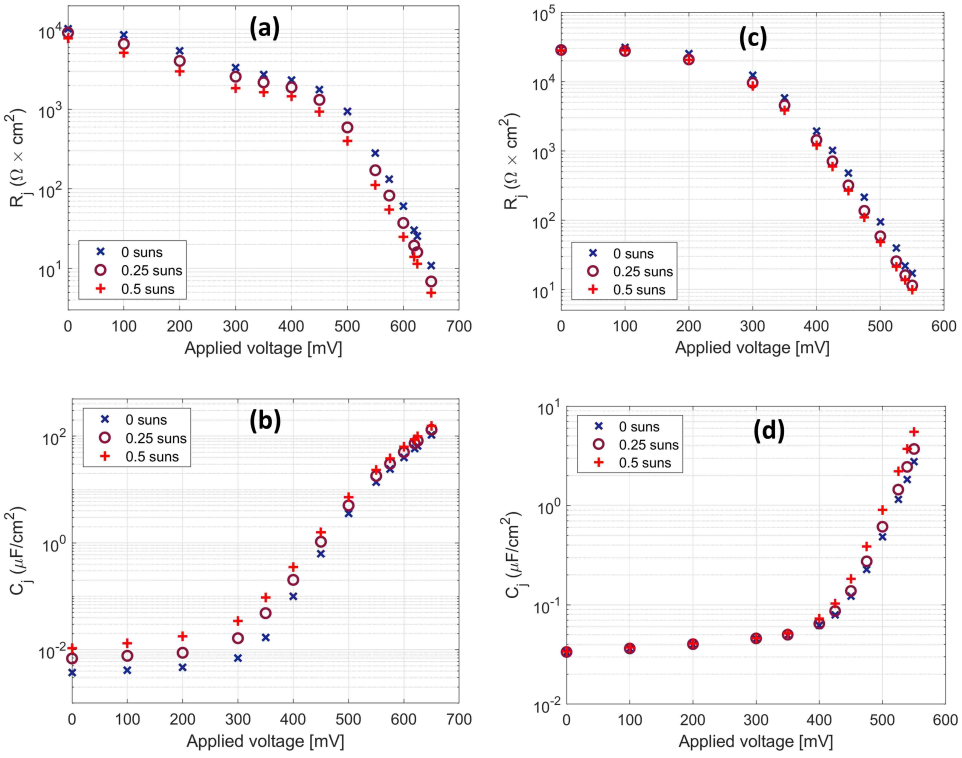


Figure B.2: Effect of illumination on R_j and C_j, as extracted through CNLS analysis from experimentally recorded impedance data of the (a-b) IBC and (c-d) PERC solar cell laminate. The irradiance is varied between dark conditions and 0.5 sun, while the temperature is kept constant at $T = 30\,^{\circ}$C.

The effect of temperature on the PN junction impedance of the single-cell laminates is shown in Figure B.3.

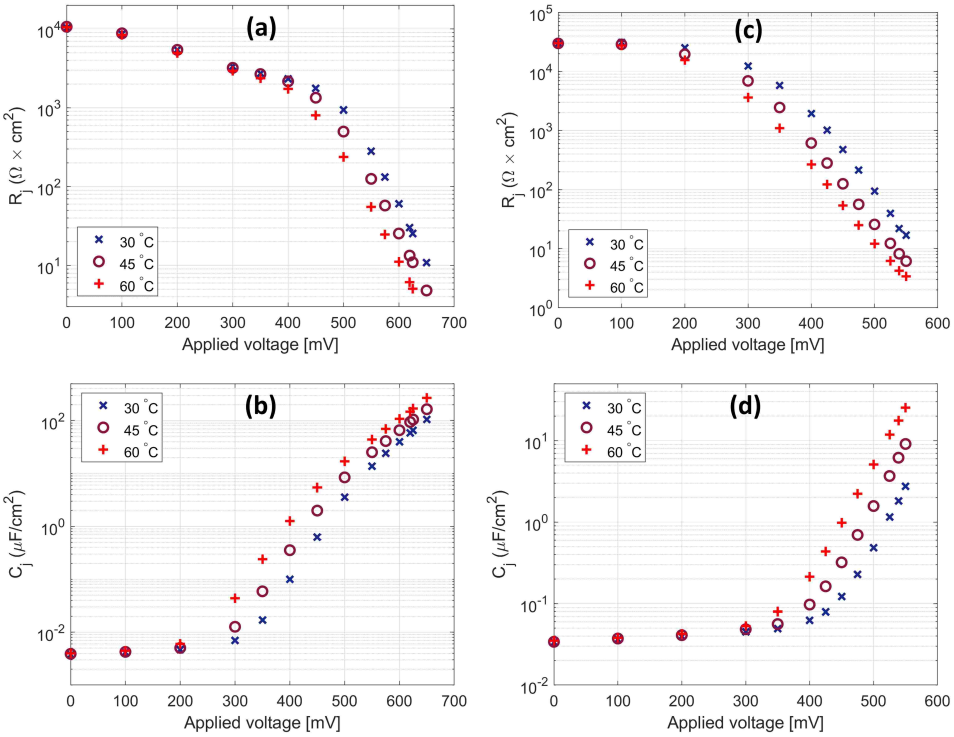


Figure B.3: Effect of temperature on R_j and C_j, as extracted through CNLS analysis from experimentally recorded impedance data of the (a-b) IBC and (c-d) PERC solar cell laminate. Temperature is varied between 30 °C and 60 °C, while the laminates are kept in dark conditions.

C

COSMOS Addendum

C.1. Additional theoretical background

This section describes the fundamental MOSFET parameters, mostly sourced from the text book by Neamen [114].

C.1.1. Threshold voltage

The threshold voltage V_T is an important characteristic of a MOSFET, representing the gate-to-source voltage V_{GS} at which a conductive channel forms beneath the gate. In the case of an n-channel MOSFET (NMOS) on a p-type substrate, the threshold voltage is given by [114]:

$$V_{TN} = \frac{|\, Q'_{SD}(\max)\,|}{C_{\text{ox}}} - \frac{Q'_{ss}}{C_{\text{ox}}} + \phi_{ms} + 2\phi_{fp} \tag{C.1}$$

where $Q'_{SD}(\max)$ is the maximum space charge density per unit area of the depletion region. Moreover, C_{ox} stands for the oxide capacitance per unit area, expressed as $C_{\text{ox}} = \epsilon_{\text{ox}} / t_{\text{ox}}$, with t_{ox} denoting the oxide thickness and ϵ_{ox} being the oxide permittivity. Q'_{ss} represents the charge density trapped around the oxide-semiconductor interface, and the negative sign in front of this term indicates that the charge at this interface is positive. ϕ_{ms} is the metal-semiconductor work function difference, and ϕ_{fp} is the potential difference (in V) between the Fermi level E_F and the intrinsic Fermi level E_{Fi} within the substrate. ϕ_{fp} is determined by the substrate dopant density, and is described by:

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) \tag{C.2}$$

where the thermal voltage V_t is given by kT/q, with k being the Boltzmann's constant, T being the temperature, and q being the elementary charge constant. In addition, N_a denotes the substrate dopant density in a p-type semiconductor, and n_i stands for the intrinsic carrier concentration.

Furthermore, $Q'_{SD}(\max)$ is also influenced by N_a, given that $\mid Q'_{SD}(\max) \mid = qN_a x_{dT}$. The depletion region width at the threshold voltage is given by:

$$x_{dT} = \sqrt{\frac{4\epsilon_s \phi_{fp}}{qN_a}} \tag{C.3}$$

where ϵ_s represents the semiconductor permittivity.

In the case of a p-channel MOSFET (PMOS) on an n-type substrate, the threshold voltage is expressed through a slightly different expression [114]:

$$V_{TP} = \frac{-\mid Q'_{SD}(\max) \mid}{C_{\text{ox}}} - \frac{Q'_{ss}}{C_{\text{ox}}} + \phi_{ms} - 2\phi_{fn} \tag{C.4}$$

Although mostly similar, this equation introduces different signs and incorporates the new term ϕ_{fn}. This term resembles ϕ_{fp} from Equation C.2, but now the donor density N_d replaces the acceptor density N_a.

C.1.2. Blocking capability

There are various mechanisms that can cause breakdown in a MOSFET once a certain V_B is exceeded. Which mechanism is limiting depends on the specific device design. For example, when the electric field in the gate oxide reaches a critical point, it results in dielectric breakdown. A thermally grown SiO_2 typically possesses a dielectric strength of about 10 MV/cm [168]. This implies that, with the 40-nm thick gate oxide employed in the COSMOS devices in this work, breakdown could occur at around 40 V across the oxide. However, it is advisable to maintain a considerable margin from this limit during actual operation, as dielectric breakdown can irreparably damage the device. Furthermore, there are two non-destructive processes that can lead to an undesired swift increase in drain current beyond a specific drain-to-source voltage V_{DS}. For instance, a relatively short channel length, coupled with a low substrate dopant density, can introduce punch-through effects. If the design is such that punch-through breakdown is avoided, the phenomenon of avalanche breakdown represents another mechanism that can cause breakdown. The mathematical expression for the avalanche breakdown voltage of a single-sided junction is provided by [114]:

$$V_{\text{av}} = \frac{\epsilon_s E_{\text{crit}}^2}{2qN_B} \tag{C.5}$$

where ϵ_s is the permittivity of the semiconductor, E_{crit} is the critical electric field at breakdown, q is the elementary charge constant, and N_B is the semiconductor doping in the low-doped region of the one-sided junction. Notably, according to Equation C.5, the breakdown voltage exhibits an inverse correlation with N_B. Given that the source and drain regions in a MOSFET are typically considerably more heavily doped than the substrate, it becomes apparent that the substrate dopant concentration plays a crucial role in the V_{av} of the MOSFET. However, it is important to recognize that Equation C.5 cannot be directly applied to a MOSFET. For instance, the electric field tends to concentrate in the depletion region at the curvature of the drain region. This phenomenon effectively diminishes V_{av}, thereby impacting the practical application of the equation in a MOSFET context [114].

C.2. Hotplate annealing

It is well known that post-metallization annealing can affect the density of localized states near the Si-SiO_2 interface region [280]. These localized states play a significant role in MOSFET characteristics, such as threshold voltage and channel mobility [114]. Therefore, the impact of a hotplate annealing step at 350 °C for 5 minutes after metallization is investigated. Figure C.1 illustrates the $I_D - V_{GS}$ curves for selected NMOS and PMOS devices, both before and after this annealing. It is evident that hotplate annealing exerts a pronounced influence on the MOSFET characteristics. Firstly, the threshold voltage can be visually identified as the V_{GS} value beyond which the I_D starts to rise, indicating the transition to the *on*-state. Figure C.1 clearly shows a shift in the threshold voltage due to annealing. Secondly, the slope of the $I_D - V_{GS}$ curves in the V_{GS} range where the NMOS and PMOS devices reach the *on*-state experiences a substantial increase following the annealing step. To precisely determine the threshold voltage values, the widely adopted linear extrapolation method [288] is employed. Specifically, V_{TN} reduces from the range of 2.01 V to 3.02 V before annealing to a range of 0.138 V to 0.253 V post-annealing. In contrast, V_{TP} increases from approximately -2.19 V to -1.63 V prior to annealing, to a range of -0.196 V to -0.181 V post-annealing. Consequently, after annealing, the threshold voltage for both NMOS and PMOS devices exhibits significantly reduced variability, and the resulting values are within the expected range based on Equations C.1 and C.4. A possible explanation for the threshold voltage changes induced by hotplate annealing is the alteration of the localized states near the Si-SiO_2 interface. Interface states, a crucial type of such states, are traps located at or near the Si-SiO_2 interface that interact rapidly with free charge carriers in the semiconductor substrate [281]. These states can trap both electrons and holes, depending on the surface potential in silicon and the availability of charge carriers [280]. Publications suggest that interface states can be reduced by performing low-temperature (between 170 °C - 500 °C) annealing either before or after metallization [289–291]. It is generally accepted that during the annealing process, hydrogen atoms saturate some form of unsaturated bonds at the Si-SiO_2 interface, thus removing interface states from the silicon bandgap energy region [280]. With this in mind, it is important to note that hotplate annealing shifts the V_{TN} of the manufactured NMOS devices in the negative direction, whereas the V_{TP} of the PMOS devices is shifted in the positive direction. Combining this observation with Equations C.1 and C.4, this suggests that for the NMOS devices, the annealing step reduces interface states that trap negative charges. Conversely, for the PMOS devices, the annealing removes interface states that trap positive charges. Additionally, the reduction in interface states after annealing can explain the heightened slope of the $I_D - V_{GS}$ curve due to enhancements in charge carrier mobility within the channel. As a result of these findings, all MOSFET results presented in this study are for wafers that underwent a hotplate annealing step.

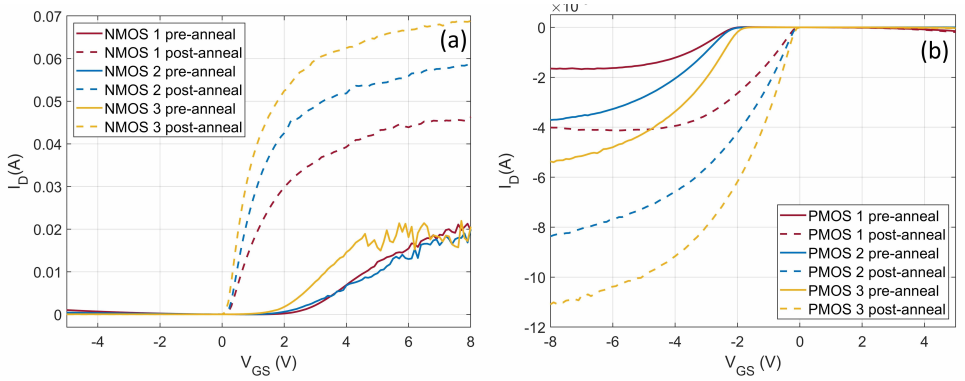


Figure C.1: The $I_D - V_{GS}$ curves before and after hotplate annealing. The variations in the curves across different MOSFETs are a result of their varying numbers of source-drain couples connected in parallel (n_{SD}). (a) includes NMOS devices from wafer P-W-2 at $V_{DS} = 0.1$ V, all with $W = 2$ mm. NMOS-1 has $n_{SD} = 5$, NMOS-2 has $n_{SD} = 7$, and NMOS-3 has $n_{SD} = 10$. (b) includes PMOS devices from wafer N-D-1 at $V_{DS} = -0.1$ V, all with $W = 2$ mm. PMOS-1 has $n_{SD} = 2$, PMOS-2 has $n_{SD} = 3$, and PMOS-3 has $n_{SD} = 4$.

D

Inductor ohmic losses

To accurately calculate the power losses in an inductor, it must be considered that the inductor is subjected to a DC current with a superimposed AC current ripple. The conventional approach involves decoupling the losses associated with different frequency components. In this study, we only consider the fundamental frequency of the AC current and neglect the harmonics. Consequently, the total power loss can be expressed as follows:

$$P_{loss} = R_{DC} \times I_{DC}^2 + R_{AC} \times I_{AC,rms}^2 \tag{D.1}$$

where P_{loss} represents the power loss in the inductor, R_{DC} denotes the DC resistance, I_{DC} is the DC current, R_{AC} signifies the AC resistance, and $I_{AC,rms}$ is the root-mean-square (RMS) value of the AC current. In this study, we approximate the ripple current as a triangular waveform. Consequently, the $I_{AC,rms}$ can be derived from the peak-to-peak value of the ripple current, divided by a factor of $2\sqrt{3}$.

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List of Publications

Peer-reviewed publications

Part of this thesis

1. **D. A. van Nijen**, P. Manganiello, M. Zeman and O. Isabella, “Exploring the benefits, challenges, and feasibility of integrating power electronics into c-Si solar cells” in *Cell Reports Physical Science*, vol. 3, 100944, 2022.*

2. **D. A. van Nijen**, M. Muttillo, R. Van Dyck, J. Poortmans, M. Zeman, O. Isabella and P. Manganiello, “Revealing capacitive and inductive effects in modern industrial c-Si photovoltaic cells through impedance spectroscopy” in *Solar Energy Materials and Solar Cells*, vol. 260, 112486, 2023.

3. **D. A. van Nijen**, T. Stevens, Y. Mercimek, G. Yang, R. A. C. M. M. van Swaaij, M. Zeman, O. Isabella and P. Manganiello, “Combined Fabrication and Performance Evaluation of TOPCon Back-Contact Solar Cells with Lateral Power Metal-Oxide-Semiconductor Field-Effect Transistors on a Single Substrate” in *Solar RRL*, vol. 8, 2300829, 2024.†

4. **D. A. van Nijen**, S. Naoom, M. Muttillo, P. Procel, M. Zeman, O. Isabella and P. Manganiello, "Analyzing the PN junction impedance of crystalline silicon solar cells across varied illumination and temperature conditions", in *Solar Energy Materials and Solar Cells*, vol. 279, 113255, 2025.

5. **D. A. van Nijen**, S. Chakravarty, J. Voorn, M. Zeman, O. Isabella and P. Manganiello, "Feasibility study on photovoltaic module-integrated planar air-core inductors to facilitate embedded power electronics", in *Energy Reports*, vol. 13, 82-89, 2025.

6. **D. A. van Nijen**, P. Procel, R. A. C. M. M. van Swaaij, M. Zeman, O. Isabella and P. Manganiello, "The nature of silicon PN junction impedance at high frequency", accepted for publication in *Solar Energy Materials and Solar Cells*, 2025.

Outside the scope of this thesis

1. T. de Vrijer, **D. A. van Nijen**, H. Parasramka, P. A. Procel Moya, Y. Zhao, O. Isabella and A. H. M. Smets, “The fundamental operation mechanisms of nc-SiO_X:H based tunnel recombination junctions revealed” in *Solar Energy Materials and Solar Cells*, vol. 236, 111501, 2022.

2. T. de Vrijer, S. Miedema, T. Blackstone, **D. A. van Nijen**, C. Han and A. H. M. Smets, “Application of metal, metal-oxide, and silicon-oxide based intermediate reflective layers for current matching in autonomous high-voltage multijunction photovoltaic devices” in *Progress in Photovoltaics: Research and Applications*, vol. 30, 1400-1409, 2022.

* This article was covered by PV Magazine: `https://www.pv-magazine.com/2022/07/04/solar-cells-integrating-power-electronics/`

† Featured on the cover of *Solar RRL*: volume 8, issue 9, 2024

3. T. de Vrijer, M. Wiering, **D. A. van Nijen**, G. Padmakumar, S. Sambamurthy, G. Limodio and A. H. M. Smets, "The optical performance of random and periodic textured mono crystalline silicon surfaces for photovoltaic applications" in *EPJ Photovoltaics*, vol. 13, 2022.

International conference contributions

First-authored

1. **D. A. van Nijen**, P. Manganiello, M. Muttillo, M. Zeman and O. Isabella, "Characterizing the capacitance of different c-Si PV cell technologies using impedance spectroscopy" in *49th IEEE Photovoltaic Specialist Conference (PVSC-49)*, Philadelphia, USA, 2022 [poster].

2. **D. A. van Nijen**, P. Manganiello, M. Muttillo, M. Zeman and O. Isabella, "Characterizing the capacitance of various industrial c-Si cell technologies" in *8th World Conference on Photovoltaic Energy Conversion (WCPEC-8)*, Milan, Italy, 2022 [oral].

3. **D. A. van Nijen**, Y. Mercimek, P. Manganiello, R. A. C. M. M. van Swaaij, M. Zeman and O. Isabella, "Recent Advances in Crystalline Silicon Solar Cells with Integrated Power Electronics" in *13th International Conference on Crystalline Silicon Photovoltaics (SiliconPV)*, Delft, The Netherlands, 2023 [oral].

4. **D. A. van Nijen**, P. Manganiello, Y. Mercimek, T. Stevens, G. Yang, R. A. C. M. M. van Swaaij, M. Zeman and O. Isabella, "Integration of lateral power MOSFETs into IBC c-Si solar cells with poly-Si passivating contacts" in *50th IEEE Photovoltaic Specialist Conference (PVSC-50)*, San Juan, Puerto Rico, 2023 [oral].*

5. **D. A. van Nijen**, T. Stevens, Y. Mercimek, G. Yang, R. A. C. M. M. van Swaaij, M. Zeman, O. Isabella and P. Manganiello, "Combined Fabrication of IBC TOPCon PV Cells and Lateral Power MOSFETs on a single c-Si substrate" in *40th European Photovoltaic Solar Energy Conference and Exhibition (EU PVSEC-40)*, Lisbon, Portugal, 2023 [oral].†

6. **D. A. van Nijen**, S. Naoom, M. Muttillo, P. Procel, M. Zeman, O. Isabella and P. Manganiello, "Variability in the capacitance of crystalline silicon solar cells due to temperature and illumination" in *52nd IEEE Photovoltaic Specialist Conference (PVSC-52)*, Seattle, USA, 2024 [oral].

7. **D. A. van Nijen**, M. Zeman, O. Isabella and P. Manganiello, "Towards integration of power electronics into crystalline silicon solar cells" in *35th International Photovoltaic Science and Engineering Conference (PVSEC-35)*, Numazu, Japan, 2024 [oral].‡

Co-authored

1. T. de Vrijer, **D. A. van Nijen**, H. Parasramka, A. H. M. Smets, "The fundamental operation mechanisms determining the performance of tunnel recombination junctions revealed by a structural study using four different multijunction PV device architectures" in *48th IEEE Photovoltaic Specialist Conference (PVSC-48)*, Virtual, 2021.

* Best student award finalist in the thematic area of "Silicon Photovoltaic Materials and Devices"
† Best student award winner in the thematic area of "Photovoltaic Modules and BoS Components"
‡ This work was presented by Patrizio Manganiello

2. R. Van Dyck, **D. A. van Nijen**, M. Muttillo, P. Manganiello, A. Bakovasilis, T. Borgers, K. Onda, R. Zulhidza, W. Martinez, H. S. Radhakrishnan, O. Isabella, A. W. Van Vuure, and J. Poortmans, "Photovoltaic Module-Integrated Capacitors to Facilitate Embedded Power Electronics" in *52nd IEEE Photovoltaic Specialist Conference (PVSC-52)*, Seattle, USA, 2024 [poster].

Patents

1. P. Manganiello, **D. A. van Nijen**, O. Isabella, "Integration of inductors on silicon-based solar cells", The Netherlands, NL2030089, 2023.

Curriculum Vitae



David van Nijen was born in Amsterdam on December 28, 1996. In 2015, he started a nine-year long academic journey at Delft University of Technology. He completed a BSc degree in Applied Physics in 2018, followed by an MSc degree in Sustainable Energy Technology (cum laude) in 2020. His MSc thesis, conducted within the Photovoltaics Materials and Devices group, focused on developing a triple-junction high-voltage silicon solar cell. Following this, David started working towards his PhD degree in the same group, under the supervision of Dr. Patrizio Manganiello, Prof. dr. Olindo Isabella, and Prof. dr. Miro Zeman. His doctoral research focused on the integration of power electronics into crystalline silicon solar cells. David's presentation at the 40th EU PVSEC was recognized with the Best Student Award in the thematic area of "Photovoltaic Modules and BoS Components". Additionally, he served as a teaching assistant for the MSc courses *Semiconductor Device Physics* and *Photovoltatronics*. From October 2024, David has taken on the role of Performance Lead at HyET Solar, a company developing flexible thin-film silicon photovoltaic modules.