

Nanoscale Electrostatic Control of Superconducting Oxide Interfaces

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NANOSCALE ELECTROSTATIC CONTROL OF SUPERCONDUCTING OXIDE INTERFACES

NANOSCALE ELECTROSTATIC CONTROL OF SUPERCONDUCTING OXIDE INTERFACES

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. ir. K. C. A. M. Luyben,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op vrijdag 13 oktober 2017 om 12:30 uur

door

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Keywords: Complex Oxide Heterostructures, $\text{LaAlO}_3/\text{SrTiO}_3$, two-dimensional electron system (2DES), gate tunable superconductivity, nanoscale top gating, superconducting quantum interference devices (SQUIDs), superconducting quantum point contact (SQPC)

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Front & Back: *Gate-tunable superconducting quantum interference devices can be created in the two-dimensional superconductor formed at oxide interfaces.* Image: Ella Marushchenko.

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*Living is no laughing matter:
you must live with great seriousness
like a squirrel, for example—
I mean without looking for something beyond and above living,
I mean living must be your whole occupation.*

*Living is no laughing matter:
you must take it seriously,
so much so and to such a degree
that, for example, your hands tied behind your back,
your back to the wall,
or else in a laboratory
in your white coat and safety glasses,
you can die for people—
even for people whose faces you've never seen,
even though you know living
is the most real, the most beautiful thing.*

*I mean, you must take living so seriously
that even at seventy, for example, you'll plant olive trees—
and not for your children, either,
but because although you fear death you don't believe it,
because living, I mean, weighs heavier.*

Nazım Hikmet Ran, 1947

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SUMMARY

This thesis investigates the two-dimensional superconductor that forms at the oxide interfaces of LaAlO_3 (LAO)/ SrTiO_3 (STO) by controlling its electronic properties with nanoscale top gates. Superconductivity of this interfacial system has several intriguing properties that set it apart from conventional superconductors. Most notably, an electric field can be used to tune its critical temperature (T_C) revealing a dome-shaped phase diagram reminiscent of high T_C superconductors. Here, we employ nanoscale top gates that efficiently modify the superconducting properties with gate voltages and thus create devices with electrostatic interfaces.

Chapter 1 starts with the introduction of basics such as materials, LAO and STO, the two-dimensional electron system (2DES) and its electronic properties followed by an overview of superconductivity at the 2DES.

Chapter 2 presents the fabrication route of nanoscale top gated devices. We use pulsed laser deposition (PLD) technique for the oxide growth in combination with multiple, aligned electron beam lithography (EBL) steps.

Chapter 3 introduces nanoscale electronic devices at the LAO/STO interface using patterned top gates which efficiently modify the potential landscape. We demonstrate that individual narrow gates (down to 200 nm) can completely pinch off the conducting channel with negligible leakage currents. At milliKelvin temperatures, when the interface is superconducting we use a single narrow top gate to drive locally a superconducting to insulating transition at the LAO/STO interface. In the superconducting state, we see evidence for a superconducting weak link with a gate dependent critical current.

Chapter 4 presents phase-sensitive measurements of the superconducting order parameter by realizing the first superconducting quantum interference devices (SQUIDs) at the LAO/STO interface. Here, nanoscale top gates enable in-situ creation and control of Josephson junctions. These gate-defined SQUIDs are unique in that the entire device is made from a single superconductor with purely electrostatic interfaces between the superconducting reservoir and the weak link. We complement our experiments with numerical simulations and show that the low superfluid density of this interfacial superconductor results in a large, gate-controllable kinetic inductance of the SQUID.

Chapter 5 demonstrates for the first time the formation of a superconducting quantum point contact (SQPC) with patterned split gates in a superconductor, utilizing the unique gate tunability of the two dimensional superfluid at the LAO/STO interface. Here, variation of the split gate voltage tunes the constriction allowing us

to identify three regimes of transport: (1) SQPC for which the supercurrent is carried only by a few quantum transport channels, (2) superconducting island strongly coupled to the equilibrium reservoirs and (3) charge island of unknown nature weakly coupled to the reservoirs.

Chapter 6 reports the on-going work on combining two-dimensional superconductor at the LAO/STO interfaces with a conventional, s-wave, superconductor in different device geometries that would enable performing phase-sensitive tests of the superconducting order parameter in a corner-SQUID geometry.

SAMENVATTING

Dit proefschrift beschrijft het onderzoek naar de tweedimensionale supergeleider die zich vormt op het grensvlak van de oxides LaAlO_3 (LAO) en SrTiO_3 (STO). De tweedimensionale supergeleider is op de nanoschaal bestudeerd met behulp van lithografisch gepatroneerde gate elektrodes. Met diverse intrigerende eigenschappen onderscheidt de supergeleiding van dit tweedimensionale systeem zich van conventionele supergeleiders. De meest opvallende eigenschap is de mogelijkheid om de kritieke temperatuur te beheersen doormiddel van een elektrisch veld. Dit resulteert in een koepelvormige fase-diagram dat doet denken aan de high- T_C supergeleiders. Met gebruik van gate elektrodes kan op nanoschaal een elektrisch veld gecreëerd worden dat efficiënt de supergeleidende eigenschappen verandert. Met deze techniek zijn elektrostatisch gedefinieerde structuren gemaakt die de basis vormen voor dit proefschrift.

In hoofdstuk 1 worden er een aantal basisprincipes geïntroduceerd; de materialen LAO en STO, het tweedimensionale elektronsysteem (2DES) en een overzicht van supergeleiding in een 2DES.

Hoofdstuk 2 beschrijft de fabricatie van het LAO/STO grensvlak en de toevoeging van op nanoschaal gedefinieerde gate elektrodes. De fabricage wordt uitgevoerd met behulp van pulsed laser deposition (PLD) voor de groei van de oxides en meerdere uitgelijnde elektronbundel lithografie (EBL) stappen.

In hoofdstuk 3 worden experimenten geïntroduceerd met elektrode structuren die efficiënt het potentiaallandschap bij het grensvlak tussen LAO en STO kunnen modificeren. Deze demonstreren dat individuele smalle elektrodes (met een breedte tot 200 nm) het geleidende kanaal compleet kunnen afknippen. Bij millikelvin temperaturen is het systeem supergeleidend en wordt een enkele smalle elektrode gebruikt om lokaal een transitie van supergeleider naar isolator teweeg te brengen. In de supergeleidende toestand zijn aanwijzingen te zien voor een supergeleidende zwakke schakel met een kritische stroom die afhankelijk is van de spanning op de elektrode. Hoofdstuk 4 beschrijft fasegevoelige metingen van de supergeleidende order parameter. Deze metingen zijn mogelijk gemaakt door het realiseren van supergeleidende kwantuminterferentie elementen (SQUIDs) op het grensvlak van LAO en STO. Elektrodes op nanoschaal maken het mogelijk om in-situ Josephson juncties te creëren en te beheersen. Deze SQUIDs zijn uniek aangezien ze geheel gemaakt zijn van een enkele supergeleider waaraan een zwakke schakel is toegevoegd met behulp van pure elektrostatische velden. Deze experimenten worden gecomplementeerd met numerieke simulaties die aantonen dat de lage superfluid density

van deze tweedimensionale supergeleider ervoor zorgt dat de SQUID een grote, kinetische inductie heeft.

In hoofdstuk 5 wordt, met behulp van gate elektrodes, de formatie van een supergeleidend kwantum punt contact (SQPC) in de LAO/STO tweedimensionale supergeleider gedemonstreerd. Dit is mogelijk door de unieke afstembaarheid van het tweedimensionale elektronsysteem bij het grensvlak tussen LAO en STO. Variatie van de spanning op de elektrodes stremt het transport door de constrictie, waardoor er drie transportregimes te onderscheiden zijn; (1) een SQPC waarin de supergeleidende stroom slechts door enkele kwantum transportkanalen kan stromen, (2) een supergeleidend eiland dat sterk gekoppeld is aan de equilibrium reservoirs en (3) een ladings-eiland van onbekende oorsprong dat zwak gekoppeld is aan de reservoirs.

Hoofdstuk 6 beschrijft lopend onderzoek betreffende het combineren van de tweedimensionale supergeleider bij het grensvlak tussen LAO en STO met een conventionele s-wave supergeleider. Dit wordt toegepast in verschillende configuraties om fasegevoelige metingen mogelijk maken van de supergeleidende order parameter met een corner-SQUID.

1

COMPLEX OXIDE HETEROSTRUCTURES

"The behavior of large complex aggregates of elementary particles, it turns out, is not to be understood in terms of a simple extrapolation of the properties of a few particles. Instead, at each level of complexity entirely new properties appear."

More is Different, P. W. Anderson

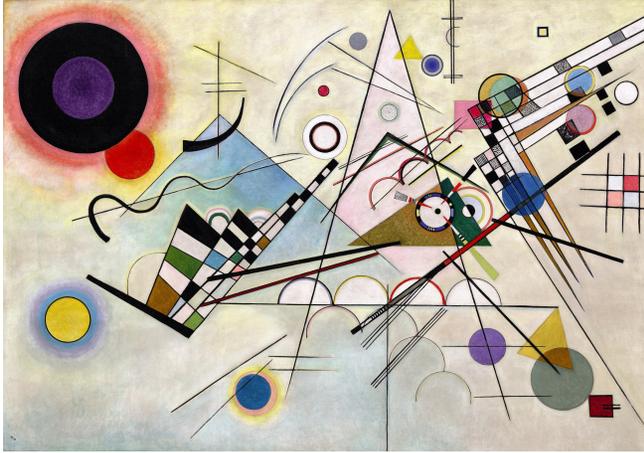


Figure 1.1: **Composition VIII** by Wassily Kandinsky. Painted in July 1923, Solomon R. Guggenheim Museum, New York USA

1.1. INTRODUCTION

Wassily Kandinsky, Russian painter, born in Moscow 1866, had investigated the interaction between colors and patterns. He, as an abstract painter, was intrigued by the music and had orchestrated musical compositions by use of these interactions in his paintings. Thus, it can be said that the music in Kandinsky's paintings is to be *emergent*.

Emergent properties of a system arise from the complex interactions among its constituents. They are unprecedented, and offer *new* functionalities which makes us curious and eager to understand the underlying mechanism of the *new*. Emergent properties give us the ambition to create new forms of matter and functionalities by understanding their nature.

Complex oxide interfaces are artificially created systems and have the emergence of new properties and functionalities at their origin. These material systems exhibit properties often non-existent in the constituent materials. One remarkable example is the heterostructure of LaAlO_3 (LAO) and SrTiO_3 (STO). Even though these materials are insulators, a two-dimensional electron system (2DES) forms at the interface when an epitaxial film of LAO is grown on STO. Furthermore, this 2DES exhibits emergent properties that interests many scientists, such as magnetism, spin-orbit interaction and gate tunable superconductivity.

This thesis investigates the superconducting properties of the LAO/STO interface by scaling down structures to the nanometer scale and using electric fields to control the properties of this system. It is an attempt to make us one step closer to understand the origin of emergent properties and create new functionalities *on demand*.

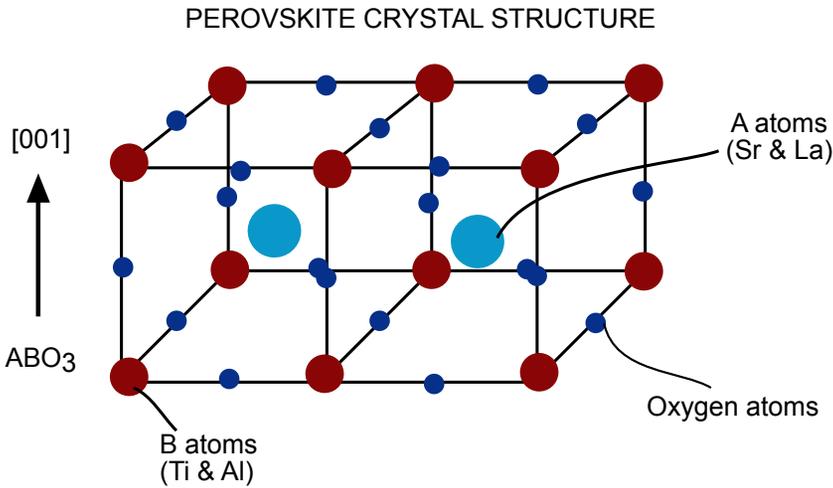


Figure 1.2: **Perovskite crystal structure.** Unit cell representation of the perovskite structure, ABO_3 . A atoms are located at the center of the unit cell. B atoms occupy the corners, while oxygen atoms are in between B atoms, creating octahedra of BO_6 . Along $[001]$ crystal axis, perovskite structure consists of AO and BO_2 planes.

1.2. TWO-DIMENSIONAL ELECTRON SYSTEM

$SrTiO_3$ (STO) has a cubic crystal structure (Space group: $Pm\bar{3}m$) at room temperature with a lattice parameter of 3.905 \AA . Strontium atoms are located at the center of each unit cell (Atomic coordinates: $1/2 \ 1/2 \ 1/2$). Titanium atoms are at the corners of the cube (Atomic coordinates: $0 \ 0 \ 0$), while oxygen atoms (Atomic coordinates: $1/2 \ 0 \ 0$) are in between titanium atoms, creating octahedra of TiO_6 . STO undergoes a structural phase transition at 105 K from a cubic to tetragonal phase (Space group: $I4/mcm$). This transition arises due to the rotation of neighboring TiO_6 octahedra in opposite directions through anti-ferrodistortive motion. On the other hand, $LaAlO_3$ (LAO) has a rhombohedral crystal structure (Space group: $R\bar{3}c$) with a pseudo-cubic lattice parameter of 3.791 \AA . $SrTiO_3$ and $LaAlO_3$ are both band insulators with band gap values of 3.2 eV and 5.6 eV , respectively. They belong to perovskite crystal structure family, represented as ABO_3 which consists of stacking of AO and BO_2 planes in $[001]$ crystal direction as shown in figure 1.2. Thus, STO can be viewed in an ionic approximation as alternating charge neutral layers of $Sr^{2+}O^{2-}$ and $Ti^{4+}O_2^{2-}$, while LAO consists of charged, polar layers of $La^{3+}O^{2-}$ (+1) and $Al^{3+}O_2^{2-}$ (-1).

Single crystal $SrTiO_3$ (001) can be found in two different configurations namely TiO_2 - (figure 1.3(a)) or SrO-terminated. In the case of TiO_2 - $SrTiO_3$, epitaxial growth of $LaAlO_3$ starts with $La^{3+}O^{2-}$ layer which has a positive charge. Then, the LAO film

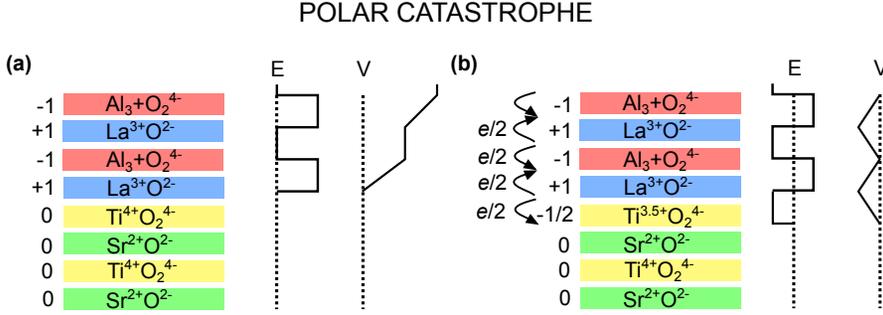


Figure 1.3: **Polar Catastrophe mechanism for formation of the 2DES at the $\text{LaAlO}_3/\text{SrTiO}_3$ interface.** (a) TiO_2 -terminated STO has neutral (001) planes while (001) LAO has alternating polar planes which produce a built-in electric potential. (b) Electronic reconstruction takes place at a critical thickness of 4 unit cells. 0.5 electron per unit cell is transferred from the surface valence of LAO to conduction band of STO, creating the 2DES. Figure is adapted from [3].

continues with negatively charged $\text{Al}^{3+}\text{O}_2^{2-}$ plane. The alternating polar layers of LaAlO_3 on TiO_2 - SrTiO_3 create an electric field. When the thickness of LaAlO_3 reaches 4 unit cells, charges at the surface valence of LaAlO_3 ($0.5 e$ per two dimensional unit cell) is transferred to the conduction band of SrTiO_3 in order to compensate the built-in electric field and thus creating the 2DES. This mechanism is referred to as polar catastrophe and is shown in figure 1.3(b). Since the TiO_2 -terminated SrTiO_3 result in n-type conductivity at the $\text{LaAlO}_3/\text{SrTiO}_3$ interface, p-type conductivity is expected for the case of SrO terminated SrTiO_3 . In this configuration, holes must transfer to the interface, however these interfaces are found to be electrically insulating [1, 2].

LaAlO_3 and SrTiO_3 are high- κ materials that allows performing field effect studies on the 2DES. LaAlO_3 has a dielectric constant $\epsilon_r \cong 25$ at room temperature and it stays constant down to 4 K [4]. On the other hand, SrTiO_3 has field dependent dielectric constant $\epsilon_r \cong 300$ at room temperature and it increases up to 30 000 when cooled down [5].

1.3. ELECTRONIC STRUCTURE

The electronic structure of SrTiO_3 arises from the fivefold degenerate d-orbitals of the titanium atom. This degeneracy is lifted to the high energy doublet, e_g , and low energy triplet, t_{2g} , states which consist of d_{XY} , d_{XZ} and d_{YZ} orbitals because of the crystal field that is introduced by the oxygen octahedra. Moreover, the anti-ferrodistortive motion of TiO_6 introduces additional splitting of these levels during the cubic to tetragonal transition at 105 K. In addition, the 2p-orbitals of the oxygen atom and the 3d-orbitals of the titanium atom interacts, which introduces an orbital

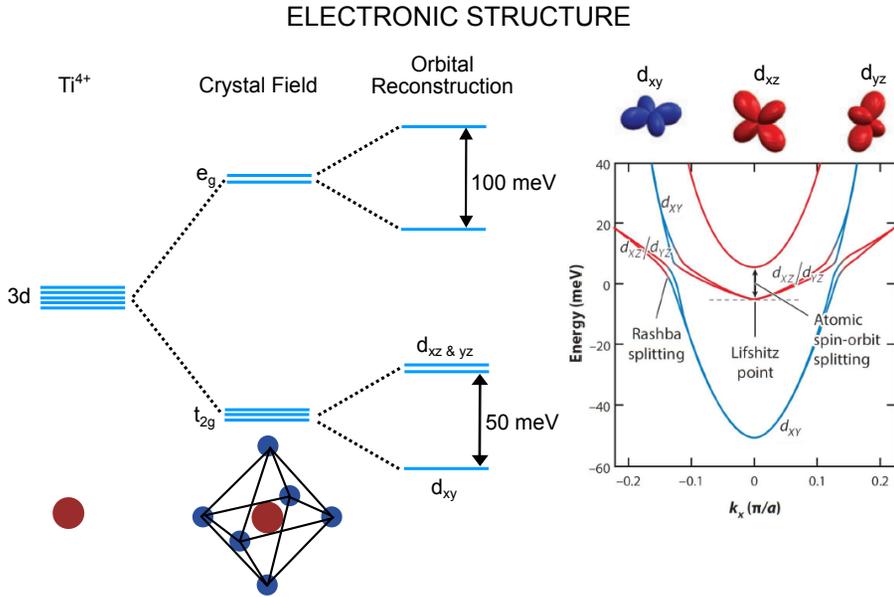


Figure 1.4: **Electronic structure of SrTiO₃ (left) and LaAlO₃/SrTiO₃ interface (right)**. 5-fold degenerate 3d levels of titanium atom splits into e_g and t_{2g} levels due to crystal field. Atomic spin-orbit and Rashba-spin orbit coupling splits the bottom of $d_{XZ/YZ}$ and couples it to the d_{XY} and $d_{XZ/YZ}$ bands. Only d_{XY} band is occupied until $d_{XZ/YZ}$ starts to get populated, referred as Lifshitz transition. Figures are adapted from [6] and [7].

reconstruction. When the 2DES forms at the LaAlO₃/SrTiO₃ interface, the d_{XY} band, which has a higher effective mass in z -direction, is shifted to lower energies compared to d_{XZ} and d_{YZ} bands [8, 9]. Figure 1.4 (left panel) depicts the band structure that is inferred from X-ray absorption measurements [8].

Atomic spin-orbit coupling (ASOC) and confinement in out-of-plane direction result in Rashba spin-orbit coupling (RSOC) [10, 11]. ASOC splits the bottom of $d_{XZ/YZ}$ bands, while RSOC couples d_{XY} band with $d_{XZ/YZ}$ [12]. The resulting band structure of the LaAlO₃/SrTiO₃ interface is given in figure 1.4 (right panel). At low carrier densities, only the d_{XY} band is populated and transport takes place within a single-band. At a critical density $n_C \cong 1.7 \times 10^{13} \text{ cm}^{-2}$, d_{XZ} and d_{YZ} bands start to be populated and multi-band transport takes place. This transition from single-band to multi-band occupation is called Lifshitz transition [13, 14].

1.4. TWO-DIMENSIONAL SUPERCONDUCTIVITY

The 2DES at the $\text{LaAlO}_3/\text{SrTiO}_3$ interface exhibits superconductivity at a critical temperature, $T_C \cong 200$ mK, in accordance with the Berezinskii-Kosterlitz-Thouless (BKT) transition [15, 16]. Furthermore, the thickness of the superconducting layer, $d \cong 10$ nm, is smaller than the in-plane coherence length, $\xi = 60\text{--}100$ nm. Thus, the system is two-dimensional in the superconducting state. Moreover, the superconducting transition exhibits a dome-shaped phase diagram where the critical temperature (T_C) can be tuned with gate voltages [17, 18]. Furthermore, the ground state of the system can be switched to its insulating state through a quantum phase transition (QPT) for example by reducing the carrier density with gate voltages. Optimally-doped 2DES has a superconducting gap (i.e magnitude of the superconducting order parameter), $\Delta \cong 40$ μeV , measured by out-of-plane tunneling experiments [19, 20]. Furthermore, it is reported that the superconducting gap does not close across the QPT. Instead, it exhibits pseudo-gap behavior analogous to the high T_C cuprates [19].

The system exhibits extremely low superfluid density, $n_S = 2 \times 10^{12} \text{ cm}^{-2}$ [21, 22]. Only 1-10 percent of the Hall carriers contribute to the superconductivity (typical Hall carrier densities $n_{\text{HALL}} = 2\text{--}3 \times 10^{13} \text{ cm}^{-2}$). The discrepancy between the Hall carrier density and the superfluid density of the system is explained by the multi-band nature of the 2DES. It is argued that the carriers that reside in the d_{XY} band exhibit low mobility and they are strongly localized to screen the disordered electronic potential. The $d_{XZ/YZ}$ bands are occupied above a critical density, i.e through Lifshitz transition, $n_C = 1.7 \times 10^{13} \text{ cm}^{-2}$ which triggers the superconductivity in the system [22, 23]. Even though it is still not clear whether superconductivity arises due to the occupation of $d_{XZ/YZ}$ bands, experimental evidence on coexistence of magnetism and superconductivity [24–26] has led to the theoretical predictions of unconventional pairing as the origin of superconductivity [23, 27–29]. Furthermore, Majorana physics is predicted to arise due to the interplay between spin-orbit interaction, superconductivity and confinement [30].

Transport studies of $\text{LaAlO}_3/\text{SrTiO}_3$ interfaces, in $100 \mu\text{m}$ size channels, have played an important role towards building a better understanding of the emergent properties. However, it is becoming increasingly clear that nanoscale electronic devices could provide direct information on the origin of and the interplay between these properties.

1.5. NANOSCALE DEVICES AT THE LAO/STO INTERFACE

Nanoscale patterning of LAO/STO interfaces requires either rendering regions of insulating interface or creating the 2DES, on demand. Insulating regions can be patterned via electron-beam or photolithography and subsequent deposition of a hard mask before LAO growth. Constrictions down to 50 nm in width have been patterned and used to demonstrate mesoscopic superconducting devices such as Josephson

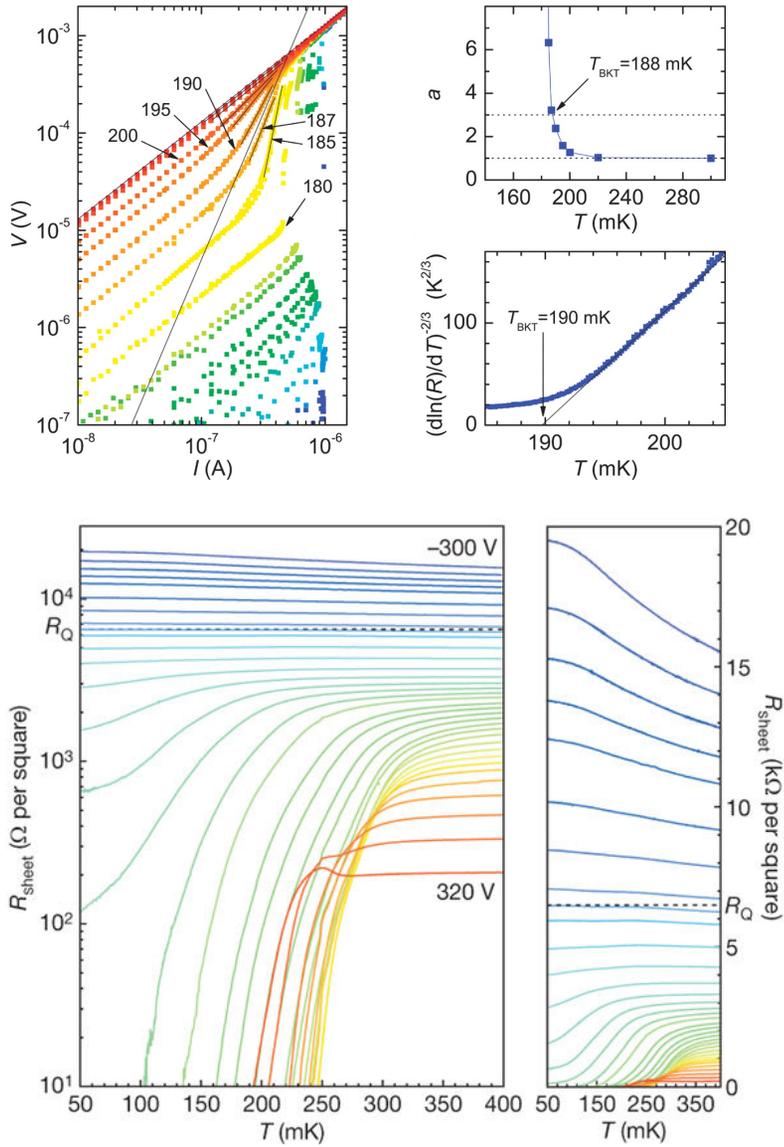


Figure 1.5: **Superconductivity at the LAO/STO interface.** The 2DES becomes two-dimensional superconductor in accordance with BKT transition. The transition temperature can be tuned with gate voltages. Figures are adapted From [15] and [17].

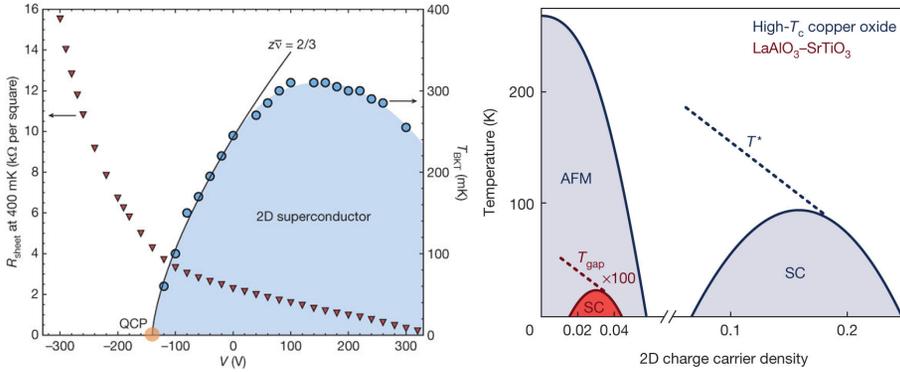


Figure 1.6: **Gate-tunable superconductivity and pseudo-gap behavior.** Left: Superconducting phase diagram exhibits a dome-shape where the insulating state can be induced with gate voltages through a QPT (solid line separates the superconducting and the insulating ground states at which it approaches to quantum critical point, i.e QCP at $T=0$ K). Right: Superconducting gap does not close across the QPT. Instead it exhibits a pseudo-gap behavior similar to high T_C cuprates. Figures are adapted from [17] and [19].

junctions [31] and Superconducting Quantum Interference Devices [32] (SQUIDs, see chapter 4 ‘Quantum Interference’). Alternatively, ion milling can be used to render regions of the LAO/STO film insulating, therefore leaving a patterned 2DES. Features down to 50-100 nm are fabricated using this technique [33] and SQUID-like modulations have been observed on superconducting rings [34].

The 2DES at LAO/STO interface nano-structures can be created upon applying electric fields to 3 unit cell thick LAO/STO samples. LAO being a high- κ dielectric allows the use of a voltage biased Atomic Force Microscopy (AFM) tip scanned on top of the LAO layer which induces the 2DES [35, 36]. This technique is used to pattern the 2DES by creating *on demand* features down to 10 nm. Devices such as Fabry-Perot cavities [37] and single electron transistors (SETs) [38] have been successfully fabricated. Moreover, superconducting nanoscale devices have shown that pairing of electrons occur even in the absence of superconductivity [39, 40].

These techniques have shown promising results on realizing nanoscale devices that is controlled either by the use of a global back gate or local side gates. However, they do not provide an obvious way to create more intricate device structures which require in-situ tunability of the potential landscape. In addition, they suffer from issues such as ion-beam induced damage or long term stability, which could have a direct impact on device performance.

In principle, these hurdles can be overcome by the use of local top gates, which can be conveniently integrated with several oxide interfaces where the top oxide layer itself acts as a high quality gate dielectric. In this device architecture the potential profile in the 2DES can be precisely controlled using appropriate gate volt-

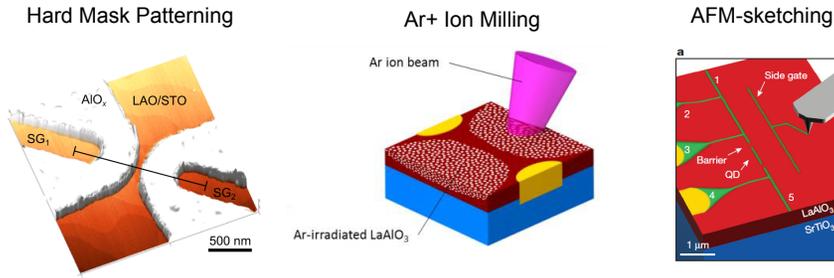


Figure 1.7: **Nanoscale patterning of LAO/STO Interfaces.** Patterning of the 2DES can be achieved by rendering the insulating regions either by ‘Hard Mask Pattering’ or removing the film via ‘Ar⁺ ion milling’. On the other hand, 2DES can be created on 3 unit cell samples by ‘AFM-sketching’. Figures are adapted from [31], [41] and [39].

ages, thus making it an extremely flexible technique to create robust tailor-made nanostructures. Such electrostatic confinement and control are routinely employed to create low-dimensional systems [42] in traditional semiconductor based 2DES which offer in-situ tunability [43, 44] and have provided insights into several aspects of mesoscopic physics (reviewed in [45]) ranging from the quantum Hall effect to the Aharonov-Bohm effect. In fact, large area top gates have been successfully employed at LAO/STO 2DESs [46–52]. However, the full potential of electrostatic control and confinement can be achieved by scaling these structures down to nanometer scale, enabling local investigations on the origin and interplay between the emergent properties of this exotic interfacial 2DES.

1.6. OUTLINE OF THE THESIS

In this thesis, we realize local nanoscale top gates on LAO/STO interfaces, exploit the full potential of gate tunability, and investigate the superconducting properties of the 2DES by creating *devices with electrostatic interfaces*.

In Chapter 2, we present the experimental methods that we use throughout this thesis. We use electron beam lithography in combination with pulsed laser deposition technique for patterning the 2DES and the nanoscale top gates. We perform electrical measurements in a dilution refrigerator with a base temperature of 40 mK.

In Chapter 3, we use local top gates and achieve nanoscale electrostatic control at the 2DES. Furthermore, we induce, locally, superconducting to insulating transition of the 2DES with the use of nanoscale top gates and we see evidence for a superconducting weak link with a gate-dependent critical current.

In Chapter 4, we perform phase sensitive measurements of the superconducting order parameter by realizing the first superconducting quantum interference devices

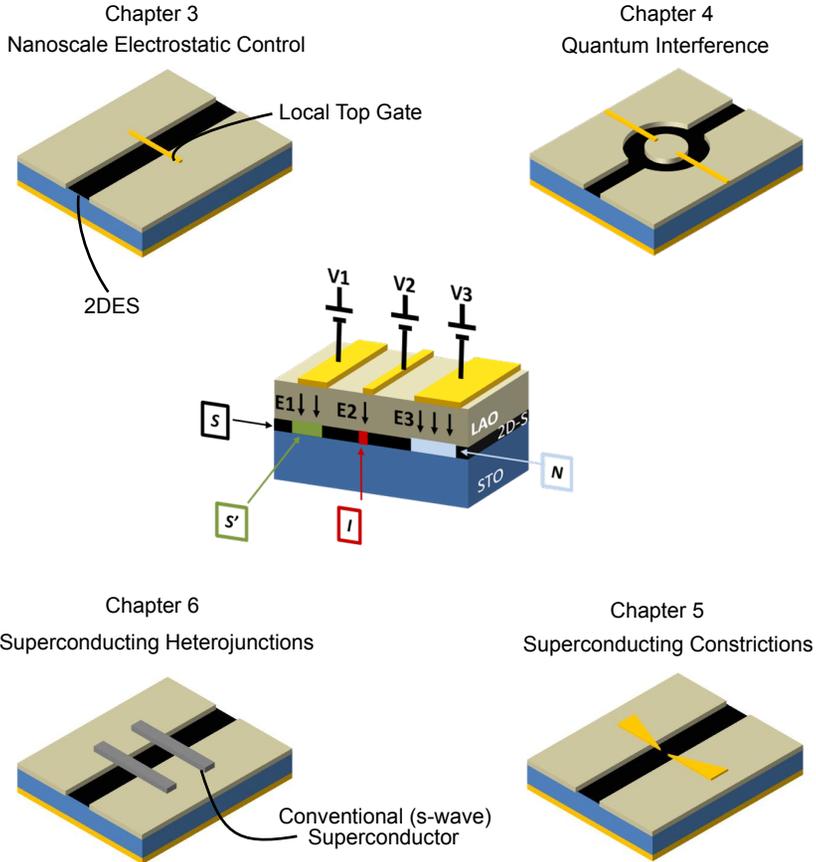


Figure 1.8: **Central Idea of this thesis and realized devices.** We realize *Devices with Electrostatic Interfaces*. Nanoscale top gates are patterned on top of 5 nm thick LAO layer and are used to create electronic devices by controlling properties of the 2DES with electrostatic gate voltages. Chapter 6 reports our on-going work on combining LAO/STO interface with a conventional, s-wave, superconductor in different device geometries.

(SQUIDs) at the LAO/STO interface. Here, nanoscale top gates enable in-situ creation and control of Josephson junctions. These gate-defined SQUIDs are unique in that the entire device is made from a single superconductor with purely electrostatic interfaces between the superconducting reservoir and the weak link.

In Chapter 5, we demonstrate for the first time the formation of a superconducting quantum point contact (SQPC) with patterned split gates in a superconductor, utilizing the unique gate tunability of the two-dimensional superfluid at the LAO/STO interface. Here, variation of the split gate voltage tunes the constriction width and its electronic properties allowing us to identify different regimes of transport.

In Chapter 6, we report the on-going work on combining two dimensional superconductor of the LAO/STO interface with a conventional, s-wave, superconductor in different device geometries that would enable performing phase sensitive tests of the superconducting order parameter in a corner-SQUID geometry.

2

EXPERIMENTAL METHODS

"New directions in science are launched by new tools much more often than by new concepts. The effect of a concept-driven revolution is to explain old things in new ways. The effect of a tool-driven revolution is to discover new things that have to be explained."

Imagined Worlds, Freeman Dyson

2.1. NANOSCALE TOP GATED DEVICES

In this chapter, we briefly overview the fabrication and characterization techniques that are used for nanoscale top gated devices. The device fabrication involves multiple, aligned electron beam lithography (EBL) and pulsed laser deposition (PLD). Following fabrication, we characterize our devices using atomic force microscopy (AFM). Last, we perform electrical measurements at low temperatures.

2.1.1. ELECTRON BEAM LITHOGRAPHY

We use a Raith® EBPG5000+ system to pattern our substrate and the nanoscale top gates in the cleanroom of Kavli Institute of Nanoscience. EBL uses a focused electron beam which is scanned over a substrate surface that is covered with an e-beam sensitive polymer (resist). The electron beam changes the solubility of the resist and allows selective removal of the exposed or non-exposed regions when immersed in a solvent. EBL offers to pattern custom made designs with *sub 10 nm* resolution and thus allows to create nanoscale structures which is not possible using standard photolithography.

A standard EBL procedure involves three steps, as given in figure 2.1. It starts with design of the pattern which can be done using various CAD softwares. Next, the pattern is transferred to the EBL software which creates the actual pattern that will be written. Thus, there are key parameters to be defined for lithography to succeed such as the dose ($\mu\text{C}/\text{cm}^2$), the beam step size (BSS) and diameter of the beam. In a writing process, the beam will scan the pattern with defined step size and deliver certain number of electrons per area. Moreover, these three parameters will also define the writing frequency and thus time. A common practice for decreasing the writing time is to create multiple patterns depending on their resolution such as a coarse (BSS >50 nm) and a fine pattern (BSS <10 nm) while keeping an overlap between these regions (≈ 500 nm).

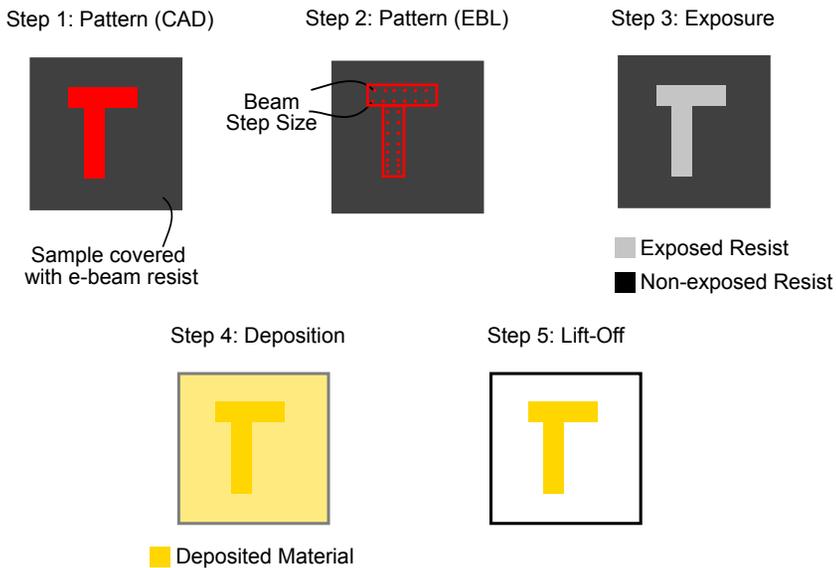
Following exposure, the sample is immersed into a solution for dissolving the resist which then creates the patterned sample. Then, desired material can be deposited onto the sample. Following lift-off, in which the sample is immersed in a solution that dissolves the resist (i.e acetone), desired pattern is achieved, as shown in figure 2.1.

2.1.2. PULSED LASER DEPOSITION

We use PLD technique to grow LaAlO_3 (LAO) films. Our PLD is from Twente Solid State Technology® and is equipped with KrF excimer laser (Coherent® LPX PRO, pulsewidth of 25 ns at 248 nm), infrared laser (DILAS®, 150 W, 980 nm) and in-situ reflection high energy electron diffraction (RHEED, STAIB® Instruments, 30 keV, 1.55 Amp).

In PLD technique, short pulse of excimer (UV) laser hits the target material and an ablation process takes place. The ionized particles react with the chamber atmo-

ELECTRON BEAM LITHOGRAPHY

Figure 2.1: **Process flow for EBL.**

sphere and creates a plasma plume directed to the heated substrate. Figure 2.2(b) shows the generated plasma plume upon delivery of the UV-pulse. Every pulse delivers the target material onto the substrate where atoms are mobile enough to arrange themselves. The growth can be monitored by measuring the RHEED diffraction spot intensity. Growth of the film results in an oscillation of the diffracted spot's intensity where minimum of the oscillation corresponds to half unit cell, while the maximum indicates completion of a full unit cell (see figure 2.2(f)). Figure 2.2(e) shows the RHEED oscillations of 76 unit cells LAO deposited at 770°C. Figure 2.2(f) which is a zoom-in to panel (e) reveals the growth rate of 32 pulse per unit cell. Figure 2.2(c) is the RHEED diffraction pattern of the STO substrate, recorded before the growth. The streaky features, indicated with white arrows arise due to atomically flat surface of STO. These features are still visible, in figure 2.2(d), after the deposition of 76 unit cell LAO which confirms the epitaxial (layer-by-layer) growth of LAO on STO.

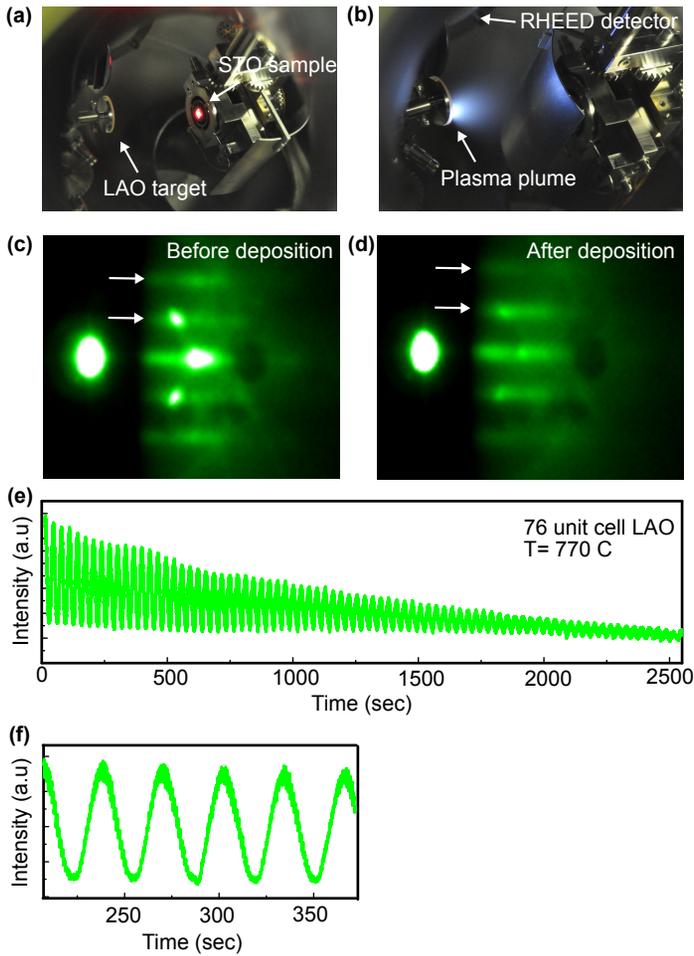


Figure 2.2: **PLD and in-situ RHEED for monitoring the growth.** (a) shows the sample-target orientation during the LAO growth. Sample to target distance is 55 cm. (b) shows the generated plasma-plume upon delivering the UV-laser pulse to the LAO target at an oxygen pressure of $P_{O_2} = 6 \times 10^{-5}$ mbar and fluency of 1 J/cm^2 . (c-d) are the RHEED diffraction pattern before and after the LAO deposition, respectively. White arrows indicate that the streaky features of atomically flat surface of TiO₂-STO substrate is preserved after the growth of 76 unit cell LAO. (e-f) show the RHEED oscillations monitored during the deposition. Maximum of the oscillations correspond to completion of a full unit cell per 32 laser pulses.

2.1.3. ATOMIC FORCE MICROSCOPY

We use Bruker© Dimension Fast Scan AFM to characterize our nanoscale structures. AFM is a high resolution scanning probe microscopy technique and offers visualization of features down to sub-nanometer scale. It uses an atomically thin tip connected to a cantilever which is scanned over a sample surface. The deflection of the tip along the surface is sensed with a laser light directed onto the cantilever and processed to offer topological information of the surface. A typical atomic force microscopy image (AFM) image of 12 unit cell LAO sample is given in the left panel of figure 2.3 and shows the step and terrace structure of STO substrate, confirming high quality of the growth. Right panel shows the nanoscale top gated device (E-SQUID, see Chapter 4).

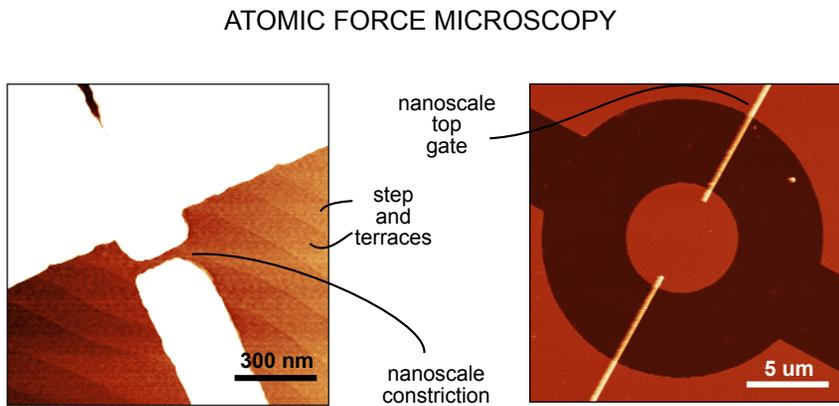


Figure 2.3: **AFM images of nanoscale devices at LAO/STO interface.** Left: AFM image of 12 unit cell LAO sample shows step and terrace structures of the STO substrate, confirms the quality of the fabrication. Constriction width is approximately 60 nm. Right: AFM image of nanoscale top gated device (E-SQUID).

2.2. FABRICATION DETAILS

After explaining the techniques that we use for nanoscale top gated devices, in this section we cover the fabrication details. Figure 2.4 shows the fabrication flow of the nanoscale top gated devices. Device specific details can be found at the end of each chapter. Fabrication of the devices starts with single crystal TiO_2 -terminated SrTiO_3 ((001) crystal direction, $5 \times 5 \times 0.5 \text{ mm}^3$) substrates that are purchased from CrysTec GmbH© and used without any further modification.

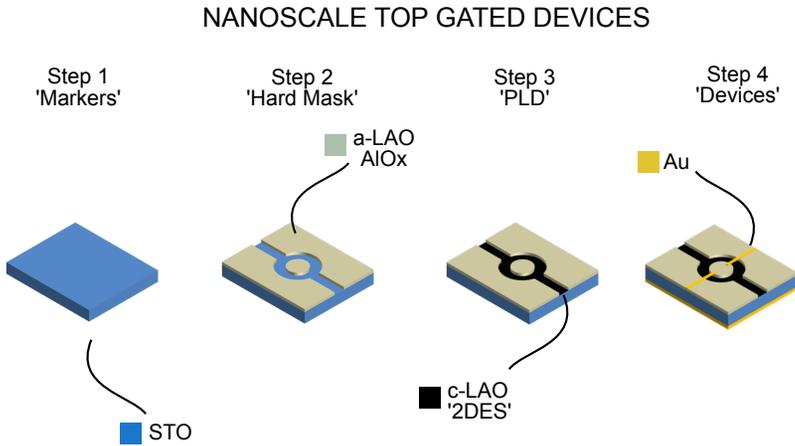


Figure 2.4: **Fabrication flow of nanoscale top gated devices.** Multiple steps of aligned EBL in combination with PLD fabricates the nanoscale top gated devices.

2.2.1. STEP 1: MARKERS

The first step of the fabrication is to pattern the reference markers using EBL. Prior to EBL, samples are typically spin coated with double layer positive resist (PMMA 495K/950K) at 4000 rpm and baked at 175 °C for 15 minutes. The total thickness of the resist layer is 300 nm (495K (100 nm)/950K (200 nm)). Moreover, samples are also coated with water soluble conducting polymer which prevents charging during the lithography process (Aquasave from Mitsubishi Rayon or Elektra91). The conducting polymer is baked at 110 °C for 1 min. Typical doses for the electron beam lithography are 800-900 $\mu\text{C}/\text{cm}^2$. After the exposure, the conducting polymer is dissolved first by soaking in water for 2 minutes. PMMA is developed in MIBK:IPA (1:3 in vol.) solution for 90 seconds followed by an IPA rinse.

In order to do well aligned EBL, it is necessary to have good quality markers that can survive high temperatures during the crystalline LAO (c-LAO) growth. We therefore make use of tungsten (W). W is deposited via RF-sputtering (Alliance Concept© AC450) at a pressure of 20 μbar . The approximate thickness of the W is 60 nm, and we remove the resist by ultrasonic lift-off in acetone.

2.2.2. STEP 2: HARD MASK

The next step is to pattern the hard mask which renders the insulating regions on STO substrate. The hard mask separates c-LAO from STO, preventing the formation of the 2DES. We use either amorphous-LAO (a-LAO) or AlO_x as hard mask material. Amorphous LAO is deposited at room temperature by PLD at a pressure of $P_{\text{O}_2} =$

6×10^{-5} mbar, 5 Hz repetition rate and a fluency of 1 J/cm^2 . AlO_x , on the other hand, is RF-sputtered at a pressure of $3 \mu\text{bar}$ using 200 W power and under 20 sccm Ar flow. Approximate thickness of the hard mask material is around 30-40 nm. This step is followed by ultrasonic lift-off in acetone. Figure 2.5(a) shows an optical image of the sample after lift-off. Dark regions correspond to the patterned insulating areas. Light regions will host the 2DES after LAO growth.

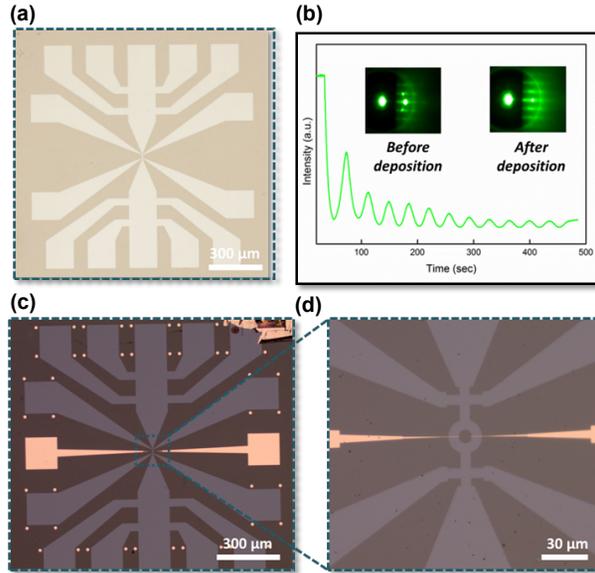


Figure 2.5: **Fabrication overview of the E-SQUIDS.** (a) 'Hard Mask Patterning': optical image after deposition of the amorphous LAO mask. (b) 'PLD': RHEED oscillations obtained during the growth of 12 unit cell c-LAO. Inset shows diffraction patterns before/after the growth. (c-d) 'Devices': optical image after top gates deposition. (d) Zoom in of (c) showing the active area of an E-SQUID device.

2.2.3. STEP 3: OXIDE GROWTH

The pre-patterned sample is attached to a heater stage with epoxy paste which is then cured for an hour at $120 \text{ }^\circ\text{C}$ in ambient atmosphere using an industrial furnace. Then, the sample is loaded into the PLD chamber with a base pressure of $P_{\text{base}} = 3 \times 10^{-8}$ mbar. The fluency of the excimer laser is set to 1 J/cm^2 . The chamber is filled with O_2 ($P_{\text{O}_2} = 6 \times 10^{-5}$ mbar). Sample to target distance is 55 cm. Figure 2.2(a) shows the sample-target orientation during the growth. Prior to deposition, the LAO target is cleaned by an ablation procedure (5 Hz, 2000 pulses). The sample is heated from the backside using the IR-laser with a ramp rate of $10 \text{ }^\circ\text{C/min}$. Temperature of

the substrate is measured using a laser pyrometer. When the growth temperature is reached (770 °C or 840 °C), the sample is aligned for in-situ RHEED. A typical RHEED diffraction pattern before the growth can be seen in figure 2.2(c). The streaky features shown by white arrow are due to the atomically flat two dimensional surface of TiO₂-STO substrate. Next, we deposit 12 unit cell of LaAlO₃ (1 J/cm² and 1 Hz frequency) while monitoring the growth via in-situ RHEED. Typical RHEED oscillations are shown in figure 2.5(b).

Growth is followed by a post-annealing treatment at 600°C in an oxygen pressure of 300 mbar for 1 hour in order to compensate for oxygen vacancies which might form in the STO substrate during the growth. The sample is then cooled down to room temperature in the same atmosphere.

2.2.4. STEP 4: DEVICES

The last step of the fabrication is to pattern nanoscale top gates. After the EBL, we perform a short oxygen plasma (15 sec, 200 W, 212 sccm O₂ flow, equipped with a Faraday cage) in order to remove possible resist residuals. This step is followed by depositing 100 nm gold (Au) via electron beam evaporation (MB-AJA, $P_{\text{base}} \leq 5 \times 10^{-8}$). The first 20 nm is deposited at a rate of 0.5 Å/sec. Then the rate is increased to 1 Å/sec. Ultrasonic lift-off is avoided to prevent Au from peeling off and thus performed with a *syringe* after keeping the sample in warm acetone (55 °C) overnight. Figure 2.5(c-d) shows an optical image of the nanoscale top gated devices (E-SQUID, see chapter 4).

2.3. MEASUREMENT SETUP

2.3.1. DILUTION REFRIGERATOR

All the devices are characterized using a dilution refrigerator (Leiden Cryogenics©) with a base temperature of 40 mK. A dilution refrigerator is a cryogenic system and provides continuous cooling to milliKelvin temperatures. In a simple picture, it consists of liquid helium (4 K) bath and a dipstick. Figure 2.6 shows our dilution refrigerator. The dipstick carries the sample, all the electrical connections and the cooling unit. When the dipstick is fully inserted into the helium bath, the sample cools down to 4 K. Then, the 1 K pot which is a part of the cooling unit sucks the liquid helium from an opening and cools down the inside of the dipstick to 1 K. Next, isotopes of ³He and ⁴He are sent to the dipstick where they are condensed and form a mixture. Continuous evaporation and condensation of ³He further cools down the sample to the base temperature.

2.3.2. ELECTRONICS

Electrical measurements are performed using a home-built (developed by Raymond Schouten, TU Delft) current-voltage supply module (IVVI module) which is fed by two batteries. Different modules such as current, voltage or high voltage sources

DILUTION REFRIGERATOR

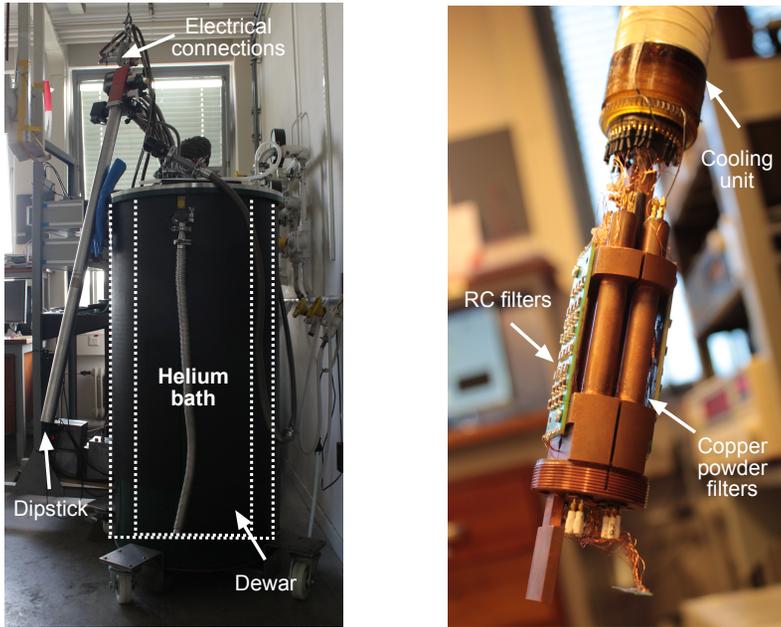


Figure 2.6: Low temperature ($T_{base} = 40$ mK) measurement setup

can be inserted into the IVVI module as shown in figure 2.7. It is controlled with a computer through GPIB connections and driven by optically coupled isolation amplifiers. The matrix module which is connected to the dipstick enables sending and sensing the input/output signals. The electrical line between the IVVI module and the sample includes π , RC and copper powder filters allowing to perform low-noise electrical measurements at mK temperatures (see figure 2.6). Right panel in figure 2.7 shows the chip carrier where sample is attached and electrical connections are created with ultrasonic wedge bonding. The chip carrier is inserted at the end of the dipstick.

2.4. MEASUREMENT CONFIGURATIONS

A typical room temperature characterization of our devices starts with performing leakage tests to the gates through applying voltage and measuring the current. Ideally, top gates should be isolated from the 2DES and thus no significant leakage current is detected (on the order of pA). Next, we characterize the gate action by performing voltage biased measurements. We typically use constant voltages of 1-10

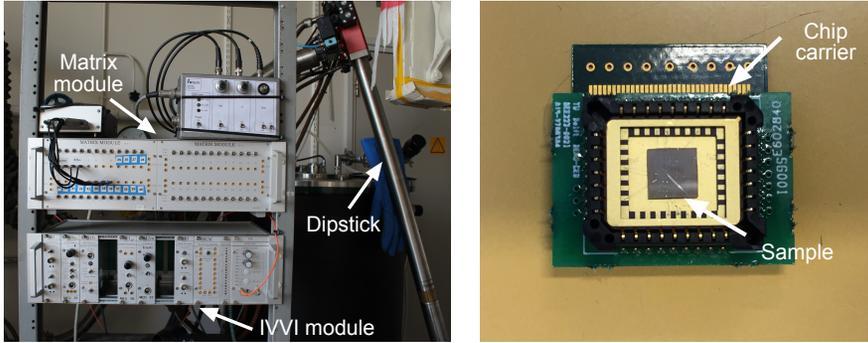


Figure 2.7: **Measurement electronics**

mV while recording the drain current as a function of gate voltages. We limit the gate voltage to ± 8 V in order to prevent damaging the gates. In a typical sample, pinch-off of the channel (i.e. FET operation) is achieved between 2-4 V.

At the temperatures at which the 2DES is superconducting, we characterize our devices in current bias configuration. We typically use ± 200 nA and record the current voltage characteristics of our devices. Moreover, gating experiments involves use of STO substrate as back gate in order to globally tune the electronic properties of the 2DES ($V_{BG} \pm 90$ V). On the other hand, local control on the superconducting properties of the 2DES is achieved through use of the nanoscale top gates.

In regimes where our devices are highly resistive (such as in Chapter 5, Coulomb blockade regime), we use voltage bias configuration for the device characterization. We source voltage across the device and measure the current and the actual voltage drop, simultaneously.

3

NANOSCALE ELECTROSTATIC CONTROL

We develop a robust and versatile platform to define nanostructures at oxide interfaces via patterned top gates. Using $\text{LaAlO}_3/\text{SrTiO}_3$ as a model system, we demonstrate controllable electrostatic confinement of electrons to nanoscale regions in the conducting interface. The excellent gate response, ultra-low leakage currents, and long term stability of these gates allows us to perform a variety of studies in different device geometries from room temperature down to 50 mK. Using a split-gate device we demonstrate the formation of a narrow conducting channel whose width can be controllably reduced via the application of appropriate gate voltages. We also show that a single narrow gate can be used to induce locally a superconducting to insulating transition. Furthermore, in the superconducting regime we see indications of a gate-voltage controlled Josephson effect.

Parts of this chapter have been published in Nano Letters, **15**, 2627 (2015).

3.1. INTRODUCTION

A superconductor can carry a certain amount of current, *supercurrent*, without any dissipation or resistance. Moreover, the magnetic field is expelled by means of dissipationless currents, known as *Meissner effect*. Thus, superconductors are perfect diamagnets. In a superconductor, electron-electron interactions becomes attractive below a critical temperature, T_C , where electrons are bound together and form *Cooper pairs*. The attractive interaction, which overcomes the Coulomb repulsion, arises from the interaction between electrons and the lattice (*phonons*)[†]. Figure 3.1 (a) depicts the mechanism of the Cooper pair formation in a simple cartoon. When an electron flows through a medium, it attracts positive ions and distorts the lattice. Local accumulation of positive charges attracts another, nearby electron. As a result, superconductivity arises if the attractive forces are stronger than Coulomb repulsion of electrons.

Cooper pairs in the superconducting state form a condensate which is protected from electron-like or hole-like excitations (*quasiparticles*) by an energy gap, Δ . Figure 1.5(b) shows the density of states (DOS) of a superconductor in the normal state ($T > T_C$, left panel) and in the superconducting state ($T < T_C$, right panel). An energy gap of Δ opens up symmetrically at the Fermi level, E_F , where there are no DOS for electrons (or holes) to occupy. Furthermore, the superconducting state has long-range macroscopic phase coherence, φ , which can leak to a non-superconducting material over its superconducting coherence length, ξ . Thus, a non-superconducting material can exhibit superconductivity, known as *proximity effect*.

A Josephson junction can be formed by placing a weak link material, having dimensions in the order of ξ , between two superconductors, shown in figure 3.1(c). The weak link creates a phase difference between the two superconductors which results in tunneling of Cooper pairs. Thus, a net supercurrent, *Josephson current*, flows through the weak link given by

$$I_C = I_0 \cdot \sin(\Delta\varphi)$$

where $\Delta\varphi = \varphi_1 - \varphi_2$ and I_0 is the critical current of the Josephson junction. Furthermore, the magnetic field penetrating through the weak link perpendicular to the current direction creates a gradient in the phase across the width of the weak link. This results in a variation of the current density and a reduction in the total critical current. For weak links that are in the short regime[‡] and have uniform critical current density across their width, the critical current oscillates with applied magnetic field according to

[†] Here, phonon-mediated superconductivity is considered for simplicity as it describes most of the known superconductors (i.e conventional superconductors), however attractive interaction can arise due to different mechanisms [53].

[‡] Here, short regime refers to the junctions that are small compared to their characteristic length scale such that self-field effects are negligible. A review on weak links and Josephson effect can be found in [54].

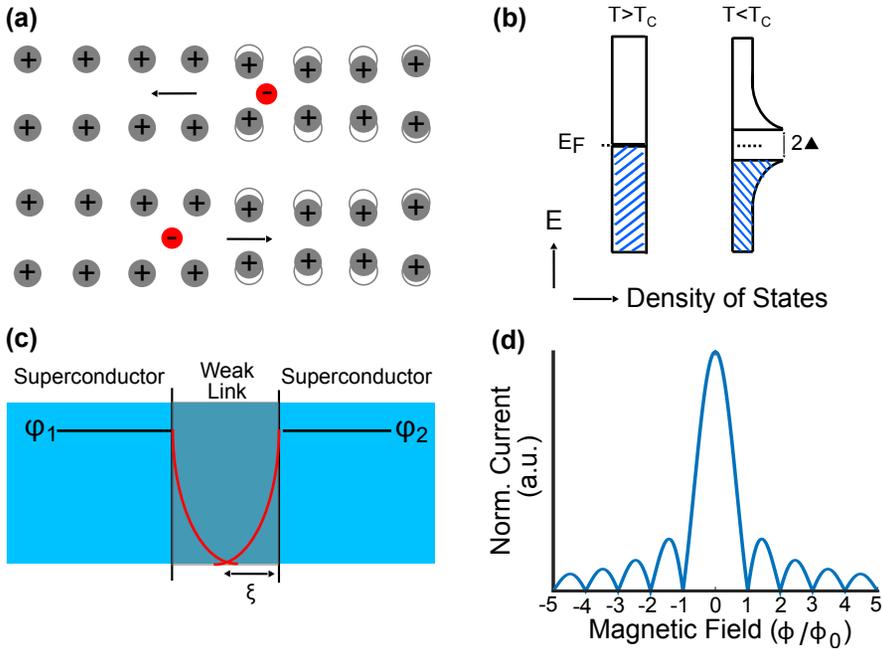


Figure 3.1: **Superconductivity, Proximity effect and Josephson Junctions.** (a) Superconductivity is mediated by attractive electron-electron interactions overcoming the Coulomb repulsion and thus forming paired electrons or *Cooper pairs*. (b) An energy gap of 2Δ at the DOS opens up at the fermi level when a metal undergoes the superconducting transition. (c) Superconducting phase can leak through a non-superconducting material, weak link, over its coherence length, ξ . (d) Fraunhofer pattern is a signature of Josephson junctions that consist of weak link in between two superconductors as in (c).

$$I_0(\Phi) = I_0(0) |\sin(\pi\Phi/\Phi_0)/(\pi\Phi/\Phi_0)|$$

where $\Phi_0 (=h/2e \cong 2.07 \times 10^{-15} \text{ Wb})$ is the flux quantum and $\Phi = (\text{Applied magnetic field}) \times (\text{Area of the weak link})$. Thus, the critical current of the junction becomes zero for every flux quanta passing through weak link. The oscillatory pattern of the critical current is shown in figure 3.1 (d) and known as *Fraunhofer pattern*, which is analogous to the diffraction of light in a single slit experiment.

Josephson junctions (JJs) have been used in many device applications. For example, Superconducting Quantum Interference Devices (SQUIDS), built by two JJs, are used in MRI machines. Moreover, the current voltage standard (1 V) is set by Josephson effect. Furthermore, recent advancements in nanolithography and nanomaterial synthesis have made JJs a unique platform to study microscopic details of superconductivity. Gate-tunable, nanoscale semiconductors have been used as a

weak link where its properties are controlled with in-situ voltages applied to a gate electrode. In these devices; ballistic, gate tunable Josephson junctions (JJ) [55], Andreev bound states (ABS) [56–59] and even-odd parity effects [60, 61] have been shown. Furthermore, one-dimensional (1D) systems connected to superconducting electrodes [62–64] have become a building block for realization of superconducting qubits and search for Majorana fermions [65].

In this chapter, we define nanoscale electronic devices in $\text{LaAlO}_3/\text{SrTiO}_3$ using patterned top gates which efficiently modify the potential landscape at the metallic interface. We demonstrate that individual narrow gates (down to 200 nm) can completely pinch off the conducting channel and display large on/off ratios with negligible leakage currents. Using two such gates in a split-gate geometry, we can further tune the flow of charge carriers by restricting them to a narrow conducting channel with a width that can be controlled in-situ via the gate voltages. At milliKelvin temperatures, when the interface is superconducting we use a single narrow top gate to drive locally a superconducting to insulating transition at the LAO/STO interface. In the superconducting state, we see evidence for a superconducting weak link with a gate-dependent critical current.

3.2. RESULTS

3.2.1. CHARACTERIZATION OF DEVICES

12 unit cell of LAO is grown at 770 °C. Under the growth conditions discussed in chapter 2, the 2DES formed at the LAO/STO interface shows sheet carrier densities of about $3 \times 10^{13} \text{ cm}^{-2}$ and electron mobilities up to $3500 \text{ cm}^2/\text{Vs}$ at 4.2 K in large ($>100 \mu\text{m}$ wide) channels. Figure 3.2(a) shows a cross-sectional schematic of a device with a single top gate. An optical image of such a device is shown in figure 3.2(b), where a narrow ($1 \mu\text{m}$ wide) gate runs across a mesoscopic conducting channel defined at the LAO/STO interface. Figure 3.2(d) shows the gate characteristics of this device (Dev1) at 300 K (see Additional Information for data from similar devices). A constant dc voltage bias of 10 mV is applied across S and D (V_{sd}) and the current (I_{sd}) is measured as a function of the top gate voltage (V_{gate}). The black curve (left axis) shows a typical field effect behavior with complete depletion under the gated region resulting in an on/off ratio of nearly 1000 (shown in the inset). The leakage current (blue trace, right axis) remains below 5 pA in this gate voltage range, thus allowing for reliable measurements of very low currents through the device. The gate width can be reduced even further (in this case to 200 nm), as seen in the (false color) scanning electron microscope (SEM) image of Dev2 (Figure 3.2(c)). In figure 3.2(e) we compare the gate response of Dev1 and Dev2 at $T = 2 \text{ K}$. Both devices (Dev1-black trace, right axis; Dev2-red trace, left axis) show comparable threshold voltages. This is consistent with the fact that they were both fabricated on 12 unit cell LAO deposited under the same growth conditions. We note that each curve consist of 10 consecutive sweeps between the on and off states. It is clear that the device completely recovers from the

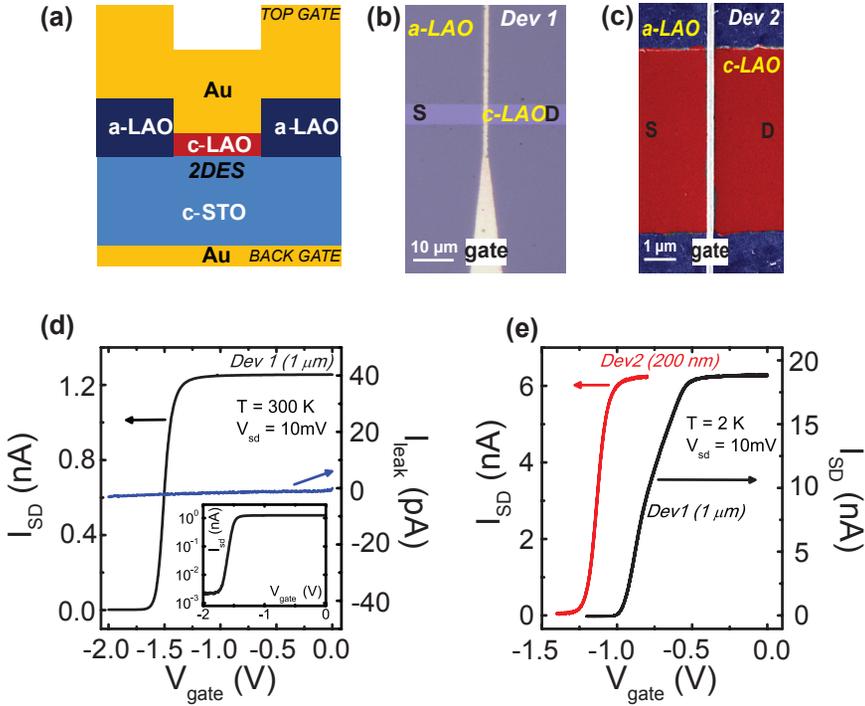


Figure 3.2: **Device description and basic characterization.** (a) Cross-sectional schematic of a typical top gated LAO/STO device. The 2DES (indicated in black) is formed at the interface between crystalline LAO (c-LAO) and STO (c-STO). The interface between amorphous LAO (a-LAO) and STO remains insulating. (b) Optical image of Dev1 with a $1\ \mu\text{m}$ wide gate running over the c-LAO. (c) False color scanning electron micrograph of Dev2, which consists of a $200\ \text{nm}$ wide top gate. Red/blue areas correspond to conducting/insulating regions. See Appendix B for full device drawings with the relevant channel dimensions. (d) Gate characteristics for Dev1 at $300\ \text{K}$. Black curve (left axis) shows the variation of source drain current (I_{sd}) with top gate voltage (V_{gate}). Inset: the same curve on a logarithmic scale. Blue curve (right axis) shows the leakage current (I_{leak}) vs. V_{gate} . (e) Gate response of Dev1 and Dev2 at $2\ \text{K}$. Each curve consists of 10 consecutive down sweeps from the on to off state.

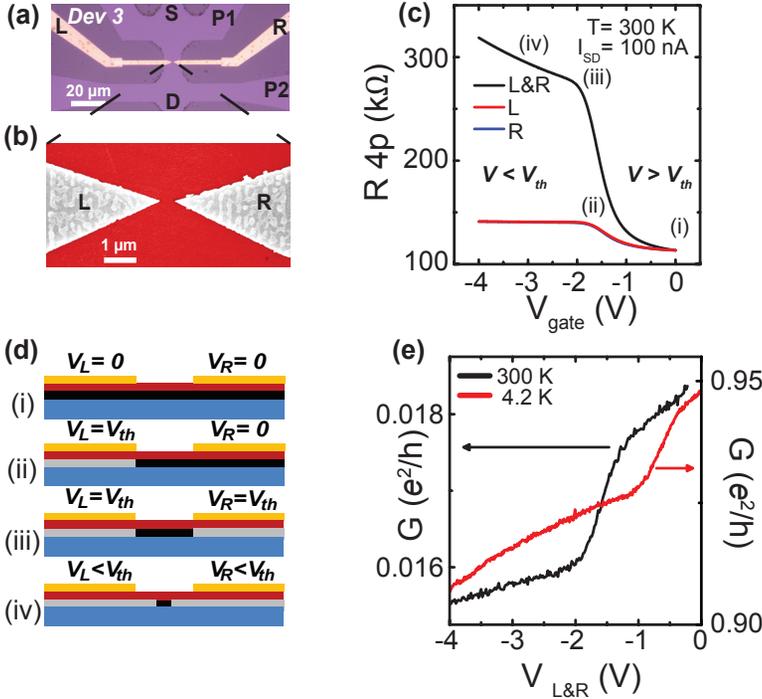


Figure 3.3: **Nanoscale split gates at LAO/STO interface.** (a) Optical and (b) SEM images of a split gate (SG) device which comprises of a left (L) and right (R) gate. (c) Four-probe resistance (R_{4p}) measurements (at 300 K) comparing the gate action of the individual gates (red and blue curves) with that of both gates together (black curve). Note that the red and blue curves show an excellent overlap, which makes it hard to distinguish between the two in the plot. The labels [(i)-(iv)] mark different transport regimes in the operation of the SG device. The corresponding density variations at the LAO/STO interface are shown schematically in (d), where black/gray represent conducting/insulating regions in the 2DES. (e) Two-probe voltage biased measurements: Conductance, G vs. $V_{L\&R}$ at 300 K (black curve) and 4.2 K (red curve). See Appendix B for device drawings with the relevant channel dimensions.

insulating state, and is extremely stable over multiple on/off cycles. This is in contrast with recent measurements on bulk top gated LAO/STO devices where (at low temperatures) going above a critical resistance rendered the interface completely insulating, and conduction could only be revived by thermal cycling [49]. We point out that the two-terminal resistance values are significantly higher than those expected from the bulk mobility and density values mentioned earlier. This discrepancy most likely arises from a contact resistance and/or local regions in the long narrow channel with a significantly higher resistivity.

Having established a reliable gate response from our local top gates we use *two*

such gates to realize a split gate (SG) geometry, using which charge carriers can be confined to narrow conducting channels. SGs have been successfully used to fabricate quantum point contacts (QPCs) in semiconductor-based 2DESs [43, 44], and have provided insights into several aspects of mesoscopic physics (reviewed in [45]) ranging from the quantum Hall effect to the Aharonov-Bohm effect. They are also extremely sensitive charge detectors [66] and spin filters [67], and serve as essential components for the creation of lower dimensional systems such as quantum dots [42]. At the LAO/STO interface, such one-dimensional (1D) confinement could possibly give rise to exotic electronic states that emerge from the interplay between 1D superconductivity and SOC [68]. Figure 3.3(a) shows an optical micrograph of a SG device on LAO/STO. It consists of a left (L) and right (R) gate, both of which start off $2.5 \mu\text{m}$ wide and taper down to a narrow point. Figure 3.3(b) shows an SEM image of the active device region. We have studied devices with tip separations of approximately 400 nm (Dev3) and 250 nm (Dev4), and both show qualitatively similar features. Here we focus on Dev3 (results from Dev4 can be found in the Additional Information)

We begin by studying the room temperature four probe resistance (R_{4p}) across the SG, as a function of the individual (L, R) gates. A 100 nA dc current is applied between S and D (I_{sd}), and resistance is measured between contacts P1 and P2 (see figure 3.3(a)). For these measurements no back gate voltage was applied. When the SG is held at zero ($V_L = V_R = 0$), the carrier density in the entire channel is uniform. This is shown schematically in figure 3.3(d) (top panel), where the uniform black area represents a wide channel with no density variations. The corresponding point in the R_{4p} vs V_{gate} plot (Figure 3.3(c)) is marked by the label (i). As one of the gates (say L) is made more negative, the carriers below this gate are depleted, resulting in a sharp increase in R_{4p} (red curve). However, at a critical threshold voltage (V_{th}) the region below R is completely depleted, indicated by (ii) in figure 3.3(c-d) (gray areas represent depleted regions in the 2DES). Throughout, we define V_{th} as the gate voltage where the magnitude of this slope is maximum. Beyond V_{th} the gate action is weaker, since depletion must now occur sideways, thereby resulting in a lower slope in the R_{4p} vs. V_{gate} curve. Sweeping only L (instead of R) should be electrostatically equivalent to the situation described above. This is reflected directly in transport by the excellent overlap between the red and blue curves. If *both* R, L are swept together the response is much stronger (black curve). When $V_L = V_R = V_{th}$ [label (iii)] a narrow constriction is formed in the 2DES, whose width is determined by the geometry of the split gates and the electrostatics of the system. Finally, going to even more negative voltages with L and R together [label (iv)] squeezes this channel further. Thus, through an appropriate device design and suitable gate voltages, it is clearly possible to electrostatically define nanoscale constrictions at an oxide interface, even at room temperature.

Next, we study this SG device (Dev3) at cryogenic temperatures in a two probe

configuration. Figure 3.3(e) shows the variation of the conductance (G) with $V_{L\&R}$ (i.e., both L and R swept together) at 300 K (black curve, left axis) and 4.2 K (red curve, right axis). Two things are immediately apparent from these plots. Firstly, the conductivity of the system increases significantly as the temperature is lowered, which is expected for such metallic samples. Secondly, V_{th} shifts to less negative voltages upon cooling down. It has been suggested that the sheet density can reduce with temperature as a result of carrier freeze-out [69]. Such a reduction in the sheet density with temperature could qualitatively explain the observed shift in V_{th} , since it now becomes much easier for the SG to deplete the carriers. However, at these temperatures an even more striking effect appears in the gate response of the SGs, which only becomes apparent through detailed phase space maps of the conductance *vs.* the individual gates.

Figure 3.4(a-b) show two such maps of G , at 300 K and 4.2 K respectively. It is worth pointing out that these maps are typically acquired over several hours, during which the device does not show any switches or obvious drifts, confirming the stability and robustness of these gates. Furthermore, both gates (L and R) have a nearly identical influence on the 2DES at the interface. This is evident from the high degree of symmetry across the diagonal (white dashed line). Such a symmetric response of the two gates can be expected if the 2DES has a homogeneous density. However, inhomogeneities in the gated regions could give rise to a reduction in this symmetry (as seen for Dev4 in the Additional Information). The entire phase space can be divided into two distinct regions. The blue portion (lower G) corresponds to a situation when both L and R have been driven beyond their respective threshold voltages. The red area (higher G), thus reflects the complementary scenario, where either one (or none) of the gates have crossed V_{th} (black circles indicate the position of V_{th} for each of the gates with the other held at zero). The narrow white band therefore separates these two electrostatically distinct regimes and provides information about the effective region of influence of the individual gates, and the extent of cross-talk between them. These effects can be examined in a more consistent manner by taking a derivative along one of the gate axes.

Figure 3.4(c-d) show the corresponding numerical derivatives taken along the V_R axis (dG/dV_R). As mentioned earlier, the maximum in dG/dV_R occurs at V_{th} associated with gate R. At 300 K, as V_L is made more negative the position of the threshold does not change, indicating that there is practically no cross-talk between the gates. This is perhaps not so surprising considering the fact that the gates are very close (~ 5 nm) to the interface, and therefore most of the electric field lines go directly downwards, creating a sharp potential profile with minimal spreading of the the electric field. However, at 4.2 K the situation is rather different. V_L obviously has a distinct effect on the threshold voltage for R, shifting it to less negative voltages, as V_L becomes more negative. This suggests that V_L has a significant influence on the region below R, in contrast with the observations at 300 K. Such a modifica-

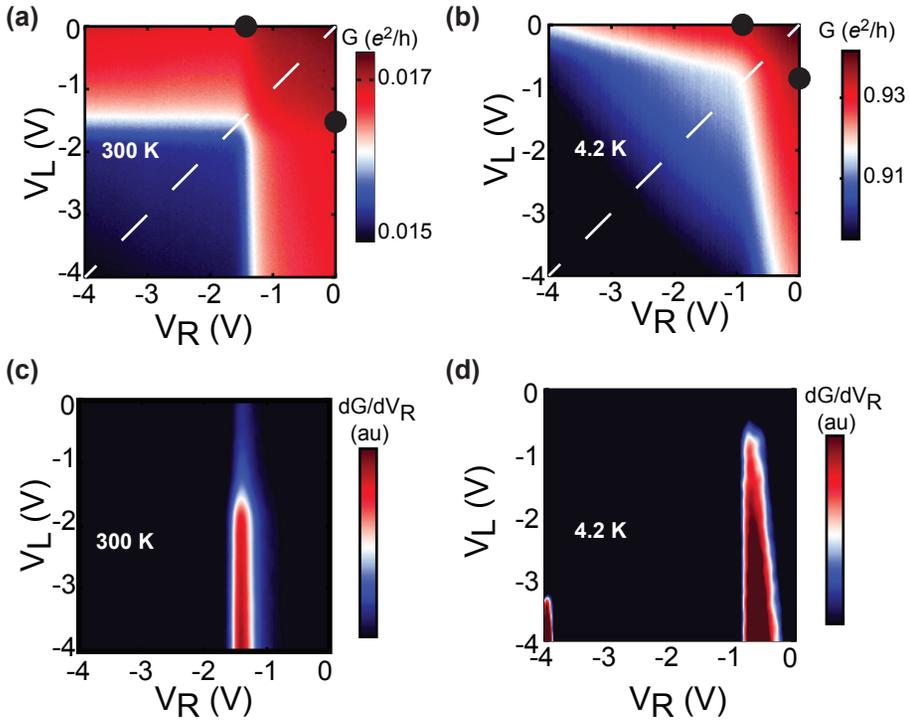


Figure 3.4: **Nanoscale split gates at 4 K.** (a) 2D conductance (G) maps as a function of left/right (L/R) split gate voltages (V_L/V_R) at $T = 300$ K and (b) $T = 4.2$ K. The gate voltage step (for both V_L and V_R) is 20 mV. Black circles mark the positions of the threshold voltage for either gate, with the other held at zero. Symmetry about the white dashed line indicates comparable gate action from both L and R. (c)&(d) show plots of the corresponding numerical derivatives taken along the V_R axis (dG/dV_R). The maximum in dG/dV_R indicates the threshold voltage for gate R. It is independent of V_L at 300 K, but shows a distinct shift at 4.2 K, indicating cross-talk between L and R at low temperatures. We note that the second maximum at low values of V_L in (d) is an artifact due to numerical derivation.

tion of the electrostatics could possibly be related to the fact that STO is an incipient ferroelectric, thereby exhibiting a strong increase in its permittivity at low temperatures [70]. A combination of this large permittivity ($\sim 10^4$ at $T = 4$ K) along with imperfect screening from the 2DES, could provide a viable mechanism for the observed cross-talk between the gates. As the carrier density below L is reduced, the extent of screening from the 2DES below L reduces. This, in turn, allows electric field lines to go *through* the STO, resulting in a significant field effect in the region below R. Though a likely explanation, the feasibility of such a scenario ultimately needs to be

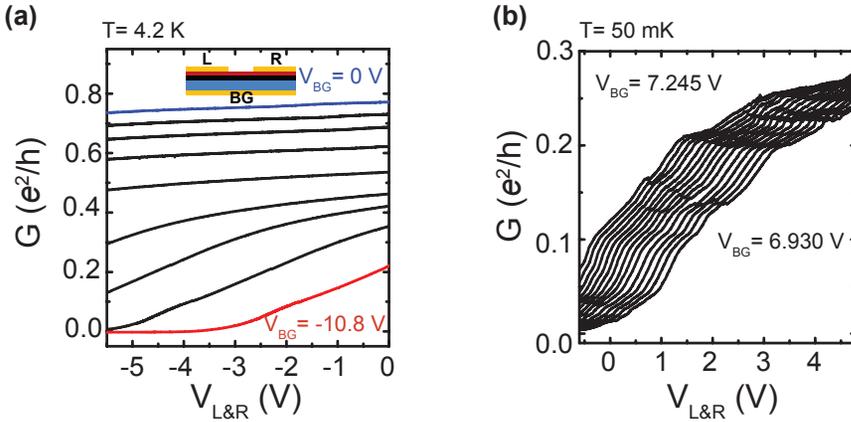


Figure 3.5: **Mesoscopic fluctuations in nano-constriction.** (a) The conductance (G) of the nano-constriction formed by the split gates can also be tuned using the back gate (BG). While G does not change appreciably with $V_{L\&R}$ when $V_{BG} = 0$ V (blue curve, a similar trace is also shown in figure 3.3e), for $V_{BG} = -10.8$ V it is possible to completely deplete the channel using split gates (red curve). Intermediate (black) curves correspond to $V_{BG} = -1.8$ V, -3.6 V, -5.85 V, -8.1 V, -9.45 V, and -10.35 V. (b) Modulation of G with $V_{L\&R}$ at milliKelvin temperatures due to mesoscopic effects in the conducting channel. The modulations evolve continuously as a function of BG.

tested using electrostatic simulations with appropriate parameters for the screening lengths at the LAO/STO interface.

In addition to local top gates, the global back gate can also modify the electrostatics at the interface, thus providing additional control over transport through electrostatically defined nanostructures. Though our SG devices show clear evidence of confinement, the relatively large separation between the gates (as compared to the distance of the gates from the 2DES) makes it difficult to pinch off the channel using just the top gates. However, by reducing the sheet carrier density via moderate negative voltages on the back gate (BG), we could indeed deplete the constriction completely, as seen in figure 3.5(a). In this geometry the entire 0.5 mm thick STO substrate is used as the gate dielectric. At $V_{BG} = 0$ V the channel remains fairly open in this gate voltage range (blue trace), but shows a clear pinch-off for $V_{BG} = -10.8$ V (red trace). We note that in all the devices studied here, we observed a strong hysteresis in the BG action at low temperatures. As the BG is taken to positive values, G typically saturates for $V_{BG} > 20$ V. Subsequently, going back to $V_{BG} = 0$ V renders the sample highly insulating. However, the conductance can be completely recovered by taking the top gate to positive voltages, which suggests that the effect arises primarily from the region below the local gates. Such an effect was not observed in larger Hall bars (channel width ~ 500 μm), fabricated in a similar fashion, but without top gates.

Figure 3.5(b) shows the variation of G with $V_{L\&R}$ at $T=50$ mK for a small range of BG voltages. This data was obtained after the BG was first swept up to 22.5 V and then reduced to 7.245 V. As described above, at $V_{L\&R} = 0$ V the sample is now less conductive, but sweeping $V_{L\&R}$ to positive values increases I_{sd} . It is also evident that there is a finer structure that emerges at these low temperatures, which is clearly absent at $T=4.2$ K (Figure 3.5(a)). These modulations in conductance are highly reproducible and show a continuous evolution with V_{BG} . We attribute this structure to mesoscopic effects which arise from disorder in the conducting channel. We believe that the integration of such split-gate devices with higher mobility oxide interfaces with significantly longer mean free paths [69, 71] should enable studies of mesoscopic transport in the 1D limit.

3.2.2. LOCAL CONTROL ON SUPERCONDUCTIVITY

Thus far we have concentrated on the flow of normal electrons through devices defined via local top gates. Of course, one of the remarkable properties of the LAO/STO interface is that it can also host 2D-superconductivity [72]. Furthermore, bulk studies have shown that reducing the carrier density at the interface with a global back gate results in a quantum phase transition (QPT) between superconducting and insulating ground states [73]. The ability to *locally* alter the ground state of the interface at the nanoscale provides the opportunity to create gate-tunable superconducting circuit elements (e.g., Josephson junctions), which may enhance our understanding of the microscopic nature of superconductivity at the interface. To study the effects of a local top gate on the superconductivity we cooled down Dev2 (see figure 3.2(c) for SEM image) to $T=50$ mK, and recorded current-voltage (I-V) characteristics as a function of V_{gate} in a four probe configuration (with BG fixed at zero). In figure 3.6(a) we plot a few representative I-V traces at different values of V_{gate} (inset shows a to-scale schematic of the measurement configuration). These curves show a clear transition from a superconducting state ($V_{gate} = 0$ V, black trace) to an insulating state as V_{gate} is made more negative. This insulating state is evident from a gap-like structure that emerges for $V_{gate} < -0.9$ V, and grows in size as the gate voltage is further reduced. Though previous studies with large top gates have shown some gate dependent modulation of the critical current [49], we believe that a local superconducting-insulating transition has thus far not been observed at the LAO/STO interface.

Figure 3.6(b) shows a 2D plot of differential resistance dV/dI (obtained via numerical differentiation of the gate-dependent I-V traces) as a function of V_{gate} and I . Two important features to note in this plot are (i) strong peaks which occur at relatively high currents (10 - 15 nA) and (ii) a weaker peak at much lower currents (< 3 nA), which closes as V_{gate} is made more negative and finally disappears around the superconducting-insulating transition. The stronger set of peaks reflect the current driven superconducting to normal transition in the areas outside the top gated

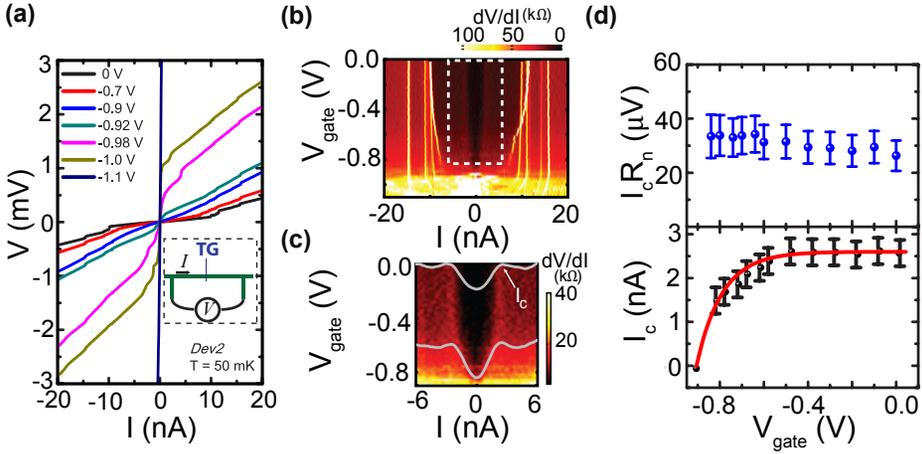


Figure 3.6: **Local control on superconductivity** (a) A local superconducting to insulating transition induced by the top gate. Inset: schematic (to-scale) of the device and measurement configuration. (b) 2D map of differential resistance (dV/dI) as a function of I and V_{gate} . (c) A closer view of the region enclosed by the dashed lines in (b), with line traces at $V_{gate} = 0$ V and $V_{gate} = -0.6$ V. (d) Lower and upper panels show the critical current (I_c) and $I_c R_n$ product respectively of a gate-tunable weak link. Red line is a guide to the eye.

region (we comment further on them towards the end of this section). To understand the origin of the strongly gate-dependent structure at lower currents, we explore the possibility that the region under the top gate acts as a weak link between the superconducting reservoirs on either side. Figure 3.6(c) shows the dV/dI map in a smaller range (indicated by dashed rectangle in figure 3.6(b)) with two representative line traces at $V_{gate} = 0$ V and $V_{gate} = -0.6$ V. We start by associating a critical current (I_c) with the first local maximum in dV/dI . Figure 3.6(d) (lower panel) shows that I_c is roughly constant from $V_{gate} = 0$ V to $V_{gate} = -0.5$ V, below which it begins to drop more rapidly and finally disappears at $V_{gate} = -0.92$ V (red line is a guide to the eye). In the upper panel we plot the product of I_c and R_n (where R_n is the resistance just above I_c), which remains roughly constant over the entire gate voltage range, a characteristic signature of a Josephson junction. For $T \ll T_c$ (T_c is the critical temperature of the superconducting reservoirs), we expect $eI_c R_n \approx \alpha \Delta$, where Δ is the superconducting gap in the reservoirs, e is the electronic charge, and α depends on the microscopic details of the weak link and can take values from $\sim 1.5 - 3$ [54]. The weak link can in general be a tunnel barrier, a superconductor or a normal metal. Interestingly, for the LAO/STO system all three scenarios are possible, and the current experiments cannot precisely determine the actual microscopic nature of the weak link. However, using the fact that we experimentally determine $eI_c R_n \sim 30 \mu\text{eV}$, we estimate that $\Delta \sim 10 - 20 \mu\text{eV}$. Though these values are slightly smaller (roughly by a

factor of 3) than recent measurements of Δ via tunneling spectroscopy [74], they are consistent with the lower $T_c \sim 100$ mK of our samples (see Additional Information). We note that similar observations of a gate-tunable weak link at the surface of STO have also recently been reported [75].

3.3. DISCUSSION

Finally, we remark on the evolution of the peaks in dV/dI at higher values of I and associated with superconducting-normal switching of the area outside the top gated region. We associate the multiple switches with inhomogeneities in the long (150 μm) and narrow (5 μm) conducting channel across which the measurements were performed. Most of the peaks run parallel to each other, showing hardly any gate-dependent shifts till about $V_{gate} = -0.9$ V, which is close to where the superconducting to insulating transition occurs. Interestingly, below $V_{gate} = -0.9$ V these peaks start coming together more rapidly. Though we do not have a complete understanding of this behavior at the moment, we present two possible explanations. The first possibility is that the significantly higher resistance of the insulating state gives rise to Joule heating which increases the local electronic temperature, thereby reducing the critical current of the neighboring regions. The second possibility relates to the earlier discussion (in the context of split gates), whereby electric field lines from the top gate could potentially spread out significantly once the density below the gate is reduced. In this scenario, the evolution of the peaks could be explained by the fact that the electrostatic region of influence of the top gate extends significantly beyond its geometric dimensions, thereby reducing the critical current in the neighboring regions. In contrast to our current device geometry, we believe that devices with significantly wider superconducting banks would be more suitable for the study of the Josephson effect. In such devices the un-gated regions would have a much larger critical current than the weak link, and the strong influence of local inhomogeneities could possibly be suppressed, thereby allowing for a clearer interpretation of the results.

3.4. CONCLUSIONS

In conclusion, we have demonstrated that top gating can be used to create electrostatically confined nanostructures at the LAO/STO interface. These gates show excellent performance and stability from room temperature down to 50 mK. Not only do they allow us to control the electrostatic landscape through which normal electrons flow, they provide a promising route to locally control the electronic ground state of the interface. The inherent flexibility in the design of such top-gated structures opens up a new and versatile platform for creating a variety of gate-tunable nanostructures at oxide interfaces.

3.5. ADDITIONAL INFORMATION

3.5.1. FABRICATION SPECIFICS

Figure 3.7(a) shows a complete flowchart of the various steps involved in the fabrication of the devices discussed in this chapter (Dev1, Dev2, and Dev3) as well those discussed later in the additional information. Bold black arrows show the process flow used to fabricate the split gate (SG) device discussed in detail (Dev3). Figure 3.7(b) shows optical images of Dev3 at different stages of the device fabrication corresponding to labels [(i)-(iii)] in figure 3.7(a). The blue/red arrows correspond to Dev1/Dev2 respectively. Dev4, Dev5 and Dev6 (described in figure 3.9) are fabricated in a similar fashion to Dev3, Dev1, and Dev2 respectively.

Dev1 is patterned using photolithography (PL). PL is performed using a deep-UV Karl Suss MJB3 mask aligner. The sample is coated with S1805 photoresist followed

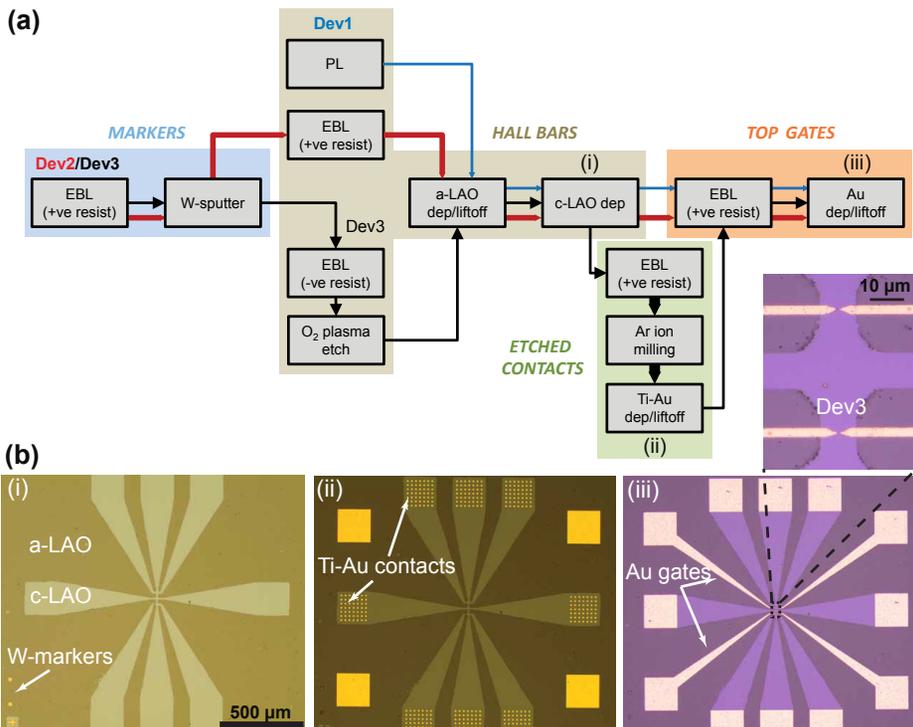


Figure 3.7: (a) Device fabrication flowchart (see text for details). (b) Optical microscope images for Dev3 at various different stages of the fabrication process corresponding to labels (i)-(iii) in (a). The differences in colors between the three images are only a result of different camera settings, and not related to the processes themselves.

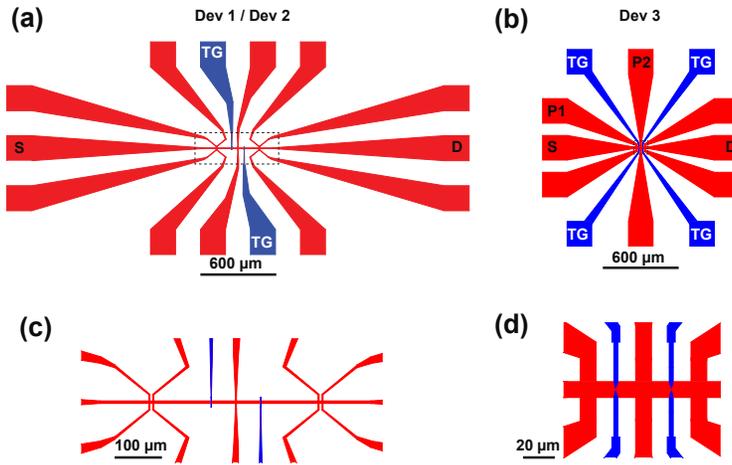


Figure 3.8: (a) Device drawing for Dev1 and Dev2 in main text showing the contacts (S and D) used for two-probe measurements. Red regions correspond to the conducting 2DES and blue regions are the top gates. (b) Similar drawing for the split gate device Dev3 in the main text. P1 and P2 are voltage probes used for four-probe measurements. (c),(d) show close-ups of regions indicated by dashed lines in (a),(b) respectively. The channel widths in the active device region are 5 μm (Dev1/Dev2) and 10 μm (Dev3).

by UV exposure. For Dev3/Dev4 we used a combination of PMMA 495K (100 nm thick) and HSQ (50 nm thick) to define the amorphous LAO (a-LAO) mask. HSQ is a negative resist and therefore allows us to expose only the region that must be protected during the subsequent a-LAO growth. HSQ is developed in TMAH (12.5% solution in H_2O), followed by an H_2O and IPA rinse. Typical dose for the electron beam lithography is 650 $\mu\text{C}/\text{cm}^2$ for HSQ. Ti/Au (20 nm/50 nm) is deposited after Ar ion milling to make ohmic contacts (in devices where no milling was performed, contacts were made by direct wedge bonding to the interface).

3.5.2. DATA FROM OTHER DEVICES

Figure 3.9 shows data from three other devices that complement the results. Figure 3.9(a) inset shows a device (Dev5) with a 5 μm wide gate across the conducting channel. The device characteristics are very similar to those of Dev1 (described in main text), in terms of the on/off ratio and leakage current. We also study transport through a device with two gates in series (Dev6). The 2D current map in figure 3.9(b) shows that the two gates act independently of one another, with no cross-talk. Figure 3.9(c) shows individual traces taken along the positions marked by the red/black arrows in figure 3.9(b). It can clearly be seen that a more negative value of V_{G1} merely reduces the overall conductance of the channel, without affecting the pinch-off volt-

age for gate G2.

In addition to the split-gate device discussed in this chapter (Dev3), we study another device (Dev4) in the same geometry, with a gate separation (tip to tip) of about 250 nm. Figure 3.9(d) shows the room temperature variation in four-probe resistance (R_{4p}) with just the left gate (L), right gate (R), and both together (L&R). Inset shows a (false color) SEM image of the device. A comparison with figure 3.3(b) shows qualitatively similar behavior to Dev3, however there is some asymmetry in the action of L and R. This is most likely a result of some local inhomogeneity in the device region. Figure 3.9(e) shows a 2D map of R_{4p} vs. V_L , V_R . Both the R_{4p} map and the derivative along V_R (Figure 3.9(f)) look very similar to Dev3 (main text), indicating minimal cross-talk between the gates.

We note that none of the devices studied showed any significant leakage at room temperature. However, we did observe some spread in the pinch-off (threshold) voltage, which varied between -1.5 V and -2.5 V.

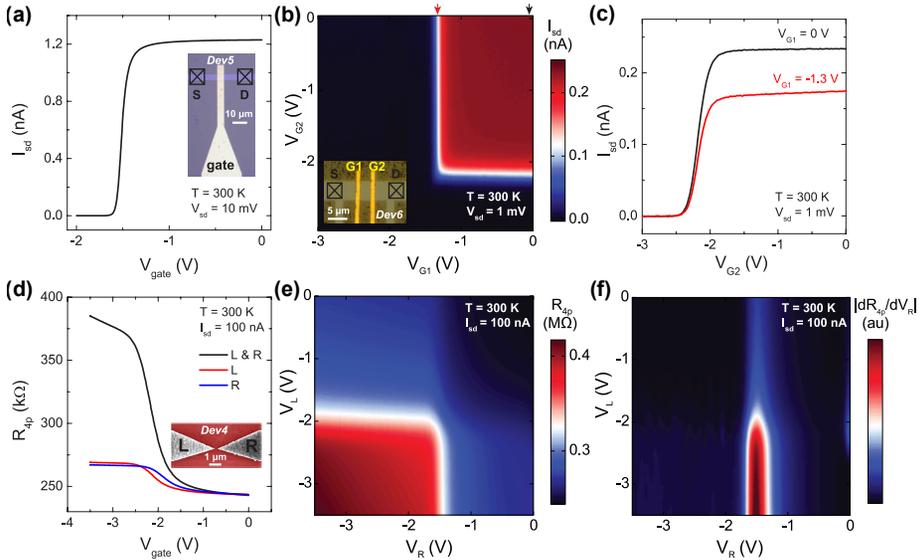


Figure 3.9: (a) Gate characteristics of a 5 μm wide single gated device (Dev5). (b) 2D map of the current for a device (Dev6) with two gates in series. Inset shows an optical image of the device. (c) Red/black correspond to individual traces taken along the positions marked by red/black arrows in (b). (d) Gate response of a split gate device (Dev4) similar to Dev3, described in the main text. Inset shows SEM image of the device. (e) 2D map of the four-probe resistance (R_{4p}) vs. the left (L) and right (R) gate voltages for Dev4. (f) Absolute value of the derivative of (e) along the V_R axis.

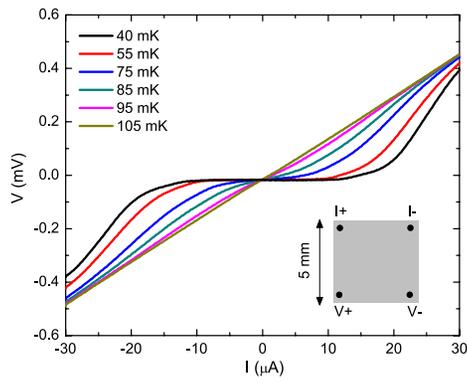


Figure 3.10: I-V characteristics of a bulk sample showing a critical temperature $T_c \sim 100$ mK. Measurements were performed in a van der Pauw geometry, as shown in the inset.

4

QUANTUM INTERFERENCE

Here, we perform phase-sensitive measurements by realizing the first superconducting quantum interference devices (SQUIDs) at the LAO/STO interface. Furthermore, we develop a new paradigm for the creation of superconducting circuit elements, where local gates enable in-situ creation and control of Josephson junctions. These gate-defined SQUIDs are unique in that the entire device is made from a single superconductor with purely electrostatic interfaces between the superconducting reservoir and the weak link. We complement our experiments with numerical simulations and show that the low superfluid density of this interfacial superconductor results in a large, gate-controllable kinetic inductance of the SQUID. Our observation of robust quantum interference opens up a new pathway to understand the nature of superconductivity at oxide interfaces.

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4.1. INTRODUCTION

A superconducting quantum interference device (SQUID) consists of two Josephson junctions (JJs) embedded in a superconducting loop and can be represented by the resistively- and capacitively shunted junction (RCSJ) model. Each of Josephson junctions has a critical current (I_0) and connected in parallel with its self-capacitance (C) and a resistance, R . When a magnetic flux (Φ_a) threads through this loop, it changes the relative difference in the superconducting phase of the two JJs giving rise to periodic oscillations in the supercurrent, analogous to interference of light waves in double slit experiments, given by

$$I_C = 2I_0 \cdot |\cos(\pi \frac{\Phi_a}{\Phi_0})|$$

where Φ_a is the applied flux and Φ_0 is one flux quantum. Thus, critical current of a SQUID, in the ideal case, oscillates between a maximum of I_C and 0 given that

$$\Phi_0 = \Phi_a = (B) \times (A_{\text{eff}})$$

where B is the periodicity in magnetic field and A_{eff} is the effective loop area of the SQUID.

These basic principles of a SQUID have two important consequences. First, by changing the device *design* its sensitivity (periodicity) can be changed. Thus, SQUIDs are the most sensitive magnetic flux detectors. Furthermore, they are also quite versatile such that any physical quantity that can be converted to magnetic flux can be measured using a SQUID.

Second, SQUIDs have been used with great success to study a variety of material systems. For example, standard superconductors have been combined with other materials such as nanowires [84], ferromagnets [81, 82], topological insulators [83] to often reveal non-trivial current-phase relations. Such phase-sensitive measurements have also emerged as a powerful tool to study more exotic superconductors such as the ruthenates [85] and high T_c cuprates [86]. Whether the two-dimensional (2D) superconductor formed at the LAO/STO interface is also unconventional is still not clear. However, to address this issue one must move beyond standard bulk transport measurements. Recent tunneling studies [74] and transport spectroscopy of confined structures [87] exemplify this point. In this context, a probe of the superconducting phase could provide complementary information about the microscopic origin of the superconductivity, but such experiments are missing.

In this chapter, we realize SQUIDs at the LAO/STO interface which enable the observation of robust quantum interference in this interfacial superconductor. We fabricate the SQUIDs using two distinct approaches. The first involves the creation of weak links using nanoscale physical constrictions (C-SQUIDs), a technique which has been used extensively in a wide variety of superconductors. Figure 4.1(a) shows a schematic of the C-SQUID. Black areas are superconducting, while the beige regions remain insulating due to the presence of an amorphous LAO (a-LAO) mask.

Each arm of the loop is interrupted by a narrow constriction (see AFM image in figure 4.1(b)). We ensure that the width of the constriction (sub-100 nm) is comparable to the superconducting coherence length of LAO/STO [72]. The C-SQUID has the advantage that it requires only a single lithography step and is particularly convenient to characterize.

The second approach used to define SQUIDs, though more involved, is novel and unique to the LAO/STO interface. We exploit the sensitivity of T_C to the field effect to create an electrostatically defined SQUID (E-SQUID). By applying negative voltages to local top gates (see schematic in figure 4.1(c)), we deplete the regions below them. These locally depleted regions serve as the weak links, thus enabling the formation of independently tunable JJs in each arm. Figure 4.1(d) shows an AFM image of one such gate-defined JJ. While other examples of gate-tunable JJs do exist [88–90], they necessarily involve physical interfaces between two dissimilar materials. In contrast, LAO/STO provides a unique material platform where a single superconductor can be electrostatically modified to allow in-situ creation and tuning of JJs in a perfectly reversible manner. In this work we study two C-SQUID devices (C-SQ1 and C-SQ2) and one E-SQUID device (E-SQ3). A back gate can be used to tune the global electronic properties of the devices, and measurements are performed in a dilution refrigerator with a base temperature of 40 mK.

4.2. RESULTS

4.2.1. CONSTRICTION TYPE SQUIDS

Figure 4.1(e) shows a V-I curve for C-SQ1 at 40 mK, which displays a distinct supercurrent branch (inset shows the measurement configuration). In order to establish the presence of Josephson coupling we test whether the devices show clear SQUID behavior. We apply a current bias (I) close to the critical current (I_c) and monitor the voltage drop (V) as a function of perpendicular magnetic field (B). Figure 4.1(f) shows that all devices undergo periodic oscillations in B . Since we expect these oscillations to be periodic in the flux threading through the SQUID, a reduction in the loop area should result in a larger period in B . This is precisely what we observe when we compare C-SQ1 (upper panel) and C-SQ2 (middle panel), where C-SQ2 is designed to have a smaller loop area. E-SQ3 also shows similar periodic oscillations (lower panel) when the top gates are appropriately tuned (discussed in more detail below). The period (ΔB) for each of the traces in figure 4.1(f) can be determined by Fourier analysis (Figure 4.1(g)) to be 19 μ T, 31 μ T and 21 μ T for C-SQ1, C-SQ2 and E-SQ3 respectively. This gives us an effective loop area $A_{\text{eff}} = \Phi_0 / \Delta B$ ($\Phi_0 = h/2e$ is the flux quantum), which is consistently larger than the lithographically defined central (insulating) area. For superconducting structures which are much larger than the magnetic field penetration depth this difference arises from the Meissner effect in the superconducting region, which focuses the applied field into center of the SQUID loop. Even for 2D SQUIDs with dimensions smaller than the penetration depth (Pearl

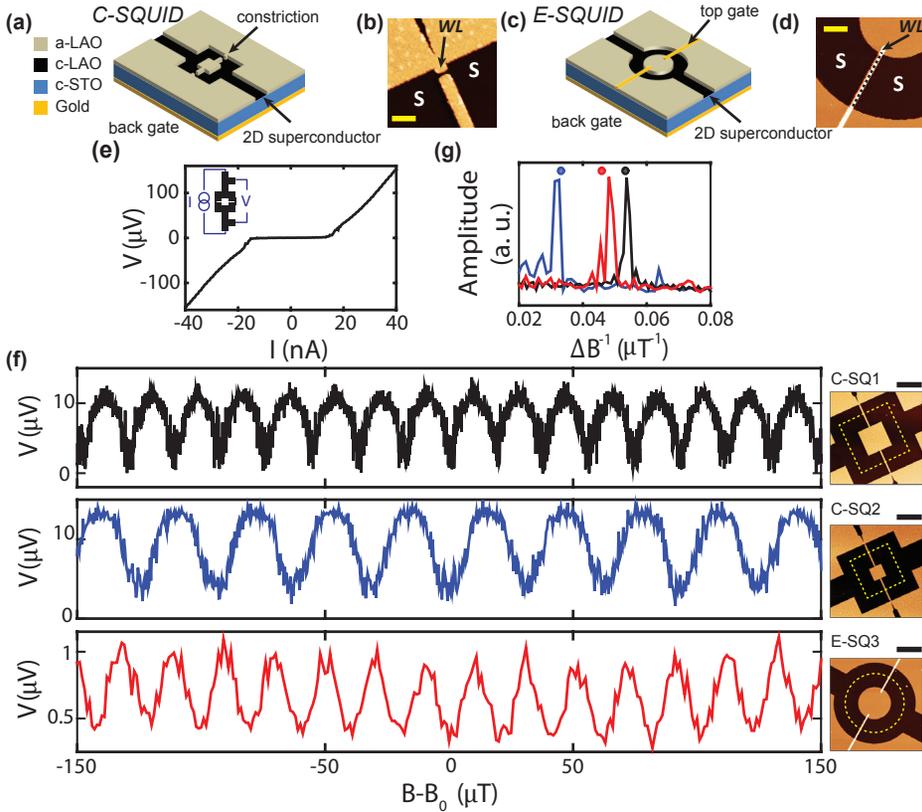


Figure 4.1: Device description and $V(\Phi)$ oscillations (a) Schematic of constriction based SQUID (C-SQUID). (b) AFM image of the constriction, which serves as the weak link (WL). Scale bar is 400 nm. (c) Schematic of electrostatically defined SQUID (E-SQUID) (d) AFM image of region around the top gate (scale bar is $2 \mu\text{m}$). Dashed line shows the region below the gate where the WL forms when a negative gate voltage is applied to the gate. (e) V - I curve for device C-SQ1 at $V_{bg} = -7 \text{ V}$. Inset shows a schematic of the measurement configuration. (f) Oscillations in voltage (V) with magnetic field ($B - B_0$) for C-SQ1 (upper panel), C-SQ2 (middle panel) and E-SQ3 (lower panel) with AFM images of the respective devices. B_0 is an experimentally determined offset in the magnetic field and has an uncertainty greater than one oscillation period. Yellow dashed line marks the effective area threaded by the flux. Scale bar for all images is $5 \mu\text{m}$. (g) Fourier transform of the oscillations shown in (f). The color scheme is the same as in (f). Circles are results of numerical simulations which yield an oscillation period in close agreement with experiments.

length) the fluxoid quantization can lead to a large flux focusing effect [91]. We confirm this via numerical simulations of 2D current distributions in thin film superconductors [92], which include the (weak) Meissner effect of the shielding currents (see Additional Information for details of the simulations and flux focussing factors). Taking into account the exact geometry of the devices, we find the calculated periods (circles in figure 4.1(g)) to agree well with the experiments.

While the $V(\Phi)$ oscillations clearly demonstrate the successful creation of the SQUIDs at the LAO/STO interface, analysis of $I_c(\Phi)$ oscillations provides a more quantitative understanding of the factors which determine the SQUID response. In the absence of thermal fluctuations the maximum critical current (I_{max}) across the SQUID is set by the Josephson coupling energy and the minimum critical current (I_{min}) is determined by the screening parameter

$$\beta_L = I_{max}L/\Phi_0$$

(L is the total inductance of the SQUID loop). In other words L plays a crucial role in determining the visibility,

$$Vis = \frac{I_{max} - I_{min}}{I_{max}}$$

of the $I_c(\Phi)$ oscillations. The exact relation between Vis and β_L can be obtained by numerical simulations (red curve in figure 4.2(c)). In order to experimentally determine Vis , we keep the gate voltage fixed and record V-I's for different Φ (Figure 4.2(a)) to estimate I_{max} and I_{min} (Figure 4.2(b)). We find that for $V_{bg} = 4$ V, $I_{max} = 88$ nA and $Vis \sim 0.3$. From figure 4.2(c) we estimate $\beta_L \sim 2.1$, giving $L \sim 50$ nH. This is nearly three orders of magnitude larger than the estimated geometric inductance of the SQUID loop. This additional inductance of the superconductor arises from the kinetic energy stored in the Cooper pairs and is known as the kinetic inductance (L_k). In general it can be expressed as

$$L_k \propto \frac{m^*}{n_s d}$$

where m^* is the effective mass of the charge carriers, n_s is the superfluid density and d is the thickness of the superconductor. The 2D nature of the LAO/STO interface ($d \sim 10$ nm) [93], combined with an extremely low n_s [94] and large m^* [95] naturally result in a greatly enhanced kinetic inductance. While for most SQUID designs the contribution of L_k can be neglected, here the SQUID response is in fact dominated by L_k . Thus, an analysis of the $I_c(\Phi)$ oscillations, as described above, allows us to estimate L_k of our SQUID loop.

Figure 4.2(d) shows that the kinetic inductance of the SQUID can be continuously tuned with the back gate (see Additional Information for details of the analysis and error estimates). To our knowledge this is the only intrinsic superconductor where the kinetic inductance can be tuned in-situ via the field effect. Increasing V_{bg} induces more carriers at the LAO/STO interface which in turn increases the superfluid

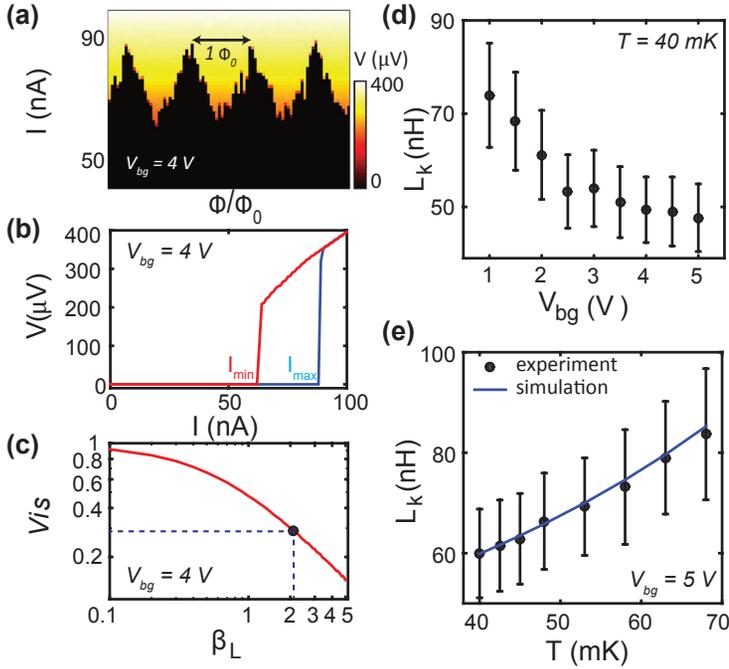


Figure 4.2: **C-SQUID: $I(\Phi)$ oscillations and kinetic inductance** (a) Color maps of V-I curves for different values of normalized flux (Φ/Φ_0) at $V_{bg} = 4$ V. (b) Individual V-I traces from (a) showing the maximum (I_{max}) and minimum (I_{min}) critical currents. (c) Numerically simulated curve for V_{is} vs. β_L in the noise free case with experimentally obtained value of V_{is} at $V_{bg} = 4$ V. (d) Variation of kinetic inductance (L_k) with V_{bg} . (e) Variation of L_k with temperature at $V_{bg} = 5$ V (black circles) and comparison with numerical simulations (blue curve). These measurements were performed in the different cooldown, resulting in a slightly different value of L_k as compared to (d).

density [94]. This results in an overall decrease in L_k . In addition to the back gate, we expect the temperature to also have a substantial effect on L_k . Increasing the temperature should reduce n_s , thereby increasing L_k . Indeed, figure 4.2(e) clearly shows that L_k increases with temperature. We therefore find that both the back gate and temperature dependence of L_k are mutually consistent with the picture that the SQUID modulations are determined predominantly by the kinetic inductance. We compare our results in figure 4.2(e) with numerical simulations, solving the London equations for our geometry [92]. Using the Ginzburg-Landau expression for the London penetration depth

$$\lambda_L(T) = \lambda_L(0)/(1 - T/T_c)^{1/2} \quad [53]$$

and the experimentally determined $T_c = 213$ mK, we find a good agreement between

the experiments and simulations (blue curve). For the Pearl length

$$\Lambda_p(T) = 2\lambda_L(T)^2/d$$

we obtain a value of 3 mm at $T = 40$ mK, which is similar in magnitude to the value obtained via scanning SQUID measurements [94]. Furthermore, we find that L_k is dominated by the constrictions, which behave as quasi-1D structures connected to the 2D bulk superconducting reservoirs (see Additional Information for a full description of the calculations).

4.2.2. ELECTROSTATICALLY DEFINED SQUIDS

The C-SQUIDS describe a simple, yet effective way to demonstrate quantum interference at the LAO/STO interface. In contrast the E-SQUID (described earlier, see figure 4.1(c-d)) uses local top gates to create and control JJs in each arm of the SQUID. Though some previous studies with a single top gate have shown evidence of a gate controllable Josephson effect [75, 96, 97], there was no clear observation of quantum interference. We now describe the operation of the E-SQUID in detail. When no gate voltages are applied to either of the gates ($V_l = V_r = 0$ V) the device is equivalent to a simple superconducting loop. The black trace in figure 4.3(a) shows the corresponding V-I trace. When a large negative voltage is applied only to the left gate $V_l = -3.4$ V the current flow through the left arm decreases, thereby reducing the total critical current across the loop (green trace). The red trace shows a similar V-I curve when only the right gate is made highly negative ($V_r = -3.8$ V) (refer to the Additional Information for more details about the tuning procedure). As expected, none of these three electrostatic configurations produce SQUID oscillations. However, when both gates are depleted ($V_l = -3.4$ V and $V_r = -3.8$ V, blue trace) the critical current reduces significantly. Figure 4.3(b) shows the V-I trace in this gate configuration over a smaller range. At this point we observe distinct SQUID oscillations (Figure 4.3(c)), thereby demonstrating the existence of an electrostatically defined JJ in each of the arms. We note that this process is completely reversible, whereby removing the gate voltages brings the device back to its original state, with no JJs.

The sensitivity of the JJs to the top gate voltages defines an optimal operating range for the E-SQUID. To quantify this we keep the right gate fixed at $V_r = -3.8$ V and monitor the visibility for different values of V_l , as shown in figure 4.3(d-g). The left inset shows the voltages applied to the left/right gates (these measurements were performed in a different cooldown to those described in figure 4.3(a-c), and therefore the absolute values of the voltages are somewhat different). When the left gate is relatively open (Figure 4.3(d)) the oscillations are hardly visible ($Vis \sim 0$). As V_l is made more negative the visibility increases, reaching a maximum value of 0.3 (Figure 4.3(f)). By depleting the region below the left gate even further, the oscillations disappear again. This continuous transition can be physically understood as follows. Since the top gates act locally, their influence on the superconducting banks is minimal. Therefore the maximum visibility is obtained when both JJs have the same

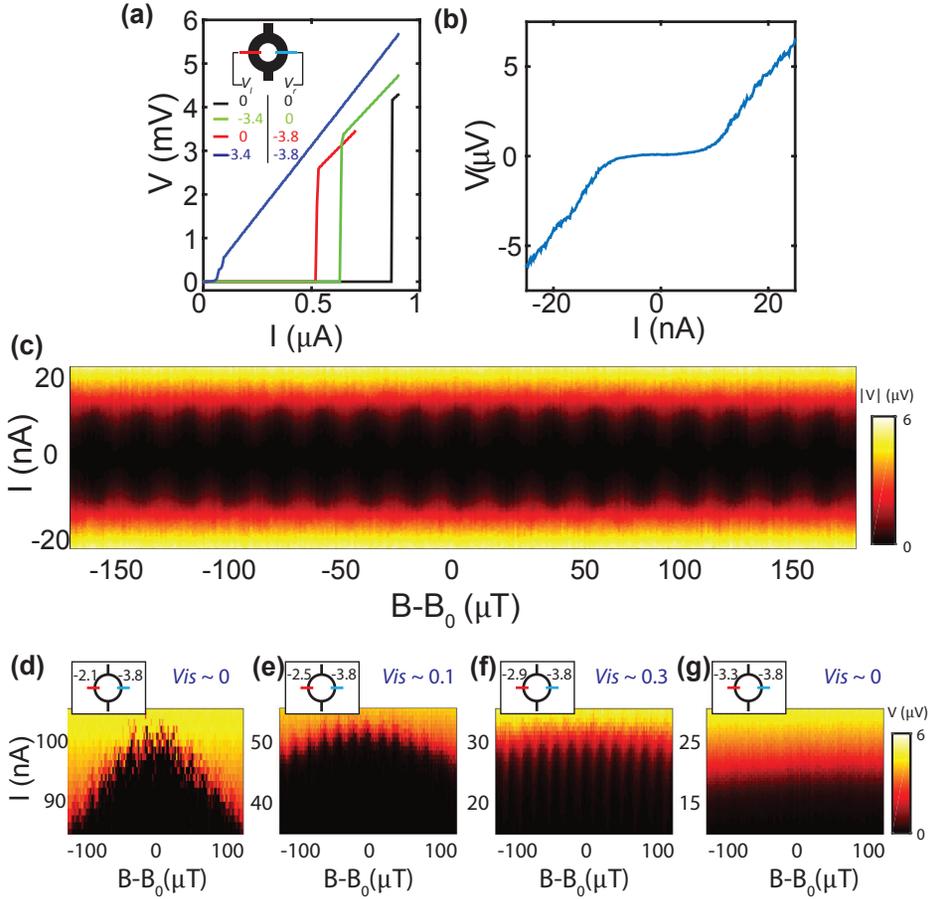


Figure 4.3: **E-SQUID: tunable Josephson junctions** (a) V-I curves for different combinations of left gate voltage (V_l) and right gate voltage (V_r), with $V_{bg} = -1$ V. Inset shows a schematic of the device. (b) Zoom in of the blue trace in (a). (c) 2D plot showing SQUID oscillations with the top gates optimally tuned ($V_l = -3.4$ V, $V_r = -3.8$ V). (d)-(g) Variation in the visibility of the modulations as V_l is reduced, with V_r held constant. The values of V_l and V_r are indicated in the left inset. These measurements were performed in a different cooldown, resulting in slightly different values of the gate voltages as compared to (a)-(c).

critical current. This condition is satisfied for figure 4.3(f) ($V_r = -3.8$ V, $V_l = -2.9$ V). Tuning V_l away from this optimal condition thus increases the asymmetry between the two JJs resulting in a reduced visibility.

For SQUIDs with a small loop inductance the dominant source of asymmetry arises due to unequal values of critical current in the two JJs (i.e., $I_{cl} \neq I_{cr}$, see SQUID schematic in inset to figure 4.4(c)). On the other hand, when L_k is large (as is the case for LAO/STO) one must consider the combined effects of asymmetries in I_c and L_k in the two arms of the SQUID loop (see Ref [98] for a description about asymmetric SQUIDs). The most important consequence of such asymmetry is that $I_c(\Phi)$ curves are offset along the Φ -axis (Figure 4.4a). Such offsets arise due to the large L_k , which produces a substantial self-flux (Φ_s), in addition to the applied flux Φ . When the phase drop across each JJ reaches $\pi/2$, I_c reaches its maximal value

$$I_{max} = I_{cl} + I_{cr}$$

and

$$\Phi_s(+) = I_{cr}L_r - I_{cl}L_l$$

Reversing the direction of current bias results in the same magnitude of self flux, but now of the opposite sign (i.e., $\Phi_s(-) = -\Phi_s(+)$.) Thus

$$\Delta\Phi = 2(I_{cr}L_r - I_{cl}L_l)$$

where $\Delta\Phi = \Phi_s(+) - \Phi_s(-)$.

By controlling the two JJs in our E-SQUID we study the effects of such asymmetry in the SQUID response. In particular, we show that the ability to independently tune the critical current of each JJ gives us an alternative method to extract the kinetic inductance. We start with an electrostatic configuration identical to the one in figure 4.3(c) and plot $I_c(\Phi)$ (black curve in figure 4.4(b)). The black dashed line confirms that there are no discernible offsets in the Φ -axis and the SQUID is in a symmetric configuration. We now hold V_r constant (i.e, I_{cr} does not change) and make V_l less negative (increase I_{cl}). We find that the $I_c(\Phi)$ curves move towards the left (right) for positive (negative) current bias. The blue dashed line clearly indicates that $\Delta\Phi$ acquires a negative sign. Performing the same experiment with V_l fixed and opening the right gate, we expect I_{cr} to increase, thereby inducing a self-flux in the opposite direction. This sign reversal of $\Delta\Phi$ can be seen in figure 4.4(d).

The variation of $\Delta\Phi$ with I_{max} is plotted in figure 4.4(c). The blue (red) points correspond to measurements performed with V_r (V_l) varying while the other gate is fixed. Since

$$\frac{\partial\Delta\Phi}{\partial I_{cr}} = 2L_r \text{ and } -\frac{\partial\Delta\Phi}{\partial I_{cl}} = 2L_l$$

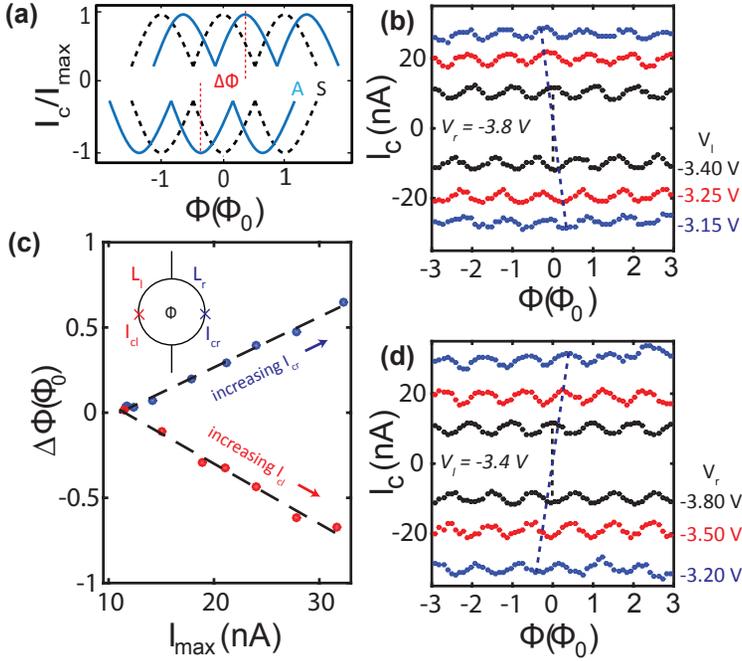


Figure 4.4: **E-SQUIDS: controllable asymmetry** (a) $I_c(\Phi)$ oscillations for a symmetric (S) SQUID (black dashed curve) and an asymmetric (A) SQUID with large kinetic inductance (blue solid curve). The maximum and minimum values of I_c shift along the Φ -axis by an amount $\Delta\Phi$. (b) $I_c(\Phi)$ oscillations with V_r fixed and selected values of V_l . Similar plots, but for fixed V_l and varying V_r are shown in (d). (c) Variation of $\Delta\Phi$ with I_{max} extracted from (b),(d) but also including more values of top gate voltage. Dashed lines show linear fits. Inset shows a schematic of an asymmetric SQUID.

linear fits to these points (dashed lines) allow us to estimate $L_r \sim 31$ nH and $L_l \sim 36$ nH. This difference is within the error bars of our estimates and we conclude that any intrinsic asymmetry in L_k of the two arms is small. Thus, the observed shifts along the Φ -axis arise from a combination of the large L_k and unequal critical currents of the JJs.

4.3. DISCUSSION

This is a particularly important finding in the context of LAO/STO since it suggests that any mesoscopic inhomogeneities in the superfluid density [99, 100] average out over a length scale of a few microns and do not have a considerable effect on the operation of these SQUIDs. Furthermore, even if such inhomogeneities are present, using the E-SQUID it is always possible to appropriately tune the critical current of

the JJs to minimize the effects of self-flux.

4.4. CONCLUSIONS

The ability to probe the phase of the superconducting order parameter opens the door to answer more specific questions about the pairing symmetry. To do so, one could create more involved devices by combining the LAO/STO superconductor with an s-wave superconductor via JJs oriented along specific crystal axes [86]. From a technological perspective, our studies of the E-SQUID demonstrate a completely new variety of JJs which are both electrostatically defined and electrostatically controlled. Such an architecture to create JJs eliminates any detrimental effects of physical interfaces between dissimilar materials. Detailed transport spectroscopy studies should allow one to ascertain whether such electrostatic interfaces are in fact superior.

4.5. ADDITIONAL INFORMATION

4.5.1. FABRICATION SPECIFICS

Figure 4.5(a) shows the complete flow of the fabrication processes. We point out two important differences relevant for the devices reported in this study: (i) the c-LAO was grown at a higher temperature of 840°C resulting in a larger critical temperature of the superconductor and (ii) the metallization for the top gates was preceded by a short oxygen plasma exposure to remove polymer residues.

4.5.2. ERROR ESTIMATES FOR KINETIC INDUCTANCE

To estimate the error bars for L_k (see Figure 4.2) we analyze the $I_c(\Phi)$ oscillations for each value of V_{bg} . We extract average values of I_{max} and $I_{max} - I_{min}$ (Figure 4.6) from 5-6 consecutive oscillations. The error bars represent the mean absolute deviation and figure 4.6(c) shows the resulting error in V_{is} . We see that V_{is} does not change with V_{bg} and we obtain $V_{is} \sim 0.29 \pm 0.03$. Since V_{is} is a strong function of β_L and $L_k = \beta_L \Phi_0 / I_{max}$, this uncertainty in V_{is} results in relatively large errors ($\sim 15\%$) on L_k .

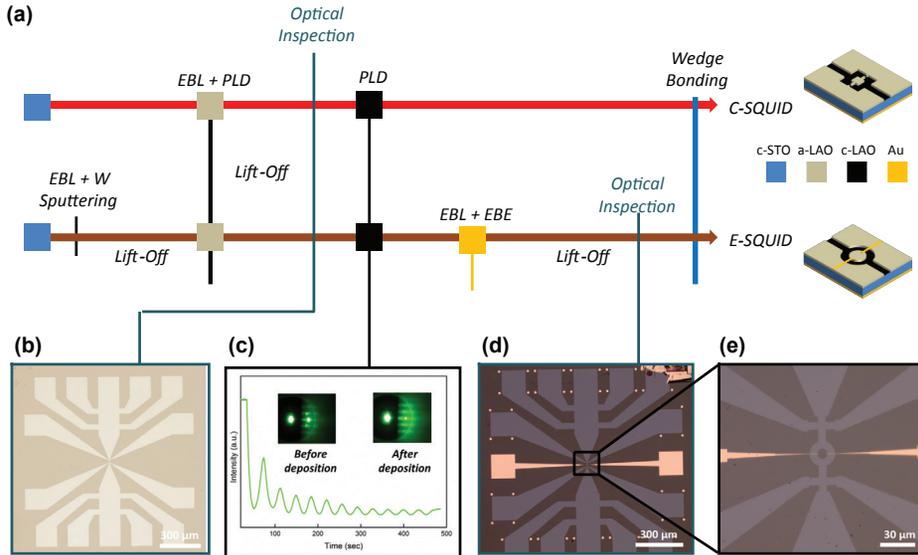


Figure 4.5: (a) Fabrication flow for SQUID devices. (b) Optical image after deposition of the amorphous LAO mask. (c) RHEED oscillations obtained during the growth of c-LAO. Inset shows diffraction patterns before/after the growth. (d) Optical image after top gates deposition. (e) Zoom in of (d) showing the active area of a E-SQUID device.

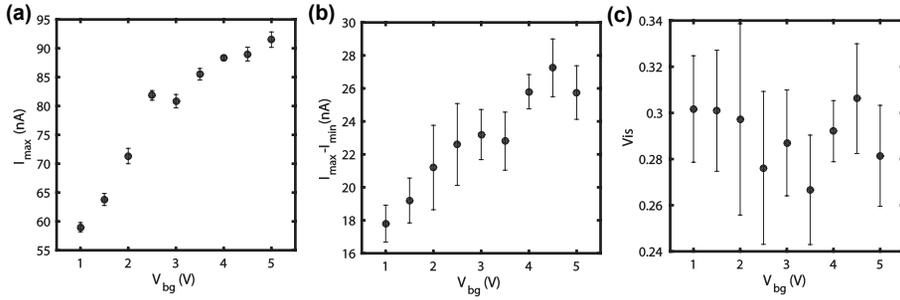


Figure 4.6: Error estimates for (a) the maximum critical current I_{max} , (b) $I_{max} - I_{min}$, and (c) visibility for different values of back gate voltage.

4.5.3. TUNING THE E-SQUID

To tune the E-SQUID into the optimal configuration we start by first recording V - I s as each top gate is depleted (with the other grounded). Figure 4.7(a(b)) show such plots for $V_{rg} = 0$ V ($V_{lg} = 0$ V), where the dark/bright regions indicate the superconducting (S)/resistive (R) branch of the V - I curve and the border is representative of the critical current. These plots give us an indication of the action of the individual gates, and allow us to identify values of gate voltage for which the regions below the top gates are being actively depleted (I_c decreases significantly). Next, we keep one gate fixed at a large negative voltage (Figure 4.7) and vary the other. Below a certain gate voltage (indicated by the dashed line) SQUID oscillations begin to appear. To check for the presence of these oscillations we found it particularly convenient to look for $V(\Phi)$ oscillations (as shown in figure 4.1(f)), since such measurements are much quicker than $I_c(\Phi)$ measurements.

4.5.4. FINITE ELEMENT SIMULATIONS †

For the simulations of effective area A_{eff} and kinetic inductance L_k we use the software package 3D-MLSI [92]. A brief summary of the theoretical background is presented in this section. For more details we refer to [92, 101] and references therein.

Initially, a given superconducting circuitry with thickness t extended in the x - y -plane is subdivided into finite sized triangles (finite element method); cf. Figure 4.8(a). For each individual element, static London equations are applied to compute the current distribution and the associated magnetic fields for the overall structure under appropriate global boundary conditions. Here, the central figure of merit is the thickness-integrated current density

† Finite element simulations are performed by our collaborators Roman Wölbling, Dieter Koelle and Reinhold Kleiner, University of Tübingen, Germany.

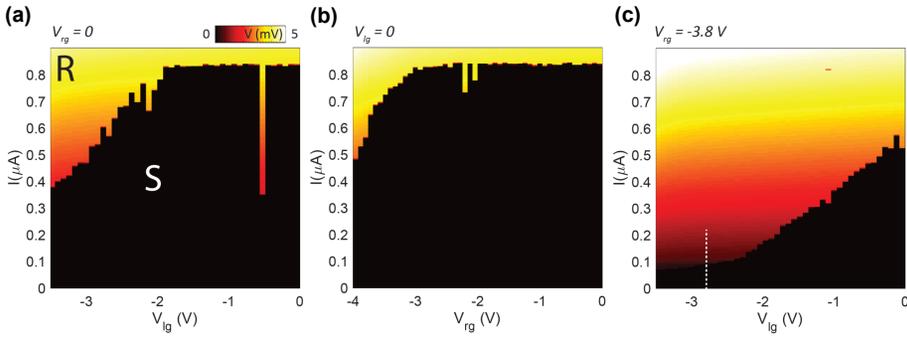


Figure 4.7: 2D color maps showing the variation of critical current with (a) V_{I_g} varied, $V_{R_g} = 0$ V, (b) V_{R_g} varied, $V_{I_g} = 0$ V, and (c) V_{I_g} varied, $V_{R_g} = -3.8$ V.

4

$$\vec{J}(x, y) = \int \vec{j}(x, y, z) dz = (J_x, J_y)$$

labeled sheet current. As long as t is much smaller than all other dimensions of the superconducting film, the assumption $\nabla \cdot \vec{J}(x, y) = 0$ remains valid and the sheet current can be expressed by a scalar potential g

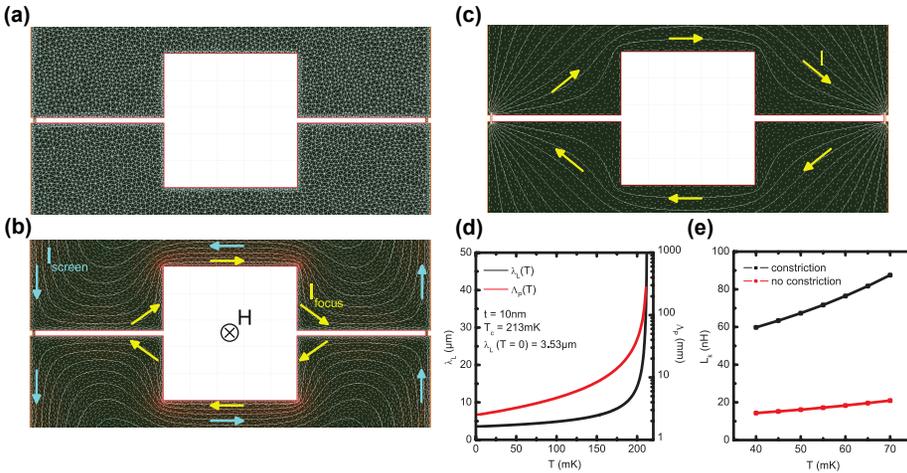


Figure 4.8: (a) Example of a mesh used for finite element simulations. Results of numerical simulations for (b) effective area, and (c) kinetic inductance. See text for more details. (d) Calculated temperature dependence of London penetration depth and Pearl length. (e) Calculated temperature dependence of kinetic inductance, with and without constrictions.

$$\vec{J}(x, y) = -\hat{z} \times \nabla g = \left(\frac{\partial g}{\partial y}, -\frac{\partial g}{\partial x} \right)$$

also called stream function. $g(x, y)$ is calculated for each finite element with $g(x_1, y_1) - g(x_2, y_2)$ being the current crossing any line connecting (x_1, y_1) and (x_2, y_2) . Furthermore, $g(x, y)$ can be used to calculate the full energy functional E of the thin film which in turn is closely related to the inductance matrix L comprising self and mutual inductances. By this means, also fluxoids Φ can be calculated for superconducting films containing holes or slits.

For the calculation of effective areas A_{eff} a homogeneous external magnetic field $H = 1 \text{ mA}/\mu\text{m}$ is applied perpendicular to the plane of the SQUID. Boundary conditions are chosen to be $g(x, y) = 0$ at the edge of the SQUID hole as well as at the outer edge of the superconducting structure, i.e. the net current circulating around the hole is $I = 0$. In other words, the current I_{screen} flowing close to the outer edge of the superconductor screens the applied field into the periphery of the SQUID while the current I_{focus} flowing at the edge of the hole focuses H into the SQUID loop. I_{screen} and I_{focus} flow in counter-clockwise and clockwise direction since the net current is set to zero. A_{eff} is obtained by computing the fluxoid in the hole and by $A_{\text{eff}} = \Phi/(\mu_0 H)$, with the vacuum permeability μ_0 . Figure 4.8(b) displays the current distribution and $g(x, y)$ for the calculation of A_{eff} for device C-SQ1. Here, white solid lines represent the contour lines of $g(x, y)$. Short white lines indicate $\vec{J}(x, y)$. For a better understanding, I_{focus} and I_{screen} have been emphasized by yellow and cyan arrows, respectively. The color code gives the amplitude of local currents with red and black areas indicating high and low current amplitude, respectively.

Turning to the calculation of the kinetic inductance L_k , the boundary conditions are $g(x, y) = 1 \text{ mA}$ at the edge of the SQUID hole and $g(x, y) = 0$ at the outer edge of the superconductor, i.e. L_k is computed for a current with amplitude $I = 1 \text{ mA}$ circulating around the hole; cf. Figure 4.8(c). Again, the circulating current I has been emphasized by yellow arrows. Film thickness t and London penetration depth λ_L are crucial input parameters for the calculation of L_k , however these quantities are initially unknown. We assume $t = 10 \text{ nm}$ and subsequently adjust λ_L to reproduce the measured L from the experiments. Choosing $\lambda_L = 3.9 \mu\text{m}$, $T = 40 \text{ mK}$ and $T_c = 213 \text{ mK}$, we find good agreement between simulation and measurement. We note here, that these values give a Pearl length of $\Lambda_P = 2\lambda_L^2/t = 3.04 \text{ mm}$ at $T = 40 \text{ mK}$ which is of the same order of magnitude as reported elsewhere [94].

To reproduce the functional evolution of $L_k(T)$ as seen in the experiments, we implement a temperature dependence of λ_L . We find reasonable agreement for

$$\lambda_L(T) = \frac{\lambda_L(T=0)}{\sqrt{1-T/T_c}},$$

which is plotted together with the related $\Lambda_P(T)$ in figure 4.8(d). Note that the same parameters ($\lambda_L(T)$, t , T_c) were used to calculate the effective area at $T = 40 \text{ mK}$.

To stress the fact that for device C-SQ1 the dominant contribution to L_k arises from the constriction type Josephson junctions, we compare the behavior of $L_k(T)$ of C-SQ1 with an otherwise equivalent device without constrictions in figure 4.8(e). We find that the overall inductance is indeed governed by the contribution of the constrictions by at least a factor of 4. This can be attributed to a large kinetic inductance since the dimensions of the constrictions are well below λ_L .

4.5.5. COMPARISON WITH THE RCSJ MODEL †

In our experiments we found that the nature of the V-I curves (value of critical current, shape of the transition to the resistive branch) depends on the back gate voltage. Since our estimates of L_k rely on the conversion of visibility (Vis) to β_L , we implicitly assume that the resistively and capacitively shunted junction (RCSJ) model [102, 103] appropriately describes our system. Below, we briefly describe the RCSJ model and how it relates to our C-SQUID devices.

To model an asymmetric SQUID we consider the circuit shown in figure 4.9(a). The Josephson junctions are described by Josephson currents with phases δ_1 and δ_2 and amplitudes $I_{01} = I_0(1 - a_i)$ and $I_{02} = I_0(1 + a_i)$, resistors $R_1 = R/(1 - a_r)$ and $R_2 = R/(1 + a_r)$, and capacitors $C_1 = C(1 - a_c)$ and $C_2 = C(1 + a_c)$. The Nyquist noise arising from the two resistors is described by two independent current noise sources I_{N1} and I_{N2} having white spectral power densities $4k_B T/R_1$ and $4k_B T/R_2$, respectively and k_B is the Boltzmann constant. The two arms of the SQUID loop have inductances $L_1 = L(1 - a_l)/2$ and $L_2 = L(1 + a_l)/2$. The total inductance L is the sum of the geometric (L_g) and the kinetic (L_k) inductance. The loop is biased with a current I . A flux Φ_{ext} is applied to the loop. In the following we normalize currents to I_0 , fluxes to the flux quantum Φ_0 , voltages to $I_0 R$ and time to $\Phi_0/2\pi I_0 R$.

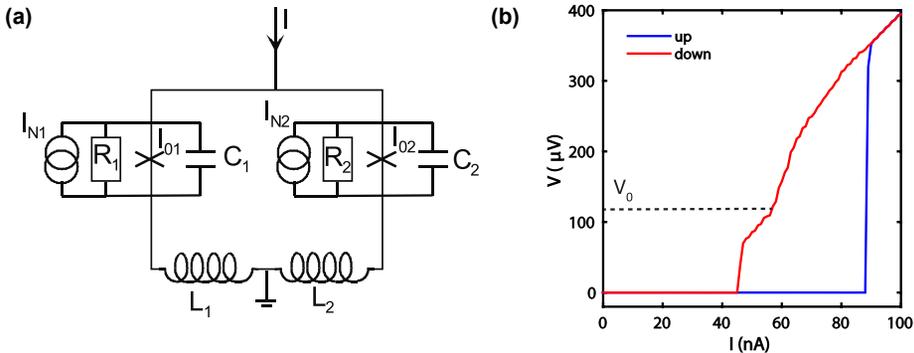


Figure 4.9: (a) Circuit for RCSJ model. (b) Experimental V-I trace at $V_{bg} = 4$ V, showing hysteresis. V_0 indicates the position of an LC resonance.

We further use the McCumber parameter $\beta_c = 2\pi I_0 R^2 C / \Phi_0$, the inductance parameter $\beta_L = 2I_0 L / \Phi_0$ and the noise parameter $\Gamma = 2\pi k_B T / (I_0 \Phi_0)$. With these units the SQUID is described by the differential equations [104, 105]

$$i/2 + j = \beta_c(1 - a_c)\ddot{\delta}_1 + (1 - a_r)\dot{\delta}_1 + (1 - a_i)\sin\delta_1 + i_{N1}$$

$$i/2 - j = \beta_c(1 + a_c)\ddot{\delta}_2 + (1 + a_r)\dot{\delta}_2 + (1 + a_i)\sin\delta_2 + i_{N2}.$$

Here i and j denote the normalized bias current and circulating current in the SQUID loop and the dots denote derivatives with respect to normalized time. The spectral densities of the normalized noise currents i_{N1} and i_{N2} are given by $4\Gamma(1 - a_r)$ and $4\Gamma(1 + a_r)$, respectively. The circulating current j is given by

$$j = \frac{1}{\beta_L} \left(\frac{\delta_2 - \delta_1}{\pi} - 2\Phi_{ext} + a_l \beta_L \frac{i}{2} \right).$$

From these equations we get the time dependent (high frequency) voltages across the junctions via the second Josephson relation, $\dot{\delta}_k = u_k$, ($k = 1, 2$). The dc (i.e. low frequency) voltage v across the SQUID is obtained by averaging $(u_1 + u_2)/2$ over sufficiently long times. From the dc voltage v one obtains current voltage (IV) characteristics i vs. v , the SQUID voltage modulation v vs. Φ_{ext} , the transfer function $dv/d\Phi_{ext}$ or the modulation of the critical current i_c vs. Φ_{ext} and $Vis = (i_{max} - i_{min})/i_{max}$. For the simulations discussed here we assumed symmetric parameters, i.e. $a_i = a_r = a_c = a_l = 0$. Calculations for $\Gamma = 0$ are shown in figure 4.2(c).

For higher values of back gate voltage V_{bg} , I_c is significantly larger showing a distinct switch in the V-I curves. Here we find a reasonable agreement with the RCSJ model. For example for $V_{bg} = 4$ V (Figure 4.2(b)) numerical simulations give $\beta_L \sim 2.3$ and $\beta_c \sim 5.5$ for the noiseless case. Including thermal fluctuations ($\Gamma = 0.015$), we find an upper limit for $\beta_c \sim 15$. In either case, since $\beta_c > 1$, we expect to observe hysteretic V-I curves. The experimental V-I trace (Figure 4.9(b)) clearly displays such a hysteresis. Furthermore, we observe a distinct bump-like feature in the return branch of the curve (red trace). In the RCSJ framework, this structure arises due to an LC resonance from the circuit shown in figure 4.9(a). One would then expect that $eV_0 = \hbar\omega = 1/\sqrt{LC}/2$. Here $V_0 \approx 120$ μ V is the position of the feature and ω is the resonance frequency. Using the experimentally determined value of $L_k \approx 50$ nH we estimate $C \approx 1$ fF. Finally using $I_0 = 44$ nA and $R = 8$ k Ω we obtain $\beta_c \approx 10$. This is indeed consistent with values of β_c predicted by the RCSJ model. Therefore, this analysis shows that (a) the RCSJ model describes our system reasonably well and (b) our estimates of L_k from the I_c oscillations are indeed correct.

We found that the V-I curves at lower back gate voltage (as in figure 4.1(e)) could not be reproduced well within the RCSJ framework. In particular, we see a large excess current, which could be indicative of non-equilibrium processes or even a

multi-valued current-phase relation. Furthermore, the low value of the critical current makes the effects of thermal noise much more significant, thus making it difficult to reliably extract the kinetic inductance. We therefore restrict our analysis to $V_{bg} \geq 1$ V (as seen in figure 4.2(d)).

† Comparison with the RCSJ model is performed by our collaborators Roman Wölbing, Dieter Koelle and Reinhold Kleiner, University of Tübingen, Germany.

5

SUPERCONDUCTING CONSTRICTIONS

Here, we demonstrate for the first time the formation of a superconducting quantum point contact (SQPC) with split gate technology in a superconductor, utilizing the unique gate tunability of the two dimensional superfluid at the $\text{LaAlO}_3/\text{SrTiO}_3$ (LAO/STO) interface [15, 17, 32]. When the constriction is tuned through the action of metallic split gates we identify three regimes of transport: (i) SQPC for which the supercurrent is carried only by a few quantum transport channels. (ii) Superconducting island strongly coupled to the equilibrium reservoirs. (iii) Charge island with a discrete spectrum weakly coupled to the reservoirs. Our experiments demonstrate the feasibility of a new generation of mesoscopic all-superconductor quantum transport devices.

Parts of this chapter have been submitted for publication.

5.1. INTRODUCTION

One of the hallmark experiments of quantum transport is the observation of the quantized resistance in a point contact formed with split gates in GaAs/AlGaAs heterostructures [43, 44]. Being carried out on a single material, they represent in an ideal manner equilibrium reservoirs which are connected only through a few electron mode channel with certain transmission coefficients [43]. It has been a long standing goal to achieve similar experimental conditions also in superconductors [106], only reached in atomic scale mechanically tunable break junctions of conventional superconducting metals, but here the Fermi wavelength is so short that it leads to a mixing of quantum transport with atomic orbital physics [107].

Various attempts have been made to combine the gate-tunability of the low electron density semiconductor with the use of conventional superconductors. However, these hybrid devices have introduced, compared to the GaAs/AlGaAs normal quantum transport case, the very important and yet very difficult to control influence of the interface between the two dissimilar materials [108]. This makes the results dependent on the complexities of the proximity effect and thus complicates their interpretation.

In principle, a new path has become available when it was discovered that in the two dimensional electronic system (2DES) at the LAO/STO interface superconductivity becomes suppressed when the electron density n is reduced below a critical value n_c , for example by means of a gate voltage [17, 109]. The Fermi-wavelength λ_F in this system can be as large as 30 to 50 nm [37] and ballistic transport in the normal state has been demonstrated [37, 110]. The superconducting coherence length is about $\xi = 100$ nm [15]. This corresponds to spatial dimensions which are commonly achieved with present day lithography techniques. The creation of an SQPC with split gates in LAO/STO should therefore be within reach [cf. Figure 5.1(a)]. This approach can also offer insight into the nature of superconducting pairing at oxide interfaces.

In this chapter, we present experiments that demonstrate the formation of an SQPC with split gates in the LAO/STO superfluid.

5.2. RESULTS

5.2.1. CHARACTERIZATION OF THE DEVICE

Figure 5.1(b) presents a false color atomic force microscope (AFM) image of the device layout. The metallic split gates (yellow) L and R cover the full width of the $5 \mu\text{m}$ wide 2DES (blue), except for a 150 nm region at its center. Transport experiments are performed in a current bias configuration (unless stated otherwise) at temperature $T_{\text{base}} < 40$ mK. The resistively measured transition to the superconducting state is observed at $T_c \approx 100$ mK. Because of gate history effects, we carry out the experiment by putting electrode L on a fixed gate voltage ($V_L = -1\text{V}$) to ensure depletion and we

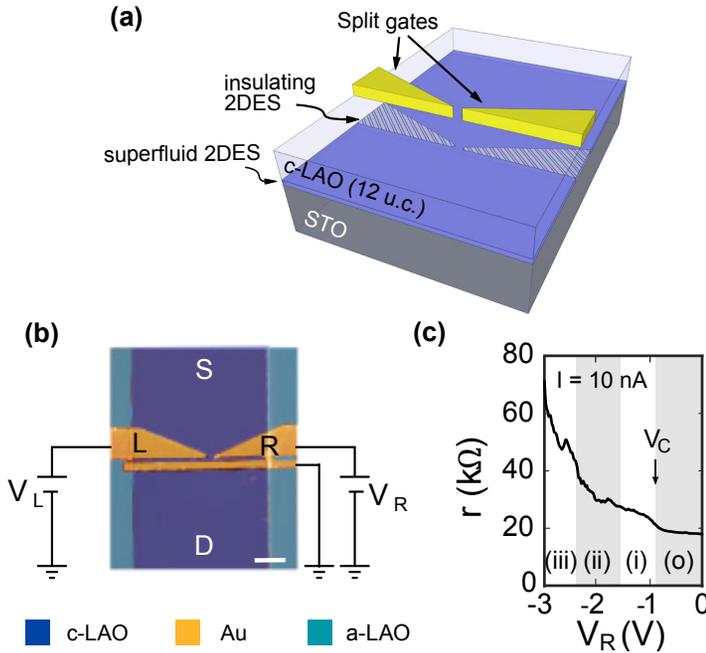


Figure 5.1: **Split gate device on the two dimensional superfluid of LAO/STO interface.** (a) Generalized sketch of the device. At the interface between the STO substrate and the 12 unit cell (u.c.) crystalline LAO (c-LAO) the superconducting 2DES (blue) is formed, which can be tuned insulating (shaded blue) locally under the split gates (yellow) thus forming a superconducting constriction. (b) False color AFM image showing the device layout. The potential of the split gates (yellow) L and R is controlled with the voltages V_L and V_R , respectively. V_L is kept at $-1V$. The conductive 2DES is formed in regions with c-LAO (blue). The thin gate spanning the channel is not used in the experiments. The scale bar corresponds to $1 \mu m$. (c) normal differential resistance r as a function of V_R measured for $I=10$ nA. (o) - (iii) indicate the different regimes of transport. V_c denotes the formation of the constriction.

tune the constriction by only varying the voltage V_R applied to gate R (see Additional Information).

We expect the following scenario: When V_R is changed towards negative values the charge carrier density n gets reduced locally underneath the gate and gets closer to the critical density n_c at which superconductivity becomes suppressed. At a certain gate voltage $V_R = V_c$ the condition $n = n_c$ is reached and a supercurrent can flow only through the constriction between the tips of gates, thus forming a weak link between the superconducting reservoirs. Outside this weak link, under the gates, the system acts as an insulator [17]. The number of transport modes available in the weak link is determined by its effective width. The constriction width is reduced when V_R is further decreased and therefore the number of transmission channels

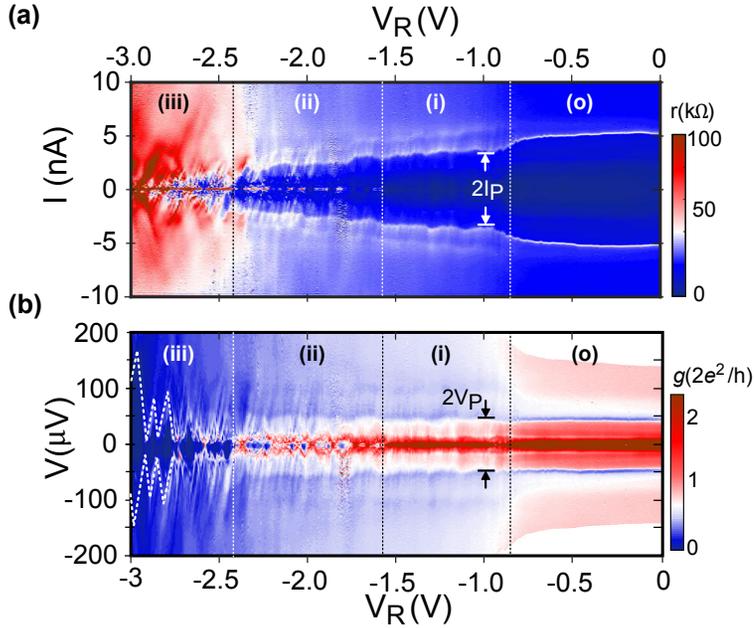


Figure 5.2: **Tunable constriction with gate voltages.** (a) Differential resistance r versus current I for gate voltage $V_R = 0$ to -3 V. Gate L is kept at $V_L = -1$ V. The four regimes of transport (o) to (iii) are indicated. I_P , reminiscent of the critical current I_c of the weak link, is indicated. (b) Same data as in (a) but with voltage drop V on the vertical axis and differential conductance g represented by the color scale. V_P denotes the voltage drop at I_P . Dotted lines in regime (iii) indicate conductance diamonds.

decreases which is expected to lead to a step-wise reduction of the critical current I_c [106]. For $V_R \ll V_c$ transport will be dominated by a low transmissivity and the current is pinched off.

5.2.2. TUNABLE CONSTRICTION

In order to study this scenario, we record a series of V - I curves and vary V_R from 0 to -3 V. Panoramic overviews of the results are given in figure 5.2(a-b) in color plots. Figure 5.2(a) presents the differential resistance $r = dV/dI$ and figure 5.2(b) shows the differential conductance $g = dI/dV$ with the current I and voltage drop V on the vertical axis, respectively. It can be seen that the constriction undergoes four different regimes of transport [labelled (o) and (i) to (iii) in the figures] as V_R is varied from 0 to -3 V. Regime (o) (ranging from $V_R = 0$ to -0.9 V) corresponds to the open current path configuration with $V_R > V_c$. A sharp peak in r is visible at $I = \pm 5$ nA, labelled I_P , which is reminiscent of a critical current I_c . Correspondingly, a dip occurs in g

at $V_p = \pm 44 \mu\text{V}$ (Figure 5.2(b)). At $V_R = V_C \approx -0.9 \text{ V}$ the critical density n_c is reached. Here I_p drops significantly because the current path becomes confined. At high currents in figure 5.2(a), as shown for $I = 10 \text{ nA}$ in figure 5.1(c), this point of confinement is apparent in a step increase in r , similar to the well-known behavior in semiconductor heterostructures [112]. It marks the transition to regime (i) ($V_R = -0.9$ to -1.6 V). In this regime I_p decreases when V_R is reduced indicating the gate tunable weak link. In regime (ii) ($V_R = -1.6$ to -2.4 V) regions of high resistance at zero bias appear and disappear periodically. As we will show below, this can be attributed to the emergence of a conductive island which dominates transport through the constriction. In regime (iii) ($V_R = -2.4$ to -3 V) the device always exhibits a high resistance at zero bias. Figure 5.2(b) reveals that this regime is controlled by conductance diamonds (indicated with dashed lines).

Let us start the discussion with the weak link regime (i). We observe a rounded supercurrent and an excess current $I_{\text{exc}} \approx 1 \text{ nA}$ (Figure 5.3 (a)). I_p , reminiscent of the critical current I_c , changes from 3.7 to 3.0 nA (Figure 5.3(b)) when V_R is varied. The voltage $V_p = 44 \mu\text{V}$ [cf. Figure 5.3(c)] can be related to the superconducting gap $V_p/2 \approx \Delta \approx 22 \mu\text{eV}$, which is compatible with the value inferred from the resistively measured T_c , $\Delta T_c = 1.76 k_B T_c = 15 \mu\text{eV}$. The high bias conductance g_n (Figure 5.3(d)) is of the order of half the quantum of conductance, changing with V_R from 0.6 to $0.47 (2e^2/h)$ [20 to $28 \text{ k}\Omega$]. As shown by Monteiro et al. [31] the phase correlation length in our 2DES is about 170 nm , whereas the lithographically determined channel-width is about 150 nm . It is therefore reasonable to interpret the data from a quantum transport perspective. For low carrier densities the Fermi wavelength λ_F is several 10 nm [37]. This and the relatively low value of g_n suggest that we have only a few modes with a finite transmissivity in the channel. With increasing V_R we do not observe the expected quantum transport step-like features in g_n , although the trace in figure 5.1(e) is obviously not monotonous. In order to extract the transmissivity of the weak link we calculate from I_{exc} and g_n the barrier strength Z as a function of V_R using the BTK-formalism for an S-S interface [113]. Z is related to the normal state transmission probability τ by $\tau = (1 + Z^2)^{-1}$. In this manner we obtain $Z \approx 0.8$ and, correspondingly, $\tau \approx 0.6$ (Figure 5.3(e)). Comparison with the measured g_n thus suggests a total mode conductance of $2e^2/h$, such that $g(\tau = 0.6) = 0.6 \times 2e^2/h$, close to the measured values. If we follow recent experiments by Gallagher et al. [110] who observed e^2/h modes in a normal state QPC, we could also consider only one mode with a higher transmissivity. However, this would require a re-analysis of the excess current based on an unconventional order parameter.

If we continue the discussion in the conventional picture, for a SQPC with perfect transmission ($\tau = 1$) Beenakker and van Houten [106] found that the critical current is given by $I_c = Ne\Delta(\hbar)^{-1}$, where N was chosen to represent the number of spin degenerate modes (which contribute each $2e^2/h$ to the normal conductance). Using this relation and including the obtained τ as a pre-factor, we can calculate

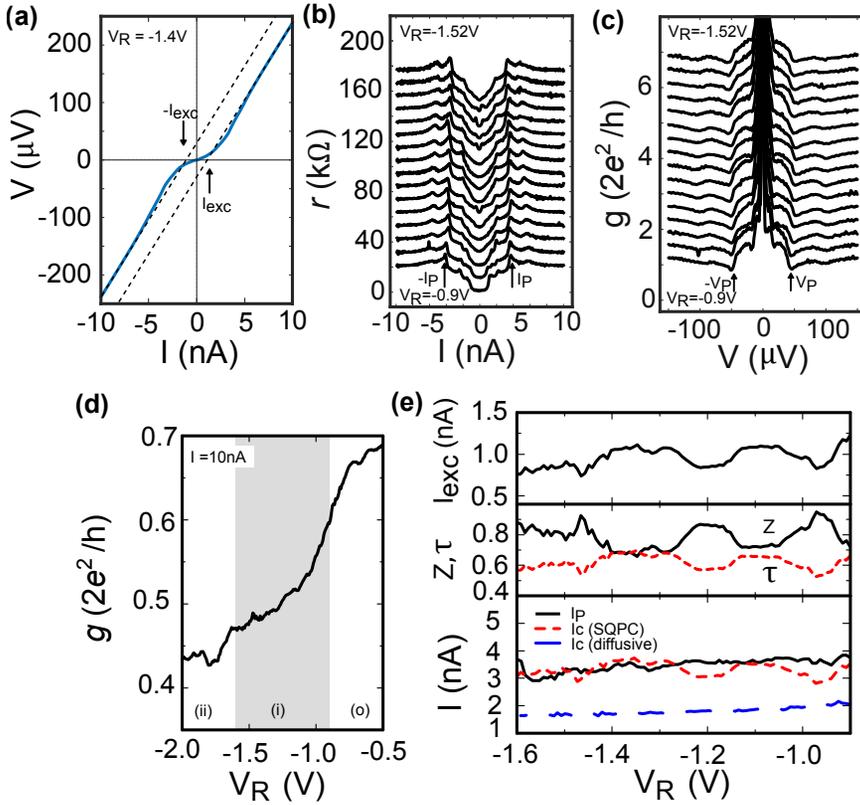


Figure 5.3: **Regime (i): Superconducting Quantum Point Contact.** (a) Representative V - I curve in regime (i) ($V_R = -1.4\text{ V}$). The rounded supercurrent is clearly visible. The excess current is denoted I_{exc} . (b) r versus I for different V_R . I_p , inferred from the sharp peak in r , is indicated. The curves are offset by $10\text{ k}\Omega$. (c) g versus V for different V_R . $V_p \approx 45\text{ }\mu\text{V}$ is indicated. The curves are offset by $0.2 (2e^2/h)$. (d) g for $I = 10\text{ nA}$. (e) top panel: I_{exc} as a function of V_R . middle panel: Barrier strength Z (solid, black line) and normal state transmission τ (dashed, red line) as obtained from BTK. Bottom panel: I_p (solid, black line) and critical current I_c as expected for an SQPC (short, red dashes). For comparison, I_c expected for a diffusive junction with conductance g is shown (blue dashes).

the maximum supercurrent expected for our device, which yields $I_c \approx 3$ nA. This is in good agreement with the measured I_p , as can be seen in the bottom panel in figure 5.3(e). For comparison we also plot the expected I_c for a diffusive junction [114], which clearly gives much smaller values. The critical current $I_c \approx 3$ nA implies a Josephson coupling energy $E_J = 6.2 \mu\text{eV}$. This is comparable to the bath temperature, $k_B T_{\text{base}} = 3.4 \mu\text{eV}$. Therefore, as for the few-mode atomic scale point contacts [115, 116], the supercurrent is rounded.

5.3. DISCUSSION

Let us now turn to the regime of conductance diamonds (CDs), regime (iii). Figure 5.4(a) presents a detailed measurement of g in this region. Note that this measurement was carried out in a voltage bias configuration. We observe a series of CDs whose size E on the (vertical) voltage axis is of the order of 80 to 150 μV . In gating experiments with non-superconducting materials, for instance in narrow semiconductor channels or graphene nano ribbons, CDs are known to occur in the low density limit because of puddles of charge carriers which form due to small inhomogeneities in the potential landscape, thus leading to quantum dot-like transport behavior [117–122]. From this analogy we infer that in regime (iii) the superfluid inside the constriction is at the transition to full depletion. The size of the CDs directly reflects the addition energy E that has to be paid in order to change the island occupation number and thus, to enable transport. E is composed of various contributions of which the most dominant ones typically are the Coulomb charging energy $U = Ne^2(2C_\Sigma)^{-1}$ (with C_Σ being the total capacitance of the island and N the number of charges to be added or removed) and the energy level quantization due to quantum confinement $\delta\varepsilon$. For quantum dots in LAO/STO [39, 40, 123], Coulomb contributions are small because the STO substrate exhibits an extremely large dielectric constant $\varepsilon_r = 25000$ at low T and for small electric fields [124] which suppresses Coulomb repulsion. For our device, however, the fields originating from the split gates can not be neglected [31]. We have performed simulations of the dielectric environment in the region surrounding the constriction using finite element techniques [see Additional Information]. Our results indicate that the geometry of the gates leads to a strong field focusing effect which reduces ε_r in the constriction such that Coulomb repulsion becomes relevant. The numerical simulations yield charging energies of $U \approx 100 \mu\text{eV}$ for an island with ~ 50 nm radius, compatible with our experiment. The data in figure 5.4(a) further show signatures of transport through excited states originating from quantum confinement, as can be seen from the fine structure of conductance lines parallel to the diamond edges between two adjacent diamonds (green arrows in figure 5.4(a)) [120, 125]. This allows us to estimate $\delta\varepsilon \approx 10$ to $20 \mu\text{eV}$, which would lead to an island size of ~ 80 nm, similar to the size obtained from the finite element simulations of the electrostatic properties. These values are also compatible with the electronic inhomogeneities typically ob-

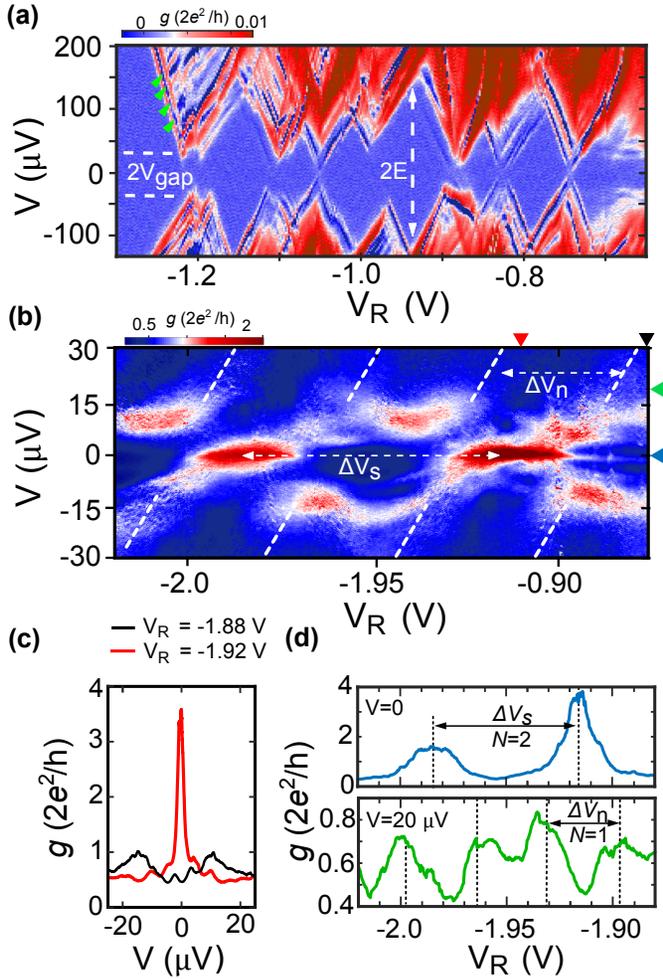


Figure 5.4: **Regimes (iii) and (ii): Conductive island.** (a) Conductance diamonds measured in regime (iii) with voltage bias V on the vertical axis. E denotes the addition energy of the island. The diamonds exhibit a gap of $V_{\text{gap}} \approx \pm 30 \mu\text{V}$. Green arrows indicate signatures of excited states due to quantum confinement. Note that due to gate history effects, this regime occurs at a lower V_R range. (b) g measured regime (ii). For small voltages g exhibits peaks with periodicity $\Delta V_s = 70 \text{ mV}$. For $V > 15 \mu\text{V}$ the periodicity increases by a factor 2, $\Delta V_n = 35 \text{ mV}$ (dashed white lines). Black, red triangles and blue, green triangle indicate the line cuts shown in (c) and (d), respectively. (c) vertical line cuts from (b) at $V_R = -1.88 \text{ V}$ and $V_R = -1.92 \text{ V}$. (d) Horizontal line cuts from (b) at $V = 0$ (top panel) and $V = 20 \mu\text{V}$ (bottom panel). The change in periodicity by a factor 2 suggests a change in number of transferred charges from $N=2$ to $N=1$, indicative for a superconducting island.

served in LAO/STO, which correlate with structural effects [26, 126, 127].

The island couples to superconducting reservoirs, which can be inferred from the voltage gap $V_{\text{gap}} \approx \pm 30 \mu\text{V}$ that separates the CDs in positive and negative bias direction [62, 128]. As expected, V_{gap} vanishes when a perpendicular magnetic field $B=1\text{T}$ is applied (see Additional Information). We further observe pronounced negative differential conductance (NDC) along the edges of the CDs, which can be related to the sharp changes in density of states in the superconducting reservoirs around $\pm\Delta$. Since NDC occurs symmetrically for both positive and negative bias, we conclude that both reservoirs exhibit a superconducting energy gap (see Additional Information). When we compare the value of $V_{\text{gap}} = 2\Delta$ with the superconducting gap in the reservoirs, $\Delta \approx 22 \mu\text{eV}$, we obtain reasonable agreement. We note that in this regime (iii) the level spacing of quantum states on the island is of the same order as the superconducting gap, $\delta\varepsilon \sim \Delta$. We are therefore in the limit of Anderson's criterion of superconductivity at small scales ($\delta\varepsilon < \Delta$) [129, 130].

Finally we turn to the strong coupling regime (ii) (Figure 5.4(b)). The pattern of gapped CDs is not visible here. Instead we observe zero bias conductance peaks which are of the order of the quantum of conductance, $g \geq (2e^2/h)$, [cf. Figure 5.4(c), red curve]. They alternate with regions where g is suppressed. This suggests that the island is more transparent in this regime, allowing for Cooper pair transport [131] at zero bias. The peaks in g occur periodically in ΔV_{R} , with a periodicity $\Delta V_{\text{S}} = 70 \text{ mV}$ (Figure 5.4(d), top panel). Above a certain bias voltage $V \approx \pm 15 \mu\text{V}$, the periodicity changes by a factor 2, $\Delta V_{\text{n}} = 35 \text{ mV}$ (Figure 5.4(d), bottom panel). This suggests that the parity of the island influences its energy state, as expected for a superconducting island [128]. In its ground state the island hosts Cooper pairs (even parity) and thus exhibits a charging energy $2U$, reflecting the Cooper pair's charge $2e$ ($N=2$). Above a critical bias voltage the odd-parity state becomes available for quasi particles in the reservoirs thus enabling single electron transport across the island ($N=1$). This results in period doubling of the Coulomb blockade oscillations. Our data therefore suggest that in the strong coupling regime (ii) the island is in a superconducting state, thus forming a superconducting quantum dot (SQD).

5.4. CONCLUSIONS

We conclude that we have realized for the first time a superconducting quantum point contact with a split gate technique, of which the superconducting and normal transport is independent of unknown material interfaces. The present technology can serve as a basis for future experiments which will make it possible to evaluate the microscopic properties of the LAO/STO interface superconductivity and the properties of genuine superconducting quantum point contacts as originally envisioned [106]. It may furthermore enable the investigation of nanoscale superconductivity in few electron quantum dots.

5.5. ADDITIONAL INFORMATION

5.5.1. FABRICATION & CHARACTERIZATION

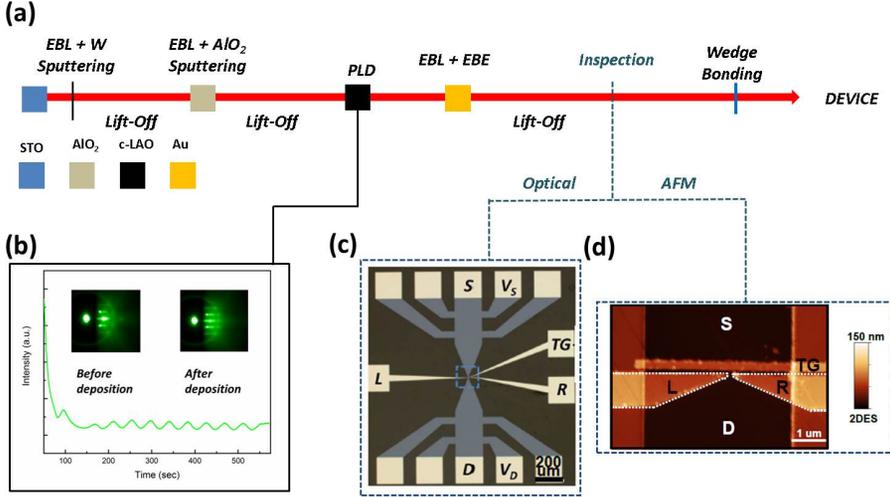


Figure 5.5: (a) Fabrication flow. The color legend indicates the deposited materials at the different stages. (b) The in-situ RHEED oscillations monitored during growth. They confirm layer-by-layer growth. The insets show the RHEED diffraction pattern before and after the deposition of the LAO layers. The 2D nature of the deposited film is evident from the horizontal streaks visible after growth. (c) Optical image of the device after the lift off process. Ohmic contacts and the gate electrodes are labelled. (d) Atomic Force Microscopy (AFM) image showing the top gate architecture of the device.

The carrier density in the 2DES is adjusted globally by applying a negative back gate voltage $V_{BG} = -1.875$ V, which corresponds to a reduced density compared to $V_{BG} = 0$. We determine the carrier density from Hall measurements performed at 300 mK using voltage probes on opposite sides of the reservoir with width $150 \mu\text{m}$. The longitudinal resistance is determined from voltage measurements between probes separated by $112.5 \mu\text{m}$. This yields a carrier density $n \approx 3 \times 10^{13} \text{ cm}^{-2}$ and a mobility $\mu \approx 800 \text{ cm}^2(\text{Vs})^{-1}$.

Figure 5.6(a) shows measurements of the gate leakage currents I_{leak} measured at $T \sim 1$ K by recording the dc drain current while varying the voltage applied to the respective gate. We find that even at $V_{L,R} = -4$ V the leakage current remains small, $|I_{leak}| < 10$ pA.

In order to characterize the influence of the gate, we bias the 2DES with a constant voltage ($V=1$ mV) and measure the drain current (I_D) while changing the applied gate voltage. Note that this was done at finite back gate voltage to reduce the global carrier density such that the insulating state (pinch-off) is reached within the

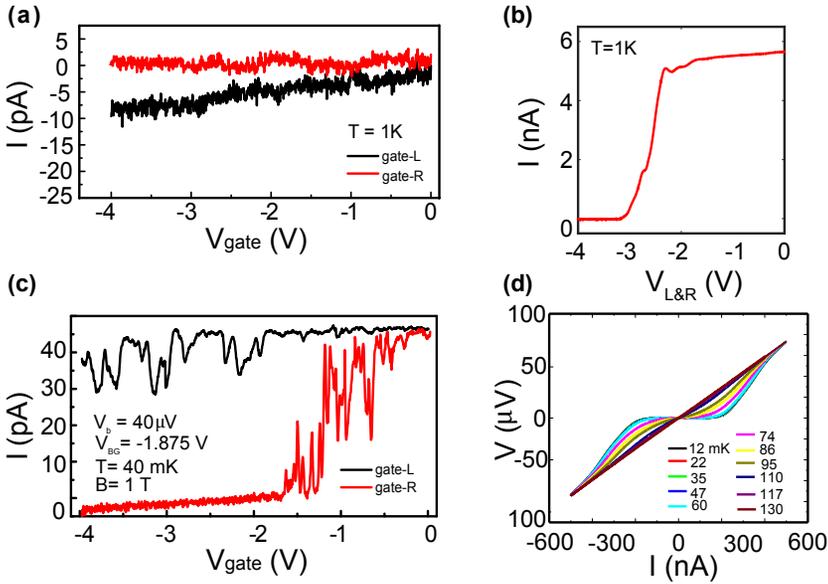


Figure 5.6: (a) Leakage currents from the gates measured at $T=1\text{K}$. (b) Pinch off curves at 1K for both gates L and R tuned simultaneously at 1K . (c) Pinch off curves when a voltage is applied only to one of the gates while the respective other one is grounded. (d) Temperature dependent voltage-current curves measured in the reservoirs of the device. We obtain $T_C \approx 100\text{ mK}$ if we use $R_{TC} = R(130\text{ mK})/2$ to define T_C , with R being the high bias slope of the curve. Using the BCS equation for the superconducting gap Δ , this yields $\Delta = 1.76k_B T_C \approx 15\text{ }\mu\text{eV}$.

available gate voltage range. Figure 5.6(b) shows the result obtained for applying a voltage to gates L and R simultaneously. At low temperature, we observe the behaviour shown in figure 5.6(c). Varying gate R alone enables us to block transport through the channel. Gate L, in contrast, does not pinch off the current, even at $V_L = -4\text{V}$. This indicates that the current does not flow through the 2DES underneath gate L, even at $V_L=0$, suggesting that it is depleted already at this stage. Note that superconductivity is suppressed in these measurements upon application of a perpendicular magnetic field $B = 1\text{T}$.

5.5.2. ADDITIONAL DATA

COULOMB DIAMOND REGIME (III)

Figure 5.7(a) shows the series of Coulomb diamonds discussed in the main text with a perpendicular magnetic field $B=1\text{ T}$ applied. Since B is much larger than the typical critical magnetic field in superconducting LAO/STO 2DES, $B_C \approx 0.2\text{T}$, superconducting transport in the leads is suppressed. Therefore, the voltage gap $V_{\text{gap}} \approx 25\text{ }\mu\text{eV}$

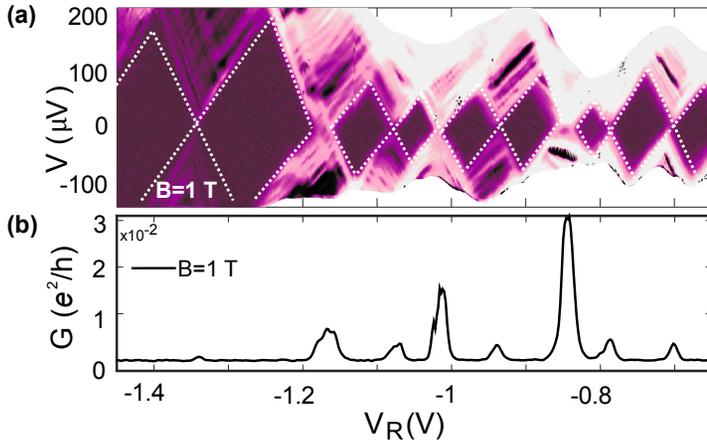


Figure 5.7: (a) Coulomb diamonds discussed in the main text with a perpendicular magnetic field $B=1\text{T}$ applied. It can be seen that the gap V_{gap} has vanished. (b) Zero bias conductance as a function of V_R extracted from (a).

5

observed for $B = 0$ vanishes. The zero bias conductance is given in figure 5.7(b). Interestingly, the amplitudes appear to alternate in an odd-even manner, resembling the parity effect in superconducting islands with two normal electrodes due to quasiparticle poisoning [132] or photon assisted tunneling processes from radiation leaking through an imperfect shielding [133]. This could suggest that despite the high magnetic field paired electrons are still present on the island. In the light of recent publications [37, 39, 40] this could hint at another signature of electron pairing without macroscopic superconductivity in LAO/STO.

We observe clear signatures of negative differential conductance (NDC) at the edges of the Coulomb diamonds. They occur for both positive and negative bias voltage, which indicates the presence of a superconducting gap in both reservoirs. As an example, a close up of the X shaped structure observed around $V_R = -0.75\text{ V}$ is presented in figure 5.8(a). Similar features have been observed recently by Cheng et al. [40], who pointed out a connection to tunable electron-electron interactions on LAO/STO quantum dots. It can clearly be seen from figure 5.8(a) that the four 'arms' of the X intersect around $V = 0$ (○). This suggests that conductance originates from alignment of the island state with states close to the Fermi levels in the reservoirs (cf. the corresponding energy diagram in figure 5.8(c). Each of the 'arms' exhibits a pronounced negative differential conductance (NDC). This becomes highlighted in figure 5.8(b) where traces of g are shown that are obtained from the vertical line cuts denoted α and β in figure 5.8(a). When going from $V = 0$ towards positive or negative bias, g exhibits first a positive peak at the intersections with the X structure, followed by a change of sign and a subsequent negative signal of approximately equal

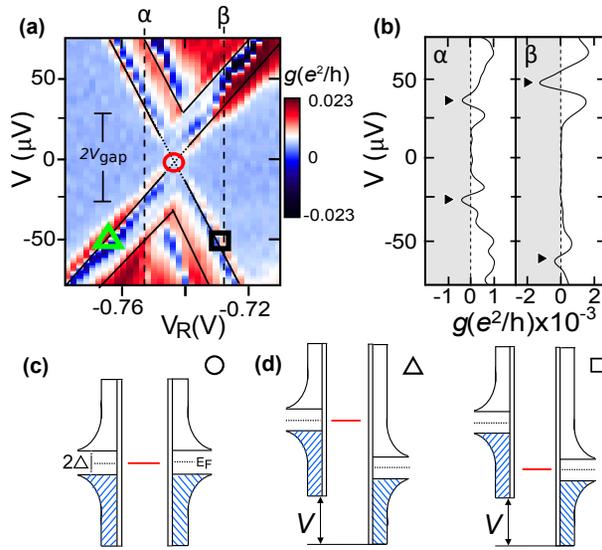


Figure 5.8: Negative differential resistance in the Coulomb diamonds of regime (iii) (a) a close-up from Fig.4a) in the main text around $V_R = -0.75$ V. α and β denote vertical line cuts shown in (b) which highlight the NDC features occurring symmetric with respect to bias voltage. The symbols (\circ, \square, Δ) indicate the energy level configurations sketched in (c) and (d).

magnitude (black arrows in figure 5.8(b)).

Generally, NDC reflects the alignment of the island state with a sharp DOS peak in the reservoirs. This becomes clear when we consider the energy diagrams presented in figure 5.8(d) which sketch the configurations indicated with Δ and \square in figure 5.8(a). For both configurations increasing the bias voltage misaligns the island state with the DOS peak in the reservoir and thus reduces the current, leading to NDC. From the symmetric occurrence of NDC with respect to both V and V_R we infer that both reservoirs exhibit a sharp DOS peak. The location of the peaks close to the Fermi level could indicate that it is related to the Cooper pair DOS. Recent tunneling experiments, on the other hand, show indications of quasiparticle sub-gap states [134], which might give rise to features similar to the ones observed here. We note that NDC at the boundaries of the Coulomb diamonds disappears if a magnetic field is applied, cf. Figure 5.7. This further confirms that the NDC observed here originates from superconductivity.

TRANSPORT DATA FROM DEVICES WITH VARIOUS GATE GEOMETRIES

We have observed series of conductance peaks in several devices with various gate layouts. Figure 5.9 shows measurements from three devices that complement the results presented in this chapter.

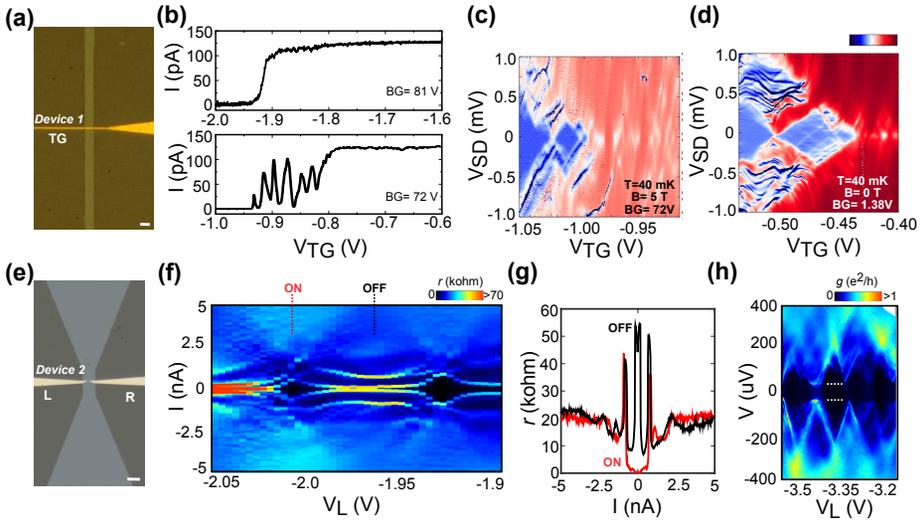


Figure 5.9: (a) is the optical image of the Device 1 which consists of a 1 μm wide top gate on 5 μm wide LAO/STO channel. Scale bar is 5 μm . (b) is the gate characteristics of the Device 1 in two different back-gate voltages. (c-d) are the 2D colormaps of differential conductance showing coulomb blockade behavior. (e) is the optical image of the Device 2 which consists of split-gate configuration. Tip-tip distance is approximately 200 nm. Scale bar is 5 μm . (f) is the 2D colormap of differential resistance as a function of V_L . It shows periodic switching between OFF-state and ON-state with $\Delta V_L \approx 84$ mV. (g) is the vertical line cuts of OFF-state (black-curve) and ON-state (red-curve). (h) is the 2D colormap of differential conductance vs V_L . It shows series of conductance diamonds that are gapped (indicated by white dashed lines) due to superconductivity in the device. $V_{\text{gap}}/4 = \Delta \approx 20$ μeV .

Device 1 (Top panel, figure 5.9(a-d)) is equipped with a single 1 μm wide top-gate across a 5 μm wide LAO/STO channel. An optical image of the device is given in figure 5.9(a). The corresponding pinch off curves for small bias current are given in figure 5.9(b). The measurements were taken at $T=40$ mK at two different back-gate voltages. For higher carrier densities ($V_{BG}=81$ V), shown in the top panel, we observe the expected current pinch-off at $V_{TG} = -1.9$ V. When we decrease the carrier density in the sample ($V_{BG}=72$ V, bottom panel) the pinch-off is reached already at a higher voltage $V_{TG} = -0.95$ V. Moreover, current pinch does not take place in a continuous transition. Instead, a series of conductance peaks arises. Figure 5.9(c) shows that the low conductance regions between the peaks close for large bias voltage, giving rise to characteristic conductance diamonds. Figure 5.9(d) presents a similar measurements on the same device for a different back gate voltage and zero magnetic field.

Device 2 (Bottom panel, figure 5.9 (e)) consists of only two split gates which are separated by a 200 nm gap (tip-tip distance). Comparable to the device discussed

in the main text, we find for Device 2 that current predominantly flows under one of the gates (here: gate L). Therefore, we use this gate to control transport. Figure 5.9(f) presents a 2D colormap of differential resistance ($r=dV/dI$ vs V_L). It shows a behaviour similar to the intermediate regime discussed in the main text. The periodicity of the ON-state is $\Delta V_L \approx 84$ mV. Vertical line cuts of the ON (red-curve) and OFF-state (black-curve) are given in figure 5.9(g). The zero-bias resistance varies between $r=44$ k Ω [OFF] and $r=0.3$ k Ω [ON]. Decreasing the gate voltage tunes the system into the Coulomb blockade regime, shown in figure 5.9(h). The Coulomb diamonds exhibit a voltage gap $V_{\text{gap}} \approx 20$ μV (white dashed lines), which is of the same order as for the device discussed in the main text.

5.5.3. ADDITIONAL ANALYSIS

ESTIMATING THE SIZE OF THE ISLAND †

We model the electrostatic environment in the constriction, by utilizing a procedure similar to the one applied in a previous work [31], using finite element analysis in COMSOL® 5.2.

The geometry which we use to model our device is shown in figure 5.10(a). 5 nm LaAlO₃ with dielectric constant $\epsilon_r = 24$ [135] cover the SrTiO₃ substrate. The conductive two dimensional electron system (2DES) is situated at the interface. The dielectric properties of STO are described by the Landau-Ginsburg-Devenshire Theory [136, 137],

$$\epsilon_{STO} = 1 + \frac{B}{[1 + (E/E_0)^2]^{2/3}},$$

with E being the local electric field, $B = 25000$ and $E_0 = 82000$ V/m [138]. The split gates L and R are modelled as 100 nm thick Au electrodes. The tips of the split gate are separated from each other by the distance $D = 150$ nm. Gate voltages V_L and V_R are applied to the respective gates with respect to the drain reservoir, which is kept at ground potential. The source reservoir is voltage biased. The island is modelled as a conductive disc with diameter d , which is separated from source and drain by gaps of width g .

Figure 5.10(b) shows the spatial map of ϵ_r at the LAO/STO interface for $V_L = -1$ V and $V_R = 0$. This visualizes the huge ϵ_r in large parts of the sample. In figure 5.10(c) the ϵ_r -map is shown for both gates at the same voltage ($V_L = -1$ V and $V_R = -1$ V). This results in reduction of the dielectric constant by more than an order of magnitude in the constriction and thus in the vicinity of the island.

The single electron charging energy of the island E_C is extracted by calculating the voltage between source and drain that is required to change the polarization on the island by e (electronic charge) while $V_{L,R} = -1$ V. This calculation is carried out

† Finite element analysis is performed by Nicola Manca.

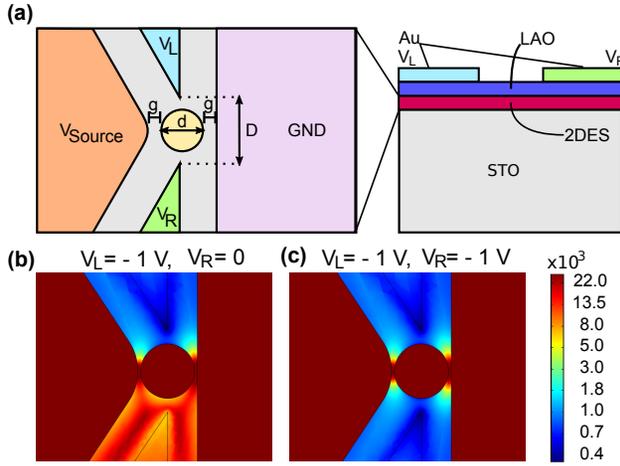


Figure 5.10: Model of the device. (a) Layer stack and geometry. (b) spatial map of the dielectric constant in the constriction at low temperature for gate voltages $V_L = -1$ V, $V_R = 0$ V and (c) for $V_L = -1$ V, $V_R = -1$ V.

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for different values of the island's diameter d and the gap g . The result is shown in figure 5.11(a). Charging energies of $60 \mu\text{eV}$ (marked by the dashed line in figure 5.11(a)) to $100 \mu\text{eV}$ are obtained for island diameters of 70 nm to 120 nm if one allows g to vary between approximately 3 nm and 6 nm.

ANALYSIS OF EXCITED STATES SIGNATURES

We can further use the transport signatures of (excited) quantum states observed in the conductance diamond regime (iv) to estimate the size of the island.

A close up of the voltage range where these features are observed is depicted in figure 5.11(b). Only positive bias voltages are shown. The delimiting lines of the Coulomb diamonds are indicated with blue lines. Transport signatures of excited states of the island due to quantum confinement can be observed in the region between two adjacent Coulomb diamonds. They appear as lines of enhanced conductance which run in parallel with the borders of the Coulomb diamonds [120, 125]. In figure 5.11(b) they are denoted with green lines. The separation between these lines along the (vertical) bias voltage axis indicates their difference in energy, $\delta\epsilon$. As an example, the energy separation of 4 such lines is indicated in figure 5.11(b) with $a = 14 \mu\text{eV}$, $b = 17 \mu\text{eV}$, $c = 21 \mu\text{eV}$. Using a simple particle-in-a-box picture, we can estimate the spatial dimension d required to obtain quantization energies of this order,

$$d = \sqrt{\frac{h^2}{8m\delta\epsilon}},$$

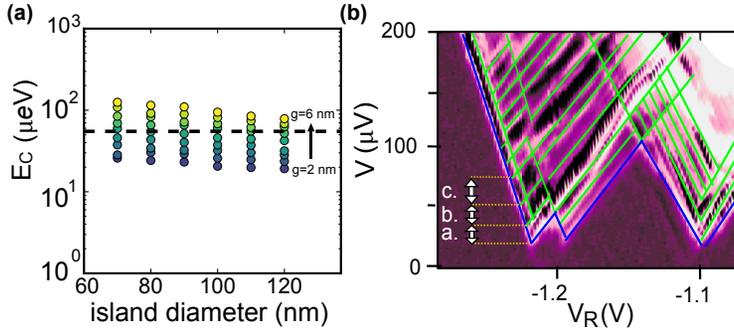


Figure 5.11: (a) Results of the numerical simulation for $V_L = -1\text{V}$, $V_R = -1\text{V}$ showing the single electron charging energy as a function of island diameter. Colors indicate the assumed gap size ranging from $g = 2$ to 6 nm. (b) Close-up of the conductive region between two adjacent Coulomb diamonds, extracted from the main text. The borders of the diamonds are denoted with blue. Green lines indicate transport signatures of excited states on the island due to quantum confinement. The energy separation between different states are indicated with $a = 14 \mu\text{eV}$, $b = 17 \mu\text{eV}$, $c = 21 \mu\text{eV}$.

where $m = 0.7m_e$ is the effective electron mass in the LAO/STO 2DES, m_e is the bare electron mass and h is the Planck's constant. Approximating by using $\delta\varepsilon = 20\mu\text{eV}$ yields an island radius of approximately 80 nm. This is in the same range as the result obtained from the purely electrostatic considerations above.

This analysis clearly shows that the energy scale of the conductance diamonds is at least a factor 3 larger than that observed for the electronic orbital contributions originating from quantum confinement. Moreover, the numerical simulations clearly show that that Coulomb repulsion cannot be neglected in the device. The results strongly suggests that Coulomb blockade is the main contribution to the observed conductance diamonds. Using both signatures to estimate island size independently yields consistent results.

5.5.4. CALCULATION OF Z AND τ

We use the Blonder-Tinkham-Klapwijk (BTK) formalism described in ref. [113] to calculate the barrier parameter Z from the excess current and the high bias conductance. The excess current I_{exc} at an S-S interface is related to the Z parameter by

$$I_{exc} = 2 \frac{g_n}{e(1 - B(\infty))} \times \int_0^\infty dE (A(E) - B(E) + B(\infty)),$$

with

$$A = \frac{\Delta^2}{E^2 + (\Delta^2 - E^2)(1 + 2Z^2)^2},$$

$$B = 1 - A,$$

for $E < \Delta$, and

$$A = \frac{u_0^2 v_0^2}{\gamma^2},$$

$$B = \frac{(u_0^2 - v_0^2)^2 Z^2 (1 + Z^2)}{\gamma^2},$$

for $E > \Delta$. Furthermore, $B(\infty) = \frac{Z^2}{1 + Z^2}$, and

$$u_0 = \frac{1}{2} (1 + ((E^2 - \Delta^2)/E^2)^{1/2}),$$

$$v_0 = 1 - u_0^2,$$

$$\gamma = (u_0^2 + Z^2 (u_0^2 - v_0^2))^2.$$

We determine I_{exc} from the experimental data by extrapolating the high bias conductance g_n at $I = 9$ nA towards $V=0$. This yields the data shown in the top panel of figure 5.3(e). Combining this with the respective g_n for each gate voltage and using $\Delta=22$ μ eV, as extracted from the dI/dV vs V curves, allows us to calculate the corresponding Z parameter, which leads to the curve shown in figure 5.12. By comparison we are then able to find the Z parameter as a function of V_R and calculate the corresponding transmission coefficient in the normal state, $\tau = 1/(1 + Z^2)$ [113].

For calculation of the critical current I_c of a disordered point contact in the diffusive transport regime we apply the equation provided by Beenakker [114]

$$I_c = 1.32 \frac{\pi \Delta}{2e} \langle G \rangle$$

where we have used the experimentally determined g_n for the average conductance $\langle G \rangle$ and $\Delta = 22$ μ eV. This yields the blue dashed curve shown in the bottom panel in figure 5.3(e).

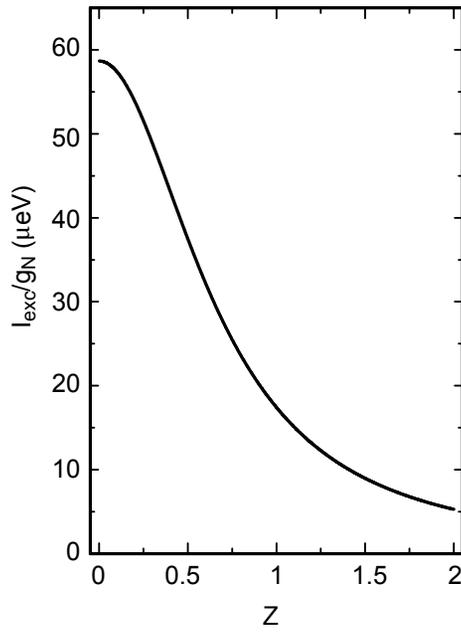


Figure 5.12: Calculated Z-parameter: Experimentally determined I_{exc}/g_n and the corresponding Z-parameter determined for an S-S interface using BTK theory.

6

SUPERCONDUCTING HETEROJUNCTIONS

Here, we report our on-going work on combining the LAO/STO interface with a conventional, s-wave, superconductor in different device geometries that would enable performing phase-sensitive tests of the superconducting order parameter in a corner SQUID geometry.

6.1. INTRODUCTION

Conventional superconductors have nearly isotropic superconducting gap (Δ) and phase (Φ) in all crystal directions. Unconventional superconductors, on the contrary, exhibit nodes at certain crystallographic directions at which the superconducting gap (Δ) is zero and the phase (Φ) shifts by π . Figure 6.1 shows some of the pairing states namely isotropic s-, $d_{x^2-y^2}$ and p_y , their magnitude of the gap and relative phase as a function of k -space direction.

The first confirmation of the unconventional superconductivity is the discovery of d-wave pairing in high T_C cuprates through experiments which are sensitive to the relative phase of the order parameter [86]. Figure 6.2(a,d) show device schematics that are used to perform such tests in a SQUID geometry. Josephson junctions (JJs) are formed by placing a weak link material between a conventional (s-wave) superconductor and the one being tested. Since the SQUID oscillations arise due to phase difference between two JJs, anisotropy in the relative phase can be probed by creating the two JJs in different crystallographic directions. Device in figure 6.2(a) is the reference SQUID because the JJs are located at the same crystal faces. On the other hand, device in figure 6.2(d) is the corner-SQUID and it probes the 90° change in the relative phase.

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Now, let us consider isotropic s- and d-wave as candidate pairing symmetries in our superconductor under test, as shown in schematics as red and purple circle respectively. SQUID oscillations in the reference device are identical for both pairing symmetries (see figure 6.2(b,e)). However, the corner-SQUID oscillations in figure 6.2(f) exhibit a π shift, equivalent of half flux quantum, revealing the d-wave pairing symmetry since it probes different lobes of the order parameter. Thus, performing such an experiment allows one to unambiguously determine the pairing symmetry of a superconductor.

The superconducting 2DES forms at the LAO/STO interface has several properties that are reminiscent of high T_C cuprates. They both have dome-shaped superconducting phase diagram where the critical transition temperature can be altered by tuning the doping or the carrier density of the system and both exhibit pseudogap behavior outside of this phase diagram. Unconventional superconductivity at the LAO/STO interface is theoretically predicted [23, 27–30] based on experimental evidence of coexistence of magnetism and superconductivity [24–26] and is subjected to experimental investigations [111]. In this chapter, we report our ongoing efforts on combining LAO/STO 2DES with a conventional superconductor in different device geometries that would enable performing phase sensitive tests in a corner-SQUID geometry and thus can shed light on the pairing symmetry of this interfacial superconductor.

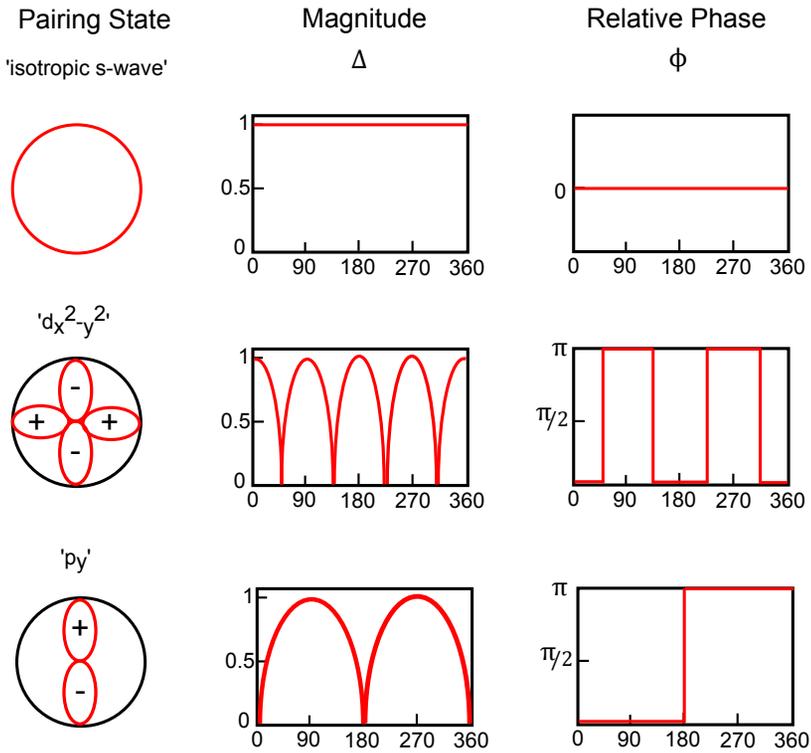


Figure 6.1: **Magnitude and phase of the superconducting order parameters.** 'isotropic s-wave', ' $d_{x^2-y^2}$ ' and ' p_y ' as a function of crystallographic direction

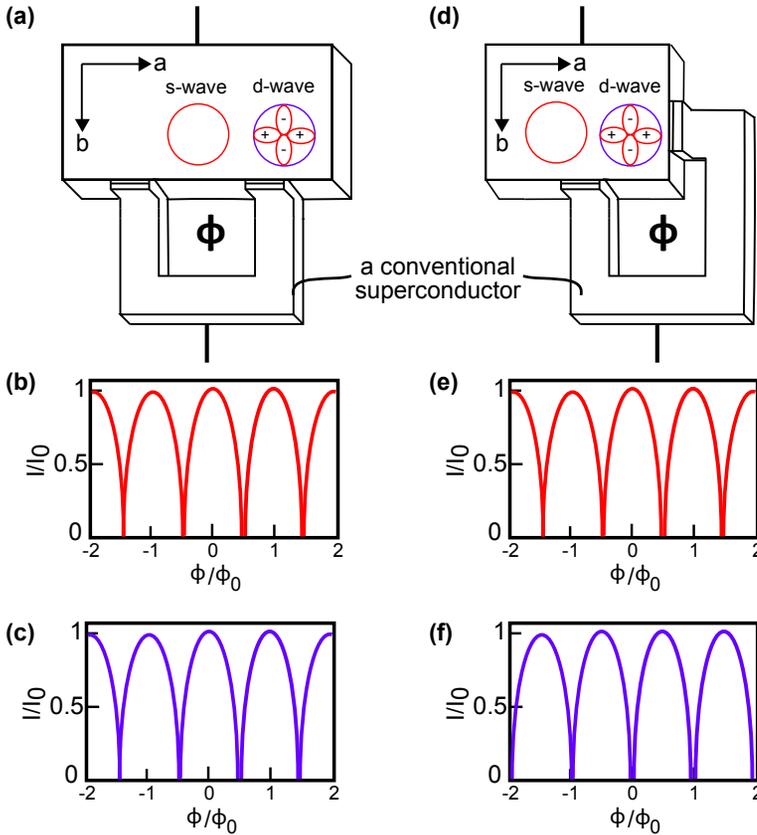


Figure 6.2: **Phase sensitive tests of the superconducting order parameter.** Reference and corner-SQUIDs for testing s- and d-wave pairing. (a) Reference SQUID-JJs are at the same crystal faces. SQUID oscillations of (b) s-wave and (c) d-wave pairing. (d) Corner-SQUID-JJs are at the orthogonal crystal faces. SQUID oscillations of (e) s-wave and (f) d-wave pairing. π shift, equivalent to half flux quanta for corner-SQUID occurs, revealing d-wave pairing symmetry.

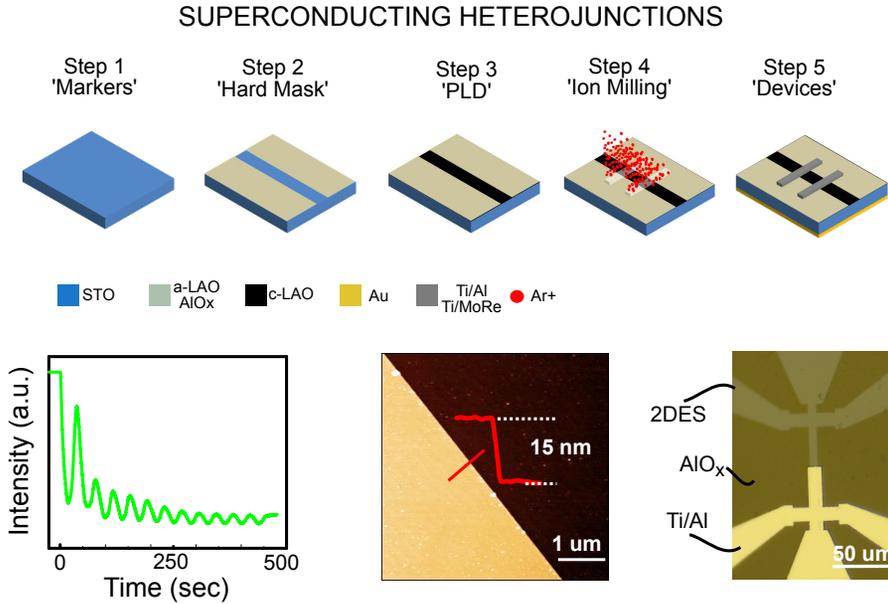


Figure 6.3: **Fabrication route of Superconducting Heterojunctions.** (Top panel) Following growth of LAO layer, ion milling and subsequent deposition of superconducting electrodes is used to create the heterojunctions. (Bottom panel) Left: RHEED oscillations recorded during the growth of 12 unit cell LAO. Middle: AFM image of 5 minutes ion milled STO substrate for determining the mill rate. Right: Optical image of the device. Ti/Al electrodes form sideways contact to the 2DES.

6.2. RESULTS

6.2.1. FABRICATION SPECIFICS

The first step is to fabricate heterojunctions at which a conventional superconductor forms sideways electrically transparent Ohmic contact to the superconducting 2DES at the LAO/STO interface. We studied two different superconductors, Al ($T_C=1$ K) and Molybdenum-Rhenium ($T_C=9$ K). Figure 6.3 shows the fabrication route for creating such devices. The details of first three steps are discussed in chapter 2. We use ion milling for the removal of the LAO layer and deposit the conventional superconductor.

We grow 12 unit cell LAO film using PLD. (RHEED oscillations during growth are shown in the bottom panel of figure 6.3). Following growth, electron beam lithography is used to pattern the superconducting electrodes. The sample is spin coated with single layer PMMA resist (950 K, 6K rpm, 500 nm total thickness) and exposed at a dose of $800 \mu\text{C}/\text{cm}^2$. Ar⁺ ion milling is performed under 5 standard cubic cen-

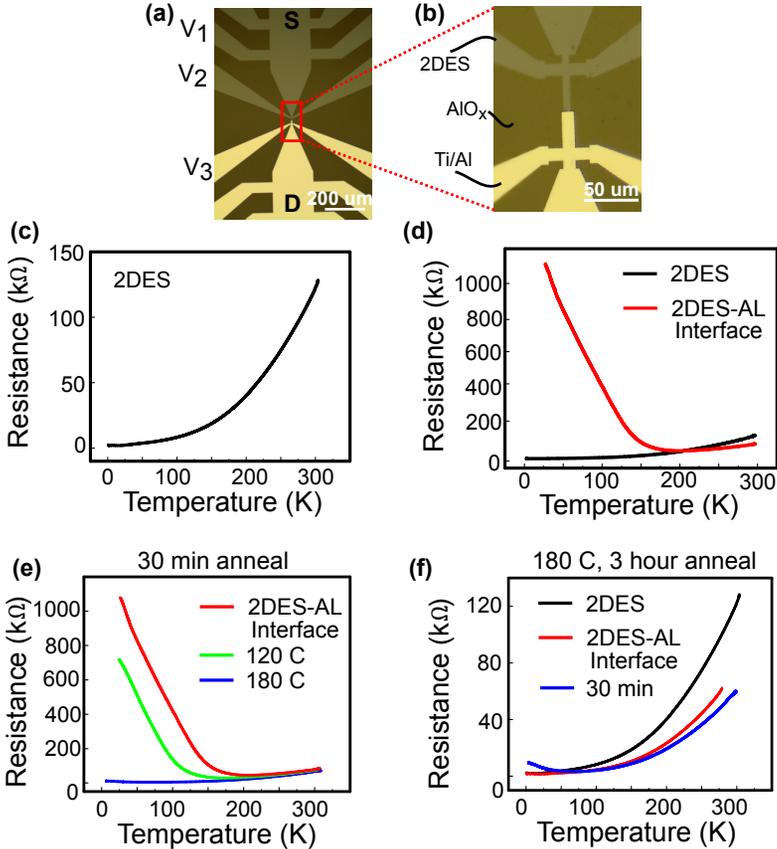


Figure 6.4: **Characterization of the 2DES and 2DES-Ti/Al interface.** (a) Optical image shows the sample layout. (b) Zoom-in of the device which consists of an interface between 2DES and Ti/Al electrodes and schematic side view. (c) Resistance versus temperature (R vs T) curve of the 2DES showing the metallic behavior of the 2DES. (d) R vs T of the 2DES-Ti/Al interface showing the insulating behavior. R vs T of the 2DES-Ti/Al electrode interface as a function of (e) post-annealing temperature and (f) duration. Annealing at 180 $^{\circ}\text{C}$ for 3 hours forms electrically transparent Ohmic contact.

timeters per minute (sccm) flow and using 10 mA beam current. Ion milling rate is determined using a bare STO substrate and found to be 3 nm/min. Bottom middle panel is the atomic force microscopy (AFM) image of 5 minute milled substrate. Ti/Al electrodes are created by depositing 20 nm titanium (Ti, 0.5 Å/sec) followed by 100 nm aluminum (Al) using electron beam evaporation technique. The first 20 nm of Al is evaporated at a rate of 0.5 Å/sec, then increased to 1 Å/sec for remaining 80 nm. Molybdenum-Rhenium (MoRe, 60/40) electrodes, on the other hand, are RF-sputtered following 20 nm Ti deposition. Electrode deposition is followed by ultrasonic lift-off in acetone. Optical image of the device (bottom-right panel) shows the 2DES in light gray, AlO_x hard mask in dark green and Ti/Al electrodes in yellow color.

6.2.2. CHARACTERIZATION OF DEVICES

We performed electrical characterization in a current bias configuration using a flow cryostat with base temperature of 1.5 K. Figure 6.4(a) shows the sample layout. 200 μm wide region tapers down to 5 μm wide channel. Figure 6.4(b) is an optical image of the device region where the Ti/Al electrode is expected to form sideways contact to the 2DES. A constant current bias of 100 nA is applied using source (S) and drain (D) pads while the differential resistance (R) is recorded at an acquisition rate of 17 Hz using standard lock-in technique (Stanford Instruments). The voltage pads V_1 and V_2 are used for electrical characterization of the 2DES, while V_2 and V_3 are for the interface between the 2DES and the Ti/Al electrodes.

Figure 6.4(c-d) show the resistance of the 2DES and of the interface as a function of temperature in the range from 300 K to 1.5 K, respectively. Resistance of the 2DES drops from 120 k Ω to 2.5 k Ω when cooled down, as expected from a metallic 2DES (black curve in figure 6.4(c)). However, the 2DES-Ti/Al interface exhibits an insulating behavior. Red curve on figure 6.4(d) shows an upturn around 150 K where resistance of the interface increases as temperature decreases, reaching to 1.1 M Ω at 1.5 K.

The insulating behavior of the 2DES-Ti/Al interface could be due to poor electrical contact between two materials and thus the formation of a Schottky barriers. In order to ensure the good electrical connectivity, we have performed an annealing treatment for 30 minutes at ambient atmosphere using an industrial furnace. The results are given in figure 6.4(e-f). Figure 6.4(e) shows resistance versus temperature curves of the device for annealing temperatures of 120°C (green curve) and 180°C (blue curve). We observe a decrease in upturn temperature to 100 K. Moreover, the resistance value at 1.5 K is dropped from 1.1 M Ω to 700 k Ω . Increasing the annealing temperature to 180°C further moves the upturn to 30 K while decreasing the resistance value to 12 k Ω as shown by blue curves in figure 6.4(e-f). Furthermore, we found that electrically transparent contacts can be formed by increasing the annealing duration to 3 hours. Red curve in figure 6.4(f) shows the resistance of 2DEG-Ti/Al

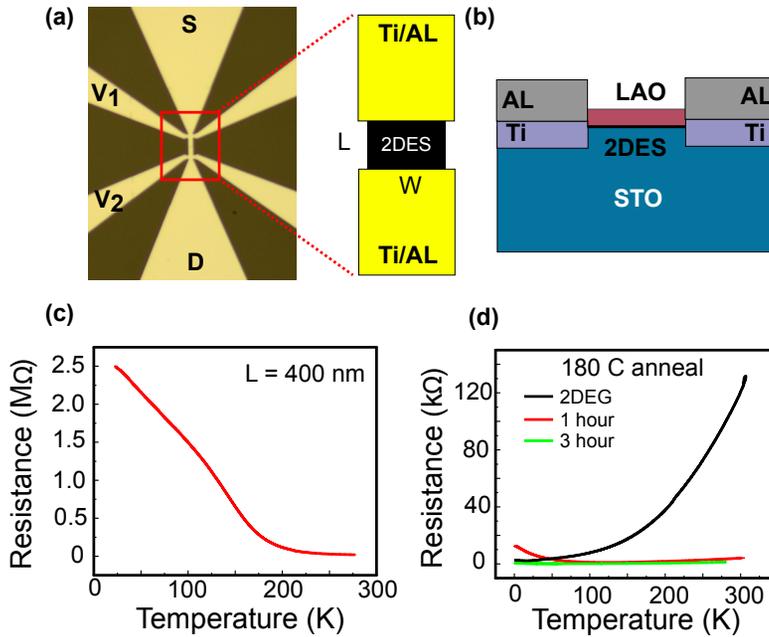


Figure 6.5: LAO/STO 2DES as weak links in Josephson junctions. (a) Optical image of the sample and the device layout. Separation between Ti/Al electrodes is 400 nm, by design. (b) Schematic cross-sectional view of the device. (c) Resistance vs Temperature curve showing the insulating behavior of the device upon cool down. (d) Effect of annealing duration on the device properties. Annealing at 180 °C for 3 hours forms electrically transparent ohmic contact.

interface annealed at 180°C. While the upturn in resistance completely disappeared, its 1.5 K value decreased to 2.5 kΩ.

Next, we fabricated superconducting heterojunctions at which LAO/STO 2DES is sandwiched between Ti/Al electrodes. These devices take advantage of the Ohmic transparent interface between the two different materials and use LAO/STO 2DES as weak links in Josephson junctions. Figure 6.5(a) shows the optical image of the device and its layout. Here, 6 μm wide Ti/Al electrodes are in sideways contact with LAO/STO 2DES with a width (W) of 5 μm and length (L) of 400 nm. Figure 6.5(b) shows cross-sectional view of the device. Electrical characterization prior to and after the post-annealing treatment is given in figure 6.5(c-d), respectively. The insulating behavior of the device as shown in figure 6.5(c) upon cooling down is consistent with formation of Schottky barriers at the interface between two materials. However, electrically transparent contacts are achieved by performing post-annealing treat-

ment at 180°C for 3 hours (green curve in figure 6.5).

6.3. CONCLUSIONS

To conclude, we demonstrated a fabrication route that allows us to obtain electrically transparent interface between Ti/Al electrodes, a conventional (s-wave) superconductor and the two dimensional superconductor forms at the $\text{LaAlO}_3/\text{SrTiO}_3$ interface.

6.4. ADDITIONAL INFORMATION

6.4.1. MOLYBDENUM-RHENIUM (MORE) ELECTRODES

Figure 6.6(a-b) shows the optical image of the sample which is fabricated by interrupting $3\ \mu\text{m}$ wide LAO/STO channel with Ti/MoRe (20/80 nm) electrodes. Separation between the electrodes is varied from 100 nm to 500 nm, allowing us to study the length (L) dependence of the LAO/STO weak links. Figure 6.6(c) shows the AFM image of the electrode area. We characterized two devices, device 1-2 (L=300 nm) and device 2-3 (L=400 nm), in a dilution refrigeration at $T_{base} = 40\ \text{mK}$ by sourcing a current bias, I_{SD} , and measuring the consequent voltage drop, V_{SD} . Both devices exhibited a non-zero resistance ($1-2\ \Omega$) below their critical current value which was approximately 150 to 200 nA. Moreover, we applied perpendicular magnetic field and recorded current-voltage characteristics of the devices. The results are presented in figure 6.6(d) and (e) by plotting the 2D colormaps of the differential resistance as a function of applied current bias and magnetic field. We observe a quick decay in the critical current which is followed by aperiodic modulations with applied magnetic fields. Figure 6.6(f-g) show the same plots with calculated Fraunhofer patterns in white dashed lines expected from a JJ.

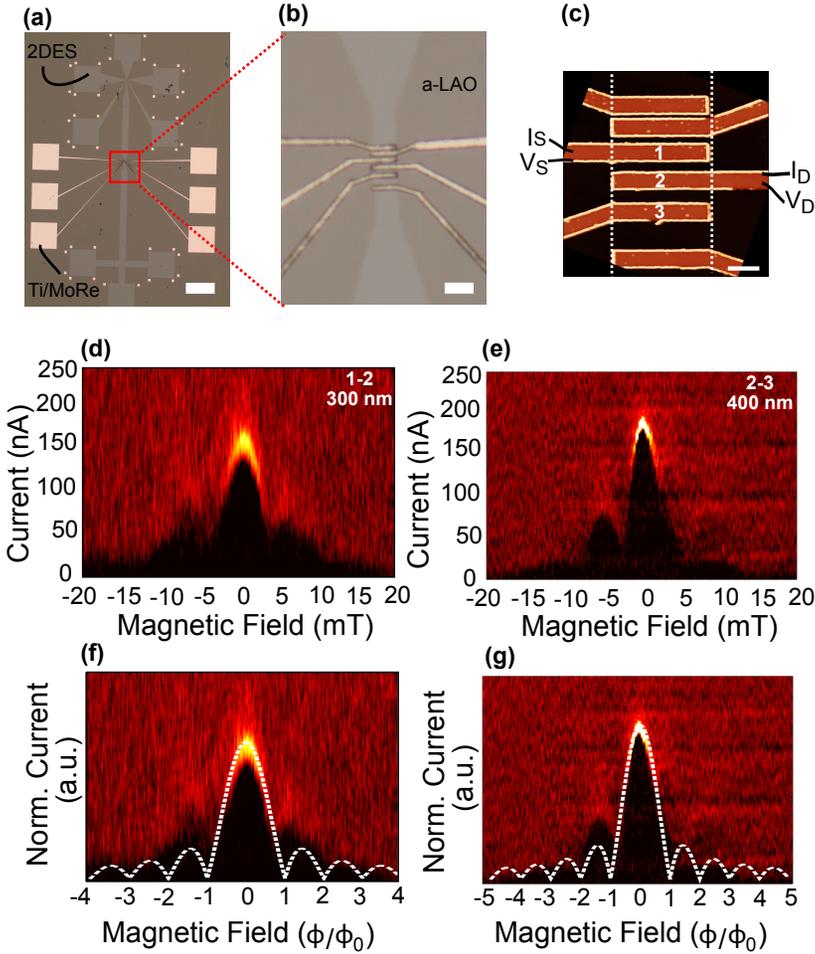


Figure 6.6: MoRe(S)-LAO/STO 2DES(S')-MoRe(S) Josephson junctions (a) Optical image of the sample. Scale bar is $150 \mu\text{m}$. (b) Zoom-in to the device area. (c) AFM image of the device area. Electrode separation varies linearly from 100 nm to 500 nm (top to bottom). Scale bar is $1 \mu\text{m}$. 2D colormaps of (d) the device 1-2 ($L=300 \text{ nm}$) and of (e) the device 2-3 ($L=400 \text{ nm}$) showing critical current and its modulations upon perpendicular magnetic fields. (f-g) Same plots of (d) and (e) with simulated Fraunhofer patterns given in white dashed lines.

7

CONCLUSIONS AND OUTLOOK

*We are the reckless
We are the wild youth
Chasing visions of our futures
One day we'll reveal the truth*

from Youth, If you leave (2013), Daughter

7.1. CONCLUSIONS

To conclude, we presented nanoscale electrostatic control on superconducting oxide interfaces, namely on the two-dimensional electron system (2DES) at the LaAlO_3 (LAO)/ SrTiO_3 (STO) interface. This 2DES exhibits emergent properties such as magnetism, strong spin-orbit interaction and gate tunable superconductivity. In addition, an electric field can be used to tune the critical temperature of the superconducting transition, revealing a dome-shaped phase diagram that is reminiscent of high T_C superconductors. Here, we exploited the gate tunable property of the system by use of patterned local top gates and achieved nanoscale electrostatic control of the electronic properties of the 2DES which enabled creation of low dimensional superconducting devices with electrostatic interfaces.

First, we fabricated our devices using pulsed laser deposition (PLD) for the oxide growth and multiple steps of aligned electron beam lithography (EBL) for patterning the 2DES and our nanoscale top gates. We patterned 60 nm wide constrictions and developed a recipe for aligned lithography using tungsten (W) markers which survives the high temperatures of the PLD process, enabling to pattern nanoscale top gates via EBL and subsequent gold deposition.

Next, we demonstrated the *nanoscale electrostatic control* on LAO/STO interfaces by use of patterned local gates. First, we used finger type top gates and achieved the field effect transistor operation at room temperature by depleting the metallic interface with gate voltages and negligible leakage currents. At milliKelvin temperatures, when the interface is superconducting we used a single narrow nanoscale top gate to drive locally a superconducting to insulating transition and we see evidence for a superconducting weak link with a gate-dependent critical current. Second, we realized a split gate geometry, through which charge carriers can be confined to narrow conducting channels. We created a nanoscale constriction whose width is set by the distance between the gates and can be further reduced with gate voltages. In addition, at low temperatures the high and field dependent dielectric constant of STO results in stray electric fields between these gates.

Third, we performed phase sensitive measurements of the superconducting order parameter by realizing the first superconducting *quantum interference* devices (SQUIDs) at the LAO/STO devices. Here, we followed two distinct approaches for creation of the SQUIDs. The first one uses 60 nm wide patterned LAO/STO constrictions at the SQUID arms which form the Josephson junctions (JJs), a widely used approach for JJs and thus SQUIDs. We showed that the low superfluid density of this interfacial superconductor results in a large, gate controllable kinetic inductance of the SQUID. In these devices, we used the STO substrate as a back gate, allowing to control the global electronic properties of the entire device. In the second approach, we developed a new paradigm for the creation of superconducting circuit elements, where local gates enable in-situ creation and control of the JJs. These gate-defined SQUIDs are unique in that the entire device is made from a single superconductor

with purely electrostatic interfaces. In addition, we demonstrated the tunability and control on the JJs with electrostatic gate voltages by creating asymmetric JJs, allowing us to estimate the kinetic inductance of the SQUID arms.

Fourth, we demonstrated for the first time the formation of a *superconducting quantum point contact (SQPC)* with patterned split gates on a superconductor, utilizing the unique gate tunability of the two dimensional superfluid at the LAO/STO interface. When the constriction is tuned with gate voltages, we identified three regimes of transport. In the first regime (i), SQPC is formed at which supercurrent is carried only by a few quantum transport channels with finite transmission probabilities extracted using Blonder-Tinkham-Klapwijk (BTK) formalism. We used excess current to calculate the transmission coefficient of the channels, which is then used to calculate the expected supercurrent for a SQPC and is in good agreement with the measured supercurrent. In the second regime (ii), a superconducting island which is strongly coupled to the equilibrium reservoirs is formed. We observed periodic zero-bias conductance peaks as a function of gate voltages. In addition, the periodicity reduces to half above a critical bias voltage, indicating that our island is in a superconducting state at low bias which allows Cooper pair transport (even parity) and at high bias voltages switches to single electron transport (odd parity). In the third regime (iii), a charge island with discrete spectrum which is weakly coupled to the reservoirs is formed. This regime is governed by the series of conductance diamonds which reflect the addition energy for enabling the transport across the island. We performed finite element simulations on the dielectric environment of STO and concluded that electric fields originating from the split gates reduces the dielectric constant of STO, as a result Coulomb charging energy dominates the addition energy of the island. Furthermore, we estimated size of the island to be 50-80 nm, compatible with our device size and also with the electronic inhomogeneities typically observed in LAO/STO.

Last, we demonstrated a recipe for combining two dimensional superconductor of the LAO/STO interfaces with a conventional, s-wave, superconductor in different device geometries that would enable performing phase sensitive tests of the superconducting order parameter in a corner-SQUID geometry and thus can shed light on the pairing symmetry of this interfacial superconductor. We used Aluminum (Al, $T_C=1$ K) and Molybdenum-Rhenium alloy (MoRe (60/40), $T_C=9$ K) as conventional superconductors and created superconducting heterojunctions in which ohmic electrical contact is sideways formed to the LAO/STO interface. We characterized the MoRe-LAO/STO-MoRe devices at millikelvin temperatures and observed modulation of the critical current upon application of perpendicular magnetic fields.

7.2. OUTLOOK

As an outlook, we discuss the future improvements and few follow-up studies regarding the results presented throughout this thesis.

As demonstrated in chapter 2, we pattern narrow nanoscale top gates, 100-150 nm in width, using double layers of positive e-beam resists. This width can be further reduced, down to ~ 10 nm, using a negative resist such as hydrogen siloxane (HSQ), as demonstrated in silicon substrates [139].

The essential requirement for a reliable gate operation is to prevent leakage between the gates and the 2DES. Throughout this thesis, we obtain negligible leakage currents, $I_{\text{leak}} < 300$ pA in a gate voltage range, $V_{\text{gate}} \pm 4$ V. We note that the gold which we use for patterning our nanoscale top gates, makes ultrasonic wire bonding difficult, and successive bonding attempts can create an electrostatic discharge, which might result in leakage. An additional e-beam lithography step for patterning the bonding pads of gold nanoscale top gates which involves deposition of a sticking layer as platinum or titanium would be beneficial for easier bonding and thus preventing possible leakage.

Patterned split gates, as demonstrated in chapter 3, can be used to create a narrow constriction, which can be further confined through electrostatic gate voltages. This would allow to reach 1D transport limit, at which charge carriers flow through the constriction in a ballistic manner with few electron modes at the high mobility metallic 2DES, where the mean free path of the electrons is comparable to the constriction width. High mobility samples ($\mu \approx 4000\text{-}5000$ cm²/V·s) can be obtained by an optimization of the oxide growth temperature, as demonstrated by Caviglia et al. [140], or by inserting a capping layer above the LAO film [69]. Furthermore, 1D transport limit at LAO/STO interfaces would allow investigations of the electronic band structure including the sub-band occupations and their spin states, as recently studied in AFM-sketched 1D devices [141].

Few nanoscale top gated devices revealed the formation of a conducting island with electrostatic gate voltages without regard of the top gate geometry, as shown in chapter 5. In low density semiconductors, emergence of the conducting islands are known to occur because of charge puddles due to local inhomogeneities present in the potential landscape, leading to quantum-dot like transport behavior [117–122]. At LAO/STO interfaces, local inhomogeneities are known to be present and our estimation of the island size is comparable with their reported size [26, 126, 127]. Thus, performing nanoscale top gating experiments, that are focused on emergence of the conducting islands might reveal the role, the nature of local inhomogeneities, and their effect on the macroscopic properties of LAO/STO interfaces. In addition, we note that the level quantization of the conducting island ($\delta\epsilon$), which arises due to quantum confinement effects, is in the order of the extracted superconducting gap (Δ), $\delta\epsilon \sim \Delta \approx 10\text{-}20$ μeV , satisfying the Anderson's criterion of superconductivity at small scales [129, 142]. Thus, further investigations of this regime can reveal

the details of microscopic superconductivity such as pairing of electrons above the T_C [87, 143].

The fabricated superconducting heterojunctions, which are presented in chapter 6 (see figure 6.4 and 6.5), are to be characterized at millikelvin temperatures. This would allow to conclude 1) the superconducting properties of such heterojunctions are governed by the 2DES since it is a low T_C superconductor and 2) Josephson junctions (JJs) and SQUIDs can be created using LAO/STO 2DES as gate-tunable weak links. Next, the titanium layer beneath the aluminum is to be replaced with a normal metal such as gold, which would be the weak link, creating Superconductor (S)-Normal Metal (N)-LAO/STO 2DES JJs. Last, the phase anisotropy can be probed by fabricating the JJs in different crystallographic directions at the LAO/STO interface in a corner SQUID geometry and can reveal the pairing symmetry of this interface.

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9. H. Thierschmann*, E. Mulazimoglu*, N. Manca, S. Goswami, T. M. Klapwijk, A. D. Caviglia *Superconducting quantum point contact with split gates in the two dimensional LaAlO₃/SrTiO₃ superfluid*, Submitted (2017).
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2. E. Mulazimoglu, S. Coskun, M. Gunoven, B. Butun, E. Ozbay, R. Turan, H. E. Unalan *Silicon nanowire network metal-semiconductor-metal photodetectors*, Applied Physics Letters **103**, 083114 (2013).
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Oude Delft, Delft
Emre Mülazımoğlu

