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An All-Digital PLL for Cellular Mobile Phones in 28-nm CMOS with −55 dBc Fractional and −91 dBc Reference Spurs

Feng-Wei Kuo, Masoud Babaie, *Member, IEEE*, Huan-Neng Ron Chen, Lan-Chou Cho, Chewn-Pu Jou, Mark Chen, and Robert Bogdan Staszewski, *Fellow, IEEE*

***Abstract*— We propose a time-predictive architecture of an all-digital PLL (ADPLL) for cellular radios, which is optimized for advanced CMOS. It is based on a 1/8-length time-to-digital converter (TDC) of stabilized 7-ps resolution, as well as wide tuning range, and fine-resolution class-F digitally controlled oscillator (DCO) with only switchable metal capacitors. The 0.4-mW TDC clocked at 40 MHz maintains 7-ps resolution for <−107 dBc/Hz in-band phase noise while the 7.3-mW DCO emits −157 dBc/Hz at 20 MHz offset at 2 GHz. Reference spurs are <−91 dBc, while fractional spurs are <−55 dBc. The ADPLL supports a 2-point modulation and consumes 11.5-mW while occupying 0.22 mm^2.**

***Index Terms*— All-digital PLL (ADPLL), digitally controlled oscillator (DCO), time-to-digital converter (TDC), spurs, long-term evolution (LTE), 4G cellular.**

I. Introduction

MOBILE phones enjoy the largest production volume of any consumer electronics product. However, the demands they place on monolithic local oscillators (LO), realized as RF PLLs, are particularly tough, especially on integration with digital processors, low area of silicon, low power consumption, low phase noise (PN), and virtually no spurious tones, while being robust against environmental changes. Moreover, as each wireless standard has its own set of specifications, the implementation of a multi-standard PLLs has become a challenging task. For instance, narrow bandwidth systems, such as GSM of 2G and enhanced data rate for WCDMA of 3G, put enormous stress on low out-of-band PN, while wide bandwidth systems, such as 4G/5G, demand particularly low in-band (IB) PN. The need for backward compatibility dictated by the 3GPP cellular standard [1]–[5] combined with strict marketing requirements to avoid expensive and bulky external SAW filters requires virtually any cellular frequency synthesizer on the market to feature ultra-low out-of-band (OOB) phase noise. The most prominent example is PN = −162 dBc/Hz at 20 MHz offset of the 915 MHz carrier in order to be backward compatible with the 2G GSM standard [6], [7]. Consequently, the focus of our research is on the implementation of multi-standard cellular PLLs capable of satisfying both the OOB and IB PN constraints, while minimizing area and power consumption.

ADPLL Parameter	4G (LTE)	5G
Frequency Range* (MHz) *lower subset	700-2690	700-6000 28000,38000
Phase Noise @ 20MHz (dBc/Hz)	-162	-156
In-Band Phase Noise @ 200kHz(dBc/Hz)	-105	
Fractional spurs (dBc)	<-40	

Fig. 1. Brief overview of most relevant RF performance targets of latest mobile standards.

As for the IB PN, the challenging requirements stem from the complex modulation schemes (e.g., 16- or 64-QAM) to support 4G/5G high data rates at good spectral efficiency of bandwidth-constrained (e.g. 20 MHz) channels [8]. A good summary of 2G/3G/4G RF PLL specifications can be found in [9]. Although the 5G requirements have not been finalized yet, extensive system-level simulations carried out in [10] jointly by Keysight, Ericsson and Huawei confirmed that the IB PN needs to be maintained at −105 dBc/Hz at 200 kHz offset also from the 6 GHz carrier. Figure 1 highlights a subset of the most critical RF specifications [9] for our ADPLL.

All-digital PLLs (ADPLL) for cellular radios have been competing with analog PLLs in terms of performance and power consumption but with clear advantages in terms of amenability with scaled CMOS, integration with digital logic, programmability and built-in self-testability [6], [7], [11]–[14]. In this paper, we propose an ADPLL architecture which reduces the required TDC range by a factor of 8, thus improving its linearity. This is instrumental in minimizing fractional spurs almost to the level normally

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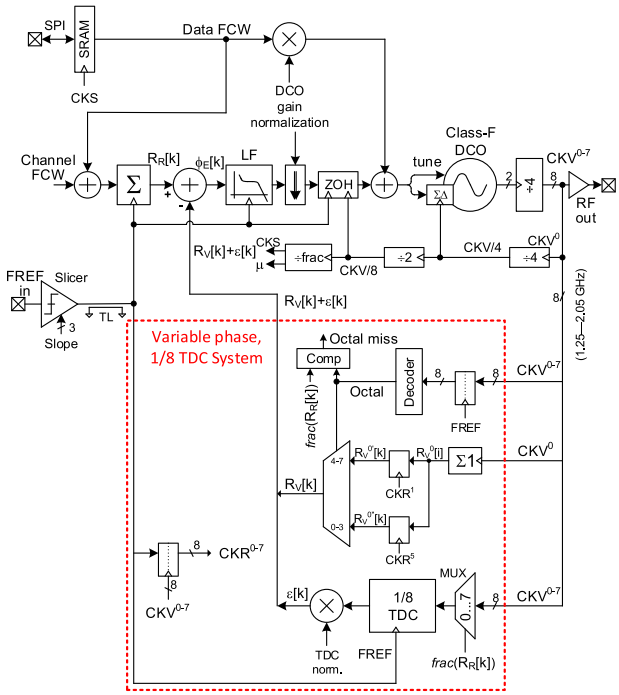

Fig. 2. Block diagram of the proposed ADPLL with 1/8-length TDC and 2-point frequency modulation.

obtained via complex schemes [15]. The TDC resolution is made 2× finer by employing an interpolating parallel sampling arrangement, and it is stabilized over process, voltage, and temperature (PVT) variations. This contributes to the minimizing of in-band PN. The DCO is based on a class-F topology and features a wide tuning range with excellent figure-of-merit (FoM). This is key to minimizing the far-out PN at low power consumption. As the DCO typically consumes disproportionately large power in ADPLLs, this leads to a substantial reduction in overall power. Realized in 28 nm CMOS, the ADPLL covers the advantages of both the low in-band and out-of-band PN while maintaining a small size and low power consumption.

This paper is organized as follows. In Section II, an overview of the proposed ADPLL architecture is provided. The design of TDC and the proposed calibration technique to maintain the TDC resolution over PVT variations are described in Section III. Section IV details the class-F DCO. Measurement results are presented in Section V. Section VI wraps up the paper.

II. Time-Predictive ADPLL Architecture

Fig. 2 shows a block diagram of the multi-rate ADPLL. It can support sampling rates for data frequency modulation (FM) much higher than the reference frequency, as was proposed in [7]. Here, it is verified for a class-F oscillator [16] featuring a transformer with two strongly coupled LC tanks for FM modulation.

Conventionally, length of the time-to-digital converter (TDC) should cover either the full period of the DCO (T_V) [17] or of reference (FREF) clock (T_R) [18]. An ADPLL that requires only a 1/8-T_V sized TDC is proposed in Fig. 2. With an 8-phase CKV generated in the loop, the phase selector chooses the one that is closest to the FREF edge and feeds it to TDC. The error compensator then corrects ϕ_E based on the fractional value of the accumulated frequency command word (FCW) [19], [20]. By this predicting process, the TDC length merely covering 1/8-T_V is sufficient. With the TDC resolution of 7 ps, 12 stages are implemented with full coverage of PVT variations.

The ~2 GHz ÷4 divider output of 8 phases, CKV^{0-7}, oversamples the external frequency reference (FREF: 10–50 MHz) generating CKR^{0-7} vector clock to sample the variable DCO phase $R_V[k]$ to calculate the phase error, $\phi_E[k]$. To avoid metastability in FREF retiming, FREF is simultaneously oversampled by different phases of CKV and an edge selection signal chooses the path farther away from metastability. The $\phi_E[k]$ is fed to the proportional-integral (PI) loop filter (LF) with a 4th-order IIR filter. The LF is dynamically switched during frequency acquisition to minimize the settling time while keeping the phase noise (PN) at optimum. The FREF slicer contains a 3-bit slope control to reduce the FREF spurs at the cost of a slight increase of in-band PN [14]. The built-in DCO gain, K_{DCO}, and TDC gain, K_{TDC}, calibrations are autonomously performed to ensure the wideband FM response. Five wide SRAMs and other digital arithmetic blocks are also integrated on-chip to enable initial system debugging.

III. Time-to-Digital Converter (TDC)

The TDC resolution has traditionally been tied to the loaded delay of the basic regenerative circuit, i.e., an inverter. With only ~10 ps inverter delay now in low-leakage 28 nm CMOS versus ~30 ps a decade ago, there are over 50 inverters needed to cover the ~2 GHz (i.e., GSM high-band) variable DCO period, T_V. With each inverter introducing a small differential type of non-linearity (DNL), these non-linearities can quickly accumulate to form a much larger integral type of non-linearity (INL) of the TDC transfer function. At the same time, the new wireless standards require low in-band PN and spurious tones. While the improved TDC resolution Δ_{TDC} ($\equiv K_{TDC}$ as defined above) helps to lower the in-band quantization noise, the TDC transfer function non-linearity (i.e., INL) can create fractional spurs especially at close to integer-N channels or at wide PLL loop bandwidths [31]. Consequently, both Δ_{TDC} and INL must improve. This is accomplished here through a *simultaneous* reduction of the quantization step and TDC dynamic range.

A. 2-Way Parallelism of TDC With PVT Stabilization

Fig. 3 shows a schematic of the new TDC that exploits a 2-way parallelism to halve its quantization step. The selected DCO variable clock, CKV' (shown later as a mux output in Fig. 6), goes through a string of $L = 12$ inverters of $t_{\mathrm{inv}} \approx 10$ ps intrinsic delay. The delays are stabilized by an outer feedback loop via "TDC tuning word" (TTW) by digitally turning on/off the NMOS capacitors loading each inverter. This is needed to prevent excessive expansion of inverters (even up to 100%) at fast process corners and high supply

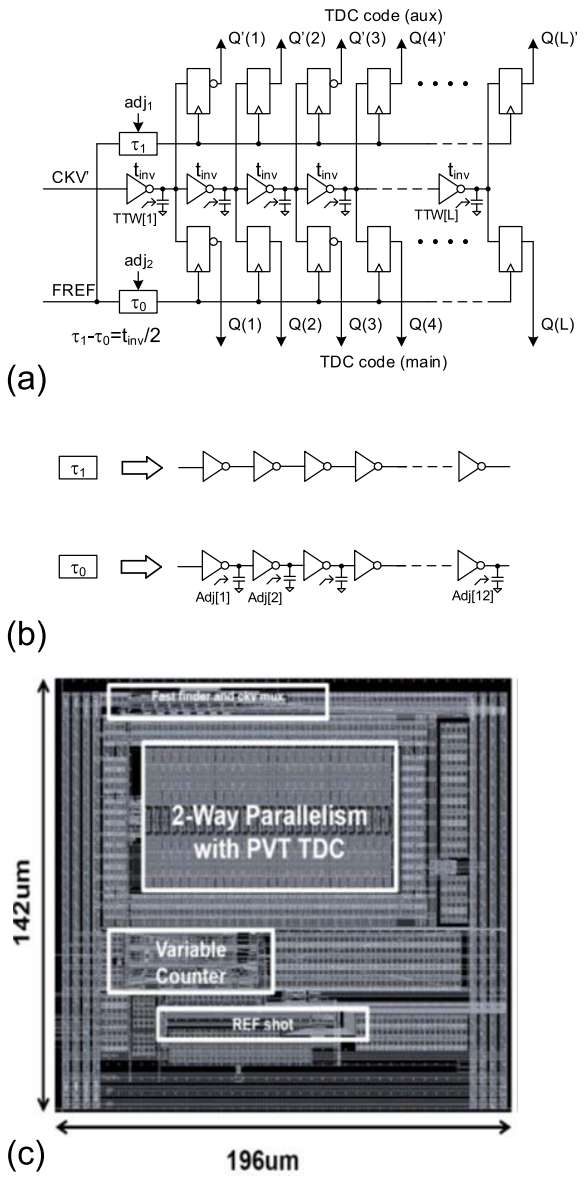

Fig. 3. Schematic (a), and layout (c), of the 2-way parallel TDC with stabilized inverter delay, t_{inv}. (b) Digital control adj[12:1] of $\tau_0 - \tau_1$.

voltages and temperatures. The inverter output bus is fed to two arrays of flip-flops (FF), which are clocked by FREF delayed by τ_0 and τ_1 for the main and auxiliary FF arrays, respectively. When the system is activated for the first time, the τ_0 and τ_1 delays are manually controlled to maintain their difference of $\tau_0 - \tau_1 = t_{\text{inv}}/2$. After that, the PVT calibration is engaged. It is based on monitoring the ADPLL's phase error (ϕ_E) and automatic fine-tuning the TTW code to reduce the TDC step size variation over PVT. The proper SEL($\tau_0 - \tau_1$) code will minimize the in-band phase noise (i.e., TDC resolution), later shown in Fig. 19 measurements. Under the extreme PVT conditions, the in-band phase noise could increase by 5–6 dB, thus likely making the LO in-compliant. Hence, the PVT calibration is utilized to reduce the in-band PN variation to only within 1dB.

Fig. 4 shows the post-layout transfer function simulations of the implemented Fig. 3 TDC. Since it only captures the

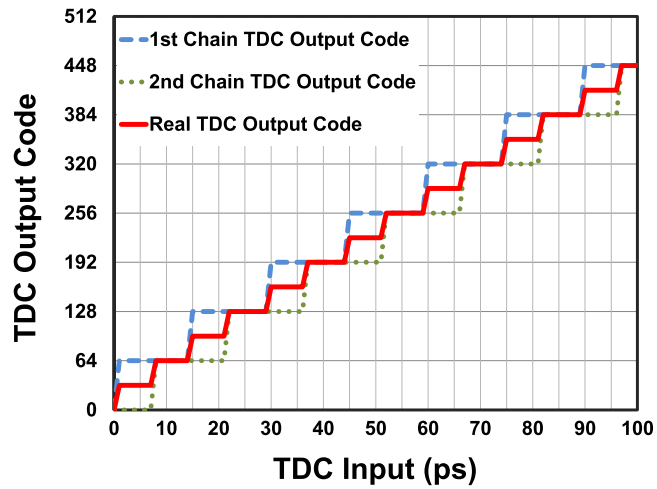

Fig. 4. Simulated nonlinearity of the 2-way parallel TDC.

deterministic mismatches in routing parasitics, the random device mismatches which account for the bulk of DNL and INL are not included. Simulation results are obtained for the two-chain delay cells. However, in practice, the TDC resolution degrades to 6–7 ps due to PVT stabilizing capacitors. For non-critical applications, the auxiliary FF array can be shut down by gating off its clock to bring the step size back to $\Delta_{\text{TDC}} = t_{\text{inv}} \approx$ 10–14 ps. The improvement in resolution is achieved by exploiting differential delays instead of actual propagation delays. Note that there is a single inverter chain but two sets of registers clocked by FREF in this scheme. Two sets of data can be combined to get a TDC noise improvement of up to 6 dB (i.e. 1 bit). However, as the loading of the inverters increases, the basic inverter delay itself rises, reducing a bit the noise improvements.

B. Short-Length TDC

Fig. 5 illustrates the principle of turning a full-length flash TDC into a short-length TDC. The traditional TDC in Fig. 5(a) passes the DCO variable clock, CKV, through a string of N_{TDC} delay elements τ (e.g., $\equiv t_{inv}$ in inverters) to create a vector of delayed clocks, CKV<0...$N_{\text{TDC}-1}$>. This vector is then sampled by an array of N_{TDC} flip-flops (FF) on rising edges of a frequency reference (FREF) clock producing a vector TDCQ < 0...$N_{\text{TDC}-1}$> with pseudo-thermometer coding of the timing separation between CKV and FREF. The full CKV period T_V needs to be covered, hence $N_{\text{TDC}} \cdot \tau \geq T_V$.

The long string of N_{TDC} delay elements τ can be broken down, for example, eight times, by running the DCO at 4× the frequency and dividing its differential output by four to create a CKV clock vector, $\text{CKV}^{0...7}$, as shown in Fig. 5(b). Each element of this vector is constructed from original edges of the DCO clock, but now it constitutes a single phase of CKV. Each of the eight phases is then fed to each of the eight short TDCs of length $N_{\text{TDC}}/8$. The eight TDCs are producing eight outputs TDCQ[0...7]. Only one of them is effective (i.e., non-saturated). The effective TDC output, which corresponds to the closest separation between FREF and CKV, is chosen by the mux via "Octal" select signal. This signal can

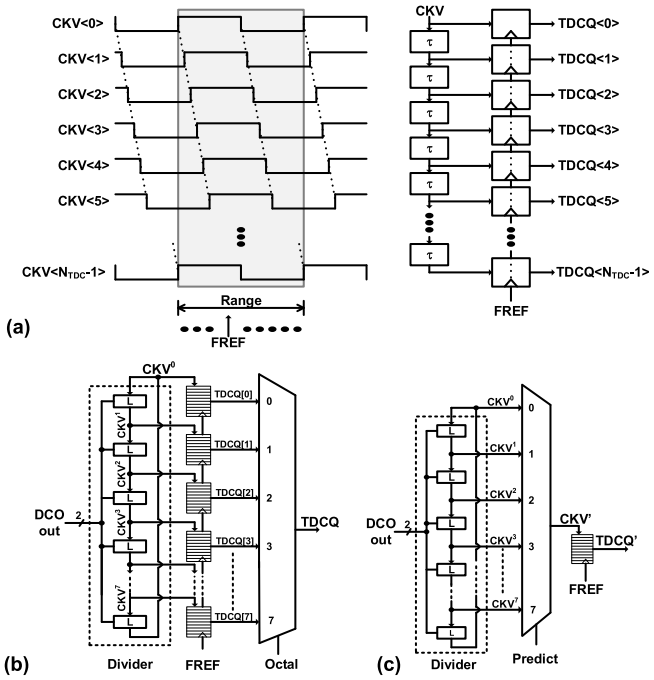

Fig. 5. Principle of turning a full-length flash TDC into a short-length TDC.

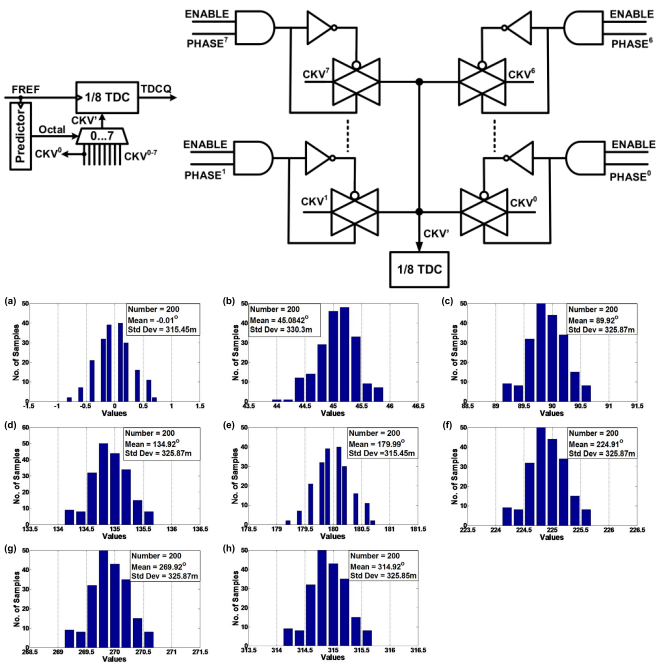

Fig. 6. Top: Block diagram of the TDC and Mux retiming circuitry. Bottom: Monte-Carlo simulation results of Mux unit cell for phases: (a) 0° (b) 45° (c) 90° (d) 135° (e) 180° (f) 225° (g) 270° (h) 315°. (Conditions: nominal case (TT), $V_{DD} = 1.05$ V, and T = 25°C).

be discerned by inspecting the TDC outputs for non-all-0 and non-all-1 patterns. The TDC output is now a composite of "Octal" value with the weight of 1/8 and the decoded TDCQ. It should be emphasized that only one of the eight short TDCs is active at a time. The circuitry is then simplified in Fig. 5(c), by merging the TDCs and moving to the mux output. However, the mux selection cannot be now deterministic but must be predicted. This can be readily done by extracting fractional bits of the accumulated frequency command word (FCW), i.e., the fractional part of the reference phase, $R_R[k]$.

In order to reduce fractional spurs, symmetry and compact layout of the TDC are critical in achieving good linearity and fine timing resolution. Fig. 6 shows details of the key TDC timing interface, which includes eight main AND gates, inverters, and Mux unit cell. The eight phase chains are symmetrical and the interconnections ensure adjacent phase error is minimized. Monte-Carlo device mismatch simulation results of the Mux unit cell are plotted in Fig. 6 for each of the eight cells (conditions: TT corner, $V_{DD} = 1.05$ V, and T = 27°C). The mean value of phase error is smaller than 0.1° with respect to the CKV period and each clock phase mismatch has a standard deviation of 0.325°. Based on such small variations, the expected linearity of the TDC should be excellent, thus yielding low level of fractional spurs.

The fractional spur level due to the TDC nonlinearity can be roughly analyzed as follows: Assume TDC has a worst-case sinusoidal INL curve of 0.15 LSB when the digital control word sweeps one cycle. Based on the 2-way TDC parallelism, the TDC unit delay is improved to 5–7 ps. The ADPLL's reference frequency is 40 MHz, $T_V = 500$ ps and FCW equals 50. Thus the fractional spur level can be written as

$$P_{\text{frac}}(\text{dBc}) = 20\log_{10}\left[\frac{\pi}{2}\cdot\frac{\text{INL}\cdot T_{\text{TDC}}}{T_V}\right] \quad (1)$$

Using the above analysis, a worst-case spur level of −51 dBc is expected at the closest fractional frequency (i.e., in-band), which is very close to our measured closest spur level of −55 dBc. Eq. (1) can be also used to estimate the spurs due to the multiplexer's non-linearity. However, its effects are much smaller than those of TDC.

C. PVT-Insensitive TDC

Fig. 7(a) shows the 1/8-length TDC within an ADPLL. The DCO and ÷4 divider produce eight CKV phases. A phase predictor ensures the TDC input is $<T_V/8$ by selecting a CKV phase that is closest to FREF. The TDC output, after decoding, is normalized to T_V and the octal estimation, normalized to $T_V/8$ is added to produce the phase error ϕ_E. The DCO tuning word is updated based on ϕ_E.

Fig. 7(b) also shows the proposed technique to stabilize the TDC step size, Δ_{TDC}. The PVT calibration is enabled after the ADPLL is locked and it can stay engaged in the background but at a much slower rate to compensate for any temperature drift. The LMS manner of calibration is robust even if the TDC resolution is far away from the target resolution (which is often the case during the first use). At this time, the "ripple" of the phase error PHE (ϕ_E) is large due to the error between the initial (typically, unknown) value and the desired target of the TDC resolution, Δ_{TDC} (i.e., 7ps). This will be later shown in Fig. 18 measurements. TTW will converge into the target resolution by forcing ϕ_E to zero using a signed-LMS algorithm [21]. This way, independent from PVT, the ADPLL will always settle to the same targeted TDC resolution. The flowchart shows the operation of signed-LMS algorithm. After the calibration though, in order to save power,

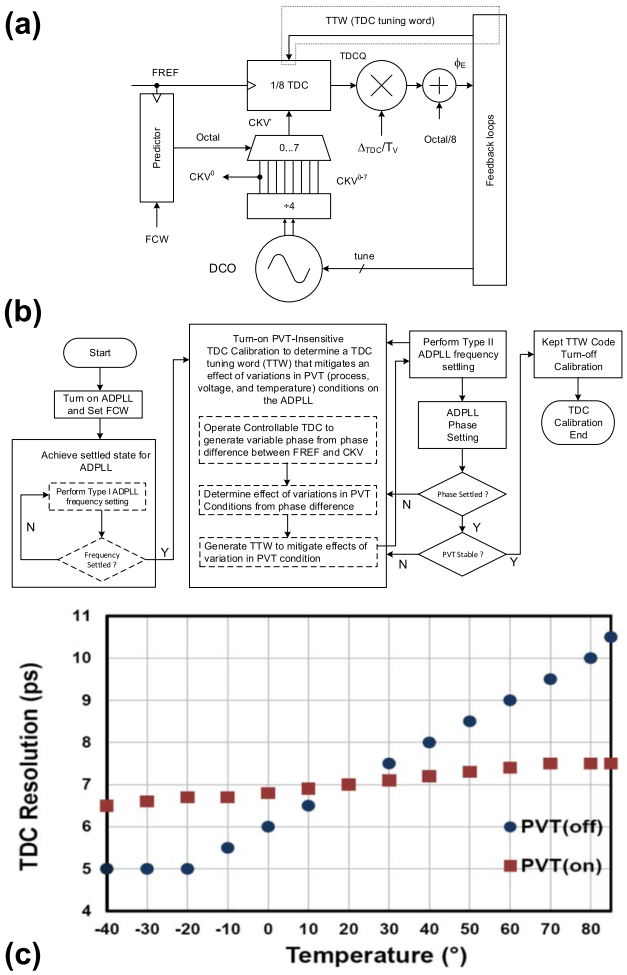

Fig. 7. (a) TDC within ADPLL and within the adaptation loop. (b) Flowchart to make its step size, Δ_{TDC}, PVT-free. (c) Post-layout simulated TDC resolution with PVT-function (on/off) at different temperatures.

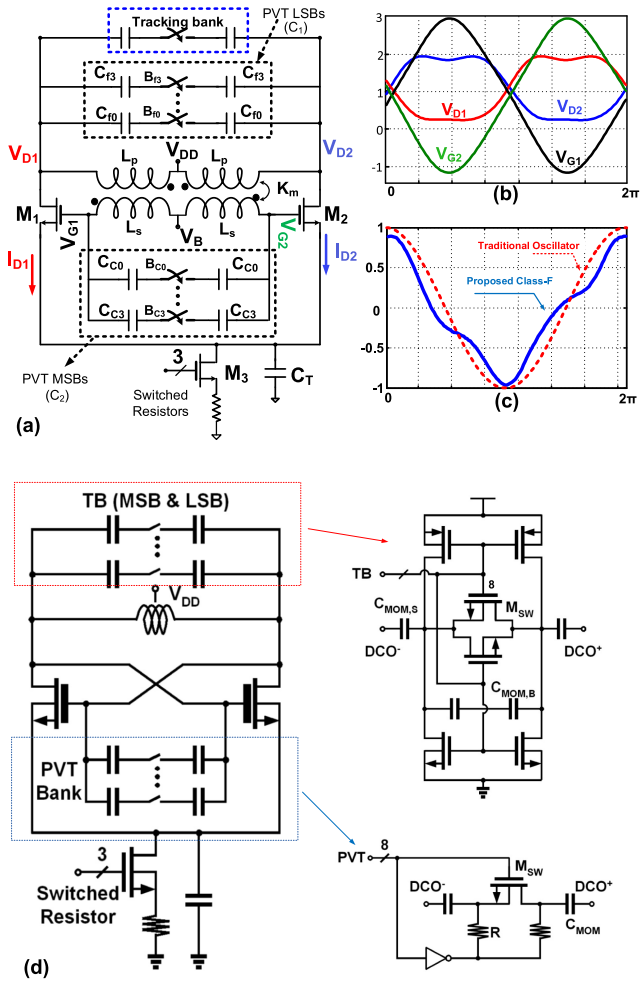

Fig. 8. (a) Schematic of class-F DCO with (b) voltage waveforms, and (c) ISF. (d) Schematic of the class-B DCO and the construction of coarse- and fine-resolution banks.

the calibration state machine could freeze the TTW code until voltage or temperature changes. However, the calibration time is very quick (~15 us) so it could also be run periodically.

Fig. 7(c) shows simulation results of the TDC resolution versus temperature with the PVT-calibration turned on/off. The TDC resolution variation, under the $\tau_0 - \tau_1$ control bits (adj [12:1]) set at SEL = 6, causes as much as 8 dB of the in-band phase noise change. When the PVT calibration is active, the in-band phase noise variation is reduced to less than 1 dB.

IV. Digitally Controlled Oscillator (DCO)

The ADPLL for cellular applications needs to satisfy the strict requirements of phase noise (PN) at low power consumption. Hence, the oscillator design is very critical since its PN dominates the ADPLL's far-out performance and it needs to be pure enough not to affect the close-in PN that is dominated by the TDC resolution. Additionally, to cover several TX/RX 4G/5G bands, the oscillator should have a wide tuning range (TR). At the same time, the finest frequency step should be on the order of 10 kHz.

The 28 nm CMOS technology has strict requirements on design for manufacturing (DFM), especially the 25–50% minimum metal density rule, which is much stricter than in the previous 40 nm node. Hence, inductors and transformers must include a lot of dummy metal pieces on *all* metal layers. Metal fills show negligible effect on the windings self-inductance and coupling factor k_m. However, eddy currents in the dummy fills increase the resistive loss and thus the transformer's Q-factor is degraded by 10–20%. Dummy fills also increase the capacitance, thus degrading the self-resonant frequency. Furthermore, the excess noise of transistor, γ, is also increased. Consequently, both phenomena hurt the RF oscillator performance.

Recently introduced class-F oscillator [16], as shown in Fig. 8(a), mitigate the above issues by: 1) enforcing a pseudo-square voltage across the primary winding of the tank ($V_{D1/2}$), thus reducing the impulse sensitivity function (ISF), and 2) exploiting the transformer's voltage gain, G_0. The phase noise is less sensitive to the loss of the tank due to its lower ISF, while the effective noise factor of the g_m-devices is reduced by G_0. Consequently, the new structure offers ~4 dB

improvement over the traditional oscillator at the same V_{DD} and tank's Q-factor. The pseudo-square waveform in Fig. 8(b) is realized by increasing the 3rd harmonic of the fundamental oscillation voltage through an additional impedance peak and strong 3rd harmonic of the drain current. Unfortunately, due to the metal-stack and metal density issues in 28-nm CMOS, its FoM is 3 dB worse than in the original prototype in 65-nm CMOS [16].

The improved g_m/C is exploited in the DCO to create an array of MOS-switchable metal-oxide-metal (MOM) capacitors of various step sizes. The digitally controlled varactors exploiting C-V characteristics of MOS devices, such as in [7], are entirely avoided here as they are more sensitive to supply pushing and temperature variations. There are 8-bit binary PVT switchable capacitors for coarse tuning, and 63-bit unary MSB (i.e., 8×) and 7-bit unary LSB (i.e., 1×) switchable capacitors for fine tuning. The segmented unit-weighted fine tuning switch-caps are well matched to provide a linear 9-bit resolution for modulation and drift tracking.

On/off ratio of the PVT varactors is 8:1. However, it is only 1.01:1 for the fine tuning to ensure linearity for a fine ~10 aF LSB step. The positive feedback is realized by a 1:2 step-up transformer with primary and secondary inductors L_p and L_s, respectively. The aluminum capping layer is strapped to the top copper layer to form the windings and improve the transformer's primary and secondary Q-factors. PVT banks are divided equally between L_p and L_s to guarantee the class-F operation over TR, while the tracking bank is located at L_p.

Measurements in Section V show a 640 MHz TR of 36%, which is due to the excellent controllable $C_{max}/C_{min} = 8$ of PVT switched-caps. This is made possible by the small resistance in on-state and small capacitance in off-state of the MOS transistors. In order to reduce parasitic effects of the biasing transistors, high-resistance R devices are used with a small inverter instead of conventional pull-down NMOS and pull-up PMOS transistors. The tracking bank consists of two "small" capacitors (CMOM,S of $C_S = 1.17$ fF) and two "big" capacitors (CMOM,B of $C_B = 57.3$ fF $\gg C_S$). The on-state capacitance is determined by two series-connected C_S and the off-state capacitance is determined by two C_S and two C_B connected in series. The difference between the on- and off-states provides a well-defined ultra-small capacitance step size ($\Delta C \approx C_S^2/2\,C_B = 10$ aF) and thus a fine frequency resolution ($\Delta f = 30$ kHz).

V. Experimental Results

The proposed ADPLL is implemented in TSMC 28-nm LP CMOS. Fig. 9(a) shows the chip micrograph and the power consumption breakdown. The ADPLL area is only 0.22 mm^2 and it represents over 35% reduction over the prior record of GSM compliant ADPLLs [7], [22] and 18% over the very recent [8]. The ADPLL consumes 11.5 mW from a 1.05 V voltage supply. Most of the current is drawn by the DCO (65%), then the digital core (15%) and divider (15%). To investigate the effects of class-F DCO, another version of the identical ADPLL but with the traditional class-B DCO was also fabricated, as shown in Fig. 9(b). Its effective area is a bit smaller but the power consumption and FOM are much worse. Therefore, the focus of this work is the version with class-F DCO, with the class-B DCO used only for comparisons.

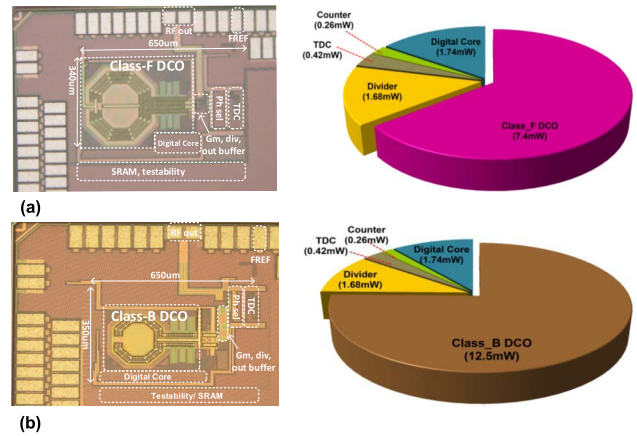

Fig. 9. Chip micrographs and power consumption breakdowns of the proposed ADPLL with: (a) class-F DCO, (b) class-B DCO.

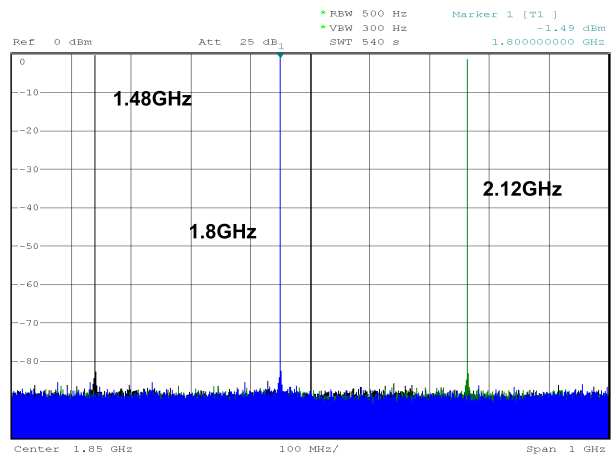

Fig. 10. Measured spectra of ADPLL output across the frequency operating range.

The ADPLL generates an RF spectrum that is largely free from spurious tones, as observed at the ÷4 DCO divider output port in Fig. 10 for the lowest (1.48 GHz), center (1.8 GHz) and highest (2.12 GHz) operating frequencies. The tuning range is 640 MHz or 35.6% fractional.

Fig. 11 shows the tuning range (TR) coverage of the class-F DCO. As monitored through the ÷4 divider, it has a TR from 5.7 GHz to 8.4 GHz (1.425 to 2.1 GHz after the divider), which is a bit wider than the locking range of ADPLL. The locking procedure of the ADPLL is sequential over the coarse and fine tuning banks. The former is binary weighted with 8 bits. The latter is switched in a thermometer way to guarantee proper locking and then the voltage and temperature tracking. This wide-TR DCO, where the resonant frequency versus tuning code is largely dependent of the MoM capacitor's characteristic, is typically highly nonlinear and requires compensation to achieve a constant loop gain in an ADPLL, i.e., constant K_{DCO}. The fine-tuning range at the coarse code of 170 is plotted in the inset. The coarse-tuning of the DCO

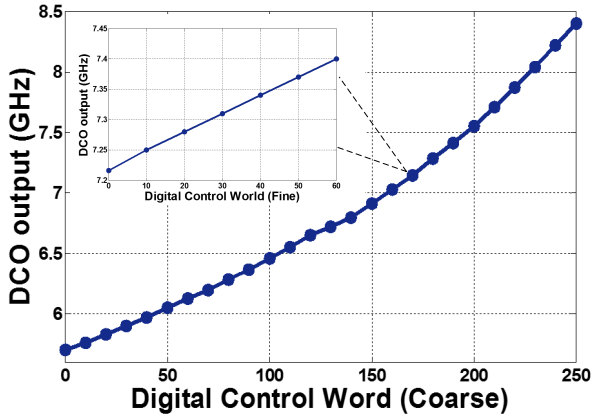

Fig. 11. Transformer-based class-F DCO frequency sweep over coarse, and fine tuning banks.

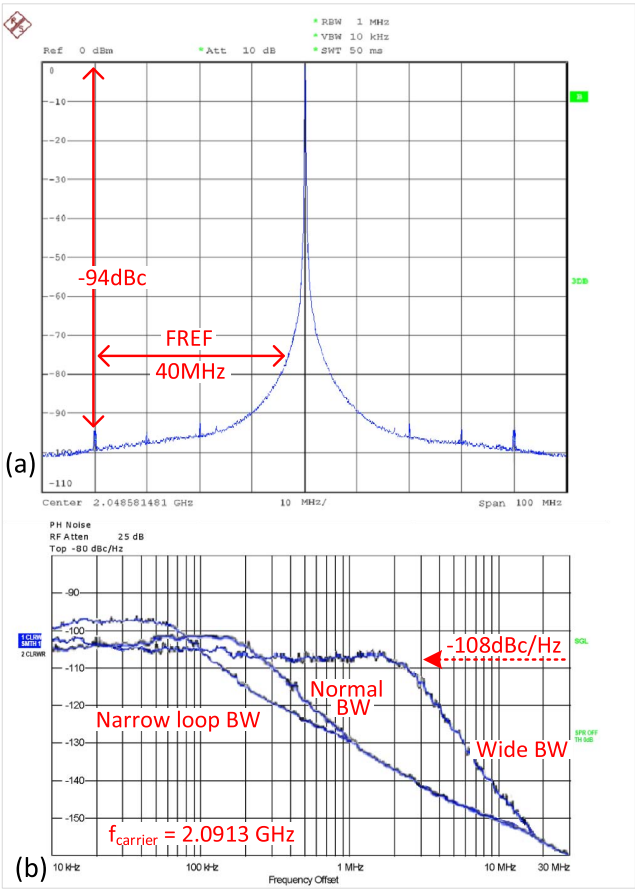

Fig. 12. Measured ADPLL spectrum (a); and phase noise (b); with 10 MHz FREF. The spectrum, taken with wide loop bandwidth of 1.5 MHz, is virtually spur-free.

realizes linear tuning at 120 MHz/bit with process variations. More than 5% overlap between the adjacent frequency tuning curves guarantees continuous tuning across the entire range. A progressive reduction in step-size from 1 MHz for the first bit in the coarse-tuning bank to 120 kHz for the last bit, is observed. For 4G/5G applications, to accommodate the PVT

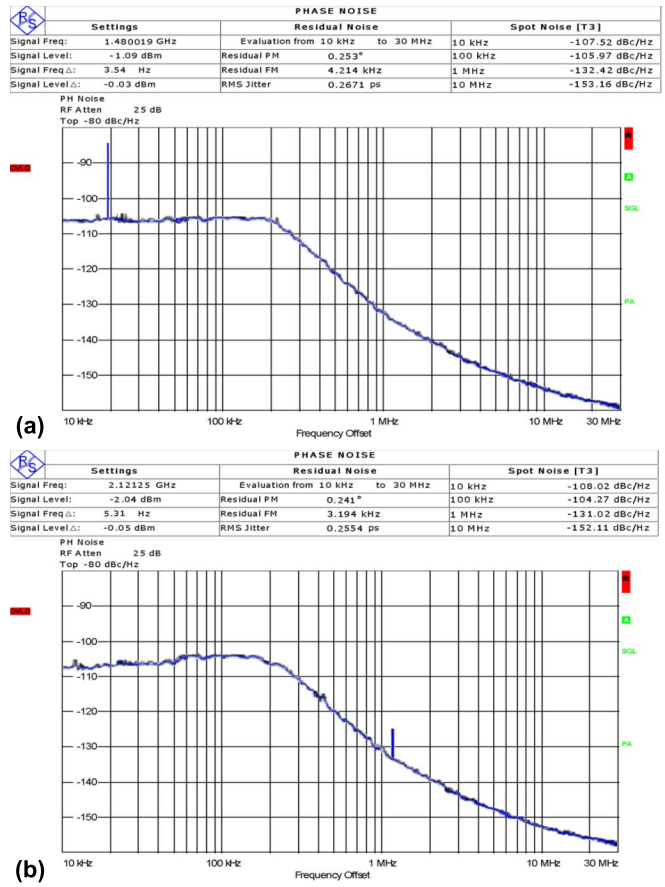

Fig. 13. Measured output spectra at fractional-N frequencies: (a) 1480.019 MHz (FCW $= 37 + 2^{-11}$), and (b) 2121.25 MHz (FCW $= 53+2^{-5}$).

variations, the overlap ratio should be increased to 50%. This can be achieved by adding more fine-tuning codes to the class-F DCO structure.

Fig. 12 shows the measured spectrum and PN at 2.0913 GHz ADPLL output with fractional FCW $= 52.2825$. An ultra-low FREF spur level of -94 dBc is measured with no other significant spurs observed. PN at 20 MHz offset from the $\sim$2 GHz carrier is -157 dBc/Hz. PN was measured for three different ADPLL loop bandwidths: narrow ($\sim$80 kHz), normal ($\sim$250 kHz) and wide ($\sim$2.5 MHz). The in-band PN of -108 dBc/Hz in wide bandwidth (to filter out the DCO noise) corresponds exactly (according to [7, eq. (2)]) to the TDC quantization noise at 6 ps resolution at 40 MHz FREF, while showing no other noise sources. The measured integrated jitter of 290 fs corresponds to the total integrated PN of 0.2°.

Fig. 13 plots the measured PN at two combinations of ADPLL frequencies with an undivided FREF of 40 MHz: (a) the low-side DCO frequency with the lowest setting of the fractional offset (FCW $= 37 + 2^{-11}$), and (b) the high-side frequency with sufficiently high fractional-N setting (FCW $= 53 + 2^{-5}$). In the former case, the fractional spur of $40\,\text{MHz}\times 2^{-11} = 19.5$ kHz falls within the ADPLL band and so it cannot be filtered out by the loop. In the latter case, the $40\,\text{MHz}\times 2^{-5} = 1.25$ MHz spurious tone frequency puts it

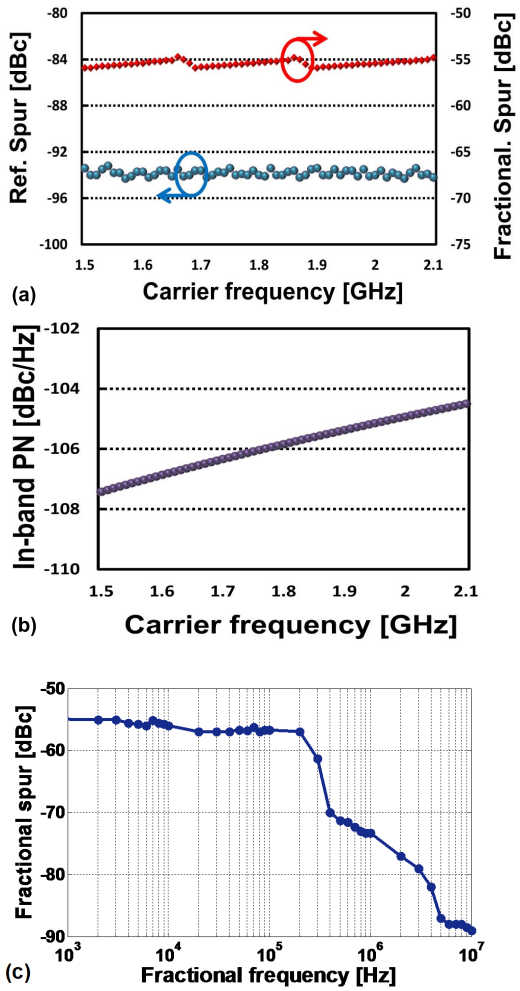

Fig. 14. (a) Measured reference and fractional spurs over 1.5–2.1 GHz in 10 MHz steps. (b) Measured in-band phase noise. (c) Measured largest fractional spurs for fractional frequencies away from 2040 MHz integer-N channel.

well outside of the 250 kHz loop bandwidth. An in-band PN level is about −107.5 dBc/Hz (at 10–30 kHz), which is mainly dominated by the thermal noise of the TDC delay stage. The integrated PN in both cases is ∼0.25°.

The ADPLL carrier frequency was swept throughout the TR to confirm the stability and well-behaving of the reference and worst-case fractional spurious tone levels [Fig.14(a)] as well as the in-band PN [Fig.14(b)]. As shown in Fig. 14(b), the in-band PN increases ∼3 dB over the full frequency range of 1.5–2.1 GHz, which agrees with the $20\log_{10}(2.1/1.5)$ formula. The reference spur is better than −91 dBc, and the fractional spurs are below −55 dBc, as shown in Fig. 14(a)(c). The ultra-low spur levels validate the short TDC approach that limits its INL non-linearity.

Fig. 14(c) shows the measured worst-case fractional spur levels when the ADPLL is operating at small offsets from the worst-case integer-N channel of 51 × 40 MHz = 2040 MHz. For this measurement, the fractional spur power levels were systematically measured at 40 different values of the fractional FCW word corresponding to 1 kHz to 10 MHz offsets from

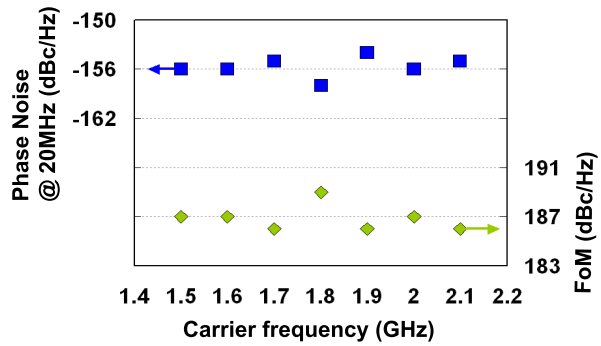

Fig. 15. Phase noise and figure-of-merit (FoM) at 20 MHz offset versus carrier frequency.

2040 MHz. The spectrum analyzer's span, sweep time and resolution bandwidth were automatically adjusted for each value to ensure the noise floor was low enough to observe the spurs. Although a higher-order loop filter can provide extra filtering of out-of-loop-band fractional spurs, this filtering is limited to a few MHz because the cut-off frequency of the higher-order filter is typically placed at approximately 10× beyond the loop bandwidth (i.e., $f_{\mathrm{LOOP}} = 250$ kHz in this work for optimum PN) for stability reasons. While the measured worst-case in-band fractional spur performance of −55 dBc is comparable to that reported in the published $\Delta\Sigma$-PLLs and TDC-PLLs, this architecture achieves such as a remarkable performance with utmost simplicity, resulting in the best FOM and lowest area.

Fig. 15 shows the average PN performance of five die samples at 20 MHz offset across the TR, together with the corresponding FoM. The PN beyond the 20 MHz offset is dominated by the thermal noise floor from the divider and buffers, which was determined to be −158 dBc/Hz. The average PN is only −156 dBc/Hz and varies less than 2 dB across the TR. The average FoM is as high as 187 dBc/Hz, also with little variation.

The proposed 2-way parallelism of TDC succeeds in shortening, at the ADPLL architectural level, the input dynamic range of TDC to 100 ps while keeping the PVT-stabilized time resolution at 7 ps, all at a single-shot conversion rate of 40 MSamples/s. Fig. 16 shows the measured transfer function and non-linearity of the TDC. The differential non-linearity (DNL) and integral non-linearity (INL) are well below 0.2 LSB and 0.3 LSB, respectively, over the entire span.

Fig. 17 proves the effectiveness of the proposed stabilization technique of the TDC resolution, Δ_{TDC}. Since the supply voltage V_{DD} has a huge effect on Δ_{TDC}, the measured in-band phase noise (PN) shows the normally expected 8 dB of variability. Turning on the stabilizing algorithm brings the PN variability to less than 1 dB.

The timing waveforms in Fig. 18 were captured by dumping the digital signals into the on-chip SRAM memory. Until the LMS algorithm starts at time = 27 us, the phase error (PHE) exhibits the expected large ripple (i.e., $R_R[k]$ does not agree with $(R_V[k] + \epsilon[k])$ in Fig. 2). The ripple then keeps on diminishing while the TDC tuning word (TTW) settles to its

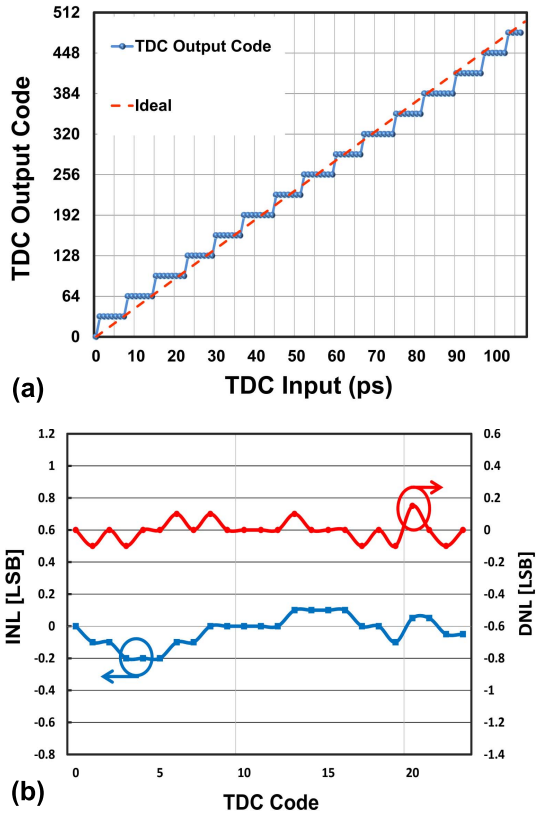

Fig. 16. Measured (a) TDC transfer curve, (b) TDC linearity (INL and DNL). The LSB is forced at 7 ps.

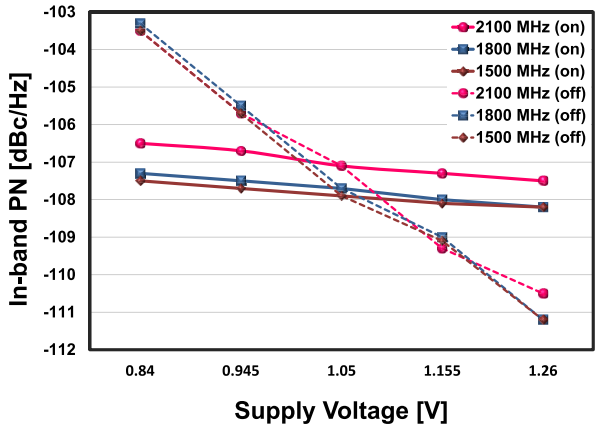

Fig. 17. Measured in-band phase noise over supply voltage at 1.5, 1.8, and 2.1 GHz with the PVT free TDC turned on/off.

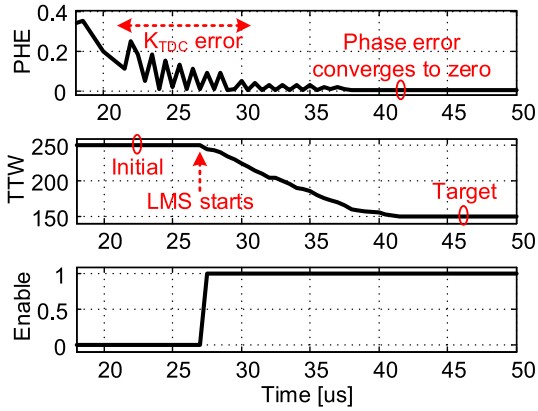

Fig. 18. Captured real-time internal signals during TDC calibration: phase error (PHE), TDC tuning word (TTW) and TDC calibration enable.

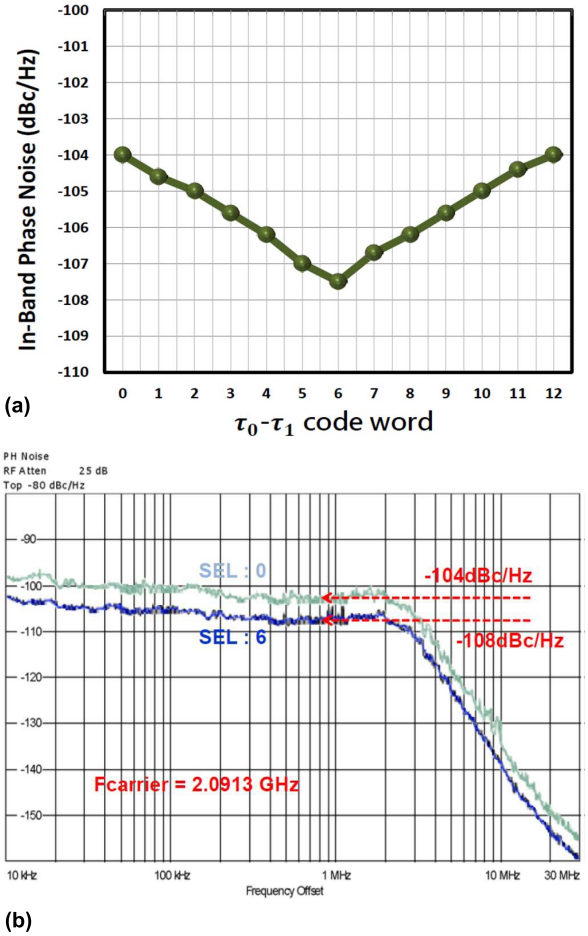

Fig. 19. In-band PN reduction characteristics: (a) with varying $\tau_0 - \tau_1$ code (b) measured phase noise plot improvement with the proposed schemes.

final value corresponding to the targeted Δ_{TDC} ($=t_{\mathrm{inv}}$). At time ~41 us, the algorithm fully settles and the phase error is almost flat at zero.

The reduction of in-band PN as a function of τ_0-τ_1 (defined in Fig. 3) is verified in Fig. 19(a) measurements. Theoretically, the PN will improve 6 dB when τ_0-τ_1 changes from 0 (full redundancy) to $t_{\mathrm{inv}}/2$ (one extra bit of conversion). The implemented digital adjustment of τ_0-$\tau_1 = t_{\mathrm{inv}}/2$ spans 12 levels and centers at 6, covering the most critical portion of the $t_{\mathrm{inv}}/2$ range. As expected, when the SEL(τ_0-τ_1) codeword is 6, we observe a 3.5 dB reduction in PN, which reaches as low as −107.5 dBc/Hz. The mismatch in τ_0-$\tau_1 = t_{\mathrm{inv}}/2$ is readily estimated in digital domain in a stochastic manner by averaging the long-term difference in the Q/Q' outputs from the two TDC flip-flop arrays (see Fig. 3). Fig. 19(b) plots the measured PN with the worst (SEL = 0) and best (SEL = 6) settings of the codeword.

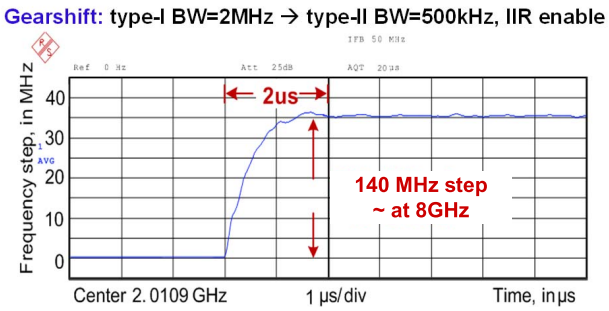

Fig. 20. Lock time of the 8-GHz ADPLL measured at divide-by-4 output for a frequency step of 140 MHz.

The 'forced' time resolution of the TDC (Δ_{TDC}) is 7 ps, which corresponds to a theoretical in-band PN contribution of −107.5 dBc/Hz for a 2.1 GHz carrier, as calculated per [6]

$$L = \frac{(2\pi)^2}{12}\left(\frac{\Delta_{\mathrm{TDC}}}{T_v}\right)^2 \frac{1}{f_R} = \frac{(2\pi)^2}{12}\left(\frac{7\mathrm{ps}}{1/2.1\mathrm{GHz}}\right)^2 \frac{1}{40\mathrm{MHz}} \tag{2}$$

This is verified in measurements in Fig. 12(b), which reports the in-band PN of −107..108 dBc/Hz at the very wide loop bandwidth of ∼2.5 MHz in which the DCO PN contributions vanish.

Aside from the above spectral purity, the lock-in time is another key metric for the synthesizer. To simultaneously achieve fast locking and excellent PN after settling, the loop bandwidth is dynamically controlled via a gearshift technique. The loop operates in type-I with a wide bandwidth of 2 MHz during the frequency acquisition. It is then gear-shifted to type-II, fourth-order IIR filter with a 500-kHz bandwidth only when it enters the tracking mode. The measured lock-in time is 2 μs for a frequency step of 140 MHz, as demonstrated in Fig. 20.

Two-point frequency modulation (FM) at the FREF rate employing only the DCO fine-tuning bank is demonstrated by FSK modulating the 1.84-GHz carrier at a rate of 50 kHz with a maximum frequency deviation of 1 MHz. The DCO gain for FBMod $K_{\mathrm{DCO}}^{\mathrm{FB}}$ and the TDC gain K_{TDC} are calibrated automatically via digital averaging techniques. The calibrated K_{DCO}^{FB} is then applied to the gain normalization multiplier in the direct modulation path (see Fig. 2). The demodulated signal is measured using a Rohde & Schwarz FSUP signal source analyzer with FM demodulation firmware, and the waveform measured at the RF output is shown in Fig. 21. The sharp transition edges in the step-response (which require many harmonics) confirm the wideband FM capability, and demonstrate the effectiveness of the built-in K_{DCO} calibration. The f_R/K_{DCO} multiplier is then perturbed intentionally from the self-calibrated optimum to demonstrate the effect of an incorrect K_{DCO} estimation. Fig. 21 thus demonstrates the ADPLL two-point FM capability when applying FCW samples corresponding to alternating (every 10 μs) sequences of zero and 1 MHz.

Fig. 22 provides a panorama of state-of-the-art PLLs based on LC-tank oscillators, both high-Q (tend to occupy larger area) and low-Q (tend to occupy smaller area), and with wide and narrow TR, including solutions with multiple oscillators. The chart covers most of the solutions for various wireless applications, not necessarily cellular. As expected, our proposed ADPLL provides an excellent FoM at the record-low area.

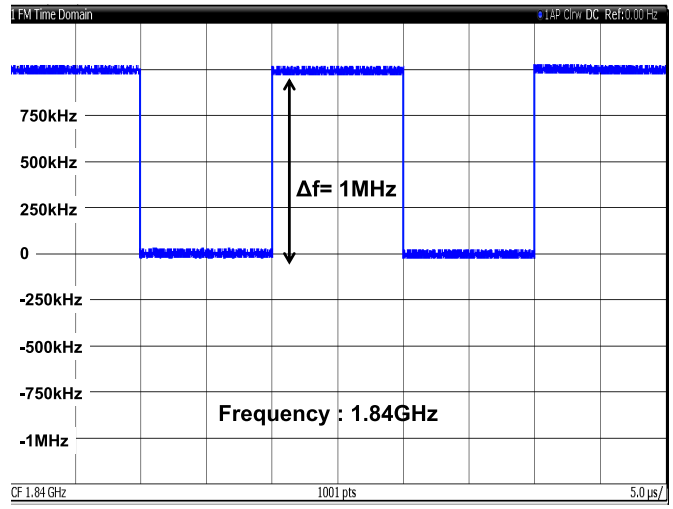

Fig. 21. Measured demodulated signal at CKV during FSK using auto-calibrated and optimal K_{DCO}.

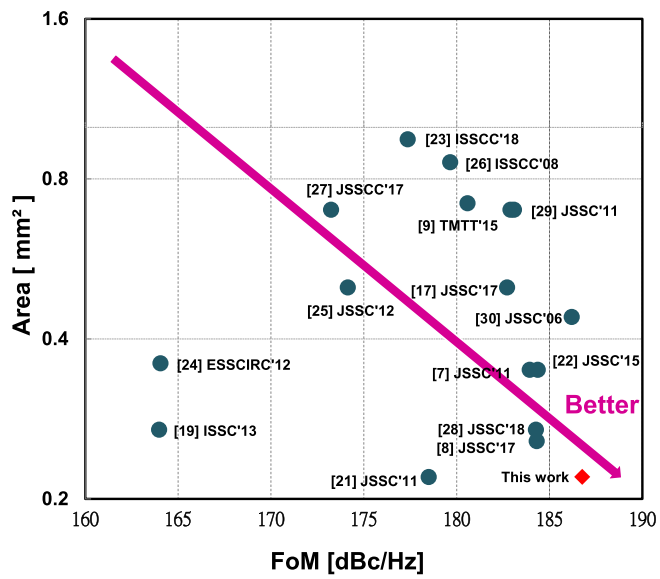

Fig. 22. FoM over area for recent state-of-the-art fractional-N LC-tank PLLs.

Table I summarizes the proposed ADPLL and compares it against state-of-the-art ADPLL designs in cellular radios. While keeping the high quality of RF performance (especially the far-out PN at 20 MHz offset), the area and power consumption are significantly improved. The power consumption of this ADPLL is 11.5 mW and represents over 70% reduction versus the prior record. The FOM that captures the output *spot* PN in the upconverted thermal region ($1/f^2$) normalized to the power consumption of DCO and PLL (here they are only within $10\log_{10}(11.5/7.4) = 1.9$ dB to each other) is

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH PUBLISHED ADPLLS (AND HYBRID PLLS) FOR CELLULAR PHONES

	This work1 Class-F	This work2 Class-B	JSSC'11 [7]	JSSC'17 [8]	TMTT'15 [9]	JSSC'17 [17]	JSSC'15 [22]	JSSC'18 [28]	Units
CMOS node	28nm	28nm	65nm	14nm	65nm	40nm	65nm	65nm	
Supply	1.05	1.05	1.2	N/A	1.2	1.1	1	0.9	V
Number of Oscillators	1	1	1	1	2	1	1	1	
RF output freq.	1425-2125	1475-2125	800-2000	2690	500-3000	1725-3400	2800-3500	6750-8250	MHz
Tuning range	39.4	36.1	22.2	N/A	44	64	22.2	20	%
PLL FOM	186.8	181.9	183.4	184.3	181.1	182.7	184	184	dB
PLL FOM_T	198.6	193	190.2	N/A	194	193	190.8	190.3	dB
Settling time	2	2	20	400	N/A	70	N/A	N/A	us
Reference Spur	-91	-91	-70	-87.6	N/A	N/A	-81	-52	dBc
In-band Fractional Spur	-55	-55	N/A	-78.6	N/A	-42	-60	-42.4	dBc
Norm. PN to 915MHz@20MHz offset	-164	-162	-167	-162.3	-162.5	-159.8	-162.3	N/A	dBc/Hz
(AD)PLL power	11.5	16.8	45.6	13.4	26.4	10.7	15.6	3.3	mW
DCO power	7.4	12.5	21.6	6.1	22.5	8.0	8.3	2.2	mW
PLL w/FM area	0.22	0.22	0.35	0.257	0.72	0.5	0.35	0.27	mm^2

prominent. Further normalizing the FOM to the TR of 36% results in FOM_T that is 4.5 dB better than the prior record. The ADPLL loop settles within only 2 us, made possible by the dynamic hitless gear-shifting of the loop filter coefficients.

VI. CONCLUSION

We have demonstrated an all-digital PLL (ADPLL) for wireless cellular transceivers realized in 28-nm CMOS that brings significant improvements in area and power consumption. The new ADPLL architecture is based on predicting the inputs to the time-to-digital converter (TDC) thus substantially narrowing its range to 1/8 of the 2 GHz output clock period. The TDC resolution is improved by a factor of 2 through parallelism and stabilized to make it largely independent from PVT conditions. The wide-range class-F DCO core helps with multi-band operation. The output spectrum is virtually spur free with the in-band phase noise dominated by the small TDC quantization noise.

REFERENCES

[1] B. Furht and S. A. Ahson, *Long Term Evolution: 3GPP LTE Radio and Cellular Technology*. Boca Raton, FL, USA: CRC Press, 2009, pp. 441–443, ch. 12.

[2] *Base Station (BS) Radio Transmission and Reception (FDD)*, document TS 25.104, 3GPP, 2010.

[3] *Base Station (BS) Radio Transmission and Reception (TDD)*, document TS 25.105, 3GPP, 2008.

[4] (Feb. 2015). *5G Vision*. [Online]. Available: www.5g-ppp.eu

[5] *FCC Website[EB/OL]*. Accessed: Aug. 1, 2018. [Online]. Available: http://wireless.fcc.gov

[6] R. B. Staszewski *et al.*, "All-digital PLL and transmitter for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2469–2482, Dec. 2005.

[7] R. B. Staszewski, K. Waheed, F. Dulger, and O. E. Eliezer, "Spur-free multirate all-digital PLL for mobile phones in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2904–2919, Dec. 2011.

[8] C.-W. Yao *et al.*, "A 14-nm 0.14-ps_{rms} fractional-N digital PLL with a 0.2-ps resolution ADC-assisted coarse/fine-conversion chopping TDC and TDC nonlinearity calibration," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3446–3457, Dec. 2017.

[9] Y.-C. Choi, Y.-J. Seong, Y.-J. Yoo, S.-K. Lee, M. V. Lopez, and H.-J. Yoo, "Multi-standard hybrid PLL with low phase-noise characteristics for GSM/EDGE and LTE applications," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 10, pp. 3254–3264, Oct. 2015.

[10] H. Wang, A. A. Zaidi, X. Chen, J. Luo, and M. Dieudonne, "Evaluation of 5G waveform candidates considering hardware impairments and above 6 GHz operation," in *Proc. Veh. Technol. Conf.*, Jun. 2017, pp. 1–5.

[11] R. Staszewski *et al.*, "Software assisted digital RF processor (DRP) for single-chip GSM radio in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 276–288, Feb. 2010.

[12] R. B. Staszewski, "State-of-the-art and future directions of high-performance all-digital frequency synthesis in nanometer CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 7, pp. 1497–1510, Jul. 2011.

[13] J. Strange *et al.*, "A HSPA+/WCDMA/EDGE 40nm Modem SoC with embedded RF transceiver supporting RX diversity," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2014, pp. 133–136.

[14] W. Wu, R. B. Staszewski, and J. R. Long, "A 56.4-to-63.4 GHz multi-rate all-digital fractional-N PLL for FMCW radar applications in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1081–1096, May. 2014.

[15] E. Temporiti, C. Weltin-Wu, D. Baldi, M. Cusmai, and F. Svelto, "A 3.5 GHz wideband ADPLL with fractional spur suppression through TDC dithering and feedforward compensation," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2723–2736, Dec. 2010.

[16] M. Babaie and R. B. Staszewski, "A class-F CMOS oscillator," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3120–3133, Dec. 2013.

[17] Y. Wu, M. Shahmohammadi, Y. Chen, P. Lu, and R. B. Staszewski, "A 3.5–6.8-GHz wide-bandwidth DTC-assisted fractional-N all-digital PLL with a MASH $\Delta\Sigma$-TDC for low in-band phase noise," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1885–1903, Jul. 2017.

[18] J. Borremans, K. Vengattaramane, V. Giannini, B. Debaillie, W. Van Thillo, and J. Craninckx, "A 86 MHz–12 GHz digital-intensive PLL for software-defined radios, using a 6 fJ/Step TDC in 40 nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 2116–2129, Oct. 2010.

[19] J.-W. Lai *et al.*, "A 0.27 mm^2 13.5dBm 2.4 GHz all-digital polar transmitter using 34%-efficiency class-D DPA in 40nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 342–343.

[20] F. W. Kuo *et al.*, "A 12 mW all-digital PLL based on class-F DCO for 4G phones in 28nm CMOS," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014, pp. 1–2.

[21] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 2.9–4.0-GHz fractional-N digital PLL with bang-bang phase detector and 560-fs_{rms} integrated jitter at 4.5-mW power," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2745–2758, Dec. 2011.

[22] C. Weltin-Wu, G. Zhao, and I. Galton, "A 3.5 GHz digital fractional-PLL frequency synthesizer based on ring oscillator frequency-to-digital conversion," *IEEE J. Solid-State Circuits*, vol. 50, no. 128, pp. 2988–3002, Dec. 2015.

[23] H. Yoon *et al.*, "A—31dBc integrated-phase-noise 29 GHz fractional-N frequency synthesizer supporting multiple frequency bands for backward-compatible 5G using a frequency doubler and injection-locked frequency multipliers," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 366–368.

[24] H.-S. Kim *et al.*, "A digital fractional-N PLL with a 3 mW 0.004mm^2 6-bit PVT and mismatch insensitive TDC," in *Proc. ESSCIRC*, Sept. 2012, pp. 193–196.

[25] G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 20 Mb/s phase modulator based on a 3.6 GHz digital PLL With −36 dB EVM at 5 mW Power," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2974–2988, Dec. 2012.

[26] H. H. Chang, P.-Y. Wangm, J.-H. C. Zhan, B.-Y. Hsieh, "A fractional spur-free ADPLL with loop-gain calibration and phase-noise cancellation for GSM/GPRS/EDGE," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 200–201.

[27] S. Ikeda *et al.*, "A—244-dB FOM high-frequency piezoelectric resonator-based cascaded fractional-N PLL with sub-ppb-order channel-adjusting technique," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1123–1133, Apr. 2017.

[28] A. Elkholy, A. Elmallah, M. G. Ahmed, and P. K. Hanumolu, "A 6.75–8.25-GHz −250-dB FoM rapid ON/OFF fractional-N injection-locked clock multiplier," *IEEE J. Solid-State Circuits*, vol. 47, no. 03, pp. 1–12, Mar. 2018.

[29] M. Youssef, A. Zolfaghari, B. Mohammadi, H. Darabi, and A. A. Abidi, "A low-power GSM/EDGE/WCDMA polar transmitter in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 3061–3074, Dec. 2011.

[30] C.-M. Hung, R. B. Staszewski, N. Barton, M.-C. Lee, and D. Leipold, "A digitally controlled oscillator system for SAW-less transmitters in cellular handsets," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1160–1170, May 2006.

[31] K. Waheed, R. B. Staszewski, F. Dulger, M. S. Ullah, and S. D. Vamvakos, "Spurious free time-to-digital conversion in an ADPLL using short dithering sequences," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 9, pp. 2051–2060, Sep. 2011.

[32] T. Tokairin, M. Okada, M. Kitsunezuka, T. Maeda, and M. Fukaishi, "A 2.1-to-2.8-GHz low-phase-noise all-digital frequency synthesizer with a time-windowed time-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2582–2590, Dec. 2010.

[33] J. Chen, L. Rong, F. Jonsson, G. Yang, and L.-R. Zheng, "The design of all-digital polar transmitter based on ADPLL and phase synchronized modulator," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1154–1164, May 2012.

[34] D. Liao, H. Wang, F. F. Dai, Y. Xu, R. Berenguer, and S. M. Hermoso, "An 802.11a/b/g/n digital fractional-*N* PLL with automatic TDC linearity calibration for spur cancellation," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1210–1220, May 2017.

[35] Y.-C. Yang, S.-A. Yu, Y.-H. Liu, T. Wang, and S.-S. Lu, "A quantization noise suppression technique for *delta sigma* fractional-*N* frequency synthesizers," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2500–2511, Nov. 2006.

[36] B. D. Muer and M. S. J. Steyaert, "A CMOS monolithic $\Delta\Sigma$-controlled fractional-N frequency synthesizer for DCS-1800," *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp. 835–844, Jul. 2002.

[37] A. Liscidini, L. Fanori, P. Andreani, and R. Castello, "A 36mW/9mW power-scalable DCO in 55nm CMOS for GSM/WCDMA frequency synthesizers," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2012, pp. 348–350.

[38] L. Fanori, A. Liscidini, and P. Andreani, "A 6.7-to-9.2GHz 55nm CMOS hybrid class-B/class-C cellular TX VCO," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2012, pp. 354–355.

[39] L. Kong and B. Razavi, "A 2.4-GHz RF fractional-*N* synthesizer with BW=0.25f_{REF}," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1707–1718, Jun. 2018.

[40] S. Levantino, G. Marzin, and C. Samori, "An adaptive pre-distortion technique to mitigate the DTC nonlinearity in digital PLLs," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1762–1772, Aug. 2014.

[41] T. Georgantas *et al.*, "A 13mm^2 40nm multiband GSM/EDGE/HSPA+/TDSCDMA/LTE transceiver," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 1–3.

[42] H. Darabi, H. Jensen, and A. Zolfaghari, "Analysis and design of small-signal polar transmitters for cellular applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1237–1249, Jun. 2011.

[43] O. E. Eliezer, R. B. Staszewski, I. Bashir, S. Bhatara, and P. T. Balsara, "A phase domain approach for mitigation of self-interference in wireless transceivers," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1436–1453, May 2009.

[44] S. Lee, J. Lee, H. Park, K.-Y. Lee, and S. Nam, "Self-calibrated two-point delta–sigma modulation technique for RF transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 7, pp. 1748–1757, Jul. 2010.

[45] M. Zanuso, S. Levantino, C. Samori, and A. Lacaita, "A 3 MHz-BW 3.6 GHz digital fractional-N PLL with sub-gate-delay TDC, phase-interpolation divider, and digital mismatch cancellation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2010, pp. 476–477.

[46] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.

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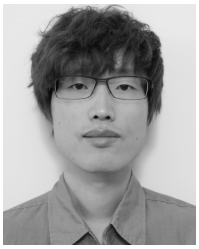

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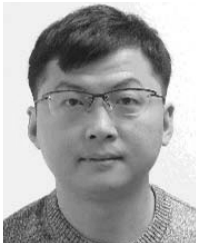

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