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A Supply Pushing Reduction Technique for *LC* Oscillators Based on Ripple Replication and Cancellation

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***Abstract*— In this paper, we propose a method to suppress supply pushing of an *LC* oscillator such that it may directly operate from a switched-mode dc–dc converter generating fairly large ripples. A ripple replication block (RRB) generates an amplified ripple replica at the gate terminal of the tail current source to stabilize the oscillator's tail current and thus its oscillating amplitude. The parasitic capacitance of the active devices and correspondingly the oscillation frequency are stabilized in turn. A calibration loop is also integrated on-chip to automatically set the optimum replication gain that minimizes the variation of the oscillation amplitude. A 4.9–5.6-GHz oscillator is realized in 40-nm CMOS and occupies 0.23 mm^2 while consuming 0.8–1.3 mW across the tuning range (TR). The supply pushing is improved to <1 MHz/V resulting in a low < −49-dBc spur due to 0.5–12-MHz sinusoidal supply ripples as large as 50 mV$_{pp}$. We experimentally verify the effectiveness of the proposed technique also in face of saw-tooth, multi-tone, and modulated supply ripples.**

***Index Terms*— Common-mode resonance, current-biased oscillator, dc–dc converter, digitally controlled oscillator (DCO), foreground calibration, *LC* oscillator, power supply rejection (PSR), ripple replication and cancellation, supply pushing, voltage-controlled oscillator (VCO).**

I. Introduction

PORTABLE internet-of-things (IoT) devices powered by batteries or energy harvesters generally need buck and/or boost switching dc–dc converters to transform the output levels of energy sources to the nominal supply voltage of IoT electronic circuitry [1]. Due to the switching operation of dc–dc converters, the resulting output ripples can severely degrade the performance of the supply sensitive circuitry, such as *LC*-tank oscillators, when connected directly.[1] To avoid this, a low dropout (LDO) linear regulator is typically inserted after the switching converter to stabilize the supply voltage [2], [3]. However, the extra voltage overhead (∼200 mV) will worsen the system's power efficiency (∼80% under 1-V supply). This will make it even more critical with the supply scaling down with technology.

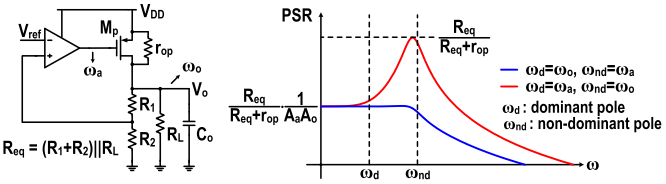

Fig. 1. Block diagram and PSR response of typical LDO topologies.

There are two main types of LDO topologies, as determined by whether the dominant pole (ω_d) is at the LDO output (ω_o) or the output of the error amplifier (ω_a) (see Fig. 1) [4], [5]. For the ω_o-dominant topology, the large C_o needed for loop stability can lead to integration difficulties, though a flat power supply rejection (PSR) response (blue curve in Fig. 1) is obtained. The ω_a-dominant topology avoids the use of large C_o, but the PSR starts to degrade after ω_a and shows a peak at a higher frequency (red curve in Fig. 1). This appears to be in conflict with the current trend of full system integration, which favors switched-capacitor (SC)-based dc–dc converters clocked at much higher frequencies than with the traditional inductor-based converters. The higher switching frequencies now benefit the dc–dc converters but require large LDO currents and/or complex circuit techniques [6], [7].

From the opposite perspective, techniques have also been proposed in the literature to reduce supply pushing of the oscillator [8]–[16]. In [8], the oscillator is deliberately biased at the point of the lowest sensitivity. The sharp slope of frequency versus current curve around this optimum point makes this approach only practical for tiny ripples (i.e., 1 mV

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[1]For example, supply pushing K_{push} = 10 MHz/V would generate −18-dB spur under 50 mV$_{pp}$ 1-MHz ripple.

in [8]). In [9] and [10], two constant-g_m bias circuits with different current sensitivities to supply are employed in a ring oscillator (RO) to generate a more stabilized current under supply variations. Furthermore, in [10], a calibration loop was added to obtain a more accurate current sensitivity ratio between the two constant-g_m stages. However, the spur-level improvement is limited to $\sim$ 10 dBc for low ripple frequencies ($f_{\text{ripple}} < 1$ MHz) and gets even worse when f_{ripple} increases [10]. Moreover, even when applied to an *LC* oscillator, the mismatches in the current mirroring ratios limit the spur level to no better than -35 dBc under a 50-mV$_{\text{pp}}$ ripple. There are also some frequency compensation techniques based on a phase-locked loop (PLL). In [13], the supply induced frequency variation is compensated by adding a replica generation block to the reference path. However, the additional block is bulky and power hungry, while the PLL bandwidth may also restrict the maximum ripple frequency that can be handled. A noise suppression loop was implemented in [14]. It detects the ripple-induced frequency variation by comparing the inverter delay in an RO with a voltage-controlled delay cell and corrects it through a feedback control. However, for *LC* oscillators that do not provide multiple phases, the delay cell should cover the full oscillation period, thus increasing its power and area consumption.

In this paper, we propose a feed-forward supply ripple replication and cancellation technique wholly contained within an *LC* oscillator in order to make it *practically* insensitive to supply ripples of switching dc–dc converters. The proposed technique manipulates the gate voltage of the customarily used tail current transistor and does not require any extra voltage headroom. The paper is organized as follows. Section II discusses the operating principles of the proposed technique, while detailed circuit design is given in Section III. Measurement results are disclosed in Section IV.

II. Feed-Forward Ripple Replication and Cancellation

As mentioned earlier, the supply pushing of *LC*-tank oscillators, even those at state of the art, needs to be substantially reduced to allow them to operate *directly* from dc–dc converters, which naturally contain a high level of ripples. In this section, the operating principle of the proposed supply pushing reduction technique based on the ripple replication and cancellation will be elaborated.

A. Mechanism of Supply Pushing

The variation of oscillating frequency f_{osc} with the supply voltage, V_{DD}, is mainly caused by the variation of parasitic capacitances seen by the resonant tank [17]. The cross-coupled transistors provide a negative transconductance to sustain the oscillation and will experience cutoff, saturation, and triode operating regions during each oscillation cycle. When V_{DD} varies, the tail current, I_0, and the corresponding oscillation amplitude, V_{osc}, will also vary. Thus, it will change the time interval during which the transistors stay in each operating region. Since the gate capacitance of MOS transistors shows the nonlinear dependence on the voltages at their terminals

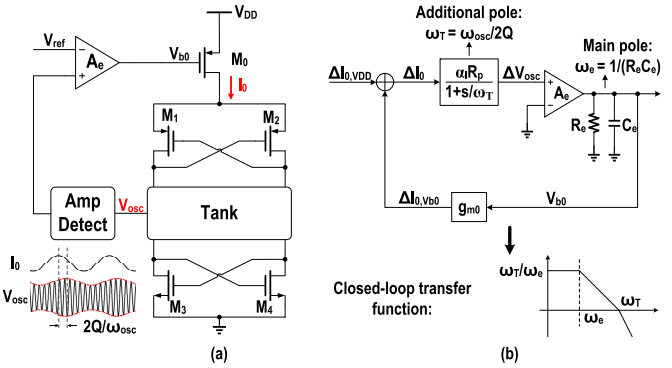

Fig. 2. (a) Schematic and (b) block diagram of an *LC* oscillator with amplitude tracking loop.

(i.e., V_{gs} and V_{ds}), the change in their operating states would vary the equivalent parasitic capacitance, $C_{\text{par,equ}}$ [18]. Thus, the oscillating frequency will be pushed. If a periodical ripple is on V_{DD}, I_0, and V_{osc} will also show periodical variations. Therefore, the change of $C_{\text{par,equ}}$ will also be periodical and could manifest itself as large spurs in the output spectrum of the oscillator. To be able to obtain a clean output spectrum when V_{DD} contains ripples, I_0 and V_{osc} should be stabilized under V_{DD} variations.

B. Amplitude Tracking Loop

Conventional solutions to stabilize the oscillating amplitude of an *LC* oscillator resort to employing an amplitude tracking loop across process, voltage, and temperature (PVT) variations [19] and to bias the oscillator at the optimum operational point [best figure-of-merit (FoM)] [20]. It is instructive to examine this loop for stabilizing I_0 and V_{osc} under supply ripples.

Fig. 2(a) shows the schematic of an *LC* oscillator with amplitude tracking loop. The tail current source transistor, M_0 is PMOS, which is fairly robust to (local) ground-induced perturbations. Replacing M_0 with an NMOS transistor will not help much as its V_{gs} will be now very sensitive to local ground perturbations and its I_0 sensitivity to V_{DD} will still be felt through the M_0's channel length modulation. The loop first detects the oscillation amplitude, and then compares it with the reference value V_{ref}. The comparison outcome will adjust I_0 by varying the gate bias voltage V_{b0} of M_0. This feedback loop will keep on working to fix V_{osc} at the level corresponding to V_{ref}. When I_0 and correspondingly V_{osc} are modulated by the supply ripple, V_{b0} will be modulated in reaction through the amplitude tracking loop. As a result, the variation of I_0 and V_{osc} will be reduced by an amount equal to the loop gain of the amplitude tracking loop, thus reducing the variation of oscillating frequency.

Unfortunately, this method is limited by the pole from the resonance tank. When the supply varies, I_0 will follow almost immediately. However, due to a "memory" of the tank, there is a time delay, $2Q/\omega_{\text{osc}}$, between the variation of the current flowing through the tank and the subsequent effect on the oscillation amplitude across the tank, as shown in Fig. 2(a) [19]. Such a time delay creates an additional

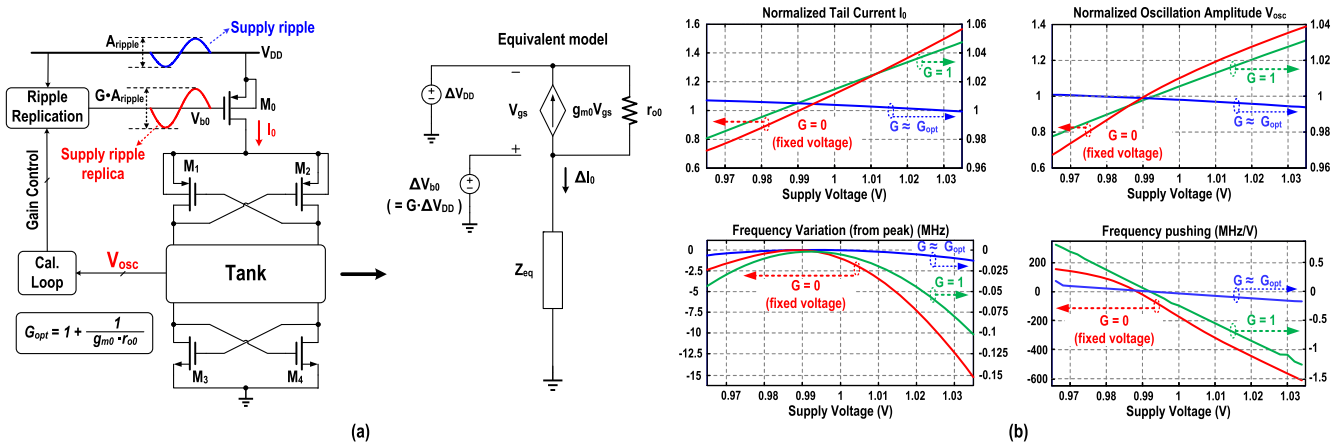

Fig. 3. (a) Conceptual block diagram of the proposed supply pushing reduction technique with the equivalent model to estimate the optimum gain (G_{opt}) of the RRB. (b) Simulation results of an *LC* oscillator with the proposed technique.

low-frequency pole located at $\omega_{\text{osc}}/(2Q)$ and will limit the bandwidth of the amplitude tracking loop [see Fig. 2(b)] [21]. This bandwidth limitation could limit the spur level that can be reached with this method. To alleviate this limitation, the pole at the output of the amplifier must be pushed to a very high frequency, since the pole related to the tank is almost fixed. However, this may lead to a significant increase in the current consumption of the loop.

C. Proposed Technique

In this section, we propose a feed-forward supply pushing reduction technique for *LC* oscillators that entirely avoids the use of the amplitude tracking loop around the oscillator core. Fig. 3(a) illustrates its principle. To stabilize I_0, and thus V_{osc}, in face of V_{DD} variations, a replica of the supply ripple is applied to the gate of PMOS current source M_0 to stabilize its V_{gs}. As a result, the variation of I_0 and V_{osc} would be largely suppressed. If M_0 is an ideal device, whose drain current is solely controlled by its V_{gs} according to the square law, then an exact copy of the supply ripple waveform is required at its gate terminal V_{b0} to keep I_0 and V_{osc} constant. As shown in Fig. 3(b), the variations of I_0 and V_{osc} do get largely suppressed when the waveform applied at V_{b0} is the same as that of the supply ripple (gain, $G = 1$). Hence, the frequency variations due to the supply voltage are largely reduced, resulting in a much lower supply pushing of the oscillator. However, for nanoscale CMOS technologies, the channel-length modulation effect is not negligible. This means that the drain current of M_0 also depends on its V_{ds}. Thus, the waveform at V_{b0} should be an *amplified* replica of the supply ripple to compensate for the residue current variation due to the variation of V_{ds} of M_0. Fig. 3(a) also shows the equivalent model to estimate the optimum gain (G_{opt}). Based on this model, the supply variation, ΔV_{DD}, induced tail current variation, $\Delta I_{0,V_{\text{DD}}}$, could be calculated as

$$\Delta I_{0,V_{\text{DD}}} \approx \frac{1 + g_{m0} \cdot r_{o0}}{r_{o0} + Z_{\text{eq}}} \Delta V_{\text{DD}} \tag{1}$$

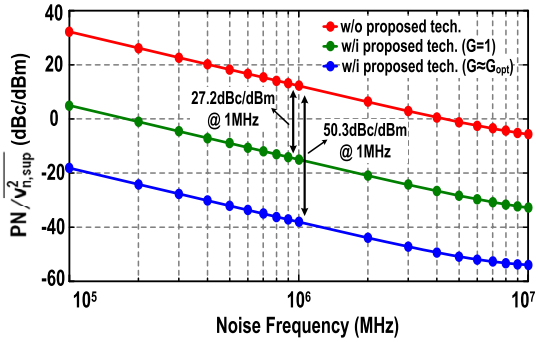

Fig. 4. Simulated transfer function of the supply noise to PN of the oscillator with/without the proposed supply pushing reduction technique.

while the tail current variation induced by $\Delta V_{b0} = G \cdot \Delta V_{\text{DD}}$ is

$$\Delta I_{0,V_{b0}} \approx -\frac{g_{m0} \cdot r_{o0}}{r_{o0} + Z_{\text{eq}}} \Delta V_{b0} \tag{2}$$

where Z_{eq} is the large-signal equivalent impedance of the cross-coupled transistors M_{1-4} and the tank that is seen by M_0, while g_{m0} and r_{o0} are the effective transconductance and output resistance of M_0, respectively. To compensate for the tail current variation due to V_{ds}, the magnitudes of (1) and (2) should be equal. Hence, G_{opt} is calculated as

$$G_{\text{opt}} \approx 1 + \frac{1}{g_{m0} \cdot r_{o0}}. \tag{3}$$

Since $g_{m0} \cdot r_{o0}$ is relatively large (e.g., >10), G_{opt} is slightly higher than 1. Fig. 3(b) also shows that I_0 and V_{osc} are further stabilized (i.e., $\sim 10\times$ smaller variations compared to $G = 1$ case) under supply variations when $G \approx G_{\text{opt}}$, thus the supply pushing of the oscillator becomes much lower. It also translates into a significant reduction in the thermal noise of supply to phase noise (PN) conversion as can be gathered from Fig. 4.

The similar feed-forward principle was applied to LDOs in order to improve their PSR at several megahertzs of ripple frequencies [22]–[24]. However, they lack a reliable calibration for the optimum gain, which will be proposed later. Also, they still tend to use large off-chip capacitors [22] or extra

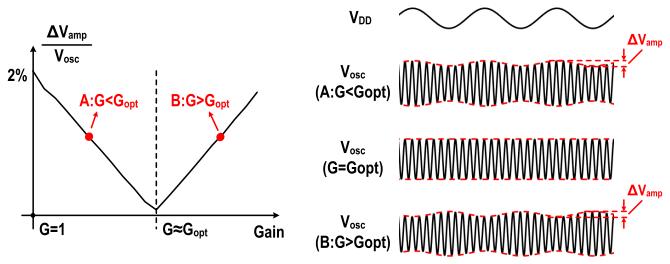

Fig. 5. Operating principle of the calibration loop based on oscillation amplitude variation (ΔV_{amp}).

on-chip capacitance occupying large silicon area [24]. When the LDO is integrated with a current-biased oscillator, the pass transistor should be placed above the tail current source M_0, thus consuming extra voltage headroom. Merging the pass transistor with M_0 would reclaim this headroom, but the oscillator becomes voltage-biased, whose current is poorly controlled over PVT variations. Also, higher supply sensitivity of a voltage biased oscillator would place higher demands on the PSR performance of the LDO, resulting in large power and area overhead [2].

The amplified supply ripple replica at V_{b0} is generated by the proposed ripple replication block (RRB). As can be gathered from (3), the optimum gain is prone to PVT variations. Therefore, a calibration loop is also integrated on-die, as indicated in Fig. 3(a). The calibration scheme is based on measuring the variation of the oscillation amplitude, ΔV_{amp}, in response to the V_{DD} perturbations. Fig. 5 shows the operating principle. When $G < G_{\text{opt}}$ (case A), $\Delta I_{0,V_{bo}}$ is smaller than $\Delta I_{0,V_{\text{DD}}}$, so ΔV_{amp} is in phase with ΔV_{DD} and decreases in magnitude as G gets closer to G_{opt}. However, when $G > G_{\text{opt}}$ (case B), $\Delta I_{0,V_{b0}}$ becomes larger than $\Delta I_{0,V_{\text{DD}}}$. Then, ΔV_{amp} is out of phase with ΔV_{DD}, and its magnitude increases again with the increase of G. At the optimum point, $G = G_{\text{opt}}$, and ideally a constant oscillation amplitude is maintained under supply variations. Thus, the calibration loop measures ΔV_{amp} under different gain settings to calculate the optimum operating point for the oscillator circuit.

III. Circuit Implementation

In this section, we discuss the detailed circuit realization of a 5-GHz *LC* oscillator with the proposed feed-forward supply pushing reduction technique and the on-chip calibration loop.

A. Ripple Replication Block

Fig. 6 shows the schematic of the implemented *LC* oscillator with the RRB. Here, the complementary cross-coupled oscillator structure is chosen due to its lower power consumption compared to its NMOS and PMOS only counterparts at the same V_{DD} and equivalent parallel resistance of the tank.

The RRB is proposed to bias the gate terminal of a tail current source of the *LC* oscillator. To generate the required replica with the desired gain larger than 1, the RRB is logically divided into two parts. The first part (gray-dashed box in Fig. 6) contains a diode-connected PMOS transistor,

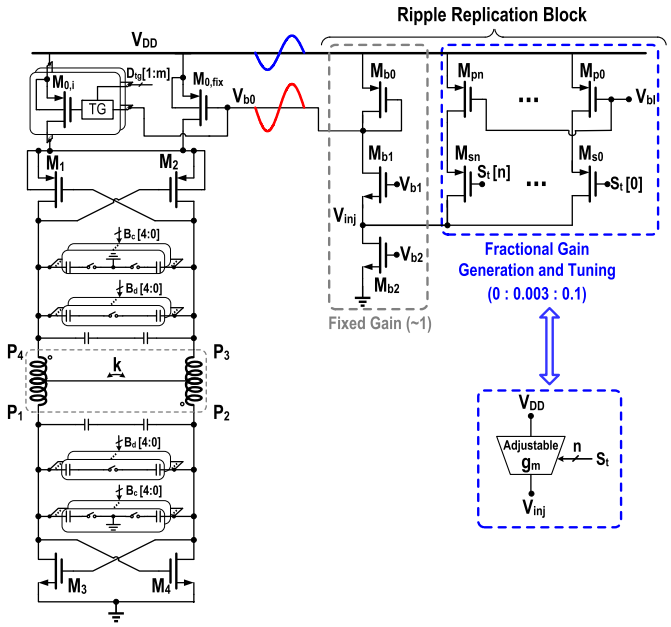

Fig. 6. Schematic of the implemented *LC* oscillator with the RRB.

M_{b0}, in series with two cascode NMOS transistors, $M_{b1,2}$. Due to the high output impedance of the cascode, M_{b0} just "replicates" the supply ripple to V_{b0} with a fixed gain of 1. Thus, the first term on the right-hand side of (3) is covered by this part. To boost the gain above 1, the fractional part (blue-dashed box in Fig. 6) is introduced to inject some extra current proportional to V_{DD} into the cascode node, V_{inj}. To digitally control the fractional gain, current sources M_{pk} $(k = 0, 1, \ldots, n)$ are individually turned on/off by switch transistors M_{sk} $(k = 0, 1, \ldots, n)$ according to the digital code S_t generated by the calibration loop. The fractional part thus provides an adjustable transconductance between V_{DD} and V_{inj}. The final gain G provided by the RRB could be approximated as

$$G \approx 1 + \frac{g_{m,f}}{g_{m,b0}} \tag{4}$$

where $g_{m,f}$ and $g_{m,b0}$ are the total equivalent transconductance of the fractional part and the transconductance of M_{b0}, respectively. Since G_{opt} is only slightly larger than 1, the required $g_{m,f}$ should be much smaller than $g_{m,b0}$. Therefore, the total current injected into V_{inj} is much smaller than the current consumed by M_{b0}, and would not lead to a large variation of the operating point of the *LC* oscillator. In practice, the gain provided by the integer part is slightly lower than 1 due to the finite output impedance of the cascode transistors. Furthermore, for designs with lower V_{DD}, the cascode transistor M_{b1} could be removed which would further reduce the gain of the integer part. However, any reasonable (i.e., ~5%) integer gain degradation can be easily covered by the fractional part.

1) Bandwidth and Power Consumption Tradeoff: The required bandwidth of the RRB is determined by the maximum spur level allowed at the highest ripple frequency.

Assuming a phase shift of θ between the supply ripple at oscillator's V_{DD}, $0.5 \cdot A_{\text{ripple}} \cos(2\pi f_{\text{ripple}} t)$, and the generated

replica at V_{b0} at the optimum gain, the tail transistor M_0 would experience an effective supply variation of

$$V_{\text{rip,eff}} = -A_{\text{ripple}} \cdot \sin\left(\frac{\theta}{2}\right) \cdot \sin\left(2\pi f_{\text{ripple}} t - \frac{\theta}{2}\right) \quad (5)$$

where A_{ripple} is the peak-to-peak amplitude of the supply ripple. Therefore, the spur level in the output spectrum of the oscillator could be calculated as

$$S_{\text{spur-carrier}} = 20 \cdot \log_{10}\left(\frac{K_{\text{push}} \cdot A_{\text{ripple}} \cdot \sin\left(\frac{\theta}{2}\right)}{2 f_{\text{ripple}}}\right). \quad (6)$$

To guarantee <-50 dBc spur level at $f_{\text{ripple}} = 20$ MHz, which is the highest ripple frequency considered in this paper, the maximum tolerable θ is calculated to be $\sim 3^\circ$ under 50-mV_{pp} ripple and $K_{\text{push}} \approx 100$ MHz/V.

In the frequency range of interest, the RRB may be approximated as a single-pole system, with the pole located at $\omega_p = g_{m,b0}/C_L$, where C_L is the capacitive load at V_{b0}. Thus, to obtain $\sim 3^\circ$ phase shift at 20 MHz, $\omega_p \approx 400$ MHz is required. Considering $\sim$800-fF load, the calculated $g_{m,b0}$ should be about 2.0 mS. With $g_m/I_{\text{ds}} \approx 12$, the current consumption of the integer part is calculated to be ~ 170 μA. Together with ~ 12 μA consumed by the fractional part at the maximum G of ~ 1.1, the total current consumption of the RRB is around 180 μA. The PMOS transistors in the fractional part are sized to achieve tuning resolution of ~ 0.003 as a tradeoff between the resolution and calibration time. Therefore, a 5-bit thermometer code is implemented to cover the aforementioned maximum G.

Due to the distributed layout design, there could be a delay between the routed V_{DD} at the oscillator's M_0 source and at the RRB. That delay can increase the ripple phase shift θ of the RRB. In this design, since the proposed RRB is simple and compact, it is easily placed next to M_0. Hence, this effect is negligible, especially at ripple frequencies <20 MHz.

2) Sizing and Biasing of Tail Transistor: The tail current transistor M_0 is designed here with a channel length of 120 nm, contributing to the capacitive load C_L mentioned earlier. The optimal gain G_{opt} is simulated to be in the middle of the 1–1.1 range provided by the RRB, leaving enough margin on both sides. By using M_0 with a shorter channel length, C_L could be reduced, leading to a lower power consumption. However, the required G_{opt} would increase due to a smaller output resistance of M_0, which could adversely affect the tuning resolution and/or calibration time.

Under the 1-V nominal supply voltage, V_{ds} of M_0 is chosen to be around 250 mV. A smaller V_{ds} may allow the oscillator to operate under lower supply voltage, thus reducing its power consumption. However, a larger M_0 would be needed to provide similar tail current, which also generates more noise, degrading the PN and FoM performance of the oscillator [25]. Moreover, with a lower V_{ds}, the output resistance of M_0 also becomes smaller, leading to an increase in G_{opt}. Combined with the increased parasitic capacitance due to the larger device size, the bandwidth of the RRB would be reduced under similar power consumption, thus increasing the phase shift θ of the replica at V_{b0}. As discussed earlier, this would increase the output spur level of the oscillator. Hence, it is not beneficial to reduce V_{ds} further.

In the actual design, M_0 is implemented as a parallel combination of a fixed part, $M_{0,\text{fix}}$, with a bank of unit transistors, $M_{0,i}$, as shown in Fig. 6. Each $M_{0,i}$ could be switched in separately to tune the oscillation swing by enabling the corresponding transmission gate (TG) before its gate terminal with the control code $D_{\text{tg,i}}$. The tail current resolution is ~ 30 μA to ensure the oscillator operates within 1 dB of its optimum PN across the tuning range (TR). To cover the required current range under PVT variations, 27 such unit transistors are implemented.

B. Calibration Loop

Fig. 7 shows the block diagram of the integrated calibration loop. As discussed in Section II-C, the perturbation of the oscillation amplitude, ΔV_{amp}, is used in the loop as a stimulus to calibrate G_{opt}. Hence, the outputs of the oscillator are first connected to a peak detector. Ideally, the output of the peak detector, V_{pd}, contains two frequency components: the desired one at f_{ripple}, and the additional one at the second harmonic of the oscillation frequency, f_{osc}. V_{pd} is then amplified through self-biased inverters. To amplify the small input level at V_{pd} (e.g., 1 mV) to a large enough amplitude (e.g., 250 mV) at the output, a large gain (e.g., 48 dB) is needed. Hence, two inverter stages with a bandwidth of ~ 20 MHz are implemented to provide the required gain [see Fig. 9(a)]. The output of the inverter chain, V_{inv}, is filtered by a simple *RC* low-pass filter (LPF). The cutoff frequency of the LPF is set to pass through the desired frequency component at f_{ripple}, while the second harmonic at $2 \times f_{\text{osc}}$ is filtered out. If there is any mismatch in the input differential pair of the peak detector, V_{pd} would contain a third frequency component at f_{osc}. Since f_{osc} (several gigahertzs) is much higher than f_{ripple} (tens of megahertz), this component is easily filtered out by the inverter chain and the LPF. Hence, the mismatch in the peak detector will not affect the calibration results. The output of the LPF, V_{lpf}, is then compared with a reference value, V_{ref}, through a comparator. V_{ref} is roughly set to a voltage higher than the product of the desired ΔV_{amp} and the dc gain of the peak detector cascade with the inverter stages. The output of the comparator is connected to the clock terminal of a D flip-flop (DFF). When V_{ref} is crossed, the comparator's output becomes high, triggering the output of the DFF to flip to "1". The digital algorithm in the loop monitors the latch output, Latch_out, and calculates the optimum control code S_t for the RRB.

The digital block attempts to find the minimum point of ΔV_{amp} versus the control code [$\Delta V_{\text{amp,min}}$ in Fig. 8(a)]. However, to precisely detect $\Delta V_{\text{amp,min}}$, a set of comparators and DFFs would be needed. The simulated amplitude variation at the output of the LPF is ~ 300 mV. Thus, 20 comparators, followed by a DFF each, are required to realize a voltage resolution of 15 mV. Some offset calibration techniques may also be needed to reduce the input referred offset of comparators to a level much lower than the voltage resolution. The digital algorithm then counts the number of "1" in the output of the DFFs to determine ΔV_{amp}. Such a method could increase the design complexity greatly. To avoid this,

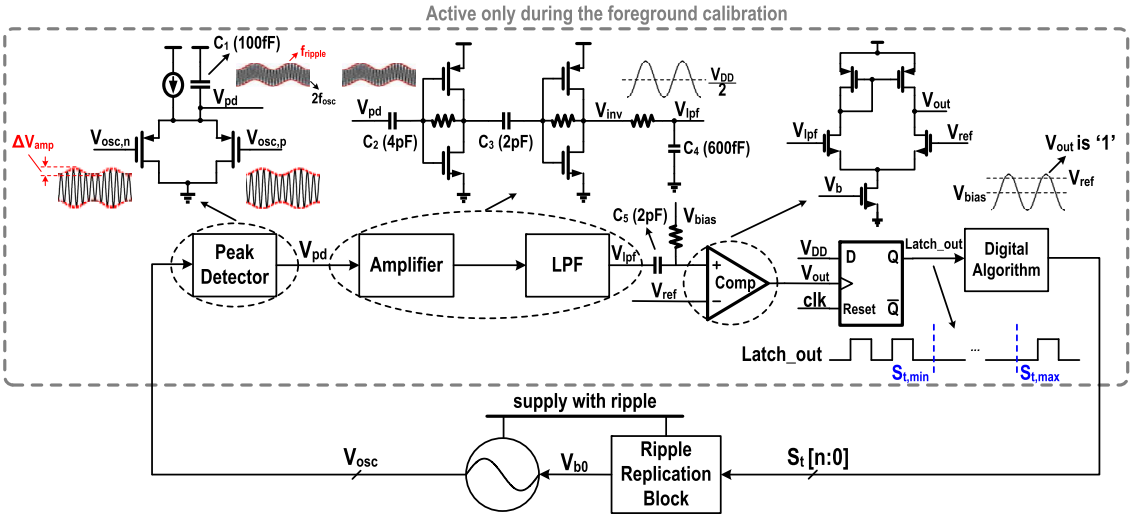

Fig. 7. Block diagram of the calibration loop.

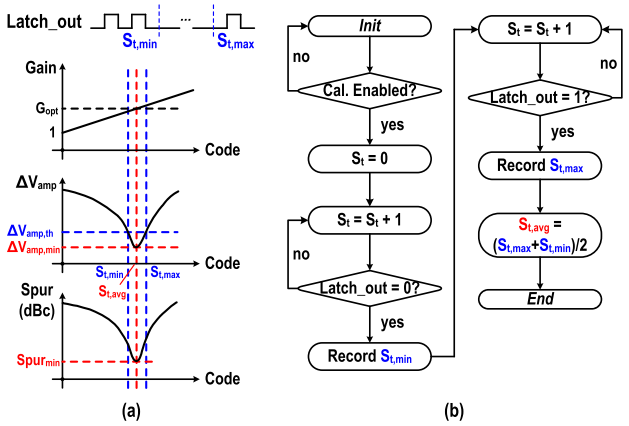

Fig. 8. (a) Operating principle and (b) flowchart of the calibration loop with the proposed algorithm.

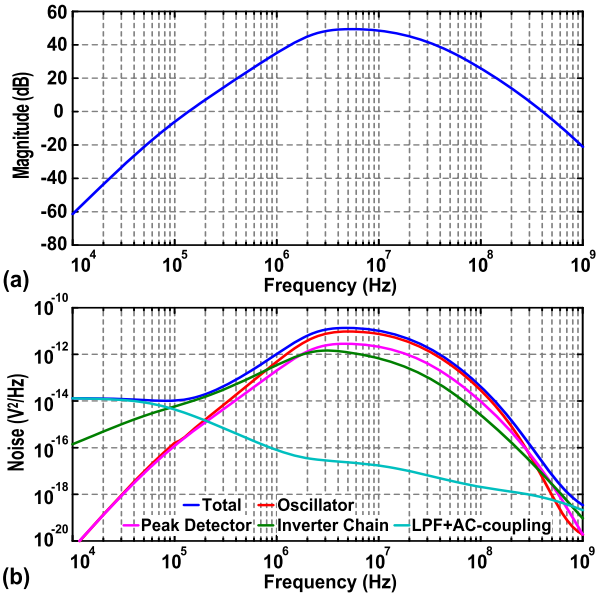

Fig. 9. (a) Simulated transfer function from V_{pd} to comparator input. (b) Simulated PSD of noise at comparator input with the contribution from different noise sources.

a calibration algorithm is proposed whereby only one comparator without any offset calibration could be used in the loop. Fig. 8(a) shows the operating principle of the proposed technique. The reference voltage, V_{ref}, at the comparator input is roughly set to a value corresponding to an oscillation amplitude variation of $\Delta V_{amp,th}$, which is higher than $\Delta V_{amp,min}$. The calibration process starts from a small value of S_t, where $G < G_{opt}$ and $\Delta V_{amp} > \Delta V_{amp,th}$. Thus, the initial value of Latch_out is "1." The algorithm keeps increasing S_t, which decreases ΔV_{amp} as G approaches G_{opt}. When ΔV_{amp} becomes lower than $\Delta V_{amp,th}$, Latch_out changes from "1" to "0." The algorithm records this code as $S_{t,min}$, and then increases S_t again. When S_t is large enough, ΔV_{amp} would be higher than $\Delta V_{amp,th}$ again, and Latch_out switches back to 1. The algorithm records this code as $S_{t,max}$, and the optimum code, $S_{t,avg}$, is calculated as the average of these two recorded codes. Fig. 8(b) reveals the operational flowchart of this calibration process.

Fig. 9(a) shows the simulated transfer function from the output of the peak detector to the input of the comparator. The lower cutoff frequency of this bandpass response is due to the ac coupling used to accommodate the dc levels of different stages in the loop. It sets the lowest f_{ripple} that the loop can handle. In this paper, this frequency is designed to be ~2 MHz. Considering the current trend in increasing the switching frequency of the dc–dc converters to several or even tens of megahertz [26]–[29], this value appears reasonable. A lower cutoff frequency could be adopted to detect lower ripple frequencies, but at the expense of increased loop settling time. When S_t changes in each calibration step, the current injected by the fractional part varies, leading to slight variations in the tail current and the oscillation amplitude of the oscillator. Hence, due to the bandpass characteristic of the loop, it needs a certain time for settling before correctly functioning. With 2-MHz corner frequency, the settling time is 0.5 μs per step.

Fig. 9(b) shows the simulated power spectrum density (PSD) of noise at the comparator's input. The major part

of it is contributed by the oscillator itself. The differential output of the oscillator is less affected by the variation of the common-mode voltage, but the output level of the peak detector would be modulated. Thus, the calibration loop is more sensitive to the common-mode noise from the oscillator, e.g., the noise of the tail current source. After being shaped by the transfer function of the inverter chain and LPF, the common-mode noise is finally passed to the comparator's input. From Fig. 9(b), the integrated noise is around 14 mV, corresponding to ∼0.095 mV equivalent input noise at the input of the peak detector. To achieve <−50-dBc spur level, ΔV_{amp} is simulated to be ∼1.8 mV (0.64 mV_{rms}), leading to an SNR of 16.5 dB, which is sufficient for an effective calibration.

The proposed calibration algorithm and RRB are still effective even if the ripple of the dc–dc converter is simultaneously coupled through the supply and other parasitic paths, e.g., into the dc output of the RRB or ground. Since the coupling through both paths would also vary the tail current, and correspondingly the oscillation amplitude, their effect would be detected and minimized by the calibration algorithm through adjusting G_{opt}. Besides the supply ripples, interference from other sources with different frequencies may also modulate the oscillation amplitude. However, with proper design techniques, e.g., shielding and placing guard rings, which are common in oscillator design, the effect of these interference should be non-dominant, and the calibrated code is still around the optimum one.

It should be pointed out that the main purpose of this paper is to verify the ripple replication circuitry and the principle of the calibration algorithm. Hence, a quiet supply is used for the calibration loop. If the ripple also exists on the supply of the loop, its effect could be suppressed with *RC* filtering since the power consumption of the peak detector and the amplifier, which are the supply sensitive blocks in the loop, is much smaller compared to that of the oscillator. When used in the whole system, e.g., PLL, the calibration loop may also be powered by the regulators used for other supply sensitive blocks, e.g., time-to-digital converter (TDC) and digital-to-time converter (DTC). Since the loop only operates for a short time (∼40 μs in the worst case) at system startup or whenever needed at the beginning of IoT packets, it would not affect the system efficiency and the performance of other blocks during the normal operation. If the entire system was to be powered by the SC converter directly, a >40-dB PSR ratio would be required for the calibration loop, which is not difficult to achieve with conventional analog design techniques at the relatively low operating frequency of the loop (i.e., <20 MHz) [30]–[32].

C. Oscillator Implementation

The designed oscillator uses a transformer-based resonant tank. Since the RRB is connected to the gate of tail current source M_0, its output noise [see Fig. 10(a)] will modulate the oscillator's tail current, thus converting into PN. Similar to the tail current noise, only the noise around dc and even harmonics of f_{osc} would cause PN degradation [33]–[35]. The thermal noise around the even harmonics of f_{osc} is filtered out due to the bandwidth of the RRB, as shown in Fig. 10(a),

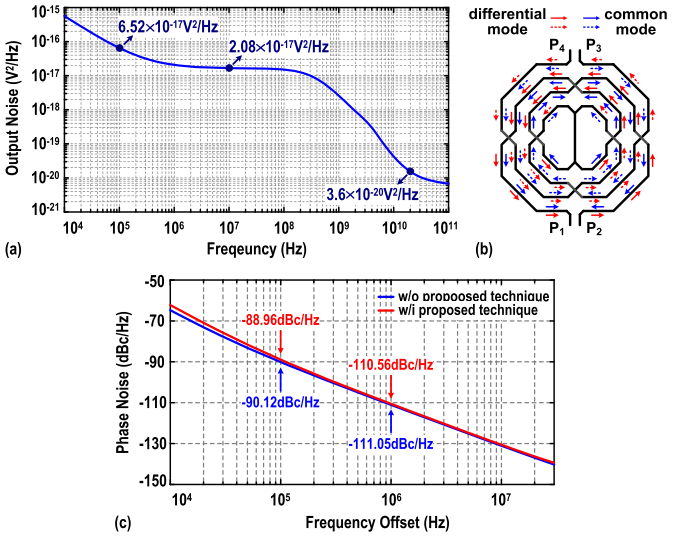

Fig. 10. (a) Output noise of the RRB. (b) Schematic of the symmetrical transformer. (c) Simulated oscillator PN with and without the RRB.

and would not limit the PN performance. For the noise around dc, it is up-conversion into PN is related to the dc component, c_0, of the impulse sensitivity function (ISF) of the tail current source [36], [37]. To achieve small c_0, the implicit common-mode resonance technique [38], [39] is employed. Single-ended capacitor banks connected to a symmetrical transformer, as shown in Fig. 10(b), are used to tune the common-mode resonance frequency to around $2\times f_{\text{osc}}$. Hence, the second harmonic component of the oscillation waveform is aligned with the fundamental one, and would not affect the symmetry of the waveform. Therefore, c_0 is kept small and the up-conversion of the low-frequency noise is largely suppressed [36], [40]. Simulation results in Fig. 10(c) show that the PN degradation is only 1.16 dBc at 100-kHz frequency offset. Note that the reported spot noise (as expressed in $\text{nV}/\sqrt{\text{Hz}}$ unit) of the LDOs in [6] and [7] at 100 kHz is more than 30× the value shown in Fig. 10(a). Hence, even with the common-mode resonance technique, the oscillator's PN would be greatly degraded when powered by these LDOs.

Both the NMOS and PMOS cross-coupled transistors M_{1-4} provide the negative transconductance in the complementary structure. The body terminals of the PMOS cross-coupled pair, $M_{1,2}$, are deliberately connected to their source terminals to avoid the body effect. Otherwise, their threshold voltage, V_{th}, would be modulated under supply variations thus varying the oscillation amplitude V_{osc}, consequently pushing f_{osc}. Simulation results show that this body effect could limit the supply pushing to no better than 9.5 MHz/V. Note that the above-mentioned NMOS alternative to the tail transistor M_0 would not be effective unless a costly triple-well technology is used.

IV. Measurement Results

The *LC* oscillator with the proposed feed-forward ripple replication and cancellation technique is implemented in TSMC 40-nm 1P8M CMOS process without ultra-thick metal layers. The proposed calibration loop is also integrated

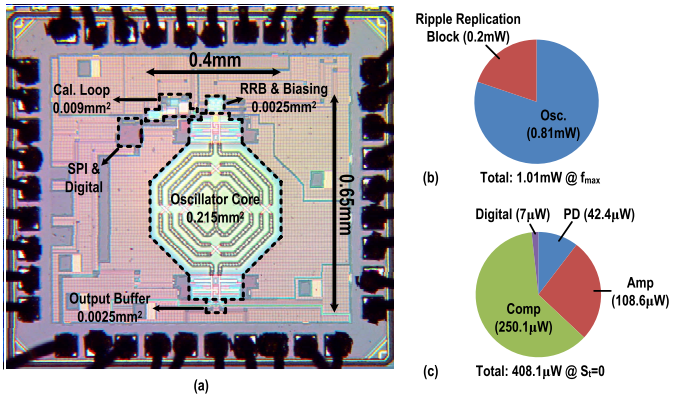

Fig. 11. (a) Chip micrograph of *LC* oscillator with reduced supply pushing. (b) Measured power breakdown of the oscillator at maximum oscillation frequency during normal operation. (c) Simulated power breakdown of the calibration loop when $S_t = 0$.

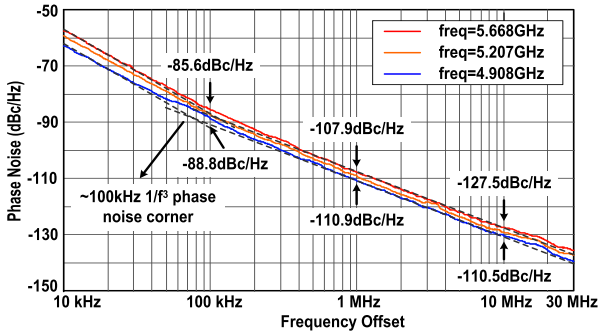

Fig. 12. Measured PN of the oscillator across the TR.

on-die. Fig. 11(a) shows the chip micrograph. The total active area is 0.23 mm^2, in which the oscillator core occupies about 0.215 mm^2. The additional area occupied by the RRB with its biasing circuit and the calibration loop is just 0.012 mm^2, including 8.7-pF capacitance of the calibration loop. To enhance the tank's Q-factor, the symmetrical transformer is designed by stacking the top two metal layers with the aluminum capping layer. The spacing between each turn of the transformer is optimized for a magnetic coupling factor of 0.31. The simulated differential inductance of the transformer is 1.7 nH. Q-factor of the whole tank is estimated to be ~7. The capacitor banks are split into a 5-bit differential bank and a 5-bit common-mode bank to tune the common-mode resonance frequency.

The measured power consumption of the oscillator is around 0.81 mW at the maximum oscillation frequency, while the RRB consumes about 0.2 mW, as shown in Fig. 11(b). During calibration, the power consumed by the calibration loop when $S_t = 0$, which is the worst case, is around 0.41 mW, and the simulated power breakdown of the loop is also shown in Fig. 11(c).

The measured TR is 4.9–5.7 GHz (15%). Fig. 12 shows the measured PN performance across the TR. PN varies from −108 to −111 dBc/Hz at 1-MHz offset, with a flicker noise corner of around 100 kHz. To verify the concept of the proposed technique, the control code S_t of the RRB is

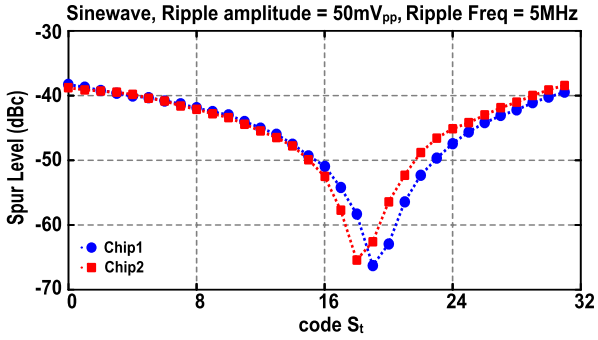

Fig. 13. Measured spur level over the control code S_t.

manually swept while a 50-mV$_{pp}$ 5-MHz sinusoidal ripple is applied on the oscillator supply. As shown in Fig. 13, there exists an optimum code at which the spur level is lower than −60 dBc, corresponding to a >27-dB improvement over the $S_t = 0$ case. Note that $G \approx 1$ when $S_t = 0$, and the oscillator already benefits from the significantly reduced supply pushing.

The effectiveness of the automatic calibration loop is verified in Fig. 15 (top), which compares the spectra before and after the calibration. With the supply contamination by a 50-mV$_{pp}$ 5-MHz sinusoidal ripple, the spur level is reduced by 30 dBc and reaches −68.7 dBc after the calibration. Fig. 14(a) shows the measured spur level over the frequency of the supply ripple. The proposed technique achieves ≤−49-dBc optimum spur levels under ≤50 mV$_{pp}$, 0.5–20-MHz sinusoidal ripples, while the calibrated spur levels closely follow the optimum ones in most cases. In Fig. 14(c), the spur level is measured across the TR of the oscillator. The worst case spur under a 50-mV$_{pp}$ 5-MHz sinusoidal ripple is ≤59 dBc. Fig. 14(b) and (d) displays the oscillator's supply pushing based on the measured spur levels. When the ripple frequency is lower than 12 MHz, the calculated supply pushing is lower than 1 MHz/V for both the optimum and calibrated cases.

Similar measurements are also performed for saw-tooth ripples. Fig. 15 (bottom) compares the spectra before and after the calibration. Under a 50-mV$_{pp}$ 5-MHz saw-tooth ripple, the spur at the fundamental offset is reduced by 22.9 dBc and reaches −61.7 dBc after the calibration. For spurs at higher harmonics, the suppression is also observed, but with lower magnitudes (5.8-dBc suppression for the second harmonic reaching −59.1 dBc after the calibration). Fig. 14(e) reports the spur levels over the ripple frequency. The worst case spur of −47 dBc is found under ≤50 mV$_{pp}$, 0.5–20-MHz saw-tooth ripples, while the calibration results follow the optima. In Fig. 14(f), the spurs are lower than −58 dBc within the entire TR under a 50-mV$_{pp}$ 5-MHz saw-tooth ripple.

Fig. 16 (top) shows the measured oscillator spectrum under a 50-mV$_{pp}$ 2.5-MHz supply ripple. A spur can also be observed at an offset frequency of 5 MHz (i.e., 2 × 2.5 MHz). This second ripple harmonic spur mainly comes from the nonlinearity of the fractional part of the RRB. To achieve fine tuning resolution, small transistors with low overdrive voltage are used in the fractional part. Hence, these transistors operate in a moderate or weak inversion region, where the nonlinearity is relatively large. The simulated

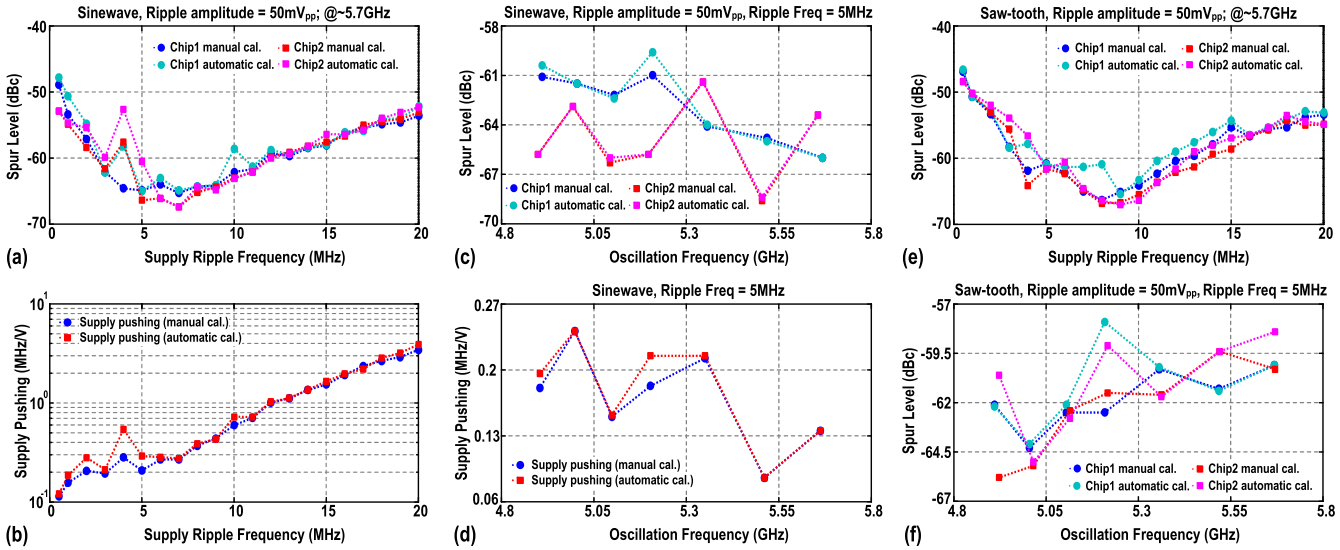

Fig. 14. (a) Measured spur levels over the sinusoidal ripple frequency and (b) corresponding supply pushing for both the manual and automatic calibrations. (c) Measured spur levels over the oscillation frequency under the sinusoidal ripple and (d) corresponding supply pushing for both the manual and automatic calibrations. (e) Measured spur levels over the frequency of the saw-tooth ripple and (f) over the oscillation frequency under the saw-tooth ripple.

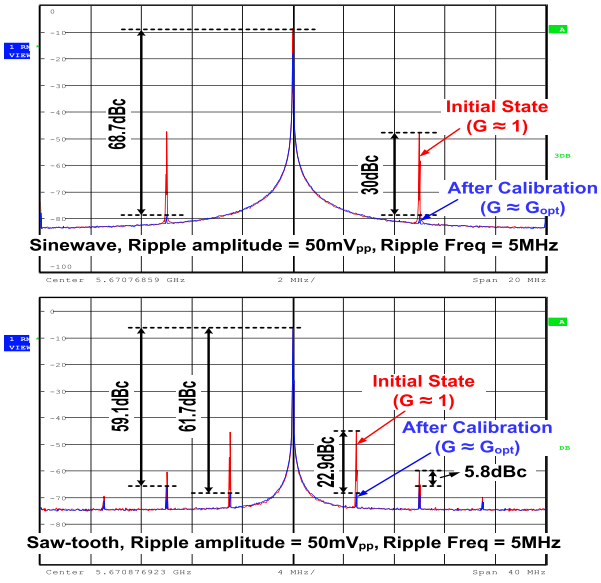

Fig. 15. Measured oscillator spectra before and after automatic calibration under 50 mV_{pp} 5-MHz sinusoidal (top) and saw-tooth (bottom) ripple.

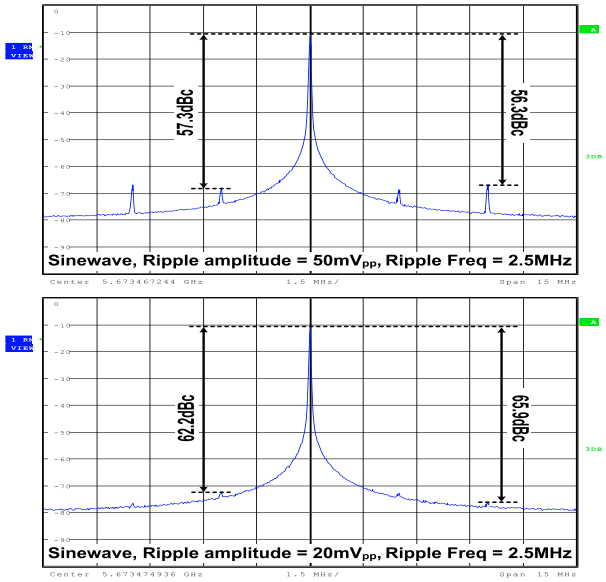

Fig. 16. Measured oscillator spectra under 50 mV_{pp} (top) and 20 mV_{pp} (bottom) 2.5-MHz sinusoidal ripple.

second harmonic intercept point of these transistors is $V_{IP2} = 2 \cdot (V_{GS} - V_{TH}) \approx 100$ mV. Consequently, with 50-mV_{pp} ripple on supply, which is already comparable to the overdrive voltage of the transistors, relatively large second ripple harmonic spur is generated. To improve the performance at the second ripple harmonic, transistors with a smaller aspect ratio (W/L) and increased overdrive voltage should be used. Simulations show that the spur at $2 \times f_{ripple}$ is improved by 4.8 dBc when the overdrive voltage of these transistors is increased to 100 mV, while the current penalty is only 3.2 μA at G_{opt}. Also, the spur at the second ripple harmonic falls drastically with a lower ripple amplitude. As shown in Fig. 16, the measured spur level at the second harmonic is reduced to -65.9 dBc under a 20-mV_{pp} ripple, which is a target of our SC converter design, and should bear little practical consequences.

Fig. 17 (top) compares the measured oscillator spectra before and after the automatic calibration when the supply is subjected to a two-tone ripple which consists of 8- and 12-MHz components of equal amplitude. The envelope of the ripple is kept at 50 mV_{pp}. The automatic calibration is still effective under this scenario, and the plot shows that the spur at 8/12-MHz offset is reduced by 22.3/20.8 dBc and reach $-65.3/-62.4$ dBc, respectively, after the calibration. The nonlinearity effect not only induces small spurs (≤ -64.9 dBc) at the second harmonics of these two tones but also generates additional spurs at the sum (20 MHz) and difference (4 MHz)

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH STATE OF THE ART

			This work	JSSC2017 [38]	ESSCIRC2016 [13]	ISSCC2014 [8]	ISSCC2016 [10]	VLSI2017 [14]
Description			Feed-forward compensation	2×f_{osc} implicit resonance	FCW compensation	Bias at lowest K_{push} point	Two constant-Gm biasing	Noise suppression loop
Osc. Type			LC	LC	LC	Ring	Ring	Ring
Tech. (nm)			40 (w/o UTM)	28 (w/i UTM)	65	40	40	65
V_{DD} (V)			1.0	0.9	1.0	1.1	1.1	1.0
Frequency Range (GHz)			4.9-5.7 (15%)	2.85-3.75 (27.2%)	3.2-4.8 (40%)	2.418 (NA)	3.2 (NA)	3.2 (NA)
PN (dBc/Hz) @1MHz			-107.9 to -110.9	-127.5 to -131	-108* @ 3.57GHz	NA	NA	-88*
Ripple Amplitude			50mV_{pp}	NA	NA	1mV_{pp}	50mV_{pp}	20mV_{pp}
Sinewave	Spur (dBc)	@1MHz	<-54	NA	NA	-45	-25	-57
		@5MHz	<-58	NA	NA	-49	NA	-48
	K_{push} (MHz/V)	@1MHz	<0.16#	6-30	NA	22.5#	45***	0.63#***
		@5MHz	<0.5#	6-30	NA	70.9#	NA	4#
	Improv. (dBc)	@1MHz	18-24**	NA	NA	28	10	30
		@5MHz	24-30**	NA	NA	19	NA	30
Saw-tooth	Spur (dBc)	@1MHz	<-50	NA	-50	NA	NA	NA
		@5MHz	<-58	NA	-51	NA	NA	NA
	Improv. (dBc)	@1MHz	11.3**	NA	15	NA	NA	NA
		@5MHz	22-27**	NA	12	NA	NA	NA
Osc. Power Cons. (mW)			0.8-1.3	6.6	18.9†	6.4†	2.95†	2.73†
Power Cons. K_{push} Reduction Tech. (mW)			0.2	NA	2.4	NA	NA	0.45
Area of K_{push} Reduction Tech. (mm²)			0.012	NA	0.35‡	NA	NA	0.004
Total Area (mm²)			0.23	0.15	0.63†	0.013‡	0.0216‡	0.047†

*Estimated from out-of-band phase noise of PLL **Compared with the case S_t=0 (Gain=1) where the supply pushing of the oscillator is already suppressed
#Calculated value from the spur level † Power/area of the ADPLL ‡ Estimate from the chip micrograph
***Ripple frequency lower than the PLL bandwidth, supply pushing is calculated assuming 20dBc/decade suppression from the loop

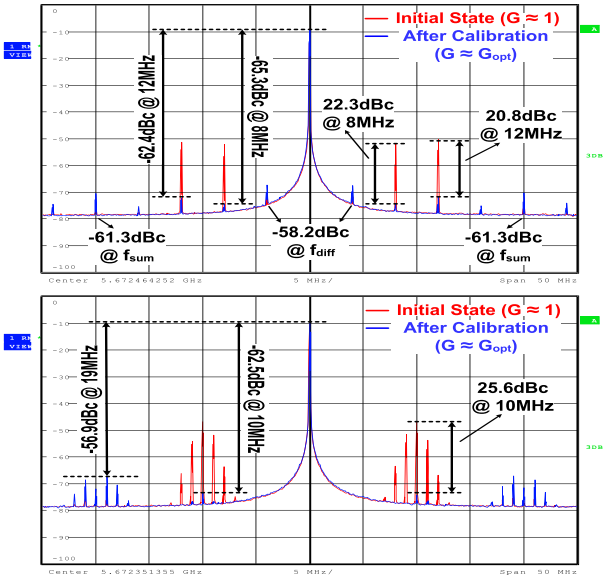

Fig. 17. Measured oscillator spectra before and after automatic calibration under two-tone (top) and frequency modulated (bottom) ripple.

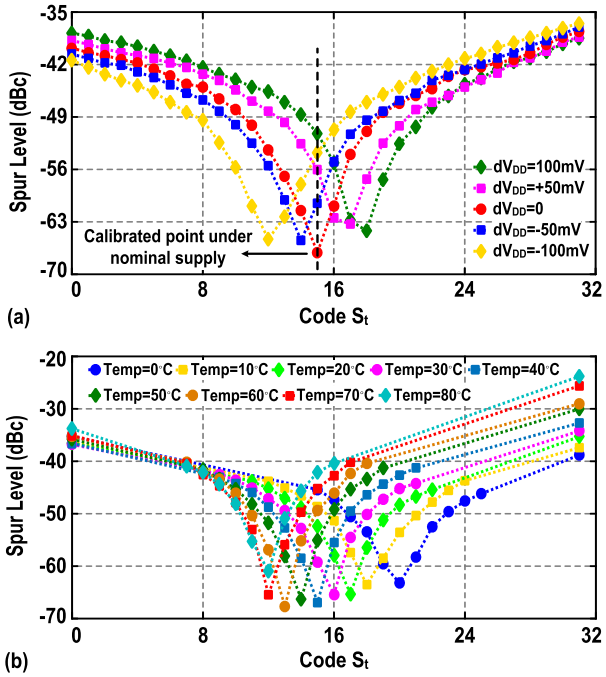

Fig. 18. Measured spur levels over the control code S_t under different (a) dc supply voltages and (b) temperatures.

frequencies of these two tones with a level of −61.3 dBc and −58.2 dBc, respectively, which are still far below the −50-dBc limitation of the IoT applications. Fig. 17 (bottom) compares the measured spectra before and after the automatic calibration when a 50-mV_{pp} 10-MHz frequency modulated (FM) ripple is applied to the supply. The modulation rate and maximum frequency deviation are both 1 MHz to clearly show the effect of modulation. The plot shows that the spurs around 10 MHz are reduced to ≤−62.5 dBc after the calibration, corresponding to a 25.6-dBc reduction at 10 MHz, while the spurs induced by nonlinearity around 20 MHz are ≤−56.9 dBc.

Fig. 18 shows the measured spur levels under a 50-mV_{pp} 5-MHz sinusoidal ripple at different dc supply voltages and temperatures. For the variation of the dc supply voltage, the optimal code varies by ∼ ±3 under ± 100-mV variation, and the spur level remains <−50 dBc without any re-calibrations. Due to a relatively low power consumption of the IoT system, the on-chip temperature variation is very slow [41]. As shown in Fig. 18(b), the optimal code only changes by ∼ ±1 under ±10 °C variation. Hence, the effect of temperature drift is slow enough to be compensated by intermittent re-calibrations.

TABLE II
COMPARISON WITH LDO DESIGNS

	This work	JSSC'10 [22]	CICC'11 [24]	JSSC'14 [6]	VLSI'17 [7]	JSSC'18 [42]
Tech. (nm)	40	130	180	180	40	65
V_{in} (LDO)/ V_{DD} (osc.) (V)	1.0	>1.15	1.8	1.8	1.1	1.2
V_{out} (LDO) (V)	NA	1	1.5	1.6	1	1
$V_{drop\text{-}out}$ (LDO)/ V_{ds} of M_0 (osc.) (V)	0.25	>0.15	0.3	0.2	0.1	0.2
PSR (dBc) @1MHz	<-55.9	-80	-50	-65	-60	-52
PSR (dBc) @10MHz	<-42.5	-60	-22	-42	-35	-37
Total Capacitance	8.6pF (on-chip)	4μF (off-chip)	125pF (on-chip)	128pF (on-chip)	104pF (on-chip)	260pF (on-chip)
Additional Current Consumption (mA)	0.2 +0.021#	0.05	0.3	0.08	0.275	0.1535
Additional Power Consumption (mW)	0.2 +0.021#	0.0575	0.54	0.144	0.3025	0.1842
Noise (LDO/RRB) @100kHz (nV/$\sqrt{Hz}$)	8**	NA	NA	270	274	NA
Total Area (mm²)	0.012	0.049	0.041	0.14*	0.008*	0.087

*100pF on-chip load capacitance not included **Value obtained from post-layout simulation
#0.2mA(mW) from RRB always exists during normal operation; 0.021mA(mW) is the average power consumption of the calibration loop, when conservatively assuming a calibration is done for every BLE packet (~400μs)

Table I summarizes the performance of the proposed technique and compares it to prior works. When compared to a state-of-the-art *LC* oscillator in [38], the proposed technique demonstrates $>10\times$ improvement of the supply pushing. In comparison with other supply pushing reduction techniques [8], [10], [13], [14], the proposed technique shows the lowest supply pushing, comparable or larger spur reduction, while the additional power is small. The proposed technique is also compared with state-of-the-art LDO designs in Table II. Though [22] achieves higher PSR with a lower power consumption, a large off-chip capacitor is used which is against the IoT miniaturization. Also, it lacks a reliable calibration which could lead to ∼20-dB PSR variation under process and temperature changes. In [24], a correlation-based calibration scheme is implemented, but non-ideal effects, such as an offset of the mixer lead to incorrect calibration results. Moreover, compared with other state-of-the-art LDOs with on-chip capacitors [6], [7], [24], [42], our work demonstrates one of the highest PSR at 10 MHz with less or comparable (extra) power. The total on-chip capacitance used in the proposed design is also the lowest, thus occupying the smallest area.

V. CONCLUSION

This paper presented a method to significantly reduce supply pushing in current-mode *LC* oscillators while consuming no extra voltage headroom. The proposed RRB generates an amplified supply ripple replica at the gate terminal of the oscillator's tail current source, in order to stabilize the tail current and oscillation amplitude under supply variations. The oscillation frequency is stabilized in turn, leading to <1-MHz/V supply pushing for supply ripples up to 12 MHz. To suppress the PN degradation due to the extra circuitry, implicit common-mode resonance is used in the resonant tank. A calibration loop with a simple and effective algorithm is also integrated on-chip, which effectively finds the optimum gain for the RRB. The operation of the loop is based on detecting and minimizing the variation of the oscillation amplitude. Hence, it is also effective when the ripple is simultaneously coupled through the supply and other parasitic paths.

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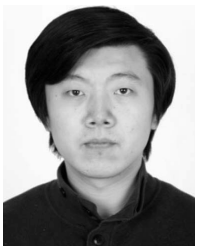

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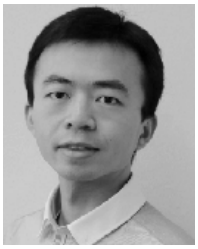

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