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A 15-Channel Digital Active Electrode System for Multi-Parameter Biopotential Measurement

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Abstract— This paper presents a digital active electrode (DAE) system for multi-parameter biopotential signal acquisition in portable and wearable devices. It is built around an IC that performs analog signal processing and digitization with the help of on-chip instrumentation amplifiers, a 12 bit ADC and a digital interface. Via a standard I^2C bus, up to 16 digital active electrodes (15-channels) can be connected to a commercially-available microcontroller, thus significantly reducing system complexity and cost. In addition, the DAE utilizes an innovative functionally DC-coupled amplifier to preserve input DC signal, while still achieving state-of-the-art performance: 60nV/sqrt(Hz) input-referred noise and ±350 mV electrode-offset tolerance. A common-mode feedforward (CMFF) scheme improves the CMRR of an AE pair from 40 dB to maximum 102 dB.

Index Terms—active electrode, biopotential measurement, digital interface, DC-coupled amplifier, common-mode feedforward.

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I. Introduction

Connected personal healthcare, or Telehealth, requires the use of smart miniature wearable devices that can collect physiological and environmental parameters during a user's daily routine, which can then be used to extract biomarkers and to determine personal trends for wellness, disease management, and independent living applications

(Fig. 1). IC technology can enable the development of such devices. However, achieving low power operation with medical grade signal quality is an on-going challenge [1]-[4].

To improve signal quality, active electrodes (AEs), i.e. the combination of electrodes with in-situ amplification, are widely used for wearable biopotential measurements [5]-[8]. Their low output impedance mitigates cable motion artifacts and interference pick-up, thereby facilitating the use of dry electrodes with fast set up time, improved user comfort, and long-term monitoring capability

However, the analog outputs of most state-of-the-art AE systems lead to several drawbacks [5]. Analog outputs are intrinsically sensitive to interference, so such AEs require power-hungry analog buffers to reliably drive biopotential signals over long measurement cables. In addition, a complete AE system requires an additional back-end (BE) readout circuit for analog signal processing and digitization of the analog outputs of multiple AEs [5][9]. A multi-channel AE system typically requires tens of wires connected to the BE readout circuit, which increases system bulk and leads to poor operational practice. Moreover, gain mismatch limits the CMRR of each pair of AEs, which means that common-mode interference may still significantly degrade the quality of the differentially sensed biopotential signals [10]. This problem is further exacerbated by the mismatch in each AE's electrode-tissue impedance (ETI), especially when dry electrodes are used.

This paper presents a digital active electrode (DAE) IC that integrates instrumentation amplifiers (IA), low-pass filters (LPF), a 12-bit SAR ADC and a digital interface on a single chip [11]. Up to 16 DAE ICs can be connected together in a daisy chain to a generic microcontroller (μC) via an I^2C bus, implementing a 15-channel system for multi-parameter biopotential measurement.

The proposed highly integrated DAE solves the aforementioned problems of analog-output AE systems. First, its digital outputs are robust to cable artifacts and mains interferences. Second, it performs on-chip analog signal processing and digitization, thus eliminating the back-end analog signal processor. Third, the use of an I^2C interface facilitates star or series connection between multiple DAEs, realizing a more flexible and compact multi-channel system. Last, but not least, the DAE system utilizes a common-mode feedforward (CMFF) technique to boost the CMRR of DAE pairs.

II. IC Architecture Overview

The DAE chip (Fig. 2) can simultaneously monitor biopotential signals (ExG channel), real and imaginary ETI signals (IMP and IMQ channels), DC and infra-low frequency (ILF) signals (DC channel). The signal chain starts with a chopper instrumentation amplifier (IA) with a voltage gain of 70, which improves the noise/power tradeoff of the following programmable gain amplifiers (PGA). The IA contains a ripple reduction loop (RRL) [12] and a DC-servo loop (DSL) [13] to attenuate chopper ripple and reject electrode offset, respectively. The IA's output is split into two channels for separate demodulation of the ETI and ExG signals.

The ETI channel consists of two chopper PGAs that demodulate the ETI signals with in-phase f_I (0^o) and quadrature-phase f_I (90^o) clocks, with respect to a square-wave current injected into the electrode. The DC outputs of IMP and IMQ then represent the real and imaginary components of the ETI respectively [5]. The new PGA of the ExG channel includes a notch filter to reject ETI signals at f_I (0^o). This prevents PGA's saturation due to the (large) ETI signals that may occur when dry electrodes are used.

The DC channel acquires the DC and ILF signals present at the output of the DSL. In the frequency domain, the normalized gain and phase of the DC channel complements that of the ExG channel, making it possible to reconstruct DC-coupled ExG signals by combining the outputs of the ExG and DC channels [15][16].

These four measurement channels are simultaneously sampled by f_{SH} and connected to an 8-to-1 analog multiplier, through which a back-end microcontroller (μC) selects the channels of interest. A 12-bit SAR ADC [14] digitizes the outputs of these selected channels at 250 S/s to 2 kS/s, and the digital outputs are transmitted to the back-end μC through the I^2C interface.

III. Analog Signal Processing

A. Functionally DC-Coupled Instrumentation Amplifier (IA)

Biopotential amplifiers should tolerate at least ±300 mV electrode offset [17]. For active electrodes, each IA should handle the same amount of offset with respective to the subject bias voltage. Prior IAs suffer from the tradeoff between electrode offset, input impedance noise and power [18]-[20]. To tolerate large electrode offset, the gain of a true DC-coupled amplifier will be reduced by the need to avoid clipping [18]. Therefore, a high resolution ADC will be required to digitize the small (μV) biopotential signals superimposed on a much larger (mV) electrode offset, leading to high power dissipation on each channel. In contrast, AC-coupled amplifiers, implemented with passive coupling capacitors, enable low-power rail-to-rail offset rejection [13][19][20]. But this comes at the cost of filtering out the DC and infra-low frequency (ILF) signals. Capacitively-coupled chopper IAs mitigate 1/*f* noise by chopping the input signal before the coupling capacitor [21][22], but their input-impedance is limited by switched-capacitor resistance. AC-coupled IAs with

voltage-to-current DC-servo loops solve this problem [15][23]. However, these IAs only compensate for a few tens of millivolts of electrode offset, limited either by noise or by the maximum current provided from the feedback loop.

This paper presents a functionally DC-coupled chopper amplifier with voltage-to-voltage feedback (Fig. 3) to facilitate (large) electrode offsets tolerance, while still maximizing the IA's performance tradeoff. The core IA is implemented with a current balancing IA [23], chopped at 4k Hz to suppress its flicker noise. This IA architecture provides high input impedance (100 MΩ at 50 Hz) and wide input CM range (0.5 V-1.2 V), making the IA robust to increased ETI mismatch and DC polarization due to dry electrode interface. The DC servo loop (DSL) consists of a g_m-C integrator that monitors the output offset and then cancels it by driving the core IA's inverting input. As a result, the IA can reject up to ±350 mV of electrode offset, which is determined by the amplifier's input CM range and noise specification.

An interesting feature of this IA is the preservation of the DC and ILF information, available at the output of the DSL. The IA's normalized AC and DC outputs have complementary gain and phase characteristic (Fig. 4), so these two outputs can be combined to implement a functionally DC-coupled IA. It has the same transfer function as a true DC-coupled IA, but with much wider DC dynamic range (±350 mV) in conjunction with high AC gain (>40 dB). The wide DC dynamic range mitigates electrode offset from dry electrodes, while the high AC gain relaxes the requirement of ADC resolution.

The DSL utilizes a weak transconductance (g_{m2}=3 μS) [24] and an external capacitor (C_{ext}=1 μF) for a low cutoff frequency (<0.5 Hz). In addition, C_{ext} reduces the impedance at input chopping node, significantly reducing the $1/f^2$ voltage noise contribution from IA's

input current noise [25]. To suppress the 1/*f* noise of the DSL and the RRL, both are chopped and run in the background during the operation of the IA.

The thermal noise PSD of the core IA, the RRL and the DSL, respectively, is given by

$$\overline{V_{n,IA}^2} = \frac{\overline{V_{n,\text{core}IA}^2}}{\left(1 - \frac{C_s g_{m1} R_o}{C_{\text{int}}}\right)^2}$$

$$\overline{V_{n,RRL}^2} = \left(\overline{V_{n,gm1}^2} + \frac{\overline{I_{n,CB}^2}}{s^2 C_{\text{int}}^2}\right) \cdot g_{m1}^2 R_i^2$$

$$\overline{V_{n,DSL}^2} = \overline{V_{n,gm2}^2} \cdot \frac{g_{gm2}^2}{s^2 C_{ext}^2}$$

where $V_{n,IA}$, $V_{n,gm1}$ and $V_{n,gm2}$ are the input referred noise of the core IA, transconductance g_{m1} and g_{m2}, respectively, $I_{n,CB}$ is input current noise of the current buffer, R_i and R_o are input and output resistors that determine voltage gain of the core amplifier. The total input referred noise of an AE is dominant by the core IA, and large integrator capacitors (C_{int}=150 pF and C_{ext}=1 μF) are selected to minimize the noise contribution of the core IA, as well as the RRL and the DSL.

At start-up, the weak g_{m2} and the external C_{ext} can take tens of seconds to settle (Fig. 5). To overcome this, the IA includes a foreground fast-settling path, a stronger g_{m3} =100*g_{m2} in parallel can be temporarily switched on during the start-up, ensuring less than 1 second settling time before ExG acquisition starts.

B. Programmable Gain Amplifier (PGA)

In the ExG channel, the PGA (Fig. 6) provides a programmable gain that facilitates both EEG and ECG applications. Chopper modulation is used to mitigate the low-frequency 1/*f*

noise. A notch filter attenuates the ETI signal before it is filtered by the succeeding LPF. The operating principle is similar the RRL. Any in-phase ETI signal at the PGA's output is first converted to an AC current via C_s, which is then de-modulated back to DC and integrated on capacitor C_{int}. Transconductor g_{m4} up-converts the DC voltage to AC current and feeds it back to the core PGA. This feedback current compensates for the effective ETI current flowing through R_i. On the other hand, the ExG signal at the PGA's output is up-modulated to 1 kHz, and so is suppressed by C_{int}. The PGA can attenuate the output ETI signal by:

$$A_{V,PGA@1kHz} = \frac{G_{PGA}}{\frac{R_{out,CB} \cdot g_{m4} \cdot R_{o,PGA}}{Z_{s@1kHz}} + 1} \approx \frac{Z_{s@1kHz}}{R_{out,CB} \cdot g_{m4} \cdot R_{i,PGA}}$$

where Z_s=C_s//$R_{in,CB}$, $R_{in,CB}$ and $R_{out,CB}$ are the input and output DC resistance of the current buffer (CB), respectively. $R_{i,PGA}$ and $R_{o,PGA}$ are the PGA's internal feedback resistors. To maximize the attenuation, the PGA utilizes cascode current buffer and large input resistor ($R_{i,PGA}$=1MΩ) , Fig. 7 shows that the notch filter can reduce the output residual ETI signal (f_{ETI}=1kHz) by a factor of 40.

The core PGA utilizes the same IA architecture but with single-ended output. The coarse gain (2, 10 and 20) is selected via $R_{o,PGA}$, while R_{DAC} is implemented with a 12 bit programmable resistor array and can be trimmed with 50 Ω resolution (Fig. 8). To achieve this goal, very large CMOS switches (W/L=500/0.18) are used. R_{DAC} can be used to trim the channel gain of two DAEs, and so can improve the CMRR at analog outputs by about 5 dB. However, the CMRR improvement at digital outputs is obscured by the 12-bit ADC's quantization [11].

To extend the dynamic range of the ETI measurements, two identical PGAs are implemented in the IMP and IMQ channels. These PGAs do not have notch filters and only contain output choppers for ETI de-modulation purposes.

IV. Digital Interface

The built-in I^2C digital interface is responsible for data transmission to the digital back-end, as well as for clock generation of analog front-end (AFE). An I^2C interface was selected because it only requires 2 wires (SCL and SDA) for bi-directional communication (Fig. 9), and it is compatible with many commercially-available μCs. Although the SPI interface can operate at higher clock speeds (up to tens of MHz), it requires 4 wires (MISO, MOSI, clock, and a separate chip select (CS) wire to each IC), which would substantially increase the system's wiring bulk.

Compare to a standard I^2C interface, the proposed digital interface allows global read and write to all DAE sensors. A global write configures and synchronizes DAEs at each I^2C cycle. A global read enables DAEs sequentially transfer the data back to the master node with only one command. This avoids the need for the I^2C master to address each DAE individually, thus reducing the control overhead and the amount of data toggling on the bus.

Each individual DAE chip can be given a 4 bit address via four external pins, allowing up to 16 DAE to be connected to a single μC. In order to align the sampling moments of the individual DAE nodes, the back-end μC first sends a broadcast packet to all ICs (Fig. 10). This broadcast packet (I^2C address = 0) is identified by each DAE chip independent of its base address on the I^2C bus. The broadcast packets realign the sample-and-hold (f_{SH}) and ADC sampling clocks of each DAE and select two internal measurement channels of each

IC (via MUX1 and MUX2 in Fig. 2), whose outputs will be sent to the μC in the next I^2C cycle. In this way the back-end μC has full control of the DAE and can flexibly select any channel of interest. The broadcast packet is followed by configuration settings from μC, including various measurement modes of DAE. The digital outputs of each IC are then transmitted to the μC during the next I^2C cycle.

The internal clocks of each DAE IC are derived from a master clock of 1 MHz, which is generated by a ring-oscillator. The clock generation module outputs configurable 1 kHz to 32 kHz clock, synchronized at each broadcast packet, for internal use by the chopper amplifier, ADC, ETI measurement, and digital logic. For flexibility, both internal clocks and DAE's sample rate are programmable.

V. CMRR Enhancement

There are two different AE mismatch mechanisms that limit the CMRR between a pair of AEs. The first is ETI mismatch, which is more of a problem with dry electrodes. The amplifier should maintain very large input impedance over the entire ExG bandwidth to mitigate any voltage division. The second is AEs' gain mismatch. Compensating for these mismatches can significantly improve the CMRR and signal quality.

A further challenge for the AE system is the need to achieve a wide CM input dynamic range for each AE. This is because each DAE can be modeled as a single-ended amplifier with a large gain (up to 1400), followed by a 12b ADC. As a result, any CM aggressors (mains interference, motion artifacts) that appear at the DAE's input can easily distort or saturate its readout circuits, even in the absence of any gain mismatch between the DAEs.

Prior arts have employed feedback techniques for improved CMRR and input CM dynamic range. The driven-right-leg (DRL) approach [26] has been widely used to

compensate for CM interference by feeding the CM signal back to the subject though a bias electrode (or ground electrode). However, the resulting feedback loop may suffer from instability when the loop gain is out of control [26], especially when large and ill-defined ETI associated with the use of dry electrodes. Common-mode feedback (CMFB) circuits solve this problem by feeding the CM signal back to the amplifier's input, instead of subject [19]. However, analog CMFB circuit [19] relies heavily on large passive components, and results in poor flexibility and area-efficiency. Alternatively, a digitally-assisted CMFB scheme [11] extracts the CM signal of all DAEs in digital domain, converts it back to analog signal via a DAC, and then feeds it back to each DAE. However, the latency induced by the I^2C bus significantly shifts the phase of the analog CMFB signal relative to the input CM signal. This results in reduced phase margin and may destabilize the CMFB loop. To mitigate this stability problem, the bandwidth and gain of CMFB loop have to be sacrificed [11]. Another major issue of all feedback based approaches is their stability during the lead-off or poor contact. Any electrode off can cause the failure of the system since the common-mode extraction loop is broken [27].

The system utilizes a new CMFF scheme to improve the CMRR of two AEs, providing advantages over a previous CMFB scheme [11] in terms of CMRR bandwidth, power-efficiency and stability. Furthermore, this CMFF scheme is generic applicable to different types of AEs, such as inverting amplifiers [11] or non-inverting amplifier [5][9], while the CMFF proposed in [5] is only suitable for non-inverting amplifiers. The key idea of the CMFF scheme (Fig. 11) is buffering the input CM signal to all the DAEs before pre-amplification. As a result, the input CM signal is applied to the inverting inputs of all IAs via a buffer and their capacitively-coupled DSLs. Therefore, the input CM signal to a

pair of DAEs is compensated at their differential outputs, while their differential ExG amplification is not affected. This CMFF scheme has another major advantage, the buffered CMFF signal is applied to all DAEs via a very low impedance, which reduces the noise and interference pick-up from the environment, similar to the principle of active electrode.

On the detailed implementation (Fig. 11), the input CM signal can be acquired from an additional electrode, or simply from the reference electrode, or from any one of the signal electrodes. This flexible selection is based on the fact that DAEs' input CM signals picked up from the environment are quite similar. On extreme cases where the electrodes are placed far from each other, several local CMFF schemes can be used for different groups of DAEs.

Fig. 12 shows the measured differential-mode gain and common-mode gain of a pair of DAEs, with different series resistors R_e (0 Ω, 50 kΩ, and 800 kΩ) to mimic different electrode types and their impedance mismatch [28]. The CMFF scheme significantly boosts the CMRR of an AE pair from 40 dB to 102 dB (at 50 Hz). When R_e increases, the CMFF is less effective due to the attenuation of the CMFF signal and the larger mismatch between AEs.

VI. Measurement Summary

A. Measurement of Performance

The DAE (Fig. 13) was implemented in a standard TSMC 1P6M 0.18 μm CMOS process, and occupies an area of 15.8 mm^2. Each chip consumes 58 μA from a 1.8V core supply, excluding the I^2C interface.

Each ExG channel (consisting of two DAEs) shows a 60 nV/sqrt(Hz) input-referred noise density (Fig. 14), and stays constant over ±350 mV electrode offset with respect to subject bias (Fig. 15). Each DAE has an input current noise density of 20 fA/sqrt(Hz) at a chopping frequency of 4 kHz (Fig. 16), and an input impedance of 100 MΩ at 50 Hz (Fig. 17). Each DAE can measure up to 400 kΩ resistance at 1 kHz (at gain of 140), this was measured by connecting multiple test resistors to the input of a DAE.

Table I summarizes the IC's performance. The analog performance is competitive to the state-of-the-art, in terms of the DC-coupled feature, noise, electrode offset tolerance, input impedance and CMRR. Besides, the major merit of the proposed DAE system is the AE based architecture, a built-in digital interface, and inter-chip CMRR boosting scheme. These eliminate the need for additional analog back-end circuitry, and enables a cost-efficient manner for multi-channel ExG acquisition.

B. Multi-Parameter ExG Measurement

Simultaneous single-channel ECG, EMG and EOG measurements are performed to demonstrate the DAEs' capability of multi-parameter acquisition. Five (wet) electrodes are attached on a subject's chest and forehead (Fig. 1), and connected to DAE test boards via cables. For simplicity, the CMFF buffer's input is connected to the reference electrode in all measurements. Fig. 19 shows the several types of physiological signals acquired by the DAEs system, such as heartbeat (ECG), face muscle movement (EMG) and eyes blinking (EOG).

In order to measure EEG on scalp, five DAE test boards are connected in a daisy chain and attached to an EEG headset (Fig. 20). The bias-, reference-, and signal-electrodes are placed at O_1, O_2, C_z, P_z, C_3, and C_4, based on standard 10-20 electrode EEG system. Fig. 21

shows alpha activity around 12 Hz are clearly distinguished between periods of eyes open and eyes closed, when dry electrodes are used.

Fig. 22 shows 1-lead ECG measured on subject's wrists to demonstrate the benefit of the CMFF. After enabling the CMFF scheme, the 50 Hz interference picked up from the same environment is significantly reduced.

Fig. 23 shows the simultaneous recording of single-channel ECG and ETI (on the chest). When one electrode is disconnected from the subject, the ECG output is lost and the ETI output saturates. After re-connecting the electrode, both ECG and ETI recovers back. This indicates the ETI output can be also used for instant lead-on and lead-off detection.

VII. Conclusion

A digital-active-electrode (DAE) incorporates amplifiers, an ADC and a digital interface on a single-chip. The functionally DC-coupled IA maximizes performance tradeoffs (between noise, electrode offset tolerance, input impedance, and power) and enables the practical use of dry electrodes. The use of a CMFF scheme between DAEs ensures a maximum 102 dB CMRR at 50 Hz. The highly integrated DAE eliminates the need of a back-end analog signal processor, and enables multi-channel multi-parameter biopotential signal acquisition via I^2C bus. These features significantly reduce system complexity/cost and enable true modularity of the IC.

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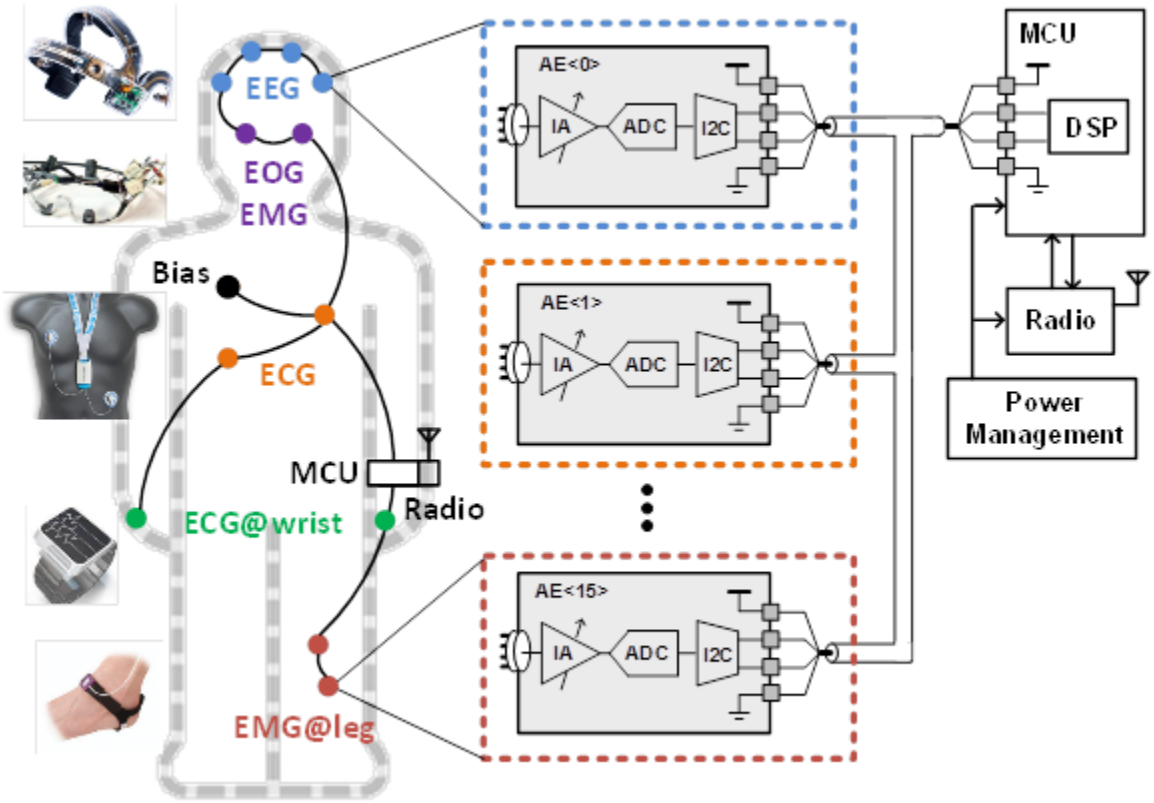


Fig. 1. Wearable digital active electrode (DAE) system for multi-parameter physiological measurement

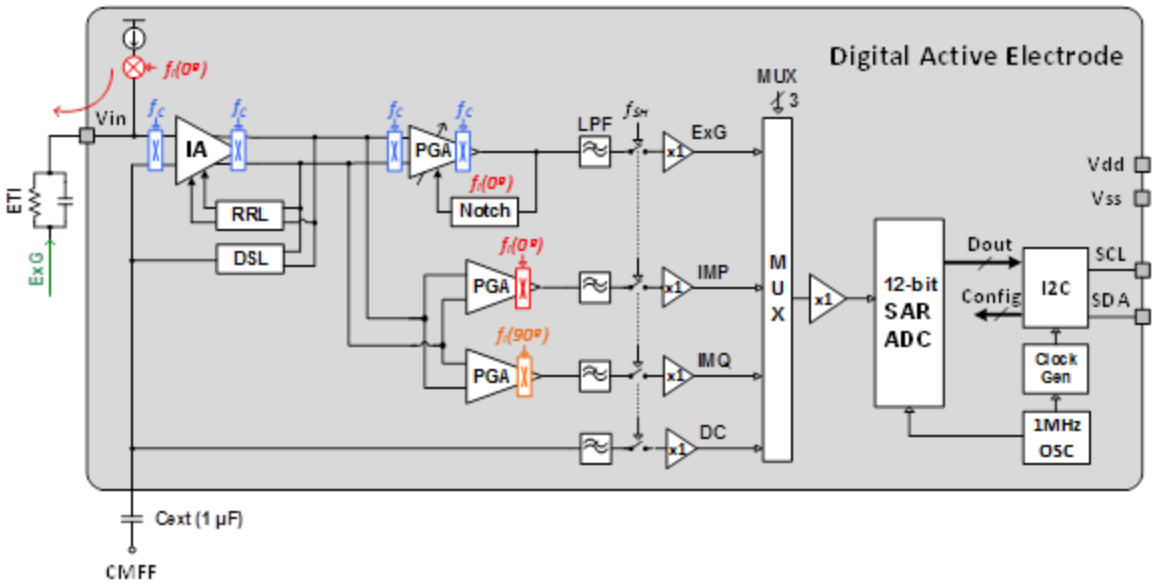


Fig. 2. Architecture of a digital active electrode IC

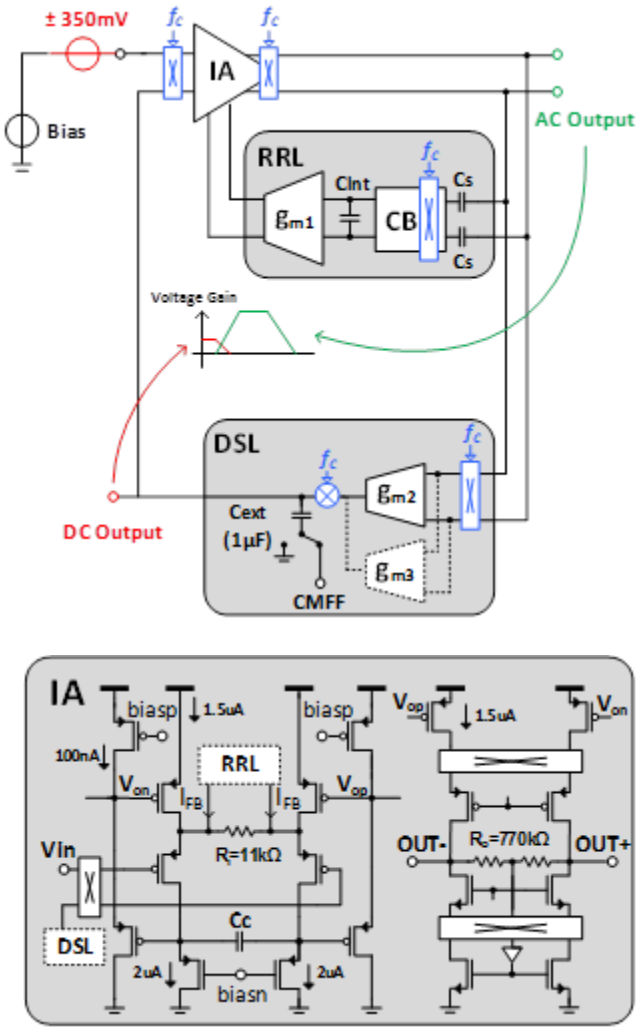


Fig. 3. Functionally DC-coupled instrumentation amplifier and schematic of core IA

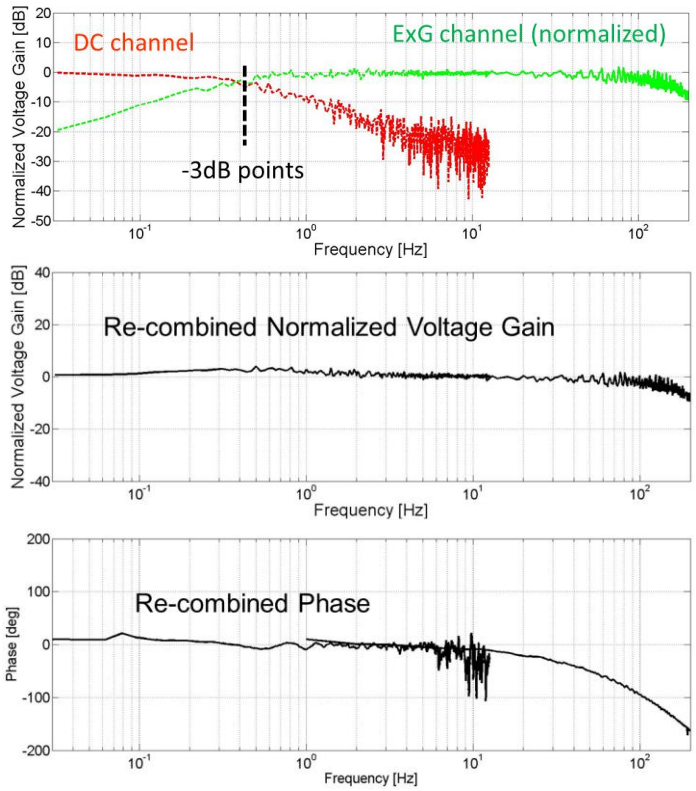


Fig. 4. Measured normalized gain of ExG and DC channel, and the re-combined gain and phase of the instrumentation amplifier (IA)

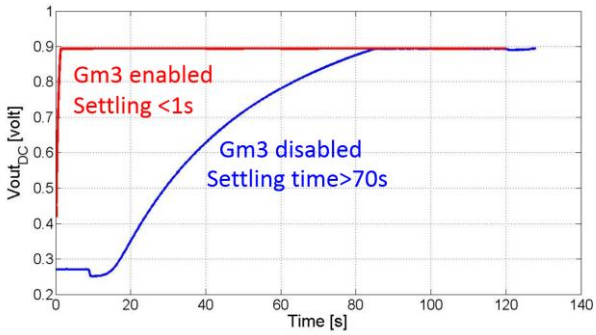


Fig. 5. Measured settling time with and without g_{m3}

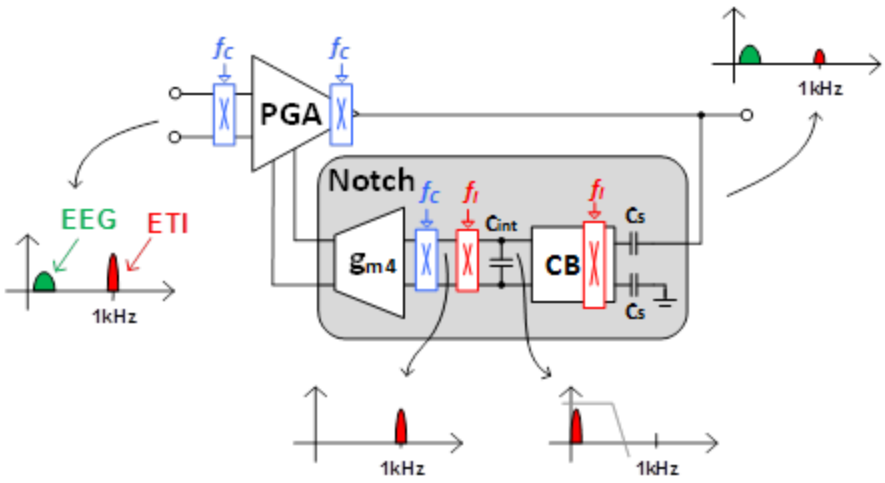


Fig. 6. PGA with notch filter for ETI signal rejection

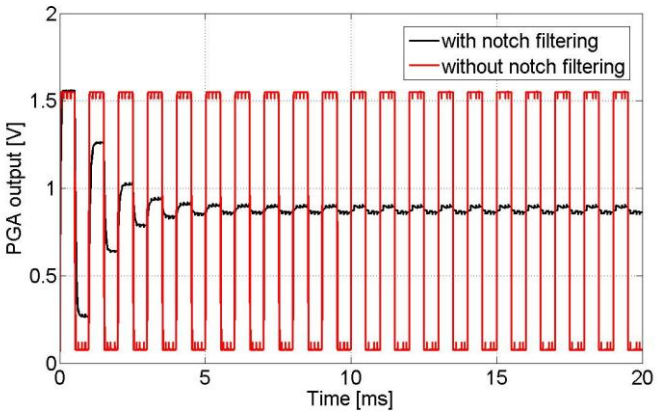


Fig. 7. Simulated residual ETI signal at PGA's output (G_{PGA}=5, V_{ETI_input} = 280mV_{pp}@1kHz)

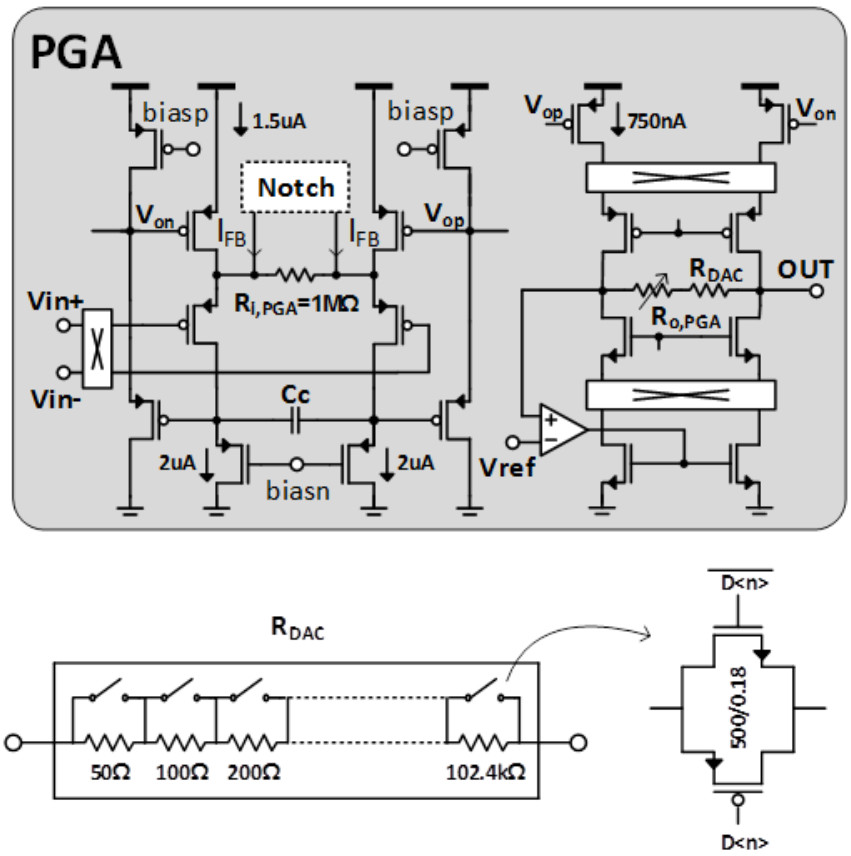


Fig. 8. Core PGA with programmable resistor load

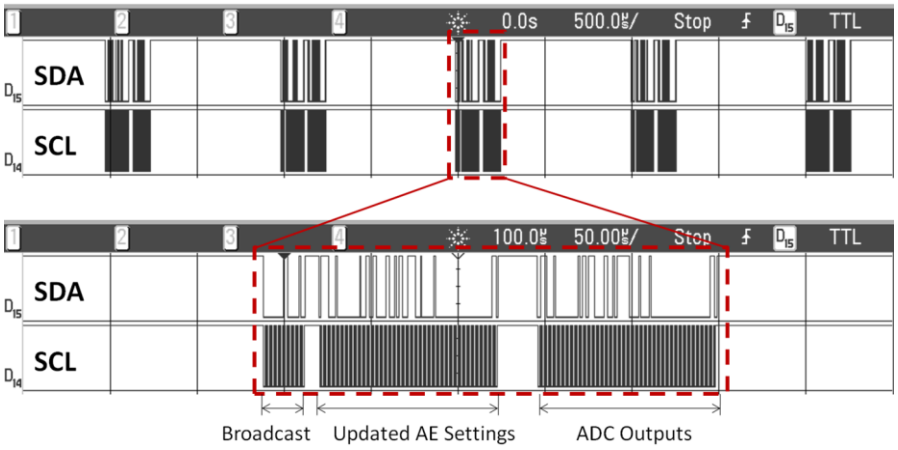


Fig. 9. Data (SDA) and clock (SCL) signal of the bus with 0.5ms I^2C interval

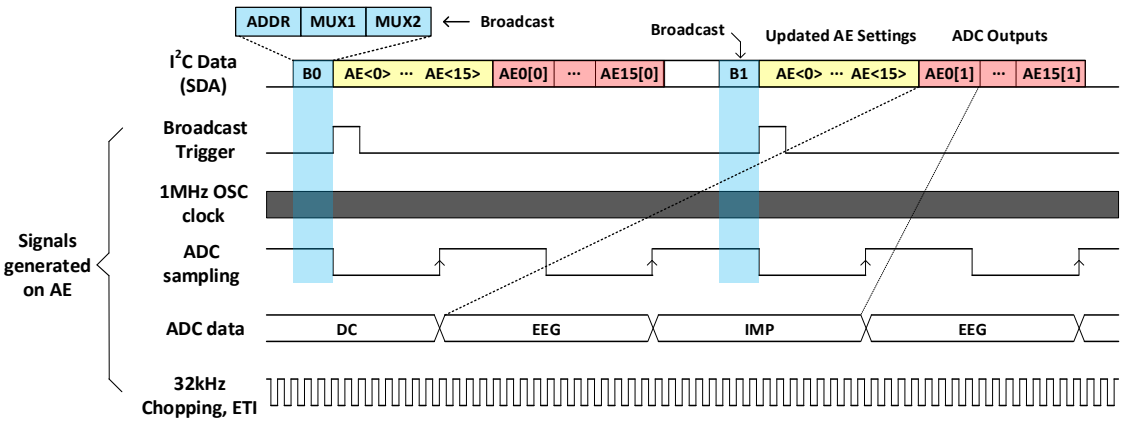


Fig. 10. Timing diagram of the I^2C interface and internal clocks on DAE

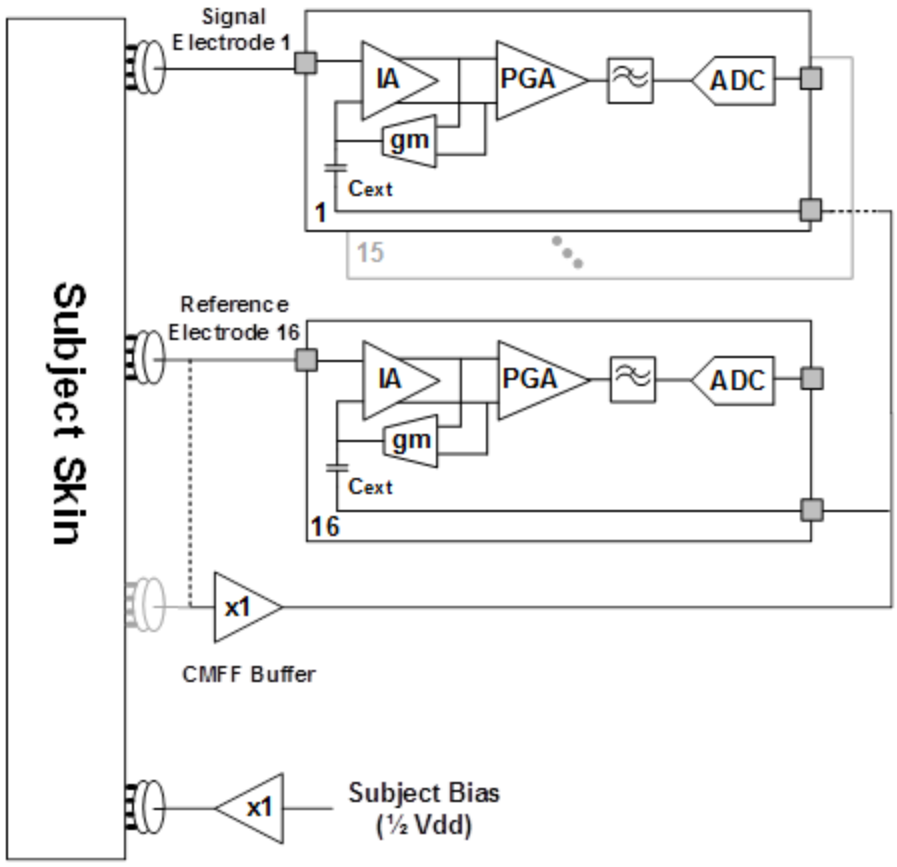


Fig. 11. CMRR improvement through the use of a CMFF electrode

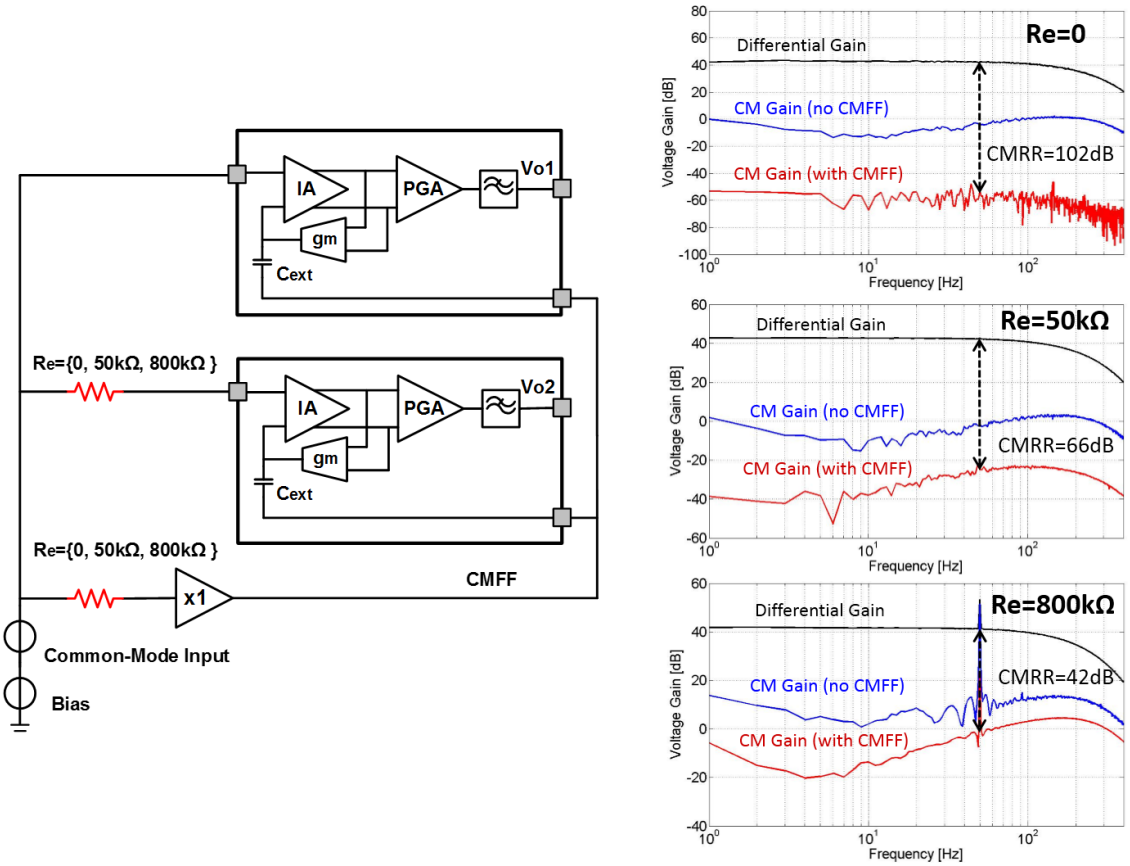


Fig. 12. Measured DM gain and CM gain (with and without CMFF) at various (electrode) impedance conditions

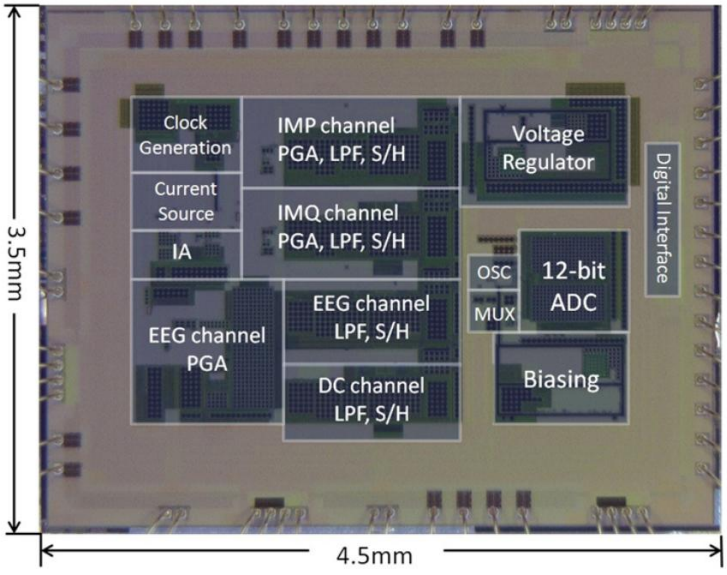


Fig. 13. Chip photograph

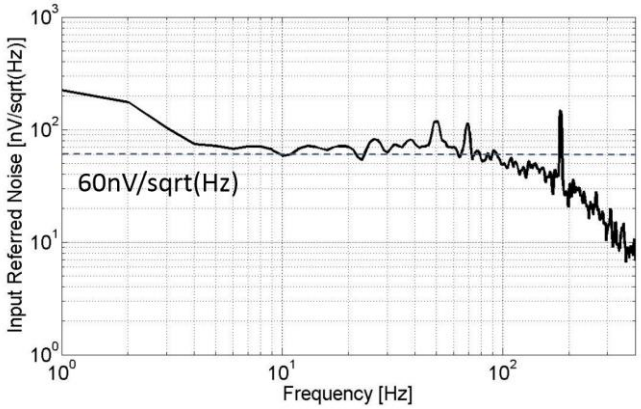


Fig. 14. Measured input-referred noise per ExG channel (G=700)

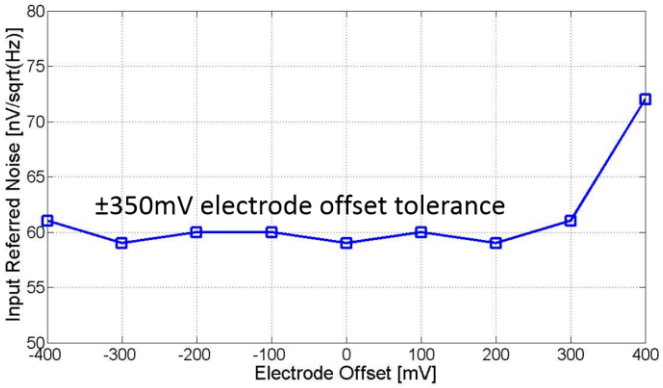


Fig. 15. Measured input noise per ExG channel versus electrode offset

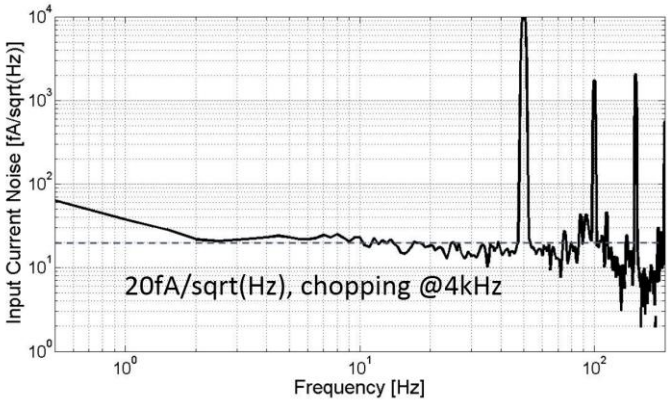


Fig. 16. Measured input current noise of a digital AE

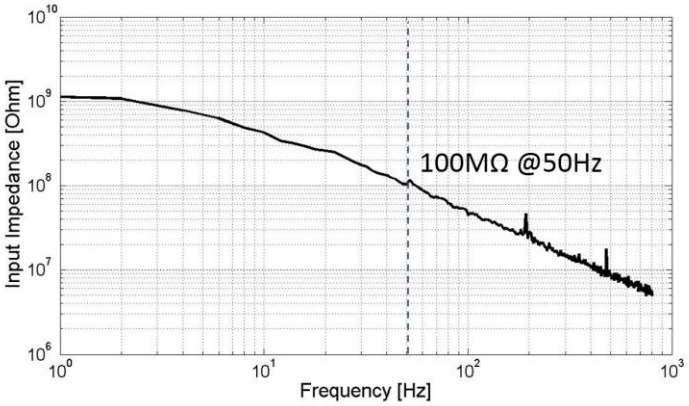


Fig. 17. Measured input-impedance of an digital AE

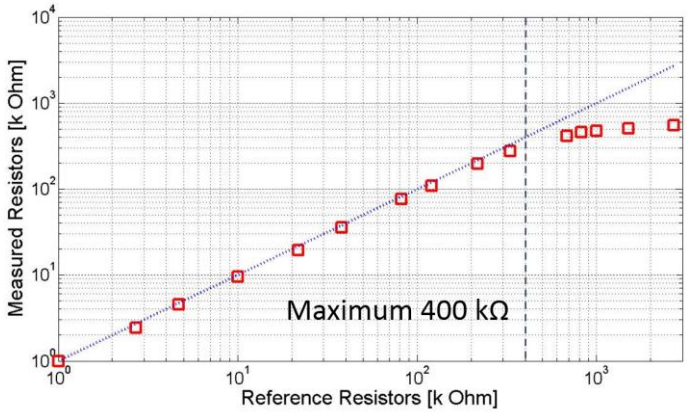


Fig. 18. Measured resistor and reference resistor showing the dynamic range of ETI

TABLE I
PERFORMANCE SUMMARY COMPARED WITH STATE-OF-THE-ART EEG SYSTEMS

	Parameters	[5]	[9]	[13]	[18]	This work
Analog Front-End	Supply	1.8 V	3.3 V	1 V	2.7-5.25 V	1.8 V
	Active Electrode	O	O	X	X	O
	DC-coupled IA	X	X	X	O	O
	Input Referred Noise	1.75 μVrms (0.5-100Hz)	0.9 μVrms (0.5-100Hz)	1.3 μVrms (0.5-100Hz)	0.7 μVrms (DC-131Hz)	0.65 μVrms (0.5-100Hz)
	Offset Tolerance	±250 mV	--	Rail-to-Rail	±250 mV	±350 mV
	Input Impedance	1.2 GΩ@20Hz	--	0.7 GΩ	1 GΩ	1 GΩ @1Hz , 100 MΩ@50Hz
	CMRR	84 dB	105 dB	60 dB	115 dB	102 dB
	Impedance Measurement	O	X	X	O	O
	ADC	12-bit SAR	--	12-bit SAR	24-bit SDM	12-bit SAR

	Supply Current per Channel	48 µA	330 µA	> 3.5 µA	250 µA	58 µA
System Integration	Digital Interface	--	--	--	SPI	I^2C
	Number of Channels	8	--	18	8	16
User Comfort	Dry Electrode Application	O	O	X	X	O

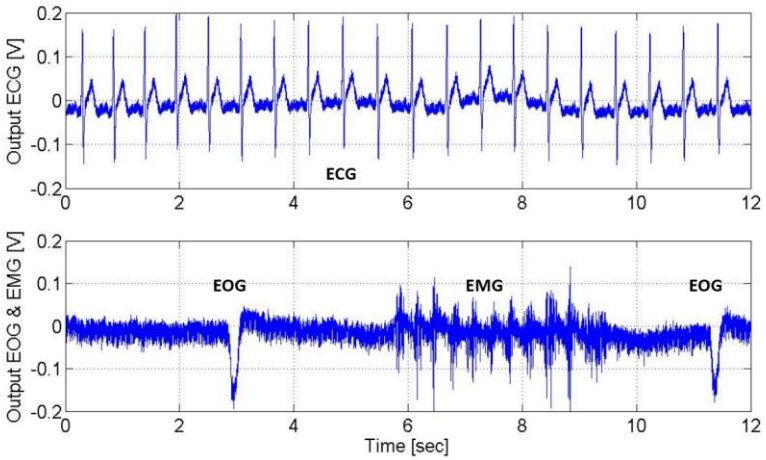


Fig. 19. Simultaneous ExG recording of the DAE system

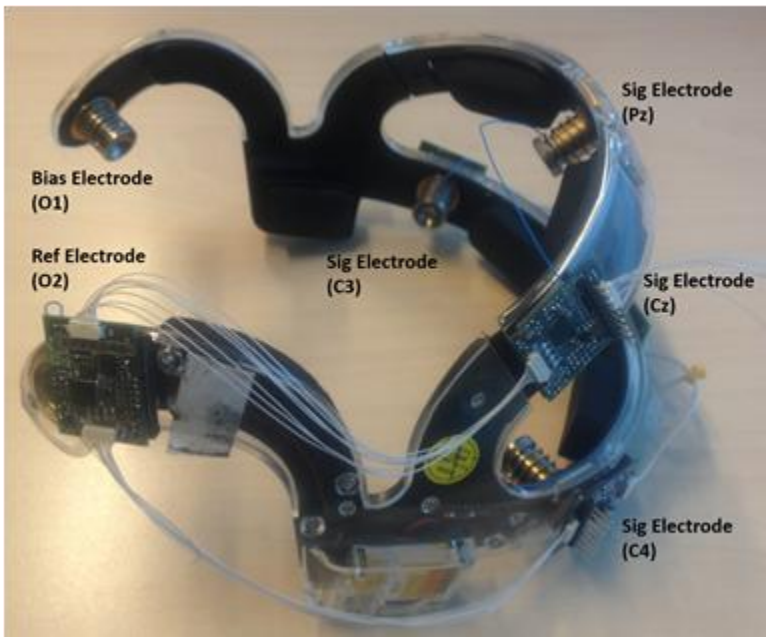


Fig. 20. 4-channel EEG headset with DAE test boards attached

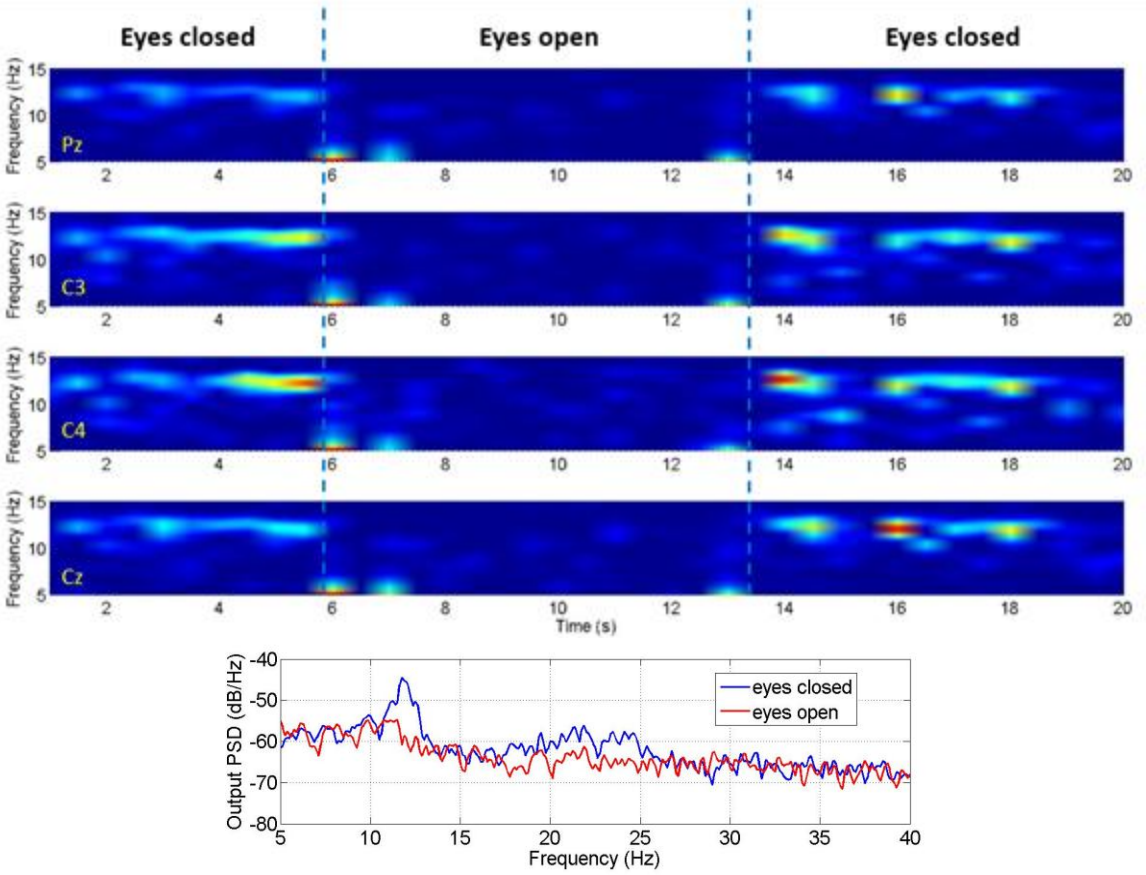


Fig. 21. 4-channel EEG recording with dry electrodes during eyes closed and eyes open,

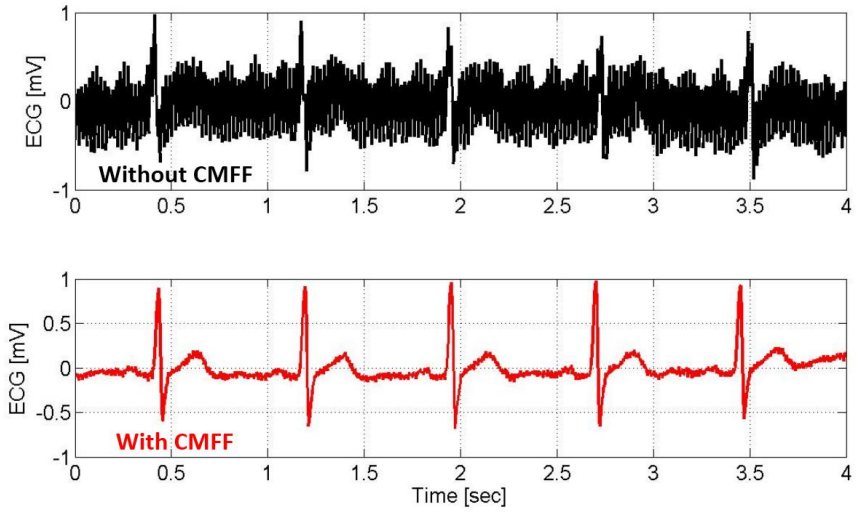


Fig. 22. 1-lead ECG recording with wet electrodes placed on wrists

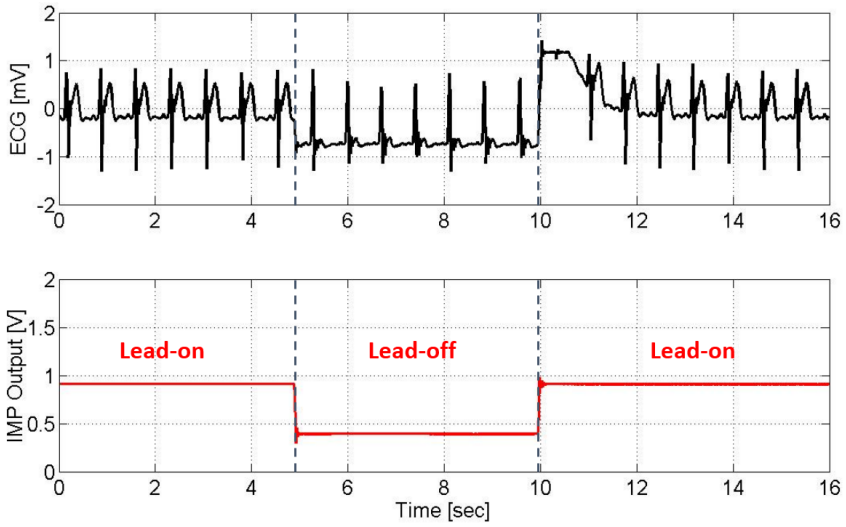
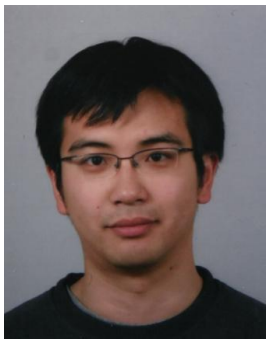


Fig. 23. Lead-off and lead-on detection through ETI output

Captions of the Figures and Tables



Jiawei Xu received the M.Sc. degree in Microelectronics from Delft University of Technology, The Netherlands, in 2006. Since then, he started as a researcher on analog IC design at imec/Holst Centre in Eindhoven, The Netherlands, where he worked on low-power readout circuits for smart sensors. In 2010, he joined Delft University of Technology as a PhD candidate in collaboration with imec, where he is currently working on low-power biopotential readout circuits. He is the recipient of IEEE Solid-State Circuits Society (SSCS) Predoctoral Achievement Award (2014), and imec Scientific Excellence Award (2014).

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After a PhD in Electrical Engineering (University of Leuven, 1992), Chris Van Hoof has held positions at imec at manager and director level in diverse technical fields (sensors and imagers, MEMS and autonomous microsystems, wireless sensors, body-area networks). He has published over 500 publications and given more than 50 keynote and invited talks. Chris Van Hoof is an imec Fellow and also full professor at the University of Leuven (KU Leuven).

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He is currently an Antoni van Leeuwenhoek Professor with the Faculty of Electrical Engineering, Computer Science and Mathematics, Delft University of Technology, which he joined in 1999. From 1989 to 1999, he was a Research Scientist with Philips Research Laboratories, Eindhoven, where he worked on interactive displays and digital recording systems. His current research interests include the design of precision analog circuitry, sigma-delta modulators, smart sensors, and sensor interfaces. This has led to four books, 18 patents and over 170 technical papers.

Kofi Makinwa is on the Program Committees of the European Solid-State Circuits Conference (ESSCIRC) and the Advances in Analog Circuit Design (AACD) Workshop. From 2006 and 2012, he was on the Program Committee of the International Solid-State Circuits Conference (ISSCC). He has been a Guest Editor of the Journal of Solid-State Circuits (JSSC) and a Distinguished Lecturer of the IEEE Solid-State Circuits Society (2008 to 2011). For his doctoral research, he was awarded the 2005 Simon Stevin Gezel Award from the Dutch Technology Foundation. He is also a co-recipient of several best paper awards: from the JSSC, ISSCC, ESSCIRC and Transducers, among others. He is an alumnus of the Young Academy of the Royal Netherlands Academy of Arts and Sciences and an Elected Member of the IEEE Solid-State Circuits Society AdCom, the society's governing board.

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Dr. Yazicioglu is the co-recipient of best (student) paper award in Int. Symp. On Circuits and Systems (ISCAS) 2013, Biomedical Circuits and System Conf. (BioCAS) 2011, Smart Systems Integration Conf. (SSI), 2008, and Sensors&Transducers Journal 2008. Dr. Yazicioglu is member of IEEE and serves in the technical program committees of European Solid State Circuits (ESSCIRC), International Solid State Circuit Conference (ISSCC) and Biomedical Circuits and Systems Conference (BioCAS). He was the co-chair of Biomedical Circuits and Systems Conference (BioCAS) 2013 in Rotterdam.