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# A 3ppm 1.5x0.8mm$^2$ 1.0µA 32.768kHz MEMS-based Oscillator

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***Abstract*—This paper describes the first precision 32kHz low-power MEMS-based oscillator in production. The primary goal is to provide a small form-factor oscillator (1.5 x 0.8 mm$^2$) for use as a crystal replacement in space-constrained mobile devices. The oscillator generates an output frequency of 32.768kHz and its binary divisors down to 1Hz. The frequency stability over the industrial temperature range (-40°C to 85°C) is ±100ppm as an oscillator (XO) or ±3ppm with optional calibration as a temperature compensated oscillator (TCXO). Supply currents are 0.9µA for the XO and 1.0µA for the TCXO at supply voltages from 1.4V to 4.5V. The MEMS resonator is a capacitively-transduced tuning fork at 524kHz. The circuitry is fabricated in 180-nm CMOS and includes low power sustaining circuit, fractional-N PLL, temperature sensor, digital control, and low swing driver.**

**Key words: real time clock, 32kHz Oscillator, 32kHz XO and TCXO, Low power design.**

## I. Introduction

Timekeeping and low power functions are commonly maintained by low-frequency oscillators, historically 32.768kHz ($2^{15}$ Hz). Applications include timing, smart metering, power conservative clocking, and sensor interfaces. In mobile and other battery powered devices, 32kHz oscillators are also employed in duty-cycling high power circuitry to prolong battery life. Key specifications for this clock are frequency accuracy, PCB area and power consumption.

Generally moderate precision applications use quartz tuning fork crystals (X), or oscillators (XO) [1], while high precision applications use temperature compensated tuning fork oscillators (TCXO). For timekeeping application, 32kHz quartz tuning fork crystals and oscillators are the most common [2]. They have a room-temperature accuracy of ±20ppm and show a downward parabolic frequency curve of ~0.035ppm/$C^2$, which causes a frequency error of about -150ppm at low and high temperature extremes [3][4]. Smart metering and other precision applications require more accurate reference clock which can be targeted by a temperature compensated tuning fork crystals trimmed to maintain ±5ppm accuracy over temperature [5-7]. Tuning fork oscillators are available in 3.2x1.5$mm^2$ surface mount ceramic packages, while TCXOs are larger, commonly constructed with tuning fork crystals embedded in leaded plastic packages. Figure 1 shows the size reduction of 32kHz quartz oscillators over the past three decades [8]. Their rate of size reduction is likely slowing due to scaling limitations and packaging/assembling difficulties [9]. However, the growth in portable devices is increasing the demand for smaller footprint clock references. .

Power consumption is commonly specified as ~1uA supply current across voltages from 1.5V to 5V. In applications with small batteries, such as wrist watches, the current consumption can be as low as ~0.2µA, and in TCXOs the consumption is commonly ~3µA. .

In the past decade, several high frequency MEMS-based oscillators (both XOs and TCXOs) have been introduced [10]. They have been shown to match or outperform their quartz crystal counterparts. This has been enabled by the development of long-term stable MEMS resonators and temperature compensation circuit architectures [11]. Low frequency MEMS oscillators have been shown in academic work for two decades but none have been commercially introduced [12][13].

This paper describes the smallest production 32kHz XO and TCXO [14]. The XO combines a temperature stable MEMS resonator with sustaining amplifier and fractional-N PLL to calibrate the output frequency over production tolerances, when configured and calibrated as a TCXO, a temperature-to-digital converter (TDC) adjusts the frac-N to compensate frequency over temperature. The oscillator can be configured as a ±100ppm XO or with temperature compensation as a ±3ppm TCXO. Package size is 1.5x0.8mm$^2$. Supply current is 0.9µA for the XO and 1.0µA for the TCXO at supply voltages from 1.4V to 4.5V. .

Section II describes the architecture. Details of the circuit design of each block in this system, including the description of the key techniques to improve their performance are presented in Section III. Measured results from the described oscillator are shown in Section IV followed by conclusions in Section V. .

## II. System Level Design

The design of a sub-µA MEMS-based oscillator presents two primary challenges: (a) initial frequency offset due to process variations in the fabrication of the MEMS resonator, and (b) temperature sensitivity of the resonator. As shown in Fig. 2, the resonator employed in this work has a nominal frequency of 524kHz that varies up to 2% over production tolerances and frequency stability of ±100ppm over a -40°C to 85°C temperature range. The initial frequency offset must be corrected, while the frequency stability is sufficient for XO operation. For TCXO operation the temperature sensitivity or the resonator must be compensated. Since the initial frequency offset is too large to be corrected by pulling the resonator, a delta-sigma fractional-N phase locked loop is employed, as shown in Fig. 2. .

The MEMS sustaining amplifier provides a 524kHz reference clock. This reference is divided to 32.768kHz using a multi-modulus divider controlled by a digital delta-sigma modulator and fed

to an integer-N PLL as shown in Fig. 2. In XO mode, the target frequency of 32.768kHz is achieved by appropriately setting the fractional value of the digital delta-sigma modulator at factory calibration. In TCXO mode, the value of the modulator is continuously varied to compensate for temperature. Temperature calibration data is obtained in factory measurements. The integer-N PLL filters the quantization noise from the digital delta-sigma modulator. In a low-power XO mode, current consumption can be further reduced by bypassing the integer-N PLL. This delivers a high jitter clock, but for applications that only count time the noise is negligible. A final programmable divider can optionally reduce the frequency in powers of two to 1Hz.

## III. Circuit Level Implementation

### A. MEMS Resonator and Sustaining Oscillator

The reference clock for this system is generated from a 524kHz silicon MEMS resonator. The resonator is an H-style capacitively-transduced tuning-fork, shown in Fig. 3(a), with a nominal quality factor of 52,000. When a bias voltage of 2.4V is applied between the tuning fork tines and the drive/sense electrodes shown in Fig. 3(b), the resonator presents an effective impedance between the drive and sense electrodes that is well-modeled as a series connection of a 70aF capacitance ($C_M$), a 1.4 kH inductance ($L_M$), and a 90 kΩ resistor ($R_M$), as shown in Fig. 3(c) [16]. The frequency variation of this resonator is less than ±100ppm over the temperature range -40°C to +85°C, which is 20x less variation than earlier commercial MEMS resonators [16] and less than earlier temperature-compensated MEMS resonators [17-19].

The oscillator circuit that drives the MEMS resonator is shown in Fig. 4. The architecture is a modified version of previously published Pierce configurations [20][21]. A current-starved

inverter with gain control provides transconductance gain ($G_M$) to initiate and sustain oscillation. This element is connected to the MEMS resonator via on-chip coupling capacitors, $C_{Drive}$ and $C_{Sense}$, which allow the DC biases of the resonator drive and sense terminals to be set by on-chip resistors $R_G$ to ground. This guarantees that the effective MEMS bias voltage is determined by the voltage applied to the tuning fork tines and is not influenced by the $G_M$ stage's DC operating point. Resistors $R_G$, together with the capacitive networks at the oscillator terminals, form high pass filters with corner frequencies well below the oscillation frequency. Before reaching the resonator, the AC output of the $G_M$ stage is attenuated by the capacitive divider between $C_{Drive}$ and $C_P$, where $C_P$ is the parasitic capacitance on the resonator drive electrode. A trimmable $C_{Drive}$ allows for adjustment of this capacitive divider, thereby enabling the power delivered to the resonator to be trimmed. While this divider might appear to lower the oscillator's loop gain, this effect is largely compensated by the gain of the $G_M$ stage, $G_M.(1/C_{Drive} + 1/C_P)$, which is inversely proportional to the series connection of $C_{Drive}$ and $C_P$ and therefore increases as the attenuation increase.

An automatic gain control circuit (AGC) controls the bias current of the $G_M$ stage in order to maintain fixed AC voltage amplitude at the $G_M$ stage's output. A simplified diagram of the AGC is shown in Fig. 5. As described in [21], the nonlinear characteristics of device $M_{AGC}$ ensure that an increase in the amplitude of the AC waveform at $G_{MOut}$ results in a decrease in the DC voltage at the gate of $M_{AGC}$. A filtered version of this gate voltage is used to generate the bias current for the $G_M$ stage, thereby providing negative feedback to control the amplitude of the system's oscillations. Resistive elements $R_B$ in the $G_M$ and AGC stages are implemented using sub-threshold MOS devices biased in the linear region. Extensive use of AC coupling makes the oscillator insensitive to the dynamic offset effects that can be produced by the nonlinear behavior

of these sub-threshold MOS devices [22], even when signal swings exceed several thermal voltages. An AC-coupled level shifter is used to transform the small-amplitude sine wave at $G_{MOut}$ into a rail-to-rail square wave, thereby providing a 524 kHz digital reference clock. The resonator's motional resistance, $R_M$, is inversely proportional to the square of the resonator's bias voltage ($R_M \propto \frac{1}{V_B^2}$), and the transconductance required to sustain oscillations ($G_{M,MIN}$) is proportional to $R_M$:

$$G_{M,MIN} = R_M \omega_0^2 \frac{(C_1C_2+C_2C_3+C_1C_3)^2}{C_1C_2}$$

Where $\omega_0$ is the resonator's resonant frequency, and $C_1$, $C_2$, $C_3$ represent the capacitance from resonator sense electrode to ground, from resonator drive electrode to ground, and from resonator drive electrode to sense electrode, respectively [20]. As a result, increasing resonator bias voltage generally results in lower oscillator power consumption. To this end, the MEMS bias voltage is supplied from a programmable charge pump that can output integer multiples of a 1.2V reference voltage, up to 3.6V. However, resonator mechanical displacement also increases with bias voltage, and this displacement must be limited to avoid unwanted nonlinear effects [23]. The sensitivity of resonant frequency to variation in the bias voltage also increases with bias voltage. Consequently, although the oscillator power consumption is minimized when the charge pump output is 3.6V, it was experimentally determined that 2.4V bias provided better system-level performance for TCXO applications. Under this condition, the total current consumption of the MEMS sustaining circuit and charge pump is 240nA.

### B. Fractional-N PLL

Figure 6 shows the detailed block diagram of the fractional-N PLL and temperature compensation path. This fractional-N PLL is a variant of the classical delta-sigma fractional-N

PLL [24]. Two specific differences can be noted. First, the multi-modulus frequency division (under the control of a digital delta-sigma modulator) is performed not in the PLL feedback path but in a pre-driver in the reference path. Second, the output is tapped from the integer divider in the feedback path rather than from the VCO itself. .

Performing the fractional division in the reference path means that the pre-divider output is 32.768kHz. This allows disabling and bypassing the PLL in the XO mode in order to reduce current consumption below 1μA. Although the output of this pre-divider is already at the target frequency, it carries the quantization noise from ΔΣ modulator. This introduces output jitter, but it is not detrimental in applications that count pulses, e.g. 32,768 pulses to define one second. In applications where the jitter needs to be low the integer-N PLL filters this noise. A $2^{nd}$ order digital delta-sigma modulator provides optimum performance to power: a $1^{st}$ order modulator would exhibit strong limit cycle behavior, whereas a $3^{rd}$ order modulator would consume unnecessary current. The power consumption of the digital delta-sigma modulator is kept low by adopting a low supply voltage that is sufficient for reliable operation. Section III. E describes the voltage regulators. .

As shown in Fig. 6, the integer-N PLL is a standard charge-pump based type II PLL [25] optimized for low power consumption. It has a phase frequency detector (PFD) and a 16nA charge pump. The loop filter sets the loop bandwidth to 1kHz to minimize the overall noise from the VCO and digital ΔΣ modulator. The VCO is a current-starved ring oscillator with a nominal frequency of 262kHz. The total current consumption of the PLL including pre-divider is 290nA.

### C. Temperature to Digital Converter (TDC)

To achieve TCXO stability, a BJT-based temperature sensor is combined into a switched capacitor delta-sigma modular as shown in Fig. 7(a). BJT-based sensors are known to achieve the best combination of accuracy and energy efficiency [26]. It is also known that switched capacitor delta-sigma modulators offer high resolution at low power, particularly for low bandwidth applications such as tracking temperature changes. .

The BJT-based sensor's block diagram is shown in Fig. 7(a). As shown, two identical NPNs are biased at a collector current ratio of $p = 6$. The resulting base-emitter voltage, $V_{BE}$, has a negative temperature coefficient of approximately -2mV/°C. The difference between their base-emitter voltages is proportional-to-absolute temperature (PTAT), i.e. $\Delta V_{BE} = V_{BE2}-V_{BE1} = (kT/q)\cdot\ln(p)$ where k is Boltzmann constant, q is charge, and T is the absolute temperature, with unit of Kelvin. Rather than the more commonly used PNPs, NPNs were used in this design because of their higher current gain [27]. The temperature to digital converter (TDC) generates a digital bit-stream, whose average value is proportional to $(\alpha\cdot\Delta V_{BE})/V_{BG}$, where $\alpha = 14$ and $V_{BG} = V_{BE1}+\alpha\cdot\Delta V_{BE}$ is a voltage with a slightly positive temperature dependence, which improves the sensor's overall linearity [28]. The TDC is based on a $2^{nd}$-order switched-capacitor (SC) $\Delta\Sigma$ modulator. As shown in Fig. 7(a), its main components are two SC integrators and a 1-bit quantizer. Both integrators are based on folded-cascode OTAs, with the first OTA gain-boosted to improve its DC gain. Depending on the quantizer's output ($bit_{out}$), the modulator's next input is either $-V_{BE1}$ ($bit_{out}=1$) or $\alpha.\Delta V_{BE}$ ($bit_{out}=0$) [28]. This charge-balancing scheme ensures that the average value of $bit_{out}$ is equal to the desired ratio $(\alpha\cdot\Delta V_{BE})/(V_{BE}+\alpha\cdot\Delta V_{BE})$. $\Delta V_{BE}$ is integrated over $\alpha$ clock cycles and then sampled exclusively [29]. This technique only have one unit sampling capacitor ($C_s$) which avoids the extra area and mismatch errors associated with implementing $\alpha$ with multiple sampling capacitors, and also ensures that the first integrator's

closed-loop gain is fixed, irrespective of the modulator's state. As shown, $-V_{BE}$ is integrated during a single clock cycle, while $\Delta V_{BE}$ is integrated over α clock cycles. In other words, each ΔΣ cycle would take either 1 or α clock cycles, when $bit_{out}$ is 1 or 0, respectively. Several dynamic techniques are used to improve the TDC's accuracy. The sensor front-end's current sources are dynamically matched to mitigate their mismatch, while the first integrator's offset and flicker noise are mitigated by employing correlated double sampling (CDS) [30]. To mitigate charge injection errors, the 1st integrator employs a fully differential structure using minimum size switches. Any residual offset is then removed by system-level chopping, at the expense of a doubled conversion time [31]. To provide a differential input to the first integrator, the positions of the current sources are swapped during the two phases of each ΔΣ clock cycle. This simultaneously averages out the mismatch between the two BJTs [28].

Applying dynamic element matching (DEM) technique to the front-end's current sources improves their matching, but since the modulator's input then changes over multiple ΔΣ clock cycles, it could also fold quantization-noise back into the signal band [32]. This could significantly impact the signal-to-noise ratio. Previous work mitigated this effect by randomization [33] or by the use of bitstream-controlled DEM [34]. We addressed this problem with the DEM principle illustrated in Fig. 7(b). Since a complete DEM cycle requires (ρ+1) clock cycles, it can be combined with the α clock cycles required to integrate $\Delta V_{BE}$. By choosing $\alpha = n.(\rho+1)$, where n=1,2,3,…, a full DEM cycle can be completed during exactly one ΔΣ cycle, thus avoiding any quantization-noise fold-back.

The total current consumption of the implemented TDC is 4.5μA operating at a 262kHz sampling clock. Of the total current consumption, 1.5μA is consumed by the front-end, 1.7μA is dissipated by the loop filter and 0.8μA is used by the decimation filter, the digital filter, and the

clock generator. System-level chopping requires two TDC conversions, which doubles the conversion time to 6ms at room temperature. The TDC achieves a resolution of 25mK (rms), which leads to a figure of merit (Energy/Conversion x Resolution$^2$) of 24pJ°C$^2$ [26]. This compares favorably with the state of the art [35]. .

To meet the 1µA total-current-consumption target, the TDC is duty-cycled to reduce its average current consumption. However, the use of duty-cycling leads to a trade-off between temperature tracking accuracy and power consumption. Applications require a frequency error of < 1ppm in the presence of temperature ramps of ±1°C/sec. To meet this, the TDC's update rate is set to 3 Samples/sec. This results in an average current of 105nA.

### D. Voltage Regulators

A significant fraction of the chip's total current consumption and area is dedicated to voltage regulation, which is important for three reasons. First, to meet the TCXO frequency stability specifications, the performance of the analog blocks must be preserved over a wide range of external supply voltages and supply ripple. In particular, the MEMS oscillation frequency is function of bias voltage and drive amplitude, so these must be regulated in the presence of supply variations or noise. Second, digital power consumption can be reduced by operating digital circuits at the minimum voltage required to meet all timing constraints. Third, some applications benefit from powering the 32kHz timing reference directly from an unregulated battery in order to reduce current consumption in standby mode. For these applications, a low power high voltage regulator has been included in the design to extend the supply range to 4.5V without requiring external components or high-voltage fabrication process options. Figure 8 shows a block diagram of the employed voltage regulation scheme. The components are

described in detail below.

*Bias Generation and Voltage Regulation for Analog Blocks*

To allow for operation down to external voltages of 1.2V in XO mode, a sub-1V bandgap reference based on the architecture proposed by Banba et al. is used [36]. This bandgap voltage serves as the reference for a programmable closed-loop master analog voltage regulator as shown in Fig. 8. The 1.2V output of this master regulator is replicated by open-loop slave stages, which provide stable independent power supplies for all remaining analog blocks on the chip. Separate power domains are important for isolating sensitive circuits from noisy ones (e.g. the highly duty-cycled TDC) and for reducing cross-talk between different clock domains. The open-loop slave architecture provides power savings compared to separate closed-loop regulators, since each slave stage maintains unconditional stability and consumes zero current. The bandgap reference and master/slave regulators consume 230nA and enable the system to achieve supply sensitivity less than ±0.25ppm/V.

*Voltage Regulator for Digital Block*

The digital regulator uses a replica biasing architecture to minimize digital power consumption while guaranteeing timing closure over process and temperature variations. The replica structure in Fig. 9 consists of a series stack of NMOS and PMOS which match the devices used in the digital standard cells. Driving a constant current $I_{set}$ into this series stack generates a voltage $VGS_{ref}$, which varies inversely with MOS process and temperature as shown in Fig. 9. Using $VGS_{ref}$ as the supply level for digital gates that match the replica transistors therefore guarantees that those gates have a minimum current drive capability of $I_{set}$. A programmable resistor $R_{set}$ is used to add margin $I_{set} \times R_{set}$ (maximum 100mV) to the digital supply to ensure this minimum current drive capability even in the presence of threshold mismatch or supply droop. This

master/slave architecture similar to that used in the analog regulators supplies the digital blocks with $VDD_{dig} \approx VGS_{ref} + I_{set} \times R_{set}$. This scheme guarantees the digital regulator's stability, even in the presence of the large supply current variations that result from duty-cycling the TDC and temperature compensation engine. .

*High Voltage Regulator* .

Operating directly from an unregulated 4.5V supply, such as a battery, requires special consideration to prevent over-voltage stress of the thick oxide devices in this 180-nm process, which have a maximum operating voltage of 3.63V. A simple means of providing over-voltage protection would be to add two diodes in series with supply $V_{Battery}$, thereby dropping the internal supply voltage ($VDD_{int}$) to $V_{Battery}$-$2V_{Diode}$, where $V_{Diode}$ is the voltage drop across one of the protection diodes. Unfortunately, this solution places severe limits on the *minimum* external supply voltage required to maintain $VDD_{int} > 1.2V$, especially considering that the voltage drop across these diodes can vary dramatically with process, temperature, and supply current. To solve this problem, a regulator in parallel with two series protection diodes is employed, as shown in Fig. 10. In this circuit, when $V_{Battery}$ is high, the two protection diodes conduct and $VDD_{int} = V_{Battery}-2V_{Diode}$. At intermediate voltages, the regulator partially bypasses the protection diodes and maintains $VDD_{int} = V_{REF}+V_{FB}$, where $V_{REF}$ is a 1.2V reference provided by internal regulators and $V_{FB}$ is the voltage drop across the feedback diodes biased with 8nA current shown in Fig. 10. When $V_{Battery}$ drops below $V_{REF}+V_{FB}$, the regulator simply acts as a switch shorting $VDD_{int}$ to $V_{Battery}$.

## E. Drivers

There are two options for the output driver: a rail-to-rail CMOS and a low swing driver. With a low-swing driver, the CVF current can be reduced by $V_{swing}/V_{DD}$. In most applications, the following block driven by this oscillator does not require full swing input. As shown in Fig. 11, as long as the output clock waveform crosses the two defined thresholds of $V_{top}$ and $V_{bottom}$ it is suitable for the application. As shown in Fig. 12, in this design the driver has two regulators which together control its output swing. CMOS transmission gates are used to alternate between independently programmable $Vref_{up}$ and $Vref_{dn}$ giving control on the swing of the output clock. Capacitive charge sharing generates fast output transitions followed by slow single pole settling from the regulators. The total power consumption of each regulator is 60nA. To further reduce the output driver power consumption, the output frequency can be divided down to 1Hz in powers of 2. Figure 13 demonstrates a quantitative comparison between the full and low-swing driver current consumption versus capacitor load. The external VDD is set to 1.8V, which limits the rail-to-rail driver to a 1.8V output swing. For the low-swing driver, the output swing is set to 0.6V. As shown, the low-swing driver reduces the total power consumption by 55% for a load capacitor of 15pF. .

## IV. Measurement Results

Figure 14(a) shows the 180-nm CMOS die with area of $1.2mm^2$, and MEMS die with area of $0.17mm^2$. On the CMOS chip, the PLL, TDC and OSC consume 0.3 $mm^2$ and the digital including 3rd order polynomial correction occupies 0.5 $mm^2$. The oscillator can be assembled in conventional wire-bonded plastic packages where the 524kHz MEMS resonator is attached and wire-bonded to a programmable MEMS oscillator system to fit in a $2x1.2mm^2$ QFN package. To reduce the size further, the MEMS resonator can be flipped-chip bonded to the CMOS die in a 1.55mmx0.85mm chip-scale package (CSP), as shown in Fig. 14(b). In this packaging, epoxy

under-fill is applied between two dies to fully insulate the MEMS-CMOS interconnections, leaving the complete package fully compatible with standard lead-free PCB assembly processes. With a 3.3V supply voltage, the measured average current of the chip is 1.0µA with 32kHz output under no external load condition. In the low power XO mode, with the PLL disabled, a current consumption reduces to 0.6µA. Figure 15 shows a break-down of the TCXO mode power consumption. SPICE-level simulation estimates that the oscillator (including charge pump) consumes 240nA, the PLL (including delta sigma modulator) consumes 290nA, and the temperature sensor (including temperature compensation engine) consumes 150nA. All the currents reported are with the internal supply voltages of the blocks set to 1.2V-1.4V. Figure 16 displays the transient current profile with a peak value of 5.5µA. The TDC conversion rate is set to 3 samples/sec. After each conversion, TDC and compensation engine sleep while a low power wake-up circuitry runs to turn on TDC every 330mS. In each conversion, it takes 1ms for the BJT core and modulator to initialize, 6ms for two back-to-back conversions at 25°C, and 2ms to evaluate the polynomial. Figure 17 shows the measured $VDD_{int}$ versus $V_{Battery}$ when high voltage regulator is enabled. As shown, with this regulator, the internal voltage safely lands between 1.5V and 3.63V when $V_{Battery}$ varies from between 1.5V to 4.5V. .

Shown in Fig. 18(a), measured frequency stability over temperature of -40°C to +85°C is better than ±100ppm for 28,000 XO devices. With only room temperature calibration, the initial accuracy of the XO devices is within ±3ppm. With temperature compensation enabled (TCXO mode), the measured frequency accuracy improved to ±3ppm for 28,000 TCXO devices as displayed in Fig. 18(b). These devices are trimmed individually at five temperature points on wafer level. The reader may wonder with individual trimming process all techniques such as DEM, CDS in temperature sensor were not necessary. However, these techniques are

implemented to reduce stress sensitivity. As a result, solder down shift is limited to be less than ±1.5ppm over temperature range of -40°C to 85°C. Figure 19 shows the temperature tracking performance of TCXO device: a temperature transient as fast as 1.5°C/sec is applied and measured normalized frequency error is plotted. An evident from the figure, temperature compensation with TDC conversion rate of 3Samples/sec is able to correct frequency changes over temperature to within ±3ppm. .

Noise performance of a 32kHz clock is critical when it is used in wake-up circuitry for phones. The overall noise performance applicable for this application is shown in Fig. 20 which demonstrates the wake-up time accuracy. It is the measured peak-to-peak long term jitter (LTJ) at stride of 2.5sec for 100 devices with a mean value of 0.7µsec. As shown, it is well below the target noise performance suited for this application. In low power mode where the PLL and TDC are powered down, LTJ is 3.6µsec. .

Table 1 summarizes the measured performance and compares it with existing quartz-based 32kHz XO and TCXO devices. As shown, the described 32kHz MEMS-based oscillator outperforms quartz crystal-based solutions in several aspects but most notably in current consumption (at least 2x less) and package area (at least 6x smaller package) while demonstrating ±3ppm frequency stability over the industrial temperature range.

## IV. Conclusion

This paper presents the first 32kHz MEMS-based oscillator. It achieves TCXO frequency stability of ±3ppm, a footprint of 1.5x0.8mm$^2$, and 1µA current consumption. Frequency stability performance and low power consumption are achieved by combining a low temperature sensitivity MEMS resonator with an accurate temperature-to-digital converter and a low power

fractional-N PLL, and by employing techniques such as sub-threshold mode circuit design, duty-cycling, open-loop voltage regulation, and low swing drivers.

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**Caption List:**

Fig. 1. Progress in size reduction of 32kHz X and XOs.

Fig. 2. Block diagram of the MEMS-based 32kHz clock generator.

Fig. 3. a) Tuning H-style fork 524kHz MEMS resonator (b) simplified block diagram and (c)

Electrical model of the resonator

Fig. 4. Simplified block diagram of sustaining circuit.

Fig. 5. Automatic gain control circuit.

Fig. 6. Block diagram of PLL and its different configurations in XO, TCXO and low power mode.

Fig. 7. a) Block diagram of the temperature sensor b) The timing diagram of the proposed DEM algorithm.

Fig. 8. Block diagram of voltage regulators. Analog regulator adopts open loop architecture.

Fig. 9. Digital voltage regulator biases digital block with a minimum required supply over process and temperature corners.

Fig. 10. Low-power high-voltage regulator.

Fig. 11. Block diagram of output driver. Low-swing driver feature to reduce power.

Fig. 12. Circuit implementation of low-swing driver. Full control on output swing by programming the regulator reference.

Fig. 13. Current consumption vs. load capacitor using CMOS and low swing driver.

Fig. 14. Die photograph of 524kHz MEMS die and a 180-nm CMOS chip in a) QFN wire-bonded and b) chip scale packages.

Fig. 15. The current consumption of each main block in the system.

Fig. 16. Transient current profile of entire chip when TDC conversion rate is 3Samples/sec.

Fig. 17. Measured $VDD_{int}$ versus $V_{Battery}$ when high voltage regulator is enabled.

Fig. 18. Frequency stability in a) XO and b) TCXO configurations.

Fig. 19. TCXO response to temperature ramp.

Fig. 20. Measured long term jitter in 2.5sec time stride for 100 TCXO devices.

Table 1. Performance summary of XO and TCXO devices and comparison table.