

A single-chip micro-opto-electro-mechanical system for optical coherence tomography imaging

Jovic, Aleksandar

DOI

[10.4233/uuid:84fa3be6-32e8-48f8-a732-deb4445b1b23](https://doi.org/10.4233/uuid:84fa3be6-32e8-48f8-a732-deb4445b1b23)

Publication date

2019

Document Version

Final published version

Citation (APA)

Jovic, A. (2019). *A single-chip micro-opto-electro-mechanical system for optical coherence tomography imaging*. [Dissertation (TU Delft), Delft University of Technology]. <https://doi.org/10.4233/uuid:84fa3be6-32e8-48f8-a732-deb4445b1b23>

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**A SINGLE-CHIP
MICRO-OPTO-ELECTRO-MECHANICAL SYSTEM
FOR OPTICAL COHERENCE TOMOGRAPHY IMAGING**

A SINGLE-CHIP MICRO-OPTO-ELECTRO-MECHANICAL SYSTEM FOR OPTICAL COHERENCE TOMOGRAPHY IMAGING

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. dr. ir. T.H.J.J. van der Hagen,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op donderdag 10 januari 2019 om 15:00 uur

door

Aleksandar JOVIĆ

Master of Science in Elektrotechniek en Informatica,
Universiteit van Belgrado, Belgrado, Servië
geboren te Bor, Servië.

Dit proefschrift is goedgekeurd door de

promotor: prof. dr. ir. P. M. Sarro

Samenstelling promotiecommissie:

Rector Magnificus,	voorzitter
Prof. dr. ir. P. M. Sarro,	Technische Universiteit Delft

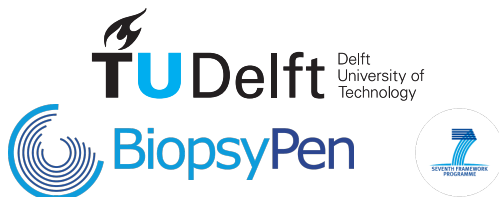
Onafhankelijke leden:

Prof. dr. P. J. French,	Technische Universiteit Delft
Prof. dr. M. Kraft,	Katholieke Universiteit Leuven
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Prof. dr. ir. W. A. Serdijn,	Technische Universiteit Delft, reservelid

Overige leden:

Dr. G. Pandraud,	Technische Universiteit Delft
Dr. ir. E. Margallo-Balbás,	Medlumics S.L., Spain

Dr. G. Pandraud heeft in belangrijke mate aan de totstandkoming van het proefschrift bijgedragen.



Keywords: MOEMS, system integration, OCT imaging, electrothermal actuators, Al-SiO_x bimorph beams, Si microlenses, Si photonics

Printed by: Ipskamp

Front & Back: Cover design by Queen of the Universe

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ISBN 978-94-028-1350-0

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To my family

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SUMMARY

A constant increase of patients with skin cancer is having a big impact on global healthcare. The number of successful treatments strongly depends on early detection which with current available medical procedures is not always possible. Therefore, an affordable, non-invasive, imaging solution, which gives live tissue morphology is needed to facilitate skin cancer detection at an early stage. Among all imaging techniques used in dermatology, optical coherence tomography (OCT) imaging has the best tradeoff between lateral resolution and penetration depth. Unfortunately, such systems are still expensive to reach out to general practitioners.

In this work, a possible solution to the above-mentioned problem is proposed. The innovative approach introduced in this work combines a passive photonic circuit, a microlens and a MEMS actuator system into a single MOEMS chip. The photonic circuit consists of waveguide system combined into a Michelson interferometer, where a measurement optical line, i.e. a waveguide, scatters the light with a 45° mirror facet towards a collimating silicon microlens made on the backside of the chip. Monolithic integration of all optical components ensures their intrinsic self-alignment. This way, optical components do not require expensive and time-consuming assembly and packaging procedures, but still have proper optical alignment which is important for high quality imaging.

The light movement is provided by a set of MEMS actuators, which generate rotation of a waveguide-mirror-lens silicon block. The rotational movement is translated into a lateral movement of the light spot on the surface. A small angular displacement preserves the light spot size. Further, the increase of the distance between the lens and the surface increases the lateral scanning range of the OCT system while using the same angular displacement. To realize the single-chip MOEMS device, each component is first separately analyzed, fabricated, characterized and optimized. Both design and fabrication process of all components, i.e. system submodules, are developed to be compatible among each other and to allow the final MOEMS device to be an almost straightforward buildup of predefined parts.

The core of any OCT system is the interferometer. Therefore, a starting point for the MOEMS device development is the design of the photonic circuit and its fabrication using a commercially available “thick” SOI waveguide technology, transferred from VTT Finland to our laboratory. The technology is slightly modified to later accommodate the MEMS actuator system. The 45° mirror facet is made using the well-known anisotropic wet etching of silicon using a TMAH based solution, which is highly selective to $\langle 110 \rangle$ crystallographic plane. The facet is positioned to be in correspondence of the microlens center.

Since the OCT for dermatology uses near infrared light, the microlens is made from Si. The spherical microlens designed is determined by the numerical aperture of “thick” SOI waveguides and the substrate thickness. A Si microlens of 500 μm radius of curva-

ture and 150 μm diameter is implemented. A good surface quality for this application is achieved, as indicated by a root mean square (RMS) value of roughness lower than 32 nm. The demand is satisfied using photoresist thermal reflow and a dry plasma etching process to accurately define the microlens geometry in silicon.

The surface scanning requires a 2D actuator system. Both x and y direction scanning actuators must be compatible to each other. Since waveguides are usually made in the device layer of SOI wafers, the waveguide-mirror-lens block must have mechanical support made from bulk silicon. Numerical analysis followed by experimental verification are carried out to optimize the mechanical hinges. As the first step towards building a 2D system the optimization of two 1D MEMS actuators is performed. Separate, but compatible, actuator designs are made using aluminum-silicon oxide electrothermal MEMS actuators. The actuator type is chosen to achieve small footprint, low operating voltage and an acceptable produced force for the desired 12° of angular displacement range of the block in both x and y directions. The maximum power consumption for x and y direction scanner is kept below 0.5 W. The fabrication process flow for the MEMS actuators is discussed in detail and critical steps are specially addressed and solved. Attention is given to the optimization of the Bosch DRIE process for the mechanical hinge definition of the single-chip OCT MOEMS scanner.

All fabricated components are individually characterized to evaluate their performance. The optical characterization of the photonic circuit and mirror showed a 1 – 2 dB higher optical loss compared to commercially available waveguides. Yet, such difference can be neglected at this stage, being a feasibility study of the single-chip MOEMS OCT system.

The developed MEMS actuators showed reliable operation. Electrical, thermal and mechanical characterization in both static and dynamic regime is carried out. The fully integrated MOEMS scanners reach about 50% of the expected angular displacement, due to lower temperature generated by the heater. A more suitable material for the heating element should be implemented to fully exploit the anticipated motion range. Dynamic characterization showed the resonant frequency to be in agreement with simulation results.

Finally, optical scanning is demonstrated using monolithically integrated MOEMS devices. The scanning is demonstrated at two different working distances proving the surface scan range increase with enlargement of the working distance, reaching a maximum range of 6 mm and 4 mm in x and y direction, respectively. No additional attenuation of the optical signal is observed during device operation. The presented results prove the successful implementation of monolithically integrated MOEMS scanner and the feasibility of single-chip OCT systems.

SAMENVATTING

EEN constante toename van patiënten met huid kanker heeft een grote invloed op de mondiale gezondheidszorg. Het aantal succesvolle behandelingen hangt sterk af van een vroege diagnose, wat met de huidige medische procedures niet altijd mogelijk is. Een betaalbare, niet-invasieve, beeldvormende oplossing welke live weefsel morfologie gegevens geeft is daarom nodig om huid kanker detectie in een vroeg stadium te faciliteren. Van alle beeldvormende technieken gebruikt in dermatologie, vertoont optische coherente tomografie (OCT) beeldvorming de beste afruil tussen laterale resolutie en penetratie diepte. Echter zijn zulke systemen nog steeds te duur om uit te reiken aan algemene gebruikers.

In dit werk wordt een mogelijke oplossing voor het hierboven genoemde probleem voorgesteld. De innovatieve aanpak geïntroduceerd in dit werk combineert een passief fotonisch circuit, een micro lens en een MEMS actuator systeem tot een enkele MOEMS chip. Het fotonisch circuit bestaat uit een golfgeleider systeem gecombineerd tot een Michelson interferometer, waarin een optische meetlijn, bijv. een golfgeleider, het licht verstrooid middels een 45 graden facet spiegel richting een collimerende silicium micro-lens, welke is vervaardigd op de achterzijde van de chip. Monolithische integratie van alle optische componenten verzekert hun intrinsieke zelf uitrichting. Op deze manier vereisen de optische componenten geen kostbare en tijdrovende assemblage en verpakking procedures, maar vertonen nog steeds een juiste optische uitrichting wat van belang is voor hoge kwaliteit beeldvorming.

De beweging van licht wordt verzorgd door een set MEMS actuatoren, welke een rotatie genereren van een blokvorige silicium golfgeleider-spiegel-lens combinatie. De rotationele beweging vertaalt zich in een laterale beweging van de licht stip op het oppervlak. Een kleine hoekverplaatsing behoudt de grootte van de licht stip. Voorts, de toename van de afstand tussen de lens en het oppervlak vergroot het laterale scanbereik van het OCT systeem, gebruik makend van dezelfde hoekverplaatsing. Om de enkele chip, het MOEMS apparaat, te realiseren, is elke component eerst apart geanalyseerd, gekarakteriseerd en geoptimaliseerd. Zowel het ontwerp als fabricage proces van alle componenten, dat wil zeggen systeem sub-modules, zijn ontwikkeld compatibel te zijn met elkaar en het uiteindelijke MOEMS apparaat bijna een eenvoudige samenvoeging van vooraf gedefinieerde onderdelen te laten zijn.

De kern van elk OCT systeem is de interferometer. Daarom is het fotonisch circuit het startpunt voor de ontwikkeling van het MOEMS apparaat en zijn fabricage gebaseerd op het gebruik van commercieel verkrijgbare 'dikke' SOI golfgeleider technologie, overgedragen van VTT Finland naar ons laboratorium. De technologie enigszins aangepast om later het MEMS actuator systeem te integreren. De 45° facetspiegel is gemaakt gebruik makend van de wel bekende anisotropische natte ets methoden voor silicium, gebruik makend van een op TMAH gebaseerde oplossing, welke zeer selectief is naar een $\langle 110 \rangle$ kristallografisch vlak.

Omdat de OCT voor dermatologie gebruik maakt van het nabije infrarood licht, is de microlens vervaardigd van silicium. Het ontwerp van de sferische microlens is vastgesteld aan de hand van numerieke apertuur van 'dikke' SOI golfgeleiders en de dikte van het substraat. Een silicium microlens met kromtestraal van 500 μm en een diameter van 500 μm is geïmplementeerd. Een goede oppervlakte kwaliteit voor deze toepassing is bereikt, zoals wordt aangetoond door een kwadratische gemiddelde (RMS) waarde van de ruwheid lager dan 32 nm. Deze vraag is bevredigd door gebruik te maken van thermische reflow van fotolak en een droog plasma ets proces om de microlens geometrie in silicium accuraat te definiëren.

Het scanproces van de oppervlakte vereist een 2D actuator systeem. Zowel in de x als in de y richting dienen de actuatoren compatibel met elkaar te zijn. Omdat de golfgeleiders gebruikelijk gemaakt worden in de apparaat laag van SOI wafers, moet het golfgeleider-spiegel-lens blok mechanisch ondersteund worden door bulk silicium. Numerieke analyse gevolgd door experimentele verificatie zijn uitgevoerd om de mechanische gewrichten te optimaliseren. Als eerste stap naar de bouw van een 2D systeem is de optimalisatie van twee 1D MEMS actuatoren uitgevoerd. Apart maar compatibel, zijn de ontwerpen van de actuatoren gemaakt gebruik makend van aluminium-silicium oxide elektro-thermische MEMS actuatoren. Het actuator type is zodanig gekozen, dat een klein oppervlak, een lage werk spanning en een acceptabele geproduceerde kracht om de gewenste 12° hoekverplaatsing bereik van het blok in x en y richting te bereikt wordt. Het maximale energieverbruik voor x - en y -richtingscanners wordt onder 0.5 W gehouden. De fabricage proces flow voor de MEMS actuatoren is tot in detail besproken en kritische stappen hebben speciale aandacht gekregen en zijn opgelost. Attentie is gegeven aan de optimalisatie van het Bosch DRIE proces voor de vorming van de mechanische gewrichten van de enkele-chip OCT MEOMS scanner.

Alle gefabriceerde componenten zijn individueel gekarakteriseerd om hun prestatie te evalueren. De optische karakterisatie van het fotonisch circuit en de spiegel vertonen een 1-2 dB hoger optisch verlies vergeleken met commercieel verkrijgbare golfgeleiders. Op dit moment kan dit verschil worden verwaarloosd, aangezien dit een haalbaarheidsstudie is van een enkele-chip MOEMS OCT systeem. De ontwikkelde MEMS actuatoren betrouwbare werking. Elektrische, thermische en mechanische karakterisatie in zowel het statische als dynamische regime is uitgevoerd. De volledig geïntegreerde MEOMS scanners bereiken ongeveer 50% van de verwachte hoekverplaatsing, wat wordt veroorzaakt door een lagere gegenereerde temperatuur door de verwarmers. Een geschikt materiaal voor de verwarmers zou moeten worden geïmplementeerd om het geanticipeerde bewegingsbereik volledig te kunnen benutten. Dynamische karakterisatie vertoonde resonantie frequenties, welke overeenstemmen met de simulatie resultaten.

Ten slotte is optische scanning gedemonstreerd, gebruik makend van de monolithisch geïntegreerde MOEMS apparaten. De scanning is gedemonstreerd bij twee verschillende werkafstanden, waarmee wordt aangetoond dat het oppervlakte scanbereik kan worden vergroot door de werkafstand te vergroten, waarbij het maximale bereik gelijk is 6 mm en 4 mm in de x en y richting respectievelijk. Er is geen toegevoegde verzwakking van het optisch signaal waargenomen tijdens de werking van het apparaat. De gepresenteerde resultaten bewijzen de succesvolle implementatie van een monolithisch geïntegreerde MOEMS scanner en de haalbaarheid van een enkele-chip OCT systeem.

1

INTRODUCTION

Better safe than sorry

Folk proverb

The average human life expectancy has increased by about 20 years in the past 50 years, mainly due to continuous improvements in the health care system. Nowadays, for many diseases either a way to cure them or to live with them exists, thanks to the availability of a variety of drugs and medical procedures and the capability of early detection that current diagnostic techniques offer. The early stage detection plays a major role in any successful medical treatment. At early stage of a disease, treatments are more effective, and recovery is faster, which significantly contributes to lower medical costs and to a better quality of life. If the diagnostic technique is non-invasive and provides live images of tissue morphology, the benefits are even greater. In fact, thanks to the digital nature of these images and the large availability of internet, these images can be sent over long distances to medical specialists, who can evaluate them, thus assessing the situation even if the patient is not physically present. Dermatological problems, especially skin cancer, are unfortunately constantly rising. Regretfully, there is still lack of non-invasive, efficient and user-friendly medical tools with fast image acquisition, which would allow 3D live in-vivo skin tissue cross sections.

1.1. MOTIVATION

DERMATOLOGICAL problems are one of the most common health issues worldwide and in the past decades they are in constant growth. Among them, skin cancer, besides being the most common skin problem among Caucasian population, is epidemically rising (3- 8 % per year) [1], indicating a serious health risk for future generations [2]. The problem equally affects Europe, North America and Australia [3] and it is caused by increased UV radiation exposure [4], both by change in everyday human habits [5] (outdoor actives, tanning studios) and by ozone layer depletion [5,6]. There are three main types of skin cancer: basal cell carcinoma (BCC) and squamous cell carcinoma (SCC) with low mortality, and melanoma with high mortality. Although the first two are not lethal, their frequent occurrence represents a great expense for the health care system [7], being one of the five most expensive medical treatments, according to some studies [8].

Risk prediction models of melanoma development showed good results in tumor prevention [9]. Also, recognition of specific skin lesions at an early stage improves diagnosis of SCC before its rapid development [10]. For all three types of cancer, an early detection has proved to have a key role in increasing the number of successful medical treatments and lowering the corresponding medical costs [11-13]. Further, from skin cancer other epithelial tumors can be developed (oral, colorectal etc.) and therefore proper monitoring of skin cancer development in the beginning has also direct influence on the diagnosis of different tumors.

A frequently used medical examination procedure, called biopsy, implies surgical tissue removal by a trained medical specialist and histopathological examination of this tissue. Except being invasive for the patient, the whole procedure is slow. Even more, it gives only a temporary disease condition and consequently it is not suitable for periodical monitoring of the lesion changes. Further, the procedure is only employed once the illness is recognized. For the patients with a lot of moles and with suspicion of melanoma, often biopsy procedures and mole removals leave body scars. However, it is still routinely employed for morphological examination of the skin.

To follow live morphological changes of moles and lesions, a non-invasive, low cost, high-resolution imaging technique is needed. An ideal imaging technique should have an imaging resolution better than the average skin cell size ($\sim 30 \mu\text{m}$) and a penetration depth of a few mm (to reach all layers of skin). Current imaging techniques used in dermatology are high-frequency ultrasound, confocal microscopy, optical coherence tomography, micromagnetic resonance imaging and multiphoton tomography. Micromagnetic resonance imaging and high frequency ultrasound have a lateral and axial resolution of around $20 - 100 \mu\text{m}$ [14,15]. On the other hand, confocal microscopy and multiphoton tomography have resolution below $5 \mu\text{m}$, but a low imaging depth of only $200 - 300 \mu\text{m}$ [16,17]. All of them suffer from long-time image acquisition and more importantly, have high equipment and ownership costs. Optical Coherence Tomography (OCT) is a non-invasive imaging technique, which by using a low coherent light interferometry, gives a good lateral and axial resolution (around $10 \mu\text{m}$) and has a penetration depth into the skin of several millimeters [18]. This allows live morphology tissue visualization, i.e. non-invasive imaging of the epidermis, the junction and the dermis layer at the same time.

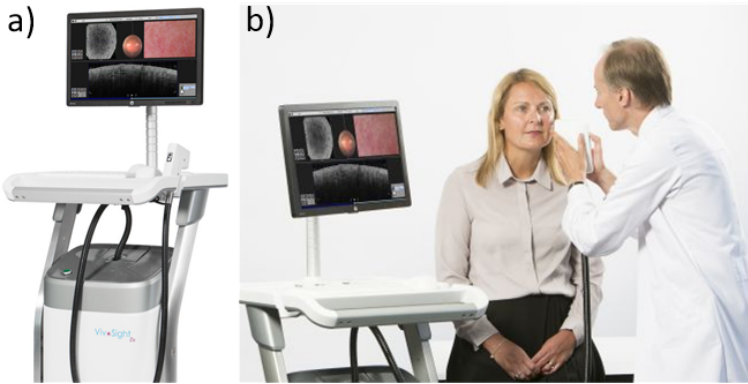


Figure 1.1: Vivosight, currently available OCT systems for dermatology by Michelson Diagnostics Ltd, UK (www.vivosight.com): (a) the complete OCT system (b) the OCT system in dermatological use.

Commercially available OCT systems (see Fig. 1.1) work in the frequency-domain (FD-OCT). They are using either a fast-tunable laser, a so called “swept-source” (SS-OCT), or a broadband light source in a combination with a spectrometer (SD-OCT). OCT as an imaging technique was first used in ophthalmology and it primarily uses the near infrared light domain [19]. One of the first demonstrated OCT applications in dermatology used $1.3\ \mu\text{m}$ wavelength [20] and had optimum trade-off between light absorption and good contrast at higher depths, which is nowadays considered to be the standard operating wavelength. There are several commercially available dermatological OCT scanners. However, all of them are very large systems, made of several discrete components and with a high price ($\sim 100\text{k€}$). Even more, due to the misalignment sensitivity of the individual components, they require frequent maintenance, resulting in high cost of ownership. Unfortunately, all listed limitations are big drawbacks for OCT application in everyday dermatological diagnostics.

To achieve wide use of OCT systems, both initial and ownership costs should be much lower. Further, portability of the devices will enable inspection of patients not only in hospital but at general physician and small clinics anywhere. Therefore, the size of the whole system must be significantly reduced without loss of performance. Although ongoing miniaturization of the system components have partially helped to reduce the system footprint, unsolved issues related to time consuming and expensive alignment and packaging procedures remain, thus still hampering a widespread use of this technique.

1.2. WORKING PRINCIPLE OF OCT

TO understand the OCT system working principle, the function of each component must be examined. Then, an analysis of how each component can be improved to generate better images can be performed. The main working principle is based on the reflection of light waves from a translucent scanning object [21]. Unfortunately, light speed propagation is beyond any of the conventional electronic detection systems. Therefore, low coherent interferometry is used to measure a time delay, i.e. the optical path length

of the light signal. The interferometer configuration and the reflection principle are illustrated in Fig. 1.2. The light emitted from a source is split by a beam splitter into a reference and a sample beam. The reference beam is reflected by a reference mirror, while the sample beam is reflected by the scanning object. Both reflected beams enter the beam splitter where part of each beam is reflected towards a detector and recombined.

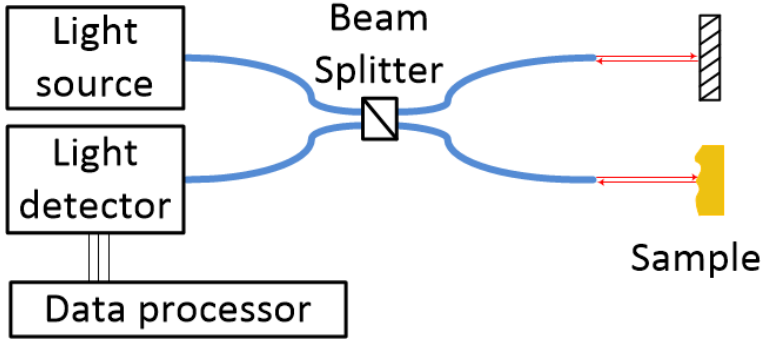


Figure 1.2: A basic Michelson interferometer configuration for OCT detection.

If the optical path difference of the reference and the sample beam is lower than the coherent length of the light source, an interferometric image can be formed, and the path difference can be measured. Thus, in-depth (axial) resolution is defined by coherent length of the source as [22]:

$$\Delta z = \frac{2 \cdot \ln 2}{n \cdot \pi} \cdot \frac{\lambda^2}{\Delta \lambda} \quad (1.1)$$

where λ is the light source central wavelength, $\Delta \lambda$ is the spectral width and n is the refractive index of the propagation medium. Lateral resolution of OCT system depends on the quality of an imaging objective, like in standard microscopy, and it is defined as [22]:

$$\Delta x = \frac{4}{\pi} \cdot \frac{\lambda}{NA} \quad (1.2)$$

where NA is the numerical aperture of the objective. To image different sublayers of the object, two modalities are available: time domain OCT (TD-OCT), in which the reference beam needs to be time delayed by a reference mirror movement; and frequency or Fourier domain OCT (FD-OCT), in which the spectrum of the recombined light beam is analyzed. In both cases, the maximum scanning depth depends on the light attenuation of the scanned object.

A typical configuration of the interferometer for a single point TD-OCT is illustrated in Fig 1.3. The light source is typically a SLED diode, a broadband light source with high output power. The beam goes through the beam splitter where it is divided in the reference and the sample beam. The sample goes through a scanning mechanism and it is focused on the sample. By changing the reference optical path, reflection of the different

depths in the sample can be measured. The recombined reference and sample beam is detected by a single photodetector. Clearly, to have fast and large in-depth scanning, the reference mirror needs to cover a large displacement and to be able to move at the same speed as the image acquisition.

The interference signal of a single wavelength from the broadband light depends on the sublayer depth from which the wavelength is reflected. A spectral analysis of the total interference signal gives information about each sublayer of the scanning object. Therefore, instead of extending the reference optical path to reach a certain sublayer, it is possible to recreate the image by using the Fourier transformation of the interference signal spectrum. Each maximum in the spectrum gives the sublayer depth, while the amplitude of the frequency holds the information about the sublayer refractive index.

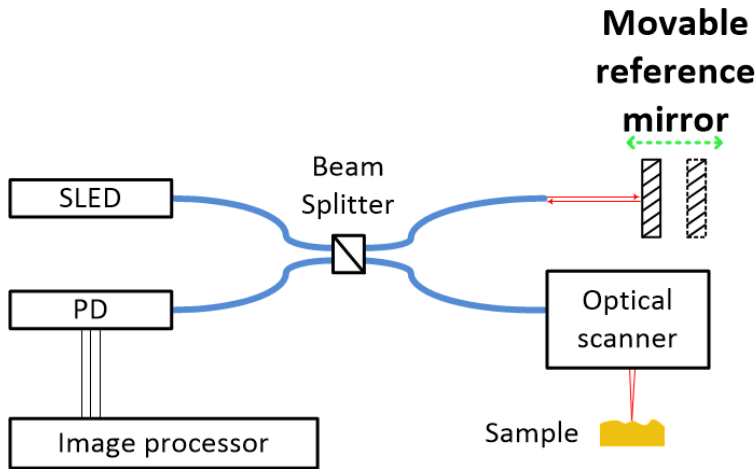


Figure 1.3: The TD-OCT interferometer configuration.

Two Michelson configurations for FD-OCT are illustrated in Fig. 1.4. The setup in Fig. 1.4a uses a broadband light source and a spectrometer as light detector to analyze the signal in the spectral domain (SD-OCT). The second one (Fig. 1.4b) has a simple photodiode but uses a fast-tunable laser, so called swept source, to generate short light pulses of single wavelengths. Thus, the spectrum is generated in single frequency steps. Using a swept source in this configuration (SS-OCT) excludes the need for the spectrometer. On the other hand, the presence of the swept source increases the OCT setup cost, but the OCT detector is just a photodiode and therefore less expensive than a spectrometer, especially in infrared domain.

All presented configurations are given as free-space interferometers which are not practical to use since any perturbation of the optical path will hamper the generation of correct images. Therefore, OCT systems are often fiber-based optical interferometers [22]. The optical path is defined by a fiber while splitters are made of fiber couplers. Fiber-optics components make OCT systems more mechanically flexible to use. Still, all the discrete components need to be properly aligned, assembled and packaged.

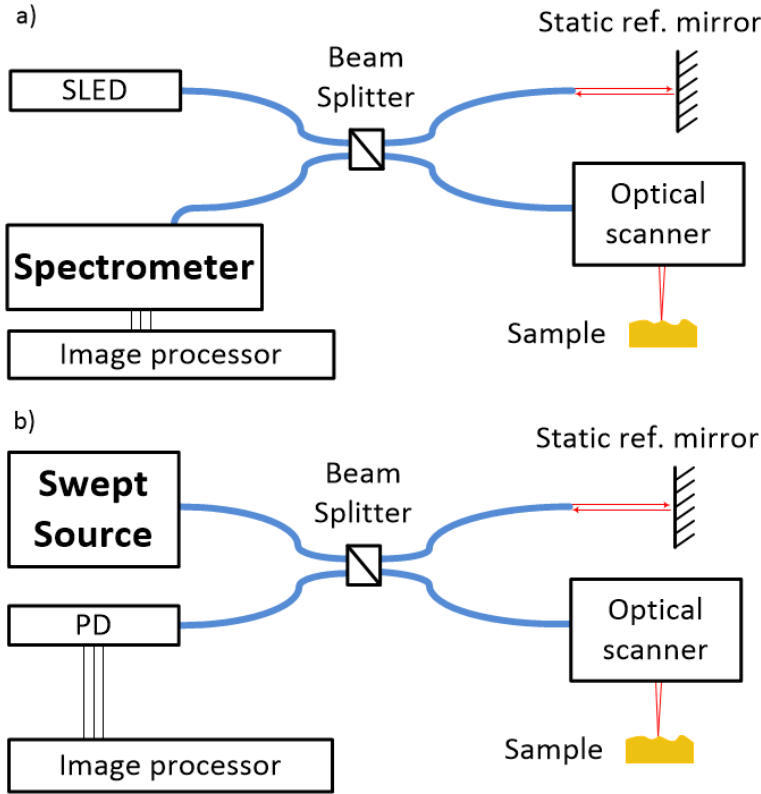


Figure 1.4: Interferometer configuration: (a) SD-OCT and (b) SS-OCT mode.

1.3. MINIATURIZATION OF OCT SYSTEMS

By replacing discrete components with integrated optics both size and costs of an OCT system can be significantly reduced, while the required image quality is preserved. Each OCT component of the TD, SD and SS OCT system has its equivalent in photonic integrated circuit technology. Further, integrated optics technology provides significant fabrication scalability, especially in silicon-based systems. In addition, if the integration is monolithic, the alignment problem is circumvented. Recent studies show promising results of integrated photonics in OCT. Integration focused on replacing the interferometer made of discrete components, such as fibers and beam splitters, by a photonic integrated circuit (PIC) [23-27]. But, the light beam movement, which is one of the key features of any scanner, has not been addressed so far.

In photonic integrated technology, fibers are replaced by waveguides, while beam splitters are replaced by multimodal interferometers (MMI) which also serve as signal combiners [26]. SD-OCT systems using a photonic integrated interferometer [23] had comparable results to a fiber-based interferometer. Additional optimization of the integrated interferometers design has been reported in [24,26], further improving the signal to noise ratio of the OCT system. However, these systems are still made from discrete

components. The possibility to fabricate different waveguides geometry in a single integrated circuit technology, resulted in fully functional array waveguide grating (AWG) spectrometers for SD-OCT [28,29].

TD-OCT does not require a spectrometer for image acquisition, therefore the interferometer design and fabrication in integrated photonics is simple and straightforward compared to SD-OCT. However, a change of the reference beam optical path (Fig. 1.5a) requires a fast and large displacement of a movable mirror to delay the reference signal in time. An alternative is to change the optical path by changing the refractive index of the propagating medium. Using the thermo-optic effect, a scan depth of 0.95 mm with 1.3 μm wavelength has been demonstrated in [30]. Further, thermo-optic delay lines using SiC as waveguide material for TD-OCT in visible have been investigated [31]. Implementation of Bragg reflectors with both electro-optic [32] and thermo-optic effect [33] provided delay lines for 1.53 μm wavelength.

Integrated Ge photodetectors [34] have a low dark current level (<0.1 nA) and a responsivity of 0.2 A/W, which is better than InP based detectors [35]. Further improvement in Ge layer quality and in the design of these diodes should result in responsivity values close to 1 A/W, which is comparable to the result presented in [36]. With the present hybrid integration technology for light sources [37] or improved III-V or group IV light sources on Si [38-42], it is possible to have almost all components for both TD-OCT and FD-OCT systems realized on one chip. However, the only component that does not yet have an equivalent in the integrated circuit technology is the one needed to provide the lateral scanning.

1.4. LATERAL SCANNING FOR OCT IMAGING

TO generate an image in more than a single point, light movement over the tissue surface is needed. Movable mirrors are mainly used to reflect the light at different angles so to cover as much surface area as possible. The introduction of microelectromechanical system (MEMS) technology decreased significantly the movable mirrors footprint and even more, increased their operation speed. Figure 1.5 gives a schematic drawing of a scanning component for a fiber-based OCT system. It uses a MEMS micromirror, a fiber and a focusing microlens assembled in a miniaturized probe. The light comes out the fiber and goes to a collimating lens which corrects the light beam divergence. The collimated beam is reflected from the mirror at different angles to provide lateral scanning. Then, the beam is focused on the sample by another lens, which translates the angular motion of the beam into a lateral scan of the surface. Investigation carried out in [43] concluded that the components must be placed at a specific distance with 0.1 mm precision to obtain good quality images. Any misalignment from the optical axes of more than 0.1 mm is not acceptable.

MEMS micromirrors have found a wide range of application in industry, especially in scanning systems [44]. It started with the digital light projector and quickly found its way into OCT technology. Using different actuation principles and the benefits offered by the silicon based integrated circuits (IC) technology, a variety of MEMS mirrors are nowadays available for OCT application [45]. In addition, with powerful finite element method (FEM) tools (Comsol, Ansys, etc.) 3D MEMS mirrors models can be built, and device characteristics can be quickly predicted. Thus, the micromirrors can be op-

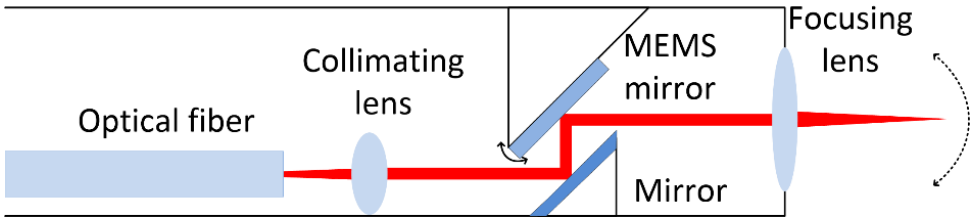


Figure 1.5: Standard configuration of a miniaturized OCT scanning component made of several discrete parts like a MEMS micromirror, a microlens and an optical fiber.

timized to decrease power consumption, increase motion range, speed or number of degrees of freedom, so the systems can be faster and more reliable.

MEMS mirrors can be distinguished according to the actuation principle employed, i.e. electrostatic, electromagnetic, piezoelectric and electrothermal. Also, depending on the application, the DOF or the scanning range can determine the most suitable type of micromirror. In general, electrostatic actuators are low power consumption devices but they require high driving voltages. Electromagnetic actuators need an external magnetic field, while piezoelectric actuators are mostly made from CMOS non-compatible materials and thus not ideal for high scale production in well controlled foundries. Electrothermal actuators are slow with high power consumption, but with low operating voltages. An overview of MEMS mirror-based OCT systems is given in [45-47] where OCT systems performance were compared based on the different actuation principles used. Yet, all analyzed OCT systems are made of discrete components and use the standard configuration presented in Fig. 1.5.

An example of endoscopic TD-OCT probe using an electrostatically driven MEMS mirror is presented in [48,49]. It has an outer diameter of only 4 mm. For an intended working distance of 6.6 mm, the MEMS mirror must provide around 20° of total angular motion along the x and y axes to cover a $1 \times 1 \text{ mm}^2$ surface area. Several types of MEMS micromirrors using the above-mentioned actuation principle have been realized and implemented in OCT systems. Thanks to the fast response electrostatic actuation can provide, the MEMS mirror is not a bottleneck for the system working speed. However, the driving voltage is rather high (100 V). Another electrostatic 2D MEMS mirror for a 5 mm diameter TD-OCT probe is reported in [50]. The mirror has a 12° angular motion in both directions of mechanical motion, which allows to cover a $1.8 \times 1 \text{ mm}^2$ surface area with a driving voltage of 150 V. The 1D MEMS mirror array presented in [51] has a low operating voltage and with only 6 V a single mirror can rotate about 8° . The low operating voltage is obtained by the special design of the hidden electrostatic comb drives. However, this solution is not suitable for extending it into 2D due to the complex system design.

A 3D SD-OCT scanning probe using electromagnetic actuators with a $2.8 \times 12 \text{ mm}^2$ footprint is presented in [52]. The mirror fabrication is simpler than for the electrostatic mirrors in [51] and [50]. In this case the mirror needs a permanent NbFeB mm-size magnet glued below the mirror surface and two external magnetic coils to generate the magnetic field and actuate the mirror. Nevertheless, with 150 mW of power consump-

tion and a driving voltage below 4 V, this mirror can cover an angular range of up to 60° which, thanks to the probe design, translates to a ~ 1.5 mm surface scan. To avoid assembly of a permanent magnet to the mirror, a dense metal line magnetic coil can be made [53]. However, the external magnet to generate the actuation force is still needed, which increases the already rather high complexity of the system.

A 2D SD-OCT system with a piezoelectric 1D micromirror is presented in [54]. The system has a lateral scanning range of ~ 1 mm which is obtained with a 15° angular range piezoelectric MEMS mirror. The driving voltage in static regime is ± 10 V and power consumption is 1 mW. Using natural frequencies of a mirror with piezoelectric cantilevers, surface scanning with low driving voltage is possible [55,56].

One of the first OCT endoscopes used electrothermal bimorph actuators for the MEMS mirror actuation [57]. With a power consumption of 0.5 mW, the mirror covers an angular range of 15° , which, thanks to the 5 mm-diameter endoscope design, translates into a 3 mm lateral range. An improved version of the mirror had two axes scanning range of $\sim 40^\circ$ with maximum power consumption of 0.25 mW [58]. Further development of electrothermal MEMS mirrors resulted in a low driving voltage, 70° range mirror, assembled in a 5 mm-diameter probe with the possibility to reduce it down to 2.8 mm [59]. Nevertheless, as all mirror-based endoscopes, high-precision probe packaging is needed.

A novel lateral scanning approach for OCT technology, where an iron-bead loaded fiber is actuated using a solenoid magnet, is reported in [60]. This approach does not need a MEMS mirror. Thus, the OCT system has one less component for the assembly. Another fiber scanner with electrothermal U-beam actuator is presented in [61]. Using two different resonant modes, a surface scan of 0.5×0.5 mm² is achieved with driving peak-to-peak voltage of 16 V and a total power consumption of 90 mW. The size of the whole scanner is $1.3 \times 7 \times 0.45$ mm³ which allows further size reduction of the probe. The wafer scale microfabrication process used, and the simplified assembly make this scanner an attractive approach to simplify packaging of OCT systems. A different approach with combination of metal-polymer electrothermal bimorph cantilever and planar waveguide beam deflector is reported in [62]. However, this 2D scanner requires micro assembly of two coupling lenses, a beam deflector chip and a printed circuit board mirror just to provide the scanning. Packaging all of them in a probe would further increase the system complexity.

MEMS technology has contributed to significantly reduce the size of OCT systems. For more than 10 years a MEMS mirror as in the configuration presented in Fig. 1.5, is considered as “the state of the art” for OCT scanners [45]. The work reported in [60] and [61] shows that the number of components in the lateral scanner, and thus the system complexity, can be reduced. However, it still requires complicated and time-consuming alignment of the system components and complex packaging procedures [63].

Clearly, the simplification of the scanning mechanism can lead to the reduction of the assembly time of OCT systems. Ideally, a micro-opto-electromechanical scanner should be integrated with a PIC interferometer, thus creating a miniaturized and self-aligned single chip OCT imaging engine.

1.5. A NEW APPROACH FOR OCT SCANNING MECHANISM

A new system can be developed in Si-based technology. It needs to integrate a collimating lens, a waveguide-based interferometer, photodetectors, optical modulators and MEMS actuators with a hybrid integrated light source to create a ‘single-chip’ imaging solution. Since the hybrid integration of Si based PIC with III-V light sources [64], the optical modulation in Si based PIC [30], and the integration of Ge photodetector with PIC for 1.3 μm wavelength [34] have already been proven, the remaining step towards the envisioned new system is the integration of MEMS actuators with the photonic components on the same chip.

The here proposed novel integrated self-aligned MOEMS scanner is illustrated in Fig. 1.6 [65]. The scanner consists of a Si waveguide ending with a 45° mirror which reflects the light down to a Si collimating lens (Fig. 1.6a). The lateral resolution is the defined by numerical aperture of the waveguide. Instead of using a MEMS mirror below the lens to provide the scanning, the whole block can be moved (Fig. 1.6b) using MEMS actuators. In addition, with the same angular displacement, the lateral scanning range can be further increased by increasing the working distance (Fig. 1.6c) and reducing numerical aperture.

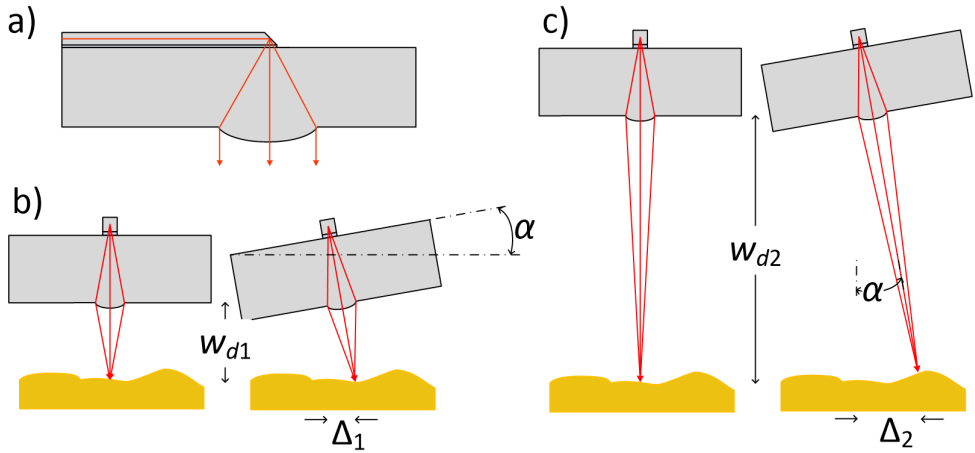


Figure 1.6: The new concept for an integrated 3D OCT on-chip imaging solution: (a) Waveguide-mirror-microlens as one block. Surface scanning with block rotation at (b) short; (c) long working distance.

To generate a 3D image, surface scanning in both x and y direction is required. Therefore, a new MEMS actuator system for the configuration given in Fig. 1.6 needs to be designed, fabricated and characterized. The envisioned 2D integrated MOEMS scanner is depicted in Fig. 1.7. The system has a set of actuators providing torsion of the plate around supporting hinges. Both actuators and hinges are anchored to a frame. The frame is further supported by another hinge and a set of actuators to deflect the frame. Torsional and deflecting motions are translated into x and y scanning directions. A Si waveguide which is part of the OCT interferometer measurement arm goes above both

hinges. The presented device needs to be part of a portable, battery supplied, handheld time domain OCT probe developed within the Biopsypen project (www.biopsypen.eu).

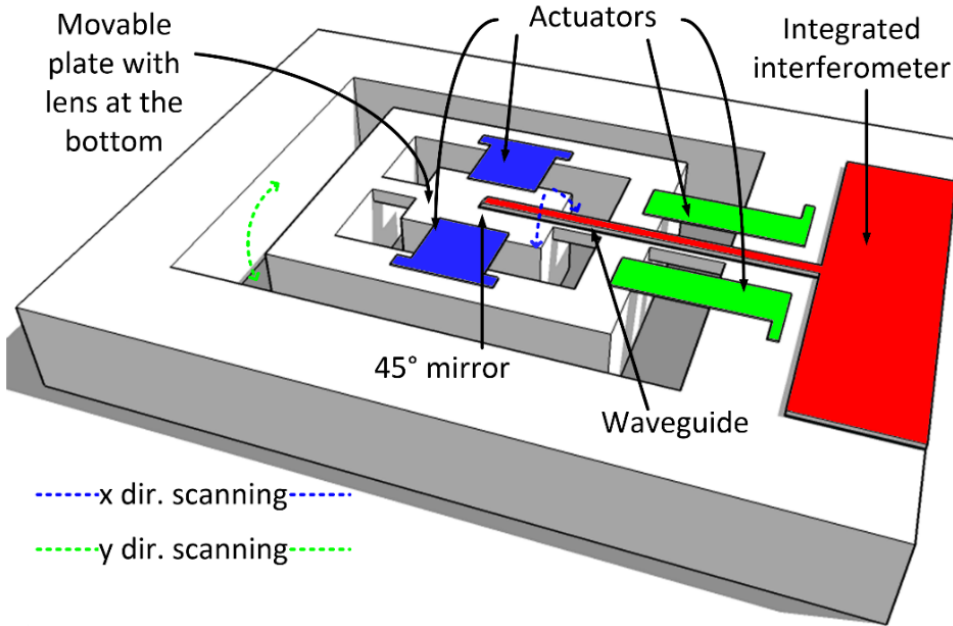


Figure 1.7: A 3D model of the new concept for an integrated 3D OCT on-chip imaging solution.

In this thesis, next to the design, fabrication and characterization of the MEMS actuator system, the integration of passive optical circuit (waveguides, mirror and lens) with the MEMS actuator system is addressed to fulfill the system specification given in Table 1.1.

Table 1.1: MEMS actuator system requirements

Parameter	Value
Power consumption	<1W
Input voltage	<12 V
Footprint	<5x20 mm ²
Rotation range in x direction	12°
Rotation range in y direction	12°

In the second chapter of this thesis the design of the integrated OCT system is presented. The chapter is split in two sections: optical components and mechanical components. The design of the photonic interferometer is provided by Medlumics S.L. Spain. Hence, in the first part, the design is presented, and key components are explained. The collimating lens is designed to be made from silicon and the detailed analysis provides the final geometrical parameters of the Si microlens. The second part explain the design

of all mechanical components of the system. First, the mechanical support is analyzed, and the most suitable torsional hinge configuration is determined. Then, the geometrical parameters for the x and y direction MEMS actuator system are derived using numerical computational models. The parameters are chosen to fulfill the system requirements given in Table 1.1. The outcome of the second chapter is a system layout design.

In the third and fourth chapters, the fabrication process developed for respectively the optical components and the MEMS actuator systems are presented and discussed in detail. The waveguide fabrication process is transferred from VTT, Finland. The fabricated photonic circuit was tested at Medlumics after the technology transfer was completed. Then, the full process development for lens fabrication is introduced. The process uses the thermal reflow of photoresist and dry plasma etching. Both steps are thoroughly analyzed and optimized in the Else Kooi Laboratory (EKL). Further, a short description of how to make 45° facets in Si is presented. The integration of all the optical components and the characterization of the fabricated devices conclude the third chapter.

The MEMS actuator system fabrication process is first developed without the optical components, but the process is designed to be fully compatible with the rest of the system. All critical steps in the process flow are investigated to find the best processing parameters. The measurement setup and characterization procedure are provided, and the electrothermal and electromechanical characterization of the fabricated MEMS devices reported. Finally, the performance of the devices is shown, and compared to the expected results given in chapter 2.

Finally, chapter 5 reports the integration process of the photonic platform given in chapter 3 with the MEMS actuator system presented in chapter 4. The integrated device is characterized both electromechanically and optically. The optical surface scanning is demonstrated using CCD camera. In chapter 6, the main conclusions of this work and recommendations for future work are provided.

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2

SYSTEM DESIGN

Have no fear of perfection — you'll never reach it.

Salvador Dalí

In this chapter the design of the integrated OCT system is introduced. The optimal geometry of all system components is determined based on the envisioned functionality and system requirements as given in Table 1.1. First, the geometry of the optical components, based on VTT photonic circuit layout, is presented and then the Si microlens design is illustrated. Next, mechanical hinges geometries for the mechanical concept illustrated in Fig. 1.7 are analyzed, and possible configurations are simulated and characterized. Test hinges are fabricated and tested to validate the simulation models and identify the most suitable configuration to be implemented in the final device. Finally, the MEMS actuators are described, and their dimensions are optimized to achieve the required motion range.

Parts of this chapter have been published in "A MEMS Actuator System for an Integrated 3-D Optical Coherent Tomography Scanner", *Journal of Microelectromechanical Systems* **27**(2), 259-268 (2018); in "An Integrated Photonic Platform for A Single-Chip MEMS-Based Optical Coherent Tomography Scanner", *Micromachines*, Under Review and in "A Monolithically Integrated MOEMS Scanner for A Single-Chip OCT Imaging Solution", To be submitted to *Journal of Microelectromechanical Systems*.

2.1. OPTICAL COMPONENTS

THE integrated OCT system concept presented in Fig. 1.7 consists of both mechanical (hinges and actuators) and optical components (waveguide, mirror and lens). The purpose of the waveguide photonic circuit is to define the optical path into the interferometer configuration needed to generate an OCT image. The mirror and the lens are also part of the interferometer. The mirror deflects the light towards the sample to be scanned, while the lens provides the desired light beam shape, either focused or collimated.

2.1.1. PHOTONIC CIRCUIT

The operating wavelength for dermatology OCT application is $1.32\ \mu\text{m}$, a wavelength for which silicon is transparent. The whole interferometer is designed by Medlumics S.L. (Fig. 2.1), in a thick silicon on insulator ("Thick SOI") photonic integrated circuit (PIC) technology developed at VTT [1-3]. These $3\ \mu\text{m}$ thick waveguides have a high refractive index contrast with the cladding materials (SiO_2 , SiN , Al_2O_3). This provides a high confinement factor and results in low bending losses and significantly reduced geometrical birefringence.

The interferometer, schematically depicted in Fig 2.1, consists of a single light input, a reference loop and a measurement path with two outputs. The light from a $1.32\ \mu\text{m}$ super luminescent emitting diode (SLED) source is split into light signals (beams). One light signal is used as measurement signal and goes through the measurement arm, deflects from the mirror towards the lens and illuminates the sample. The reflected light from the sample travels the same path backwards. The other part of the input light signal is used as a reference. Then, these two signals are recombined. Further, the recombined sample-measurement signal is split into two identical signals to improve signal to noise ratio (SNR) with the so-called balanced detection.

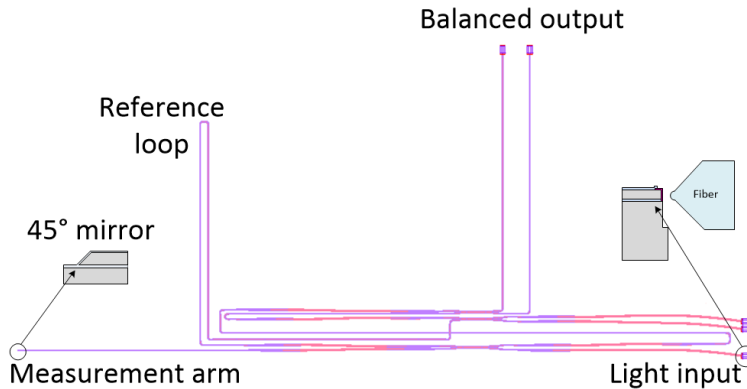


Figure 2.1: Interferometer design for integrated OCT imaging system(Medlumics, S.L.).

The interferometer consists of rib and ridge waveguides, rib to ridge waveguide converters and 2×2 multi modal interferometers (MMIs) for beam splitting and recombination (Fig. 2.2). The light is coupled (Fig. 2.1) to the rib waveguide. If the waveguide width

w_{wg} , step height h_{wg} and total height H_{wg} satisfy the following relationship:

$$\frac{w_{wg}}{H_{wg}} < 0.3 + \frac{\frac{h_{wg}}{H_{wg}}}{\sqrt{1 - \left(\frac{h_{wg}}{H_{wg}}\right)^2}} \quad (2.1)$$

and $h_{wg} > H_{wg}/2$, while $H_{wg} \geq 2\lambda$, the waveguide will confine always one mode independently of the light wavelength [4] as required for OCT imaging. The drawback of these waveguides is that they require mm size bending radius, thus the footprint of the PICs with rib waveguides is large. On the contrary, ridge waveguides using S and Euler bends can have radii down to 1 μm without significant losses and preserve guided modes. Hence, the light is coupled into a rib waveguide that is converted into a ridge waveguide to reduce the PIC footprint. The waveguide parameters of the commercially available VTT “thick SOI” PIC technology for OCT imaging are reported in Table 2.1.

Table 2.1: VTT “thick SOI” waveguide parameters for OCT imaging

Parameter	Value
Waveguide thickness H_{wg}	3 μm
Waveguide step height h_{wg}	1.8 μm
Buried oxide thickness t_{box}	> 1 μm
Cladding SiO ₂ layer thickness t_{clad}	240 nm
Antireflective SiN layer thickness t_{arc}	165 nm

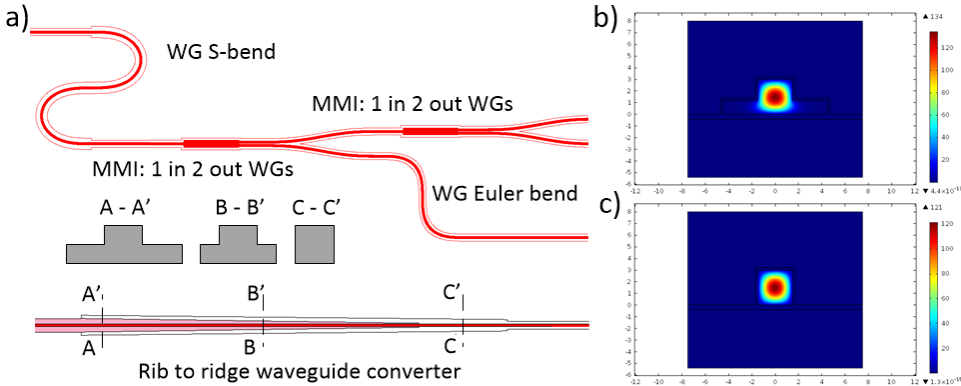


Figure 2.2: The “Thick SOI” PIC: (a) Geometry (top view and cross section) of S-bends, Euler bends, MMI and rib to ridge converter. Optical power distribution of fundamental mode for (b) rib waveguide with $w_{wg} = 3 \mu\text{m}$, $h_{wg} = 1.8 \mu\text{m}$ and $H_{wg} = 3 \mu\text{m}$; and (c) ridge waveguide with $w_{wg} = 3 \mu\text{m}$ and $H_{wg} = 3 \mu\text{m}$ with buried oxide thickness of 440 nm.

These dimensions satisfy Eq. 2.1 for an input light of 1.32 μm , thus defining single mode operation for the whole SLED bandwidth. These commercially available wave-

guides are tested for optical losses to determine a reference optical performance. The 1 cm long straight reference waveguide with two rib-to-ridge converters including light coupling, gave a total optical loss of 2 dB, while the measured numerical aperture NA_{air} for ridge waveguides is 0.38 in air. Since the standard buried oxide thickness of 1 μm can introduce stress related problems during the fabrication of the integrated OCT system, the buried oxide thickness is reduced. A thickness of 440 nm is chosen, to still be above the minimum required oxide thickness (400nm) for proper light confinement.

2.1.2. SI MICROLENS

To obtain high quality OCT images, the signal to noise ratio must be high. All light from the measurement arm must be directed to a single point which creates one pixel of the image. Thus, the focusing lens, which is at the output of the OCT scanner, should be directly fabricated at the backside of the integrated OCT chip as proposed in Chapter 1. However, once the waveguide-mirror-lens block is tilted, the sample will not be in focus anymore (Fig. 2.3a). Also, the OCT chip with integrated focusing lens can be used for only a predefined working distance.

A configuration with collimated lens requires an additional focusing lens for which assembly is needed. Due to the properties of a collimated beam, this configuration is less sensitive to alignment (Fig. 2.3b). Moreover, light will not lose focusing during lens actuation (Fig. 2.3c). Due to alignment insensitivity and preservation of the focal plane during scanning, the collimating beam configuration is more robust compared to a direct focusing system. In addition, the chip with collimated beam at the output can be used in systems with different working distances. To preserve system resolution, focusing lens must have high numerical aperture.

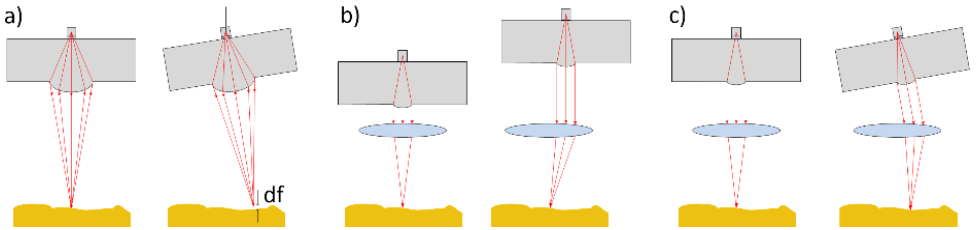


Figure 2.3: Lens actuation: (a) Defocusing during scanning with focusing integrated lens (b) Alignment insensitivity and (c) focus plane preservation during scanning due to collimated beam properties.

The collimated microlens can be made as a spherical, Fresnel or planar binary optic lens. Fresnel and binary optic lenses are diffractive optical components; thus, their design strongly depends on the wavelength used. They are sensitive to chromatic aberrations when broadband light is used. If the refractive index of the material has a low chromatic dispersion, then the spherical lens has a high bandwidth. For the bandwidth of 1.32 μm wavelength super luminescent light emitting diode source, silicon has low chromatic dispersion [5], making Si spherical lens the best choice to collimate the light at the output of the interferometer optical path.

The goal is to collect at the chip backside the light beam diverged from the 45° facet into the chip (Fig 2.1). The integrated lens ensures intrinsic alignment with the other

components. To have good quality images, low surface roughness for all the optical components, i.e. less than 1/10 of the working wavelength in the medium, is required. This means that for the single chip OCT system operation at 1.32 μm wavelength in Si, the roughness of the Si microlens must be below 38 nm.

The first element to consider for the design of the Si lens is the focal length, which is the distance from the focal point and the lens surface. If a point light source is placed in the focal point, the refracted/reflected beams from the spherical surface will be parallel. Also, the focal point of a spherical surface is determined as the cross section point of incident parallel light beams. The Si microlens is formed as a spherical surface separating solid silicon from air (Fig. 2.4).

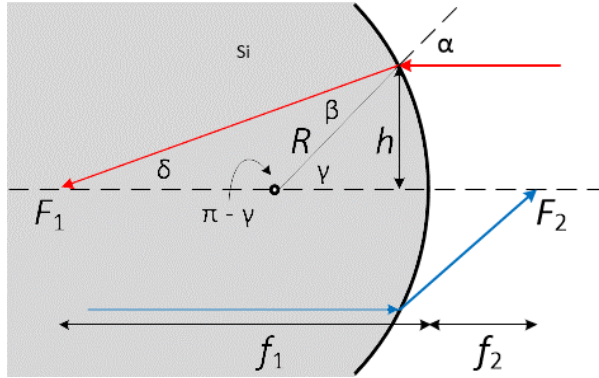


Figure 2.4: Illustration of focal point formation on a Si spherical surface. The focal point in Si is illustrated by the light beam (red line) while the focal point in air is illustrated by the blue line.

Using Gauss approximation for α , β , γ and δ , the height h (Fig. 2.4) can be expressed as:

$$h = f_1 \cdot \tan \delta \approx f_1 \cdot \delta \quad (2.2)$$

$$h = R \cdot \tan \gamma \approx R \cdot \gamma \quad (2.3)$$

where R is Si surface radius of curvature, f_1 is focal distance in Si, α is the incident and β is the refracted angle of the light beam. Both α and γ are angles formed by parallel lines, therefore

$$\alpha = \gamma. \quad (2.4)$$

Further, by the triangle postulate we have:

$$\delta + \beta + \pi - \gamma = \pi \rightarrow \delta + \beta = \gamma = \alpha \quad (2.5)$$

Angles α and β are related through the Snell's law:

$$n_{air} \cdot \sin \alpha = n_{Si} \cdot \sin \beta \Rightarrow n_{air} \cdot \alpha = n_{Si} \cdot \beta \quad (2.6)$$

Finally, by combining Eq. 2.2-2.6, the focal length in Si can be expressed as:

$$f_1 = R \cdot \frac{n_{Si}}{n_{Si} - 1} \quad (2.7)$$

and following the same procedure, the focal length in air can be expressed as:

$$f_2 = R \cdot \frac{1}{n_{Si} - 1}. \quad (2.8)$$

2

The lens equation gives information about the image position, namely:

$$\frac{1}{l_o} + \frac{1}{l_i} = \frac{1}{f} \Rightarrow l_i = \frac{l_o \cdot f}{l_o - f} \quad (2.9)$$

where l_o is the object (mirror) distance from the lens, l_i is the image distance from the lens and f is focal length of the lens in Si, given by Eq. 2.7. If the image distance is negative, the image projection is virtual, i.e. it is on the same side as the object, and the beam is diverging. If the image distance is infinite, the beam is collimated, and the image projection is at infinity. Finally, if the image distance is positive the image projection is real, and light can be focused at one point. This is schematically illustrated in Fig. 2.5.

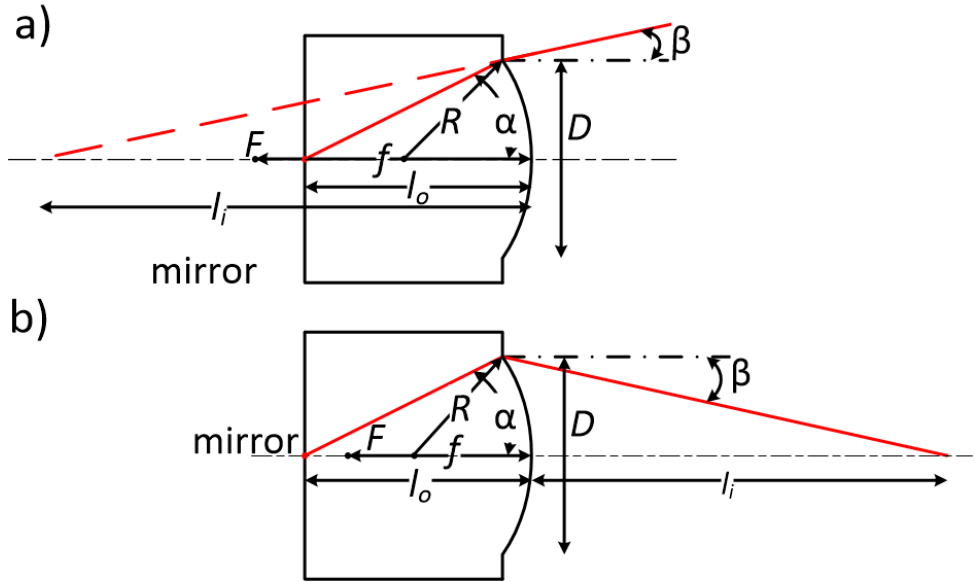


Figure 2.5: (a) Diverging mirror-lens configuration (b) Converging mirror-lens configuration.

The diverging/converging angle is defined at the edge of the Si microlens. Figure 2.5 shows that $D/2$ of the lens equals to:

$$\frac{D}{2} = -l_i \cdot \tan \beta = \frac{l_o \cdot f}{l_o - f} \cdot \tan \beta. \quad (2.10)$$

Therefore, the divergence angle β is defined as:

$$\beta = \arctan \left(\frac{D \cdot (f - l_o)}{2 \cdot f \cdot l_o} \right). \quad (2.11)$$

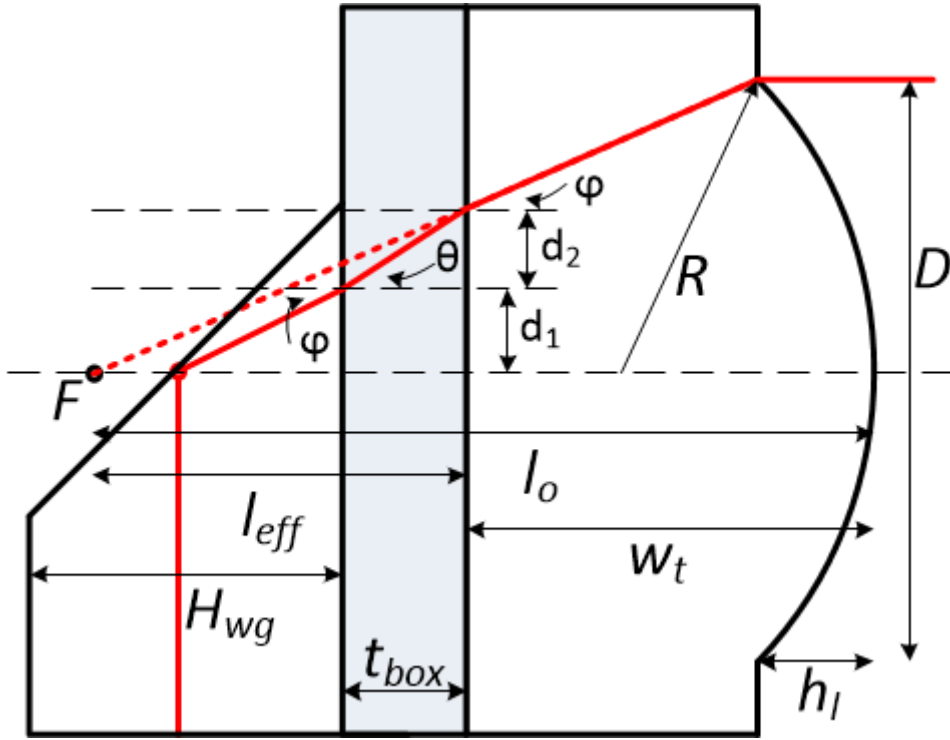


Figure 2.6: (a) Diverging mirror-lens configuration (b) Converging mirror-lens configuration.

To have a collimated beam, focal length and object distance must be equal. The beam is reflected from the mirror and deflected towards the lens through the buried SiO₂ and then through the bulk Si from which the lens is made (Fig. 2.6). Due to differences in refractive index of Si and SiO₂, the object distance cannot be defined as the simple sum of wafer thickness w_t , buried oxide thickness t_{box} , and half the thickness of the waveguide H_{wg} . It must be expressed as:

$$l_o = l_{eff} + w_t. \quad (2.12)$$

If ϕ is the incident angle of the beam, l_{eff} is given by:

$$l_{eff} = \frac{d_1 + d_2}{\tan \phi}. \quad (2.13)$$

where

$$d_1 = \frac{1}{2} H_{wg} \cdot \tan \phi \quad (2.14)$$

and

$$d_2 = t_{box} \cdot \tan \theta. \quad (2.15)$$

The total internal reflection is obtained for incident angles higher than:

$$\phi_{tot} = \arcsin \frac{n_{SiO_2}}{n_{Si}} = 0.432 \text{ rad}. \quad (2.16)$$

Since $\sin \phi_{tot} = 0.418 \approx \phi_{tot}$ we can apply Gauss approximation for Eq. 2.6 - 2.8. Following Srell's law for small angles we have:

$$n_{Si} \cdot \phi = n_{SiO_2} \cdot \theta \Rightarrow \theta = \frac{n_{Si}}{n_{SiO_2}} \phi. \quad (2.17)$$

Using Eq. 2.5 – 2.8 and Eq. 2.10, the object distance can be expressed as:

$$l_o = w_t + \frac{1}{2} H_{wg} + \frac{n_{Si}}{n_{SiO_2}} t_{box}. \quad (2.18)$$

The waveguide and the buried oxide thickness are already predefined to 3 μm and 0.44 μm , respectively. Thus, the object distance is determined only by the wafer thickness. Following Eq. 2.7 and Eq. 2.11, the collimated beam profile in integrated waveguide-mirror-lens configuration with fixed photonic circuit design depends only on the wafer thickness:

$$\beta = \arctan \left(\frac{D \cdot (f - l_o)}{2 \cdot f \cdot l_o} \right) = 0 \Rightarrow f = l_o \Rightarrow R \cdot \frac{n_{Si}}{n_{Si} - 1} = w_t + \frac{1}{2} H_{wg} + \frac{n_{Si}}{n_{SiO_2}} t_{box}. \quad (2.19)$$

Therefore, the lens radius of curvature for a collimated lens linearly depends on the wafer thickness:

$$R = \frac{n_{Si} - 1}{n_{Si}} \cdot w_t + \frac{n_{Si} - 1}{2n_{Si}} \cdot H_{wg} + \frac{n_{Si} - 1}{n_{SiO_2}} t_{box}. \quad (2.20)$$

which is also illustrated in Fig. 2.7.

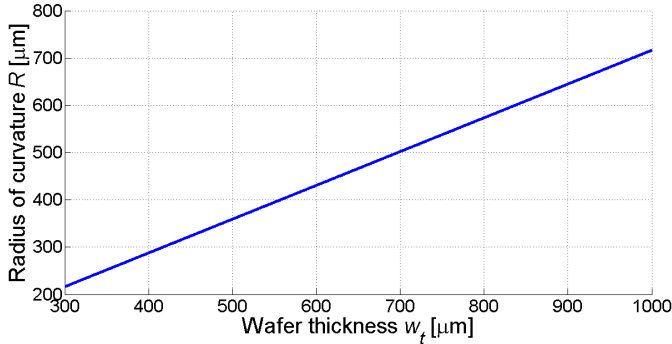


Figure 2.7: Lens radius of curvature versus wafer thickness.

The lens diameter must be large enough to collect all light coming from the waveguide and the mirror. Therefore, the lens numerical aperture $NA = \tan \theta$ must be larger or equal to the numerical aperture of the Si waveguide, namely NA_{Si} . Usually, a margin of 50% is added to the lens diameter to ensure all light from the focal point is collected. The lens diameter can be defined as:

$$D = 2 \tan \theta \cdot f = 2 NA_{Si} \cdot f = 2 \frac{NA_{air}}{n_{Si}} \cdot \left(w_t + \frac{1}{2} H_{wg} + \frac{n_{Si}}{n_{SiO_2}} t_{box} \right) \quad (2.21)$$

where NA_{air} is the waveguide numerical aperture in air. In Fig.2.8 the lens diameter (with and without 50% margin) versus substrate thickness are given

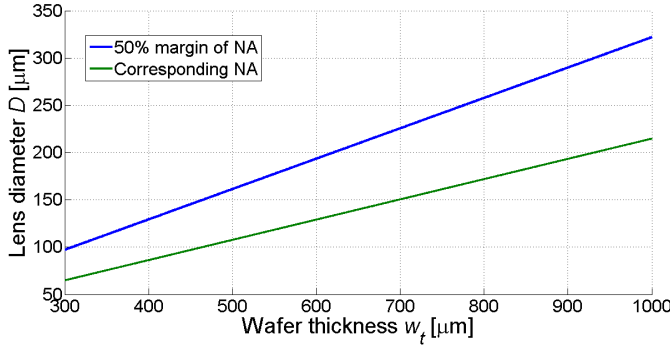


Figure 2.8: Lens diameter versus wafer thickness.

The last geometrical parameter which must be considered for the lens design is the lens height h_l (Fig. 2.6). The lens height h_l can be expressed as:

$$h_l = R - \sqrt{R^2 - \frac{D^2}{4}} \quad (2.22)$$

and depends on the wafer thickness as illustrated in Fig. 2.9.

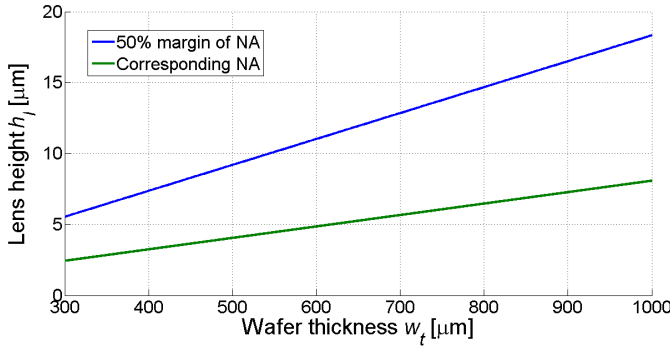


Figure 2.9: Lens height versus wafer thickness.

Considering that the waveguide parameters are already fixed, the lens design parameters are essentially determined by the wafer thickness. The whole fabrication process for the integrated OCT scanner should in the end be transferred to a foundry for production. Thus, we must use one of the standard wafer thickness for Si photonic technology (300 μm, 500 μm, 700 μm, 1 mm). Thin wafers (<500 μm) may suffer from high bow caused by the intrinsic stress in the deposited layers. On the other hand, thick wafers

(>700 μm) may be problematic for the deep silicon etching needed for the actuators fabrication (see section 4.1). Therefore, a wafer thickness of 700 μm seems to be a good compromise to reduce the stress influence on the wafer bow and avoid a challenging etching process for the final device release.

The chosen wafer thickness of 700 μm for the collimated lens translates in a radius of curvature $R = 500 \mu\text{m}$. A lens diameter $D = 150 \mu\text{m}$ is chosen based on the corresponding waveguide numerical aperture. We decided not to include the 50% increase numerical aperture margin as this would severely increase the backside topography making further fabrication of the integrated device not feasible with the equipment available in our laboratory. The minimal lateral resolution of 5 μm which can be achieved by waveguide-mirror-lens system is mainly defined its NA and Eq. 1.2. Finally, the focusing lens from Fig. 2.1 should have a focal length of 5 cm, which is equal to the defined working distance and must have $NA > 1$ not to destroy the system resolution.

2.2. MECHANICAL COMPONENTS

THE light spot movement over the sample will provide the surface scanning for OCT imaging (Fig. 2.3). The system design presented in Fig. 1.7 makes use of actuators for motion in x and y direction. The horizontal, x direction, scanning is provided by two sets of actuators tilting the microplate (waveguide-mirror-lens block) around a supporting hinge. These horizontal actuators with the microplate are integrated into a frame. The frame is supported by a hinge and another set of actuators for vertical, y direction, scanning. The system requirements are defined in Table 1.1 Thus, a suitable mechanical system which supports the integrated waveguide-mirror-lens block (Fig. 2.3) and provides a 12° angular translation is needed.

2.2.1. MECHANICAL HINGES

CENTRAL HINGE

The mechanical support for the integrated waveguide-lens block must ensure proper positioning of the bulk Si microplate (the block) and at the same time provide mechanical support to the measurement arm waveguide. Figure 2.10 depicts the angular displacements of the microplate for both x and y direction scanning. The hinges supporting the microplate and the frame must be flexible enough to reduce the force needed for the actuation and at the same time, stiff enough to withstand the actuation force without failure. The actuators for x direction scanning (Fig. 1.7) will tilt the microplate around a torsional hinge (Fig. 2.10a). The y direction scanning is achieved by deflecting the supporting hinge with actuators, providing out-of-plane displacement of the frame (Fig. 2.10b).

The **torsional hinge** must have a low torsion spring constant k_θ but it must be stiff enough to withstand any force on the microplate in the vertical direction, i.e. should have a high k_z . There is a variety of torsional hinge designs used in numerous applications, such as Lamina Emergent Torsional (LTE) joints [6,7], serpentine [8,9] and many other shapes [10,11]. However, we must here also consider that during the torsion, the waveguide will be twisted which result in built-in stress. This stress consequently changes the material refractive index n . Figure 2.11 compares a simple straight hinge and a ser-

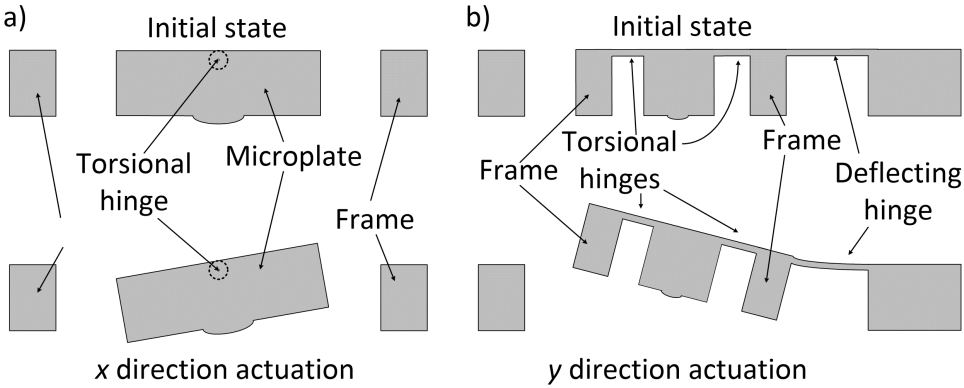


Figure 2.10: Microplate and frame motion during actuation: (a) Tilted microplate within the supporting frame for x direction scanning. (b) Out-of-plane displacement of the frame by deflecting the supporting hinge for y direction scanning. Actuators are not shown for simplicity sake.

pentine hinge with the same torsional stiffness, when a waveguide is placed on top.

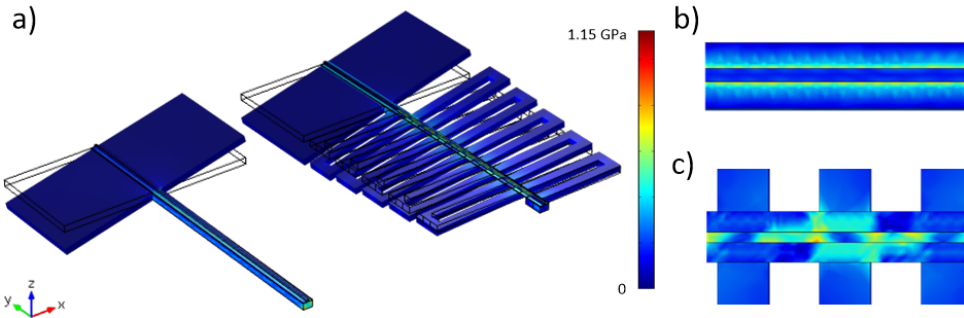


Figure 2.11: Comparison of simple straight and serpentine hinge with a waveguide on top: (a) FEM calculation of the stress in the waveguide. Stress distribution in (b) straight (c) serpentine hinge.

Finite element method (FEM) stress calculations are presented in Fig. 2.11a, while stress distribution in the waveguide is given in Fig. 2.11b-c. The straight hinge provides a constant stress in the waveguide, while the serpentine gives discrete jumps of stress among the suspended and the supported waveguide regions. Since the refractive index of the material also depends on the stress, there will be discrete jumps in n along the waveguide. This can increase optical losses, create a lot of internal reflections, influence the birefringence etc. Thus, stress distribution in the waveguide must be uniform, a condition that can be met only with a straight hinge configuration.

As the waveguide has to be placed on top of the torsional hinge, the minimal width of this hinge will be dictated by the photonic circuit design. In our case, the width of the torsional hinge cannot be smaller than $15\text{ }\mu\text{m}$. The torsional stiffness of a straight beam is defined by its material properties as well as its cross-section area and its length. A smaller cross-section and a longer beam will result in lower stiffness. To minimize

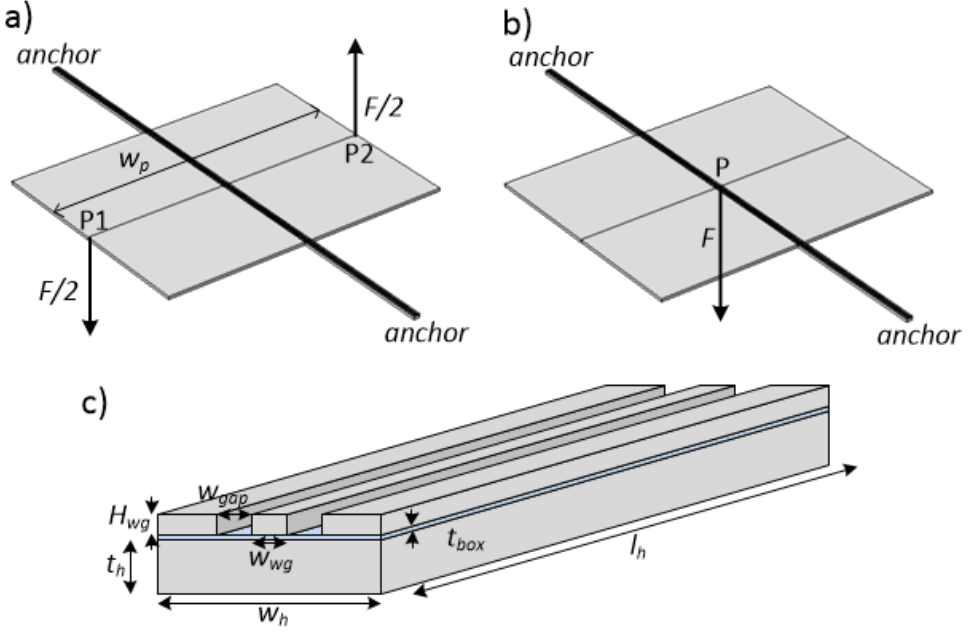


Figure 2.12: Geometry of a straight hinge with the measurement arm waveguide.

stress, and consequently optical losses, the waveguide must be as close as possible to the neutral axis of rotation, meaning the hinge should be as thin as possible. Drawback of a thin hinge is the mechanical fragility and the low spring coefficient k_z in the vertical direction. Therefore, a compromise must be found. To do this a FEM simulation of the hinge geometry is carried. To calculate torsional stiffness k_θ , a force $F/2$ is applied at both edges of the plate with opposite directions (Fig.2.12a). The hinge torque τ can be expressed as:

$$\tau = \frac{1}{2} F \cdot w_p = k_\theta \cdot \Delta\theta \quad (2.23)$$

where w_p is the plate width and $\Delta\theta$ is the angular displacement defined by the vertical displacement Δz of points P1 and P2:

$$\theta = \arctan\left(\frac{|\Delta z_{P1} - \Delta z_{P2}|}{w_p}\right). \quad (2.24)$$

For the analysis of the vertical stiffness k_z , the force F is applied at the center of the plate (Fig. 2.12b). The force is directly proportional to the vertical displacement of the point P:

$$F = k_z \cdot \Delta z_p \quad (2.25)$$

The geometrical parameters of a straight hinge with a waveguide on a top are illustrated in Fig. 2.12c, while the values are summarized in Table 2.2.

This geometry is analyzed using FEM computation model in Comsol Multiphysics. The computational results for k_θ and k_z are given in Fig. 2.13 to Fig. 2.15, respectively.

Table 2.2: Geometrical parameters in FEM simulations for hinge analysis

Parameter	Value
Hinge length l_h	300 - 700 μm
Hinge width w_h	15 - 40 μm
Hinge thickness t_h	5 - 30 μm
Waveguide with w_{wg}	3 μm
Waveguide thickness H_{wg}	3 μm
Gap around the waveguide w_{gap}	3 μm
Buried SiO ₂ thickness t_{box}	0.44 μm

First, the torsional k_θ and vertical k_z hinge stiffness versus hinge length for several combinations of hinge width and thickness values is presented in Fig. 2.13. The hinge length is set to 500 μm as a compromise between low k_θ and high k_z . Next, in Fig. 2.14 the influence of the hinge width w_h on k_θ and k_z for $l_h = 500 \mu\text{m}$ and variable thickness.

The width is set to 20 μm , a value for which the torsion constant is still low, but the vertical elastic constant is high. Finally, after the length and the width are chosen, the hinge spring constants k_θ and k_z versus hinge thickness t_h are analyzed. The results are presented in Fig. 2.15. Following the same reasoning to compromise between k_θ and k_z , the hinge thickness is set to 10 μm .

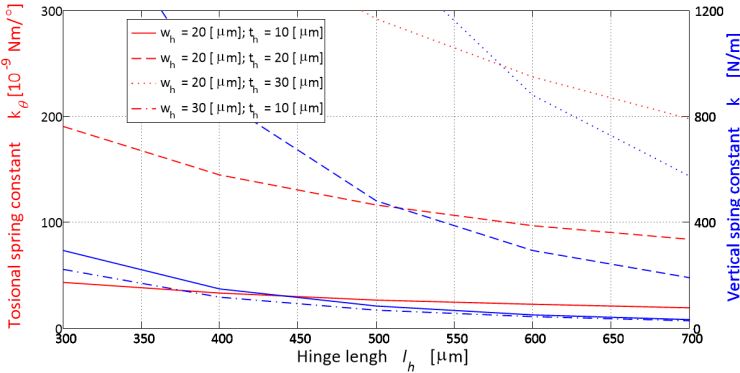


Figure 2.13: Influence of hinge length on: torsional spring constant k_θ (red lines) and vertical spring constant k_z (blue line) for several combinations of w_h and t_h .

The presented analysis for the torsional hinge supporting the optical waveguide permits to derive the optimum design specification for a straight rectangular hinge. A trade-off between low torsional spring constant k_θ and high vertical stiffness k_z is necessary. Also, the influence of hinge dimensions on the total stress in the waveguide has to be considered. The geometrical parameters determined for the optimum rectangular straight hinge (Fig. 2.12c) are summarized in Table 2.3.

The **deflecting hinge** geometry is dictated by the y direction scanning actuator system footprint (Fig. 1.7), as well as by the optical circuit and the electrical circuit for powering the x direction scanning actuator system. The deflecting hinge should be a straight

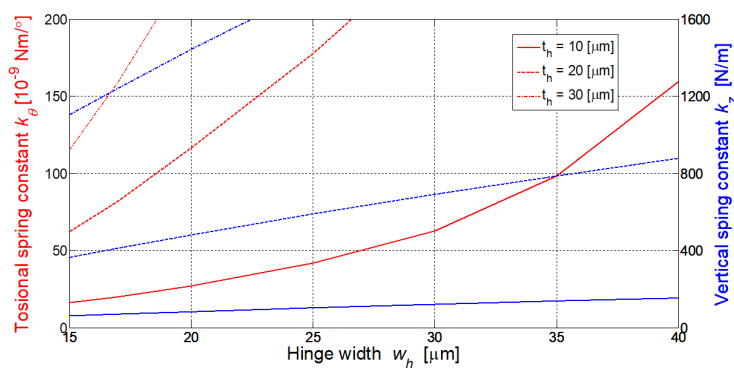


Figure 2.14: Influence of hinge width on: torsional spring constant k_θ (red lines) and vertical spring constant k_z (blue line). The hinge length l_h is set to 500 μm while the hinge thickness t_h is varied between 10 μm and 30 μm .

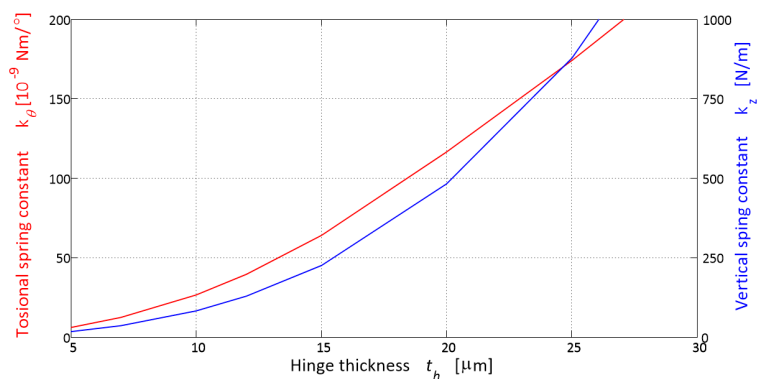


Figure 2.15: Influence of hinge thickness on: torsional spring constant k_θ (red lines) and vertical spring constant k_z (blue line). The hinge length l_h and hinge width w_h are set to 500 μm and 20 μm respectively.

Table 2.3: Geometrical parameters of torsional hinge

Parameter	Value
Hinge length l_h	500 μm
Hinge width w_h	20 μm
Hinge thickness t_h	10 μm
Waveguide width w_{wg}	3 μm
Waveguide thickness H_{wg}	3 μm
Gap around the waveguide w_{gap}	3 μm
Buried SiO_2 thickness t_{box}	0.44 μm

thin hinge which, in combination with actuators, should support the Si frame with the x direction scanning system. Since, both x and y scanning systems must be compati-

ble from both design and fabrication point of view, the deflecting hinge must have the same thickness as the torsional hinge. Based on the proposed design shown in Fig. 1.7, the hinge length should be equal to the length of the actuators system for y direction scanning and should be optimized together with the actuator design. Therefore, a dedicated analysis of the deflecting hinge will be included with the overall actuator design in section 2.2.2.3 of this chapter.

SIDE HINGES

The torsional hinge with the waveguide on top is designed as a straight hinge with a rectangular cross section. The integrated waveguide-mirror-lens block is combined into a single bulk Si microplate (Fig. 1.7). The mass of this microplate will cause the hinge with the waveguide to bend, resulting in a rotational-translation motion instead of only rotational motion around one rotational axis. Adding an extra pair of hinges next to the central one will increase the total vertical spring constant k_z . Without side hinges, the total spring constant is only the central hinge vertical spring constant k_{zc} . An extra pair of side hinges with a vertical spring constant k_{zsh} will increase k_z to $k_{zc} + 2 \cdot k_{zsh}$ (Fig. 2.16a). Hence, to increase the vertical spring constant, while keeping the same k_θ , the influence of different side hinge geometries is investigated using a FEM computational model. To validate the model, test hinges are fabricated in crystalline Si and their torsional stiffness is compared to the model. To simplify the test, these hinges do not carry waveguides.

In all designs, the central hinge is the simple straight beam, as it carries the waveguide and must provide proper light confinement (Fig. 2.11). Additional side hinges with straight, triangular and circular shape have been considered. In Fig. 2.16b the investigated shapes and their parameters are depicted, while the parameter values are presented in Table 2.4. The central hinge width was fixed at $15 \mu\text{m}$, the minimum value as determined by the photonic circuit constraints.

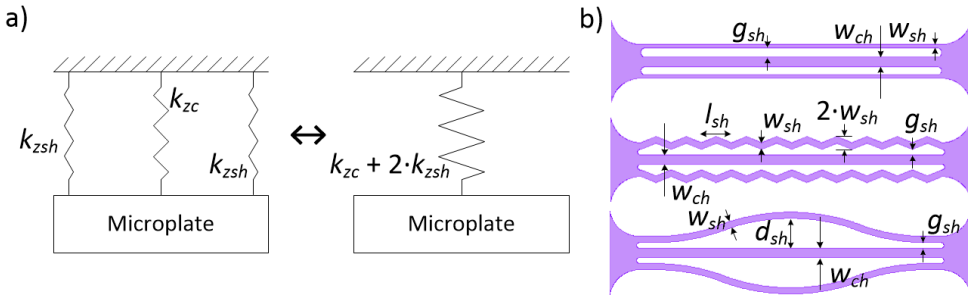


Figure 2.16: Side hinges: (a) Influence of the side hinge on the vertical spring constant (b) Geometry of side hinges which should provide larger k_z .

The total vertical and torsional spring constant is calculated using FEM calculations for each specific configuration of the side hinge geometry. Both values are compared with the initial straight hinge (geometry parameters presented in Table 2.3). The difference for k_θ and k_z between initial hinge and specific side hinge configuration is reported in Table 2.5. Presented results show that all designs have improved vertical stiffness from

Table 2.4: Geometrical parameters of side hinges

Parameter	Value
Central hinge width w_{ch}	15 μm
Number of side hinges N_{sh}	2 - 10
Side hinge width w_{sh}	5 - 10 μm
Side hinge gap g_{sh}	10 - 20 μm
Triangular hinge length period length l_{sh}	5 - 100 μm
Maximum side hinge distance d_{sh}	50 - 100 μm

20 up to 160%. However, not all presented hinges have lower torsional stiffness. The best result is for 2 straight side hinges. Logically, increasing the number of side hinges increases both torsional and vertical spring coefficient. Larger spring coefficients can be observed when the triangular length is increased as well. Increasing the maximum distance of circular hinge reduces vertical stiffness while increases torsional stiffness. To validate simulation results, test structures are fabricated and characterized.

Table 2.5: Comparison of side hinge geometries

Hinge type	Δk_θ	Δk_z
Straight: $N_{sh} = 2$, $w_{sh} = 5 \mu\text{m}$, $g_{sh} = 10 \mu\text{m}$	-16.99%	+21.58%
Straight: $N_{sh} = 4$, $w_{sh} = 5 \mu\text{m}$, $g_{sh} = 10 \mu\text{m}$	-2.30%	+61.48%
Triangular: $N_{sh} = 4$, $w_{sh} = 10 \mu\text{m}$, $g_{sh} = 10 \mu\text{m}$ $l_{sh} = 5 \mu\text{m}$	-9.32%	+41.48%
Triangular: $N_{sh} = 4$, $w_{sh} = 10 \mu\text{m}$, $g_{sh} = 10 \mu\text{m}$ $l_{sh} = 50 \mu\text{m}$	+89.69%	+113.75%
Circular: $N_{sh} = 2$, $w_{sh} = 10 \mu\text{m}$, $g_{sh} = 10 \mu\text{m}$ $d_{sh} = 50 \mu\text{m}$	+38.55%	+158.04%
Circular: $N_{sh} = 2$, $w_{sh} = 10 \mu\text{m}$, $g_{sh} = 10 \mu\text{m}$ $d_{sh} = 100 \mu\text{m}$	+49.63%	+49.27%

The test hinges are fabricated following the process flow schematically depicted in Fig. 2.17. First, front side definition of the structures is done by 20 μm deep silicon anisotropic etch (Fig. 2.17a). Then, a stop layer of plasma enhanced chemical vapor deposited (PECVD) layer of SiO_x is added on the front side (Fig. 2.17b). Another PECVD SiO_x is deposited and patterned at the backside as a hard mask for the second backside deep reactive ion etching (Fig. 2.17c). Then, the silicon wafer was etched from the backside until approximately 10 μm of Si is left, thus defining the hinge thickness. The mechanical structure is released by removing the oxide mask and the oxide stop layer (Fig. 2.17d). A detailed process flow chart for the fabrication of the mechanical test structures is given in Appendix A.1.

SEM images of fabricated test hinges are shown in Fig. 2.18. All presented hinges are fabricated on the same wafer and due to some non-uniformity of the etch process over the wafer surface, the hinge thickness varies between 6 and 15 μm from device to device. Yet, for each device, the thickness of a single hinge is quite uniform (within 0.5 μm).

The angular displacement of the suspended plate versus applied momentum is characterized using a stylus profilometer (*Veeco Dektak 150*). The measurement setup is shown in Fig. 2.19a. The profilometer needle applies a constant force of 0.1 mN on the surface of the plate. During the measurement, the needle records vertical displacement

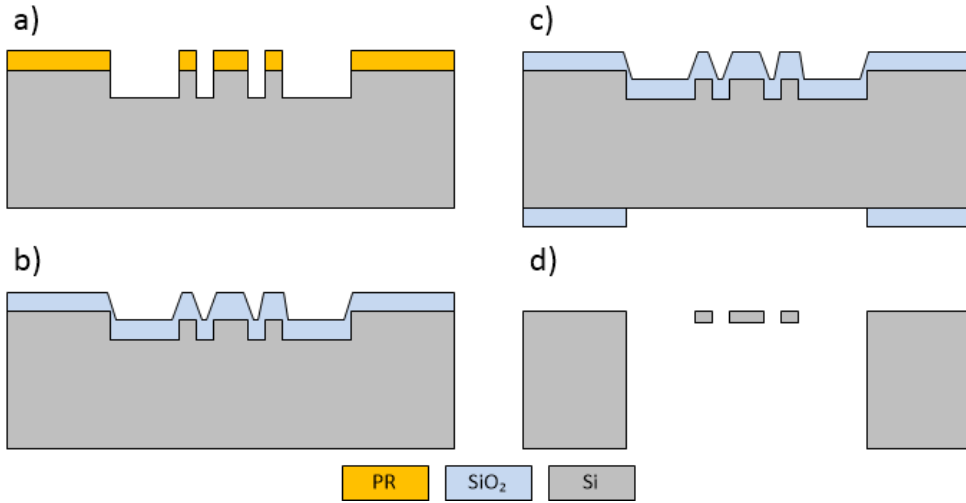


Figure 2.17: Main process steps for the test hinges fabrication: (a) Photolithography for hinge geometry definition and frontside 20 μm deep silicon anisotropic etching; (b) 5 μm thick PECVD SiO_x stop layer deposition; (c) 5 μm thick PECVD SiO_x backside hard mask deposition and patterning; (d) Backside silicon etching until 10 μm thick hinge is left and mechanical release of the defined hinge by oxide stop layer removal.

of the tip and its horizontal position. To calculate the applied momentum and the angular displacement for a central hinge of $w_{ch} = 15 \mu\text{m}$ with 4 straight side hinges of 5 μm width and 10 μm gap, the raw data is translated in both x and z directions to have the center of the hinge at (0,0) position (Fig. 2.19b). Having vertical z and horizontal x distance relative to the center of the plate, the angular displacement and applied momentum can be calculated as:

$$\alpha = \arctan\left(\frac{z}{x}\right), \quad (2.26)$$

$$M = F \cdot x. \quad (2.27)$$

A comparison between measurement and numerical results for different side hinges configurations is presented in Fig. 2.20. The hinge thickness used in the numerical calculation is measured using SEM and the average value is within 0.5 μm accuracy. Good matching between simulated and measured values indicates that the FEM model is sufficiently accurate and can be used to define the most suitable configuration.

Following the validation of FEM simulation model, the final hinge geometry can be finalized based on presented results in Table 2.5. The straight side hinge design with 2 and 4 side hinges and the triangular side hinge with l_{sh} of 5 μm show improvement in torsional stiffness. Among these 3 designs, the 4 straight side hinge design has the highest vertical spring constant. Thus, this design is chosen and the final torsional hinge geometry. The parameters are summarized Table 2.6.

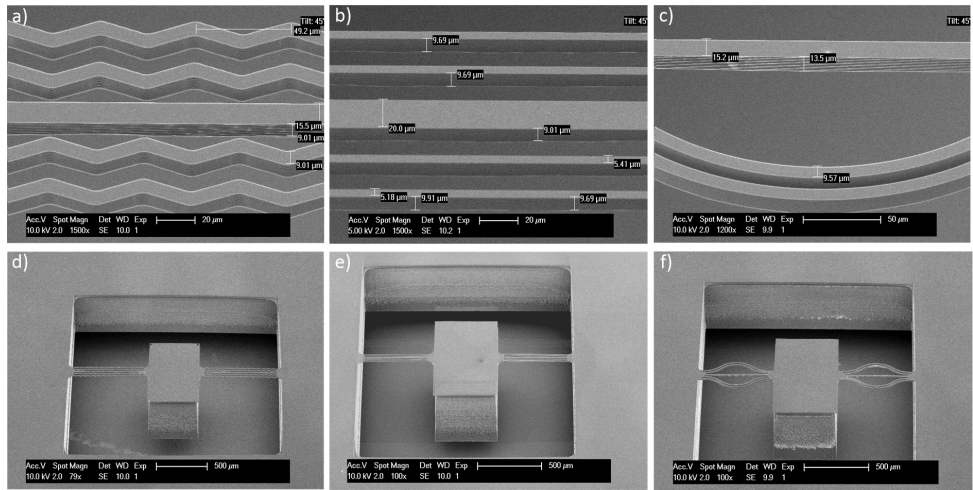


Figure 2.18: SEM images of some fabricated test hinges: Close look of (a) Triangular side hinges: $w_{ch} = 15 \mu m$, $N_{sh} = 4$, $w_{sh} = 10 \mu m$, $g_{sh} = 10 \mu m$ and $l_{sh} = 50 \mu m$; (b) Straight side hinges: $w_{ch} = 15 \mu m$, $N_{sh} = 4$, $w_{sh} = 5 \mu m$, $g_{sh} = 10 \mu m$; (c) Circular side hinges: $w_{ch} = 15 \mu m$, $N_{sh} = 4$, $w_{sh} = 10 \mu m$, $g_{sh} = 10 \mu m$, $d_{sh} = 100 \mu m$; Tilted view of a microplate supported by a central hinge and: (d) 4 triangular side hinges; (e) 2 straight side hinges; (f) 4 circular side hinges.

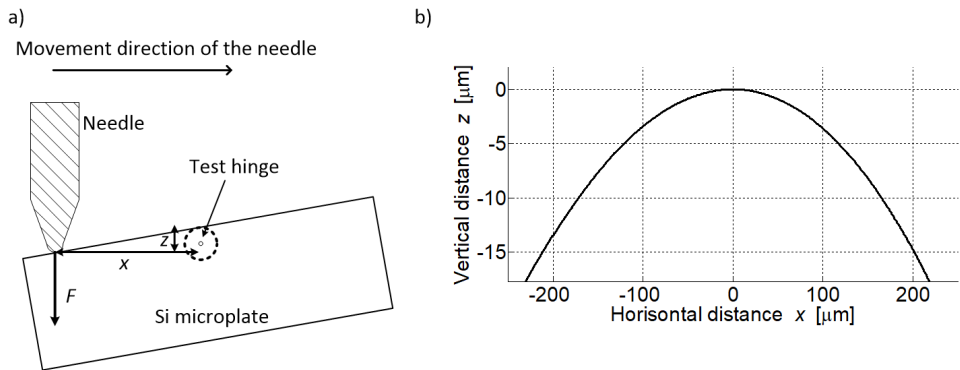


Figure 2.19: Test hinges characterization: (a) Measurement setup with the stylus profiler; (b) Measurement data of horizontal and vertical needle position.

Table 2.6: Design parameters for torsional hinge

Parameter	Value
Hinge length l_h	$500 \mu m$
Central hinge width w_{hc}	$15 \mu m$
Side hinge type	straight
Side hinge width w_{sh}	$5 \mu m$
Hinge thickness t_h	$10 \mu m$
Number of side hinges N_{sh}	4

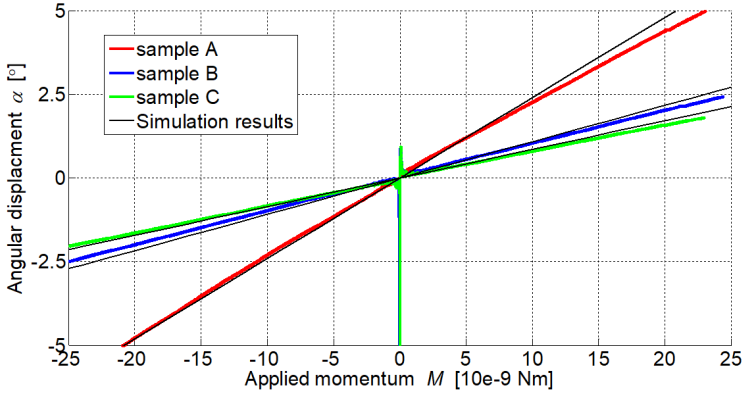


Figure 2.20: Comparison between simulated and measured hinges with central hinge width of 15 μm : Sample A - straight side hinge with $N_{sh} = 4$, $w_{sh} = 5 \mu\text{m}$, $g_{sh} = 10 \mu\text{m}$ and $t_h = 6 \mu\text{m}$; Sample B - triangular side hinge with $N_{sh} = 4$, $w_{sh} = 10 \mu\text{m}$, $g_{sh} = 10 \mu\text{m}$, $l_{sh} = 5 \mu\text{m}$ and $t_h = 7.5 \mu\text{m}$; Sample C - triangular side hinge with $N_{sh} = 4$, $w_{sh} = 10 \mu\text{m}$, $g_{sh} = 10 \mu\text{m}$, $l_{sh} = 50 \mu\text{m}$ and $t_h = 6 \mu\text{m}$;

2.2.2. ACTUATOR SYSTEM

The MEMS actuator system must provide the required angular motion range of 12° . This angular range should translate in a 1 cm linear scanning range in both directions, thus being comparable with commercially available scanners. In addition, to be suitable for a portable OCT probe, it must have the smallest footprint possible and require low operating voltage. The first step in the MEMS actuator design is the choice of the actuation principle. MEMS actuators can be grouped, based on the working principle, in electrostatic, piezoelectric, thermal and magnetic actuators.

The working principle for electrostatic actuators is the conversion of electrostatic energy into mechanical motion. The most used configurations of electrostatic actuators are comb drives (Fig. 21a). Comb drives are mainly used for lateral displacement. They can provide high force but have low displacement range [12]. To increase the motion range, the number of combs must be increased, which drastically increases the device footprint. Also, the displacement range depends on the square value of the driving voltage [13]. Typically, operating voltages of 100 V result in an 80 μm displacement range [14]. Finally, although vertical and torsional motions can be achieved with complicated combination of combs [15-17], this severely complicates the design of the system.

Piezoelectric actuators use the piezoelectric effect to convert an electrical field into a mechanical motion (Fig. 2.21b). They have a high output force (1 mN) and high displacement range (up to mm) [12]. Piezoelectric actuators are made of piezoelectric materials (quartz, PZT, AlN, ZrO and etc) which are generally not compatible with standard Si IC technology. They use high operating voltages but in resonant mode, the driving voltage can be significantly reduced [12,18]. The biggest advantage of both piezoelectric and electrostatic is the low power consumption and fast response time.

Magnetic actuators use the Lorentz force in a magnetic field to generate the motion. They require an externally generated magnetic field and usually have densely packaged

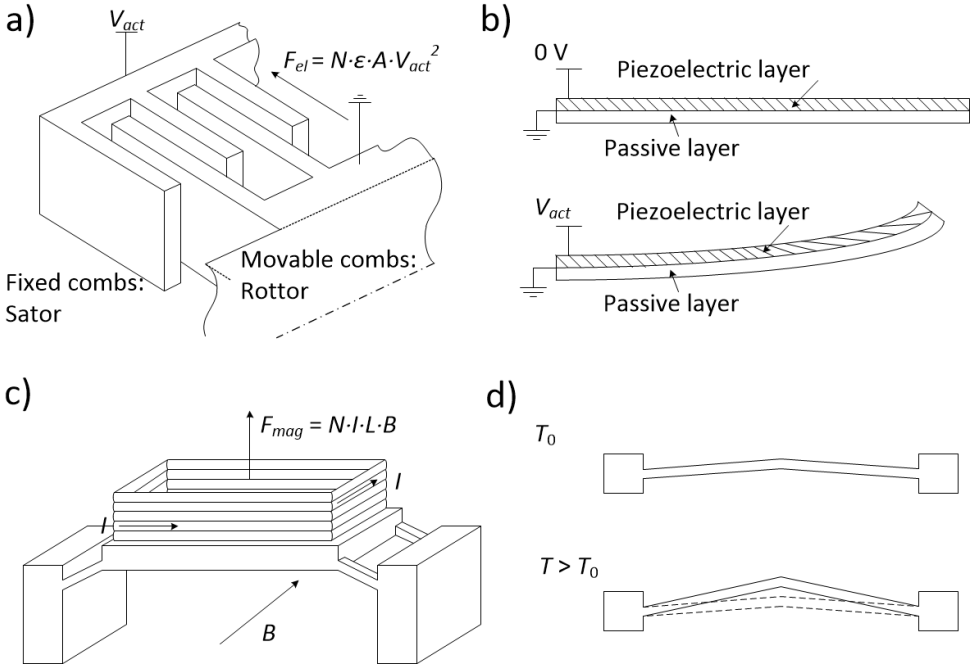


Figure 2.21: Si based MEMS actuators: (a) Electrostatic comb drive with N combs and overlap area A in a medium with electrical permittivity ϵ (usually air). Actuators are driven with voltage V_{act} . (b) Piezoelectric bimorph beam with one passive and one piezoelectric layer. The stress in the piezoelectric layer changes with applied voltage V_{act} . (c) Magnetic force applied on a MEMS coil with N turns of length L . The actuator is driven with current I and externally generated magnetic field B . (d) Thermal V-beam actuator at room temperature and during thermal actuation. Initial shape determines direction of the actuator motion.

coil fabricated on a Si chip (Fig. 2.21c) [19-21]. They have low output force that can be increased by increasing the size of the coil. Hence, these actuators are not the best choice for a compact, small footprint device. Also, coils have high current flow (for higher force) which implies a large power consumption. [12]. Another approach is mounting a magnet on the device [22,23]. However, for this approach additional micro assembly is needed, which is in contrast with the goal of this work, namely a fully integrated system with a minimal assembly of individual components.

Thermal actuators are based on the thermal expansion of a material, mainly using Joule heating as drive mechanism. Thus, often they are called electrothermal actuators. Electrothermal actuators can provide high output force as well as high displacement range [12]. Due to high energy density, electrothermal actuators usually have small footprint [24] and can be used for both in plane (U and V beams) and out-of-plane (bi-morph beams) motion (Fig. 2.21d). Typical in-plane displacement range is several tens of micrometers [25] while the out-of-plane displacement can be up to several hundreds of micrometers [26]. It is possible to amplify the motion range, using a cascade configuration with these actuators with moderate increase of device footprint.

The main characteristics of Si-MEMS actuator types are summarized in Table 2.7.

Considering the system requirements given in Table 1.1, electrostatic and thermal actuators are a better choice than piezoelectric and magnetic actuators. A big drawback of the electrostatic actuators for their application in fully integrated OCT chips is the high driving voltage and the large footprint. Electrothermal actuators are slow in response and have higher power consumption than electrostatic ones. However, as the proposed OCT system does not require a fast response time and the non-continuous operation limits the power consumption to 1 W, electrothermal actuators are selected as the best choice for our system.

Table 2.7: Actuator type systems

Parameter	Electrostatic	Piezoelectric	Magnetic	Thermal
F [μN]	$10^0 - 10^2$	10^4	10^5	$10^1 - 10^2$
P [W]	0	0	1	<0.5
CMOS	High	Low	High	High
Footprint	1 mm^2	0.01 mm^2	1 mm^2	0.01 mm^2

As the integrated system given in Fig. 1.7 requires out-of-plane motion of the microplate and the frame, among all Si based thermal actuators, **electrothermal bimorph beams** are the straightforward choice among all thermal actuators. These actuators have already been proven as a good choice for OCT application [27-29]. To increase the motion range of bimorph actuators, metal and insulator [26,27], metal and semiconductor [28,29] or metal with polymer [30,31] are used as materials for the bimorph beam.

ELECTROTHERMAL AL-SiO_x BIMORPH BEAM

A bimorph is a two-layer structure made of different materials. In Si MEMS technology, an electrothermal bimorph actuator is usually a beam or a cantilever made of two layers with different coefficient of thermal expansion α_{cte} . Once the actuator is heated up, the layer with larger α_{cte1} tends to expand more than the layer with lower α_{cte2} . However, since both layers are forming the bimorph they cannot expand independently, which results in building up stress in both layers. The built-up stress will cause a deflection of the beam (Fig. 2.22a).

In microfabrication technology the two layers forming the bimorph are deposited using different deposition techniques, which often takes place at a temperature above room temperature. The difference in coefficient of thermal expansion of the bimorph layers, as well as with respect to the Si substrate, results in building up stress in each layer, once the substrates are cooled to room temperature. This built in stress causes a deformation of the final structure upon release (Fig. 2.22b).

The maximum deflection of the bimorph beam can be expressed through its radius of curvature [26] as:

$$d_0 = r_0 \cdot (1 - \cos \phi_0) = r_0 \cdot \left(1 - \cos \frac{l}{r_0}\right) \quad (2.28)$$

where l is the length and r is the initial radius of curvature of the bimorph beam (Fig. 2.22b). The radius of curvature can be expressed as:

$$r_0 = \frac{t_1 + t_2}{C \cdot \Delta \epsilon} \quad (2.29)$$

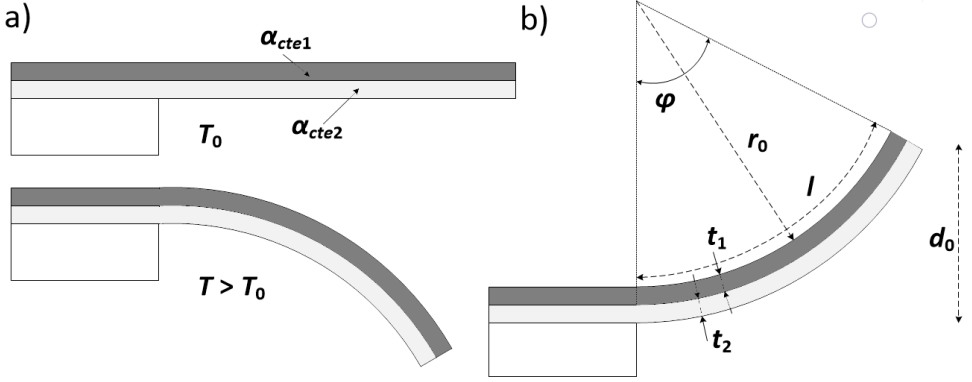


Figure 2.22: Electrothermal bimorph actuator: (a) Actuation principle (b) Actuator parameters of the pre-stressed bimorph beam.

where t_1 and t_2 are the bimorph layers thickness, C is the radius coefficient of the bimorph beam which strongly depends on the materials biaxial Young's moduli E and on geometrical parameters [26,32]:

$$C = 6 \cdot \frac{\left(1 + \frac{t_1}{t_2}\right)^2}{\frac{E_1}{E_2} \left(\frac{t_1}{t_2}\right)^3 + 4 \left(\frac{t_1}{t_2}\right)^2 + 6 \frac{t_1}{t_2} + 4 + \left(\frac{E_1}{E_2}\right)^{-1} \left(\frac{t_1}{t_2}\right)^{-1}}. \quad (2.30)$$

The strain mismatch between layers, $\Delta\epsilon$, is given by the intrinsic strain mismatch $\Delta\epsilon_{in}$ and the extrinsic strain generated during thermal actuation $\Delta\epsilon_{act}$:

$$\Delta\epsilon = \Delta\epsilon_{in} + \Delta\epsilon_{act}. \quad (2.31)$$

For the initial state, where there is no actuation, $\Delta\epsilon_{act} = 0$. Therefore, the initial radius of curvature and the deflection can be written as:

$$r_0 = \frac{t_1 + t_2}{C \cdot \Delta\epsilon_{in}} \quad (2.32)$$

$$d_0 = \frac{t_1 + t_2}{C \cdot \Delta\epsilon_{in}} \cdot \left(1 - \cos\left(\frac{l \cdot C}{t_1 + t_2} \cdot \Delta\epsilon_{in}\right)\right). \quad (2.33)$$

The mismatch of the intrinsic strain has two components:

$$\Delta\epsilon_{in} = \Delta\epsilon_T + \Delta\epsilon_{in0} \quad (2.34)$$

where $\Delta\epsilon_T$ is the strain mismatch induced by the temperature excursion during material deposition and $\Delta\epsilon_{in0}$ is induced by other deposition parameters, such as pressure,

power etc. The strain mismatch $\Delta\epsilon_T$ of a bimorph beam deposited on a silicon substrate strongly depends on deposition temperatures of both layers [26]:

$$\Delta\epsilon_T = \alpha_{cteSi} \cdot (\Delta T_1 - \Delta T_2) - (\alpha_{cte1} \cdot \Delta T_1 - \alpha_{cte2} \cdot \Delta T_2). \quad (2.35)$$

Heating the actuator will cause a strain change, $\Delta\epsilon_{act}$, in the beam. This will result in a change of beam radius of curvature as well as beam deflection. The strain change is proportional to the difference of thermal expansion coefficient and the temperature change, usually generated by Joule heating:

$$\Delta\epsilon_{act} = (\alpha_{cte1} - \alpha_{cte2}) \cdot \Delta T_{act}. \quad (2.36)$$

To maximize the beam deflection during the actuation, the difference in α_{cte} must be as large as possible. Table 2.8 gives the Young's moduli and coefficient of thermal expansion values for Si [33,34], SiO_x [35,36], SiN [37,36], SiC [38,39], Al [40,41], Mo [40] and Ti [40] which are the CMOS compatible materials available in our laboratory.

Table 2.8: Material properties

Parameter	Si	SiO _x	SiN	SiC	Al	Mo	Ti
E [GP]	169	50 - 70	146 - 290	120 - 334	60 - 70	329	116
α_{cte} [10 ⁻⁶ 1/K]	2.43 - 2.60	0.60	1.19 - 3.89	4.30	23	4.80	8.60

The biggest mismatch of α_{cte} among these materials is between Al and SiO_x. This combination is also widely used as a driving actuator for large scanning MEMS mirrors in OCT systems [27,42,43], as optical phase arrays [44] or as a driver for scanning waveguides [45]. Additionally, these actuators found their application as electrical microprobes for wafer probe cards [46] and as well as in atomic force microscopes [47]. All presented examples encourage the choice of Al and SiO_x as the best layer combination for electrothermal bimorph actuators.

The thermal and actuation strain mismatch can be calculated using Eq. 2.35 and Eq. 2.36. But, to determine the initial beam deflection using Eq. 2.33, $\Delta\epsilon_{in0}$ must be known. Thus, a bimorph actuator design can be based on the effective strain mismatch obtained after the beam is released and all post annealing steps are performed. The strain mismatch $\Delta\epsilon_{in0}$ is directly connected to the residual stress σ_{in} in the beam. Since the residual stress of beam layers depends on available deposition processes in the laboratory, a combination of deposition techniques for both Al and SiO_x which gives a stable initial deflection independent on any thermal cycling is investigated.

A test beams are used to determine the residual stress in the Al-SiO_x bimorph combination. The test beams are fabricated by depositing a 2 μm-thick PECVD SiO_x layer at 350 °C or 400 °C and 2 μm-thick sputtered Al layer at 50 °C or 350 °C. The beam release is done using dry etching of Si substrate in SF₆ plasma at 20 °C. Details of the fabrication process are given in Appendix A.2. Different deposition conditions resulted in initial deflection ranging from 10 μm for combination of sputtered Al1%Si at 350 °C and silane based PECVD oxide deposited at 400 °C to 120 μm to combination of sputtered Al1%Si at 25 °C and PECVD TEOS oxide deposited at 350 °C. These results show it is possible to

fabricate flat bimorph Al-SiO_x cantilevers by choosing right deposition conditions and right layer thicknesses. However, after thermal annealing of all these samples at 400 °C, all tested cantilevers had same deflection of 300 μm. Therefore, the first actuation of the beam will also influence the beam deflection if it is not annealed before.

To have a good model of Al-SiO_x bimorph in simulations, a COMSOL Multiphysics 4.4. model is used. A range of -300 MPa to 300 MPa for σ_{in} in both materials is used to find the best fit of the initial beam deflection to the experimental findings including a 400 °C annealing step. The stress value of 100 MPa tensile for Al and 40 MPa tensile for SiO_x are the best fitting values and they are used for modeling the actuator system.

ACTUATOR SYSTEM FOR x DIRECTION SCANNING

The actuator system for x direction scanning consists of a set of actuators which need to provide a torsional motion of the microplate with the lens, around the hinge with the waveguide (Fig. 2.10). The actuators must be equidistantly positioned on both sides of the microplate. Since the actuators are pre-stressed and have an initial deflection, Al must be placed below SiO_x layer to use this initial deflection (Fig. 2.23a). On each side, the actuators are pushing the microplate at the edge with force F_0 . Since both set of actuators have the same distance from the central hinge with the waveguide (torsional axis), there is no angular displacement of the microplate. If one side is actuated with Joule heating, the beams will move upwards. Thus, the applied force F_a will be lower than F_0 , which results in a rotation around the torsional axis. The heated bimorph now acts like a spring with a constant k_b (Fig. 23b).

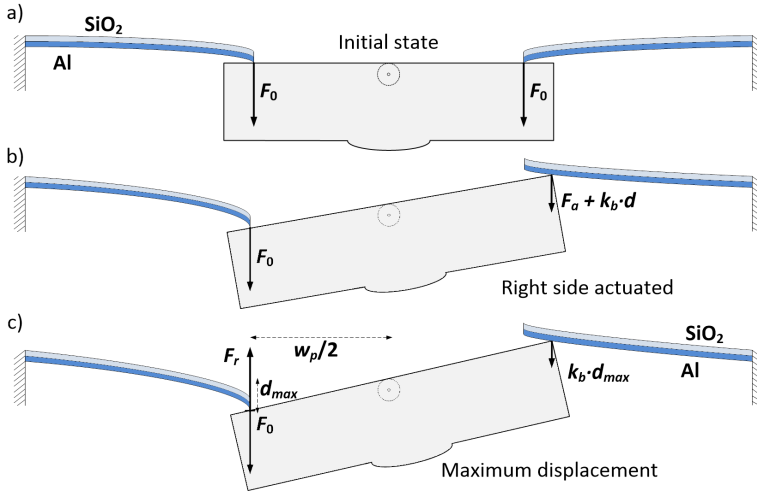


Figure 2.23: Working principle for x direction scanning OCT system using Al-SiO_x electrothermal bimorph cantilevers: (a) Initial state where both group of actuators are applying the same force. (b) Right side is actuated, and cantilevers are bending up resulting in lower force applied to the plate. (c) Maximum torsional angle in the final state of the actuation.

In the final state which is illustrated in Fig. 2.23c, when all initial strain $\Delta\epsilon_{in}$ is compensated with $\Delta\epsilon_{act}$, the force F_a equals to zero and the system reaches maximum tor-

sional displacement. The whole rotation is now generated with force F_0 from the non-actuated beam. By the third Newton's law, a reaction force F_r is applied to the actuator in the opposite direction than F_0 . In the final state, the not heated actuator deflection, d_{max} , is determined by the residual stress in the beam after fabrication and the reaction force F_r from the plate. The maximum angle is defined by:

$$\alpha_{max} = \arctan\left(\frac{2 \cdot d_{max}}{w_p}\right) \quad (2.37)$$

where d_{max} is the deflection of the bimorph beam and w_p is the distance from the actuator tip to the torsional axis.

The actuator system design, i.e. the electrothermal bimorph actuators and the microplate supported with the torsional hinge (design parameters given in Table 2.6), is optimized using numerical FEM calculation. The inclusion of both actuators and the microplate with hinges makes the 3D FEM model complex for numerical calculation. The maximum angular displacement is defined in the steady state of the system, as illustrated in Fig. 2.23c. Therefore, the numerical computation can be divided in two parts: the actuator displacement calculation and the plate rotation calculation.

Figure 2.24 illustrates the geometrical models used in the FEM simulations of the electrothermal bimorph beam actuator (Fig. 2.24a) and the microplate with hinges (Fig. 2.24b). The length of the single actuator, l_a , is varied from 300 μm to 800 μm , the width, w_a , from 50 μm to 150 μm , while layer thickness, t_{al} , of Al and t_{ox} of SiO_x from 1 μm to 3 μm . For optimization of the electrothermal bimorph beam actuator, the reactive force F_r is applied at the actuator tip to simulate the maximum displacement state given in Fig. 2.23c and to estimate the beam spring constant k_b . Then, for the microplate width w_p and number of actuators N_a optimization, a distributed force $N_a \cdot F_0$ is applied on one side of the microplate while on the other side, the actuators are modeled using their spring coefficient k_b (Fig. 2.23c).

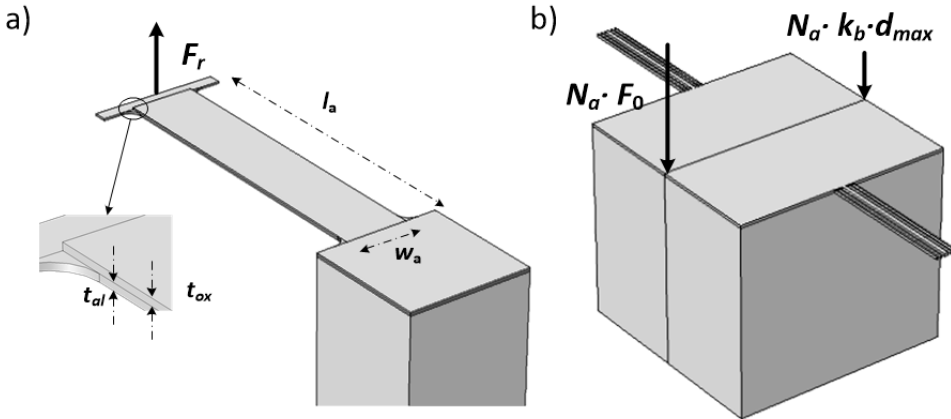


Figure 2.24: (a) Geometric parameters used for the simulation model of an electrothermal actuator beam. (b) 3D simulation model for a microplate supported by torsional hinges.

Numerical simulations of the maximum actuator tip displacement, d_{max} , caused by the residual stress and the applied force F_r for different values of l_a , w_a , and the total actuator thickness ($t_{al} + t_{ox}$) are presented in Fig. 2.25. We are interested only in the linear regime of the actuator deformation when a force F_r is applied, i.e. when Hook's law is valid. The presented results give the actuator spring coefficient value k_b . The Young's moduli of Al and SiO_x have close values (Table 2.8). Therefore, similar elastic properties are expected between beams of 1 μm of Al and 3 μm of SiO_x or 3 μm of Al and 1 μm of SiO_x .

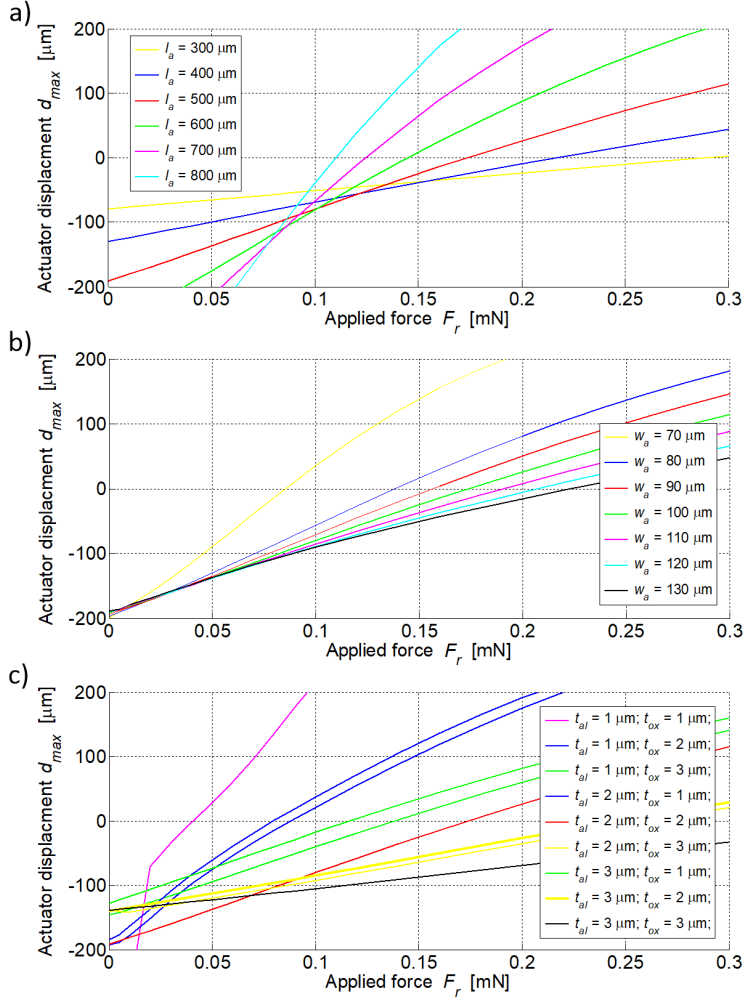


Figure 2.25: Maximum displacement versus applied force for: (a) Different actuator length: $w_a = 100 \mu\text{m}$, $t_{al} = 2 \mu\text{m}$, $t_{oxl} = 2 \mu\text{m}$; (b) Different actuator width: $l_a = 500 \mu\text{m}$, $t_{al} = 2 \mu\text{m}$, $t_{oxl} = 2 \mu\text{m}$; (c) Different layer thicknesses: $l_a = 500 \mu\text{m}$ and $w_a = 100 \mu\text{m}$.

For each length, width or total bimorph layer thickness, the spring coefficient of the beam is calculated and is reported in Fig. 2.26. All results are as expected, i.e. longer beams have lower spring coefficient while wider and thicker beams have larger spring coefficient. If the actuator spring coefficient is larger, the delivered force F_0 is also larger (Fig. 2.23c). However, the resistive force $k_b \cdot d_{max}$ is also larger. For the range of thicknesses considered, a total thickness of $4 \mu\text{m}$ is chosen as a trade-off between flexibility and generated force. Based on the analysis carried out in [26], the optimal ratio of layer thickness should be equal to the square root of the layer biaxial Young's modulus. We selected a total thickness of $4 \mu\text{m}$, in which the Al layer should be $1.965 \mu\text{m}$, while the SiO_x should be $2.035 \mu\text{m}$. These values are quite close, so to ease fabrication, the thickness for both layers is fixed at $2 \mu\text{m}$. Similarly, the trade-off sets the actuator width w_a is set at $90 \mu\text{m}$ and the length l_a at $500 \mu\text{m}$.

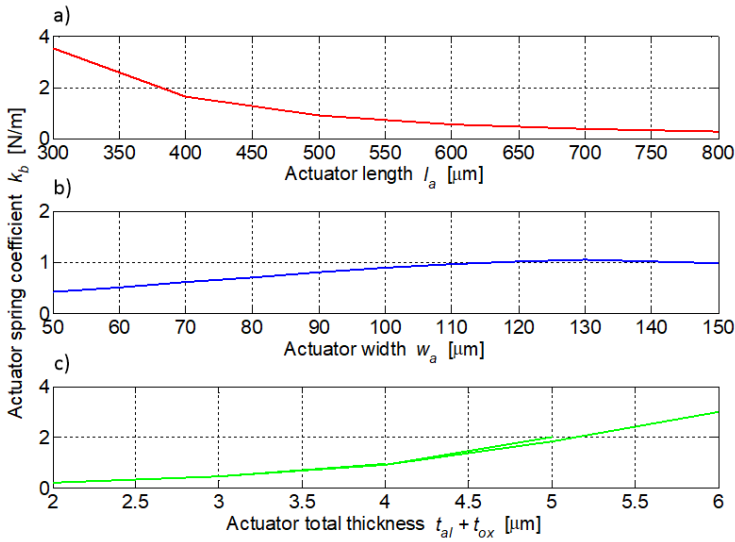


Figure 2.26: Calculated spring coefficient k_b , based on data reported in Fig 2.25, for a) varying actuator length, b) varying actuator width and c) varying layer thicknesses.

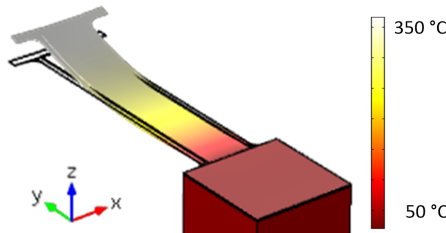


Figure 2.27: Simulation results of the temperature distribution in an Al-SiO_x bimorph cantilever for 70 mW applied power.

For a chosen geometry of the actuator, the calculation of the vertical displacement versus applied force is done using the model given in Fig. 2.24a. The simulation showed that the required power per actuator to achieve an average temperature of 260 °C is estimated to be 70 mW (Fig. 2.27). At this temperature, the actuator stops pushing the plate further (see Fig. 2.23c). Thermal changes of Young's modulus are neglected here. Although this assumption is not valid for the temperature range used as indicated in [48], the discrepancy in a first order analysis is acceptable. Figure 2.28 reports the simulation results of d_{max} as a function of F_0 or F_r . The solid line represents d_{max} versus F_r for the actuator tip, while the dashed lines represent the dependency of d_{max} on F_0 applied at the edge of the plate for several combinations of N_a and w_p . The intersection points indicate possible combinations for the maximum displacement of the system. The angular displacement is calculated based on these values for F_0 and N_a for different combinations of w_p .

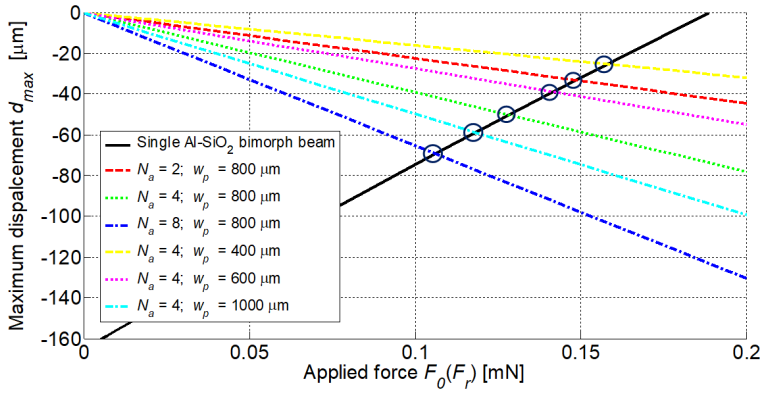


Figure 2.28: Dashed lines represent the maximum displacement of the microplate for several combinations of N_a and w_p as function of the applied force F_0 . The intersections with the maximum deflection of the actuator tip (circles) versus F_r (solid line) give the possible combinations for maximum displacement of the system.

Figure 2.29 shows the maximum angular displacement α_{max} versus the number of applied actuators N_a when w_p is set to 800 μm (Fig. 2.29a), and versus plate width w_p with 4 actuators on each side ($N_a = 4$) (Fig. 2.29b). As expected, more actuators can generate a larger angular displacement. However, more actuators would linearly increase the power consumption, while it would not linearly increase the generated angular displacement. An acceptable tradeoff between increasing α_{max} and reducing the power consumption is to have 4 actuators on each side of the plate. For $N_a = 4$, a maximum angular displacement of 6.16° is achieved for a plate width of 800 μm . Each group of 4 actuators must be placed 400 μm away from the central axis on each side.

To heat up the Al-SiO_x bimorph beams a microheater is used. Materials like Mo, TiN, highly doped polycrystalline Si or SiC are generally employed due to high melting point, high thermal conductivity and high electrical resistivity [49]. Unlike Mo or TiN, Al has a much lower electrical resistivity which makes this material not the best choice for heat production. For a fixed voltage supply (Table 1.1), a higher heater resistance will reduce Joule heating. The average beam temperature is estimated to be only 260 °C. Thus, Al

can be used as a heater material in this application.

As a tradeoff between resistance and power consumption, the heater is designed as a $10\text{ }\mu\text{m}$ line with $20\text{ }\mu\text{m}$ pitch and thickness of 300 nm . Thus, within one actuator beam there are 4 heater lines giving a resistance $0.036\text{ }\Omega/\mu\text{m}$, i.e. $18\text{ }\Omega$ for a $500\text{ }\mu\text{m}$ long actuator. The heaters are connected on each actuator side according to the electrical scheme presented in Fig. 2.30. The heater is placed below the actuator. This increases thermal losses, but it simplifies device fabrication, as discussed in Chapter 4.

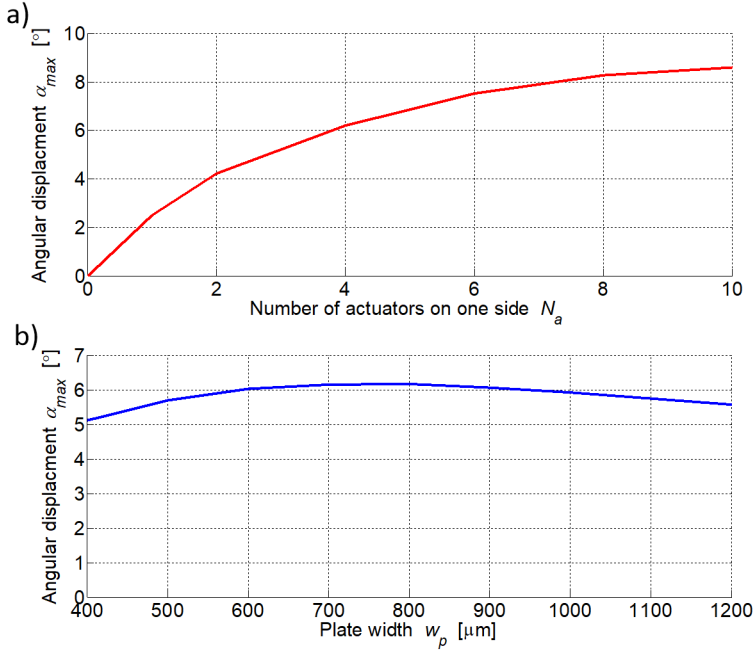


Figure 2.29: Maximum angular displacement versus (a) number of actuators for $w_p = 800\text{ }\mu\text{m}$ and (b) plate width with 4 actuators per side ($N_a = 4$).

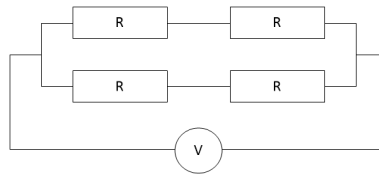


Figure 2.30: Electrical schematics of heater connections on each side of the actuator system.

In Fig. 2.31 the final 3D model of the MEMS actuator system with 4 actuators on each side is depicted. The microplate has a lens at the bottom and is supported by two torsional hinges. A waveguide with a 45° ending facet runs along the hinges. Design parameters and expected working parameters for the MEMS actuator system for x directional scanning are summarized in Table 2.9.

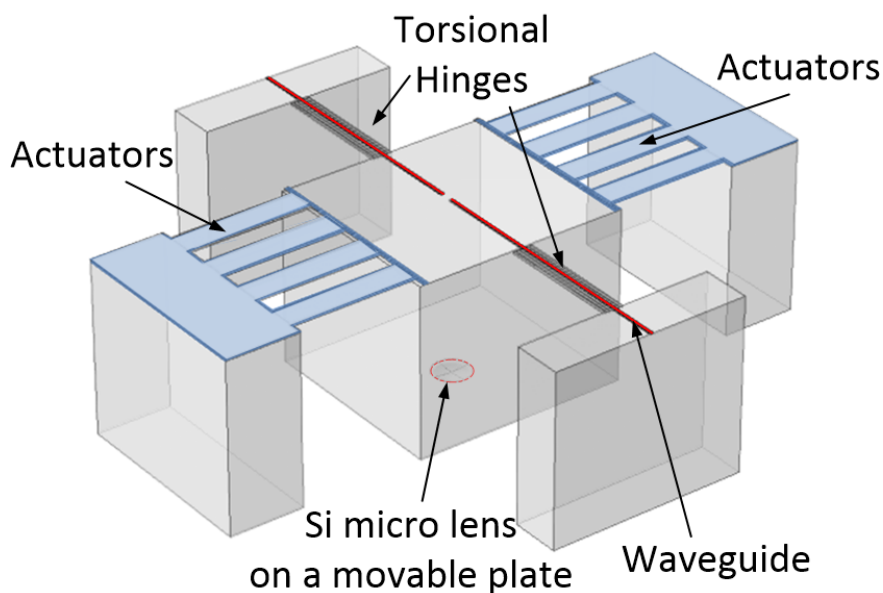


Figure 2.31: Final design of the MEMS actuator system for x direction scanning together with the optical components for OCT imaging.

Table 2.9: Parameters of the MEMS actuator system for x direction scanning

Parameter	Symbol	Value
Actuator length	l_a	$500\ \mu\text{m}$
Al layer width	w_{al}	$110\ \mu\text{m}$
Al layer thickness	t_{al}	$2\ \mu\text{m}$
SiO _x layer width	w_{ox}	$90\ \mu\text{m}$
SiO _x layer thickness	t_{ox}	$2\ \mu\text{m}$
Number of actuators per side	N_a	4
Gap between actuators	g_a	$90\ \mu\text{m}$
Hinge length	l_h	$500\ \mu\text{m}$
Hinge thickness	t_h	$10\ \mu\text{m}$
Central hinge width	w_{ch}	$15\ \mu\text{m}$
Side hinge width	w_{sh}	$5\ \mu\text{m}$
Gap between hinges	g_h	$10\ \mu\text{m}$
Microplate width	w_p	$840\ \mu\text{m}$
Microplate length	l_p	$800\ \mu\text{m}$
Maximum angular displacement	α_{max}	$\pm 6.16^\circ$
Maximum power consumption	P_{max}	$280\ \text{mW}$
Average working temperature	T	$260\ ^\circ\text{C}$
Resonant frequency	f_r	$534\ \text{Hz}$

ACTUATOR SYSTEM FOR y DIRECTION SCANNING

The y direction scanning is provided by out-of-plane motion of the frame with x direction scanning system (Fig. 2.10b). The actuator system brings the frame up by deflecting the supporting hinge with the waveguide. Also, the hinge must carry electrical connections for the x scanning system heaters. Therefore, the minimum hinge width must be $120\text{ }\mu\text{m}$. However, to simplify integration of optical components and MEMS actuators, a separate, 1D y directional scanning system is designed and presented in this section. For 2D scanner, the y direction scanning actuator system will consist of 2 1D scanners.

The y scanning system design must be fully compatible with the x direction scanning from both layout and fabrication point of view. Therefore, for the y direction scanning system with a deflecting hinge supporting the waveguide and a microplate with Si microlens, the same Al-SiO_x electrothermal bimorph beam actuators can be used in the configuration given in Fig. 2.32. Initially, actuators and hinge are deflected due to residual stress of the actuators, thus giving an initial angular displacement of the plate (Fig. 2.32a). Using Joule heating, hinge and actuators will deflect in the opposite direction, rotating the plate at the same time. This is illustrated in Fig. 2.32b.

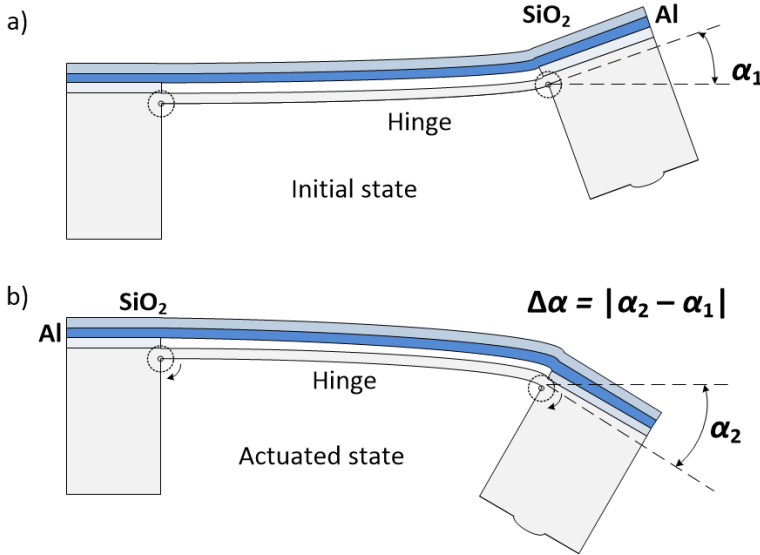


Figure 2.32: The y direction MEMS scanning system: (a) Initial and (b) Actuated state.

The type and the thickness of the bimorph layers should be the same as for the x direction scanner. Also, the deflection hinge must have same thickness as the torsional one. The hinge width is chosen to be $60\text{ }\mu\text{m}$ as we are designing half of the 2D y direction scanning. The only two parameters here optimized for the desired motion range of 12° are the number of actuators and the actuator/hinge length. The system optimization is done using FEM simulations in COMSOL Multiphysics 4.4. To find the desired number of actuators N_a , a system with 2, 4 and 6 actuators is analyzed. To choose the best actuator/hinge length l_y , this parameter is varied between $400\text{ }\mu\text{m}$ and $1000\text{ }\mu\text{m}$.

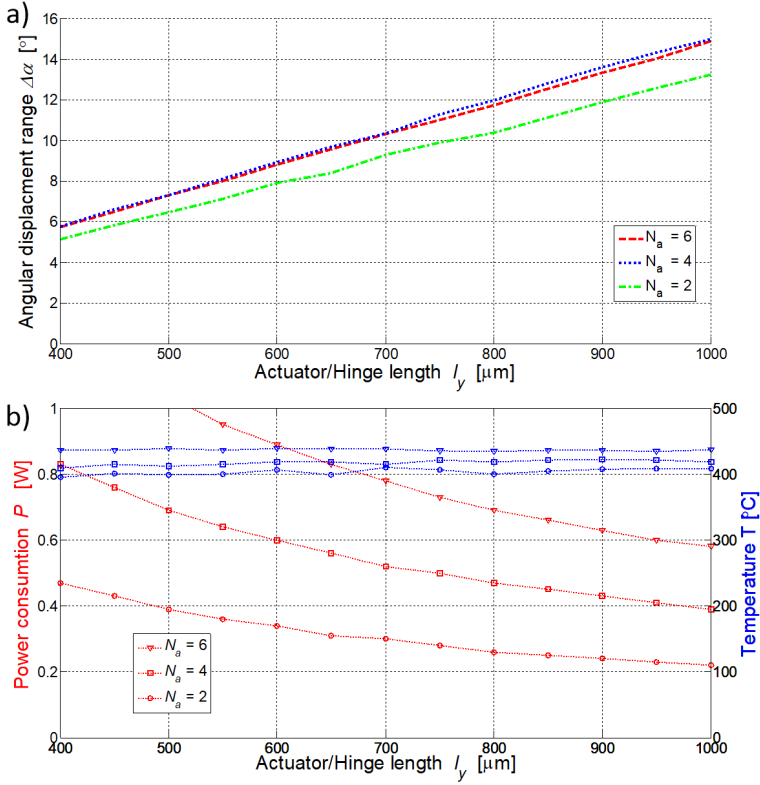


Figure 2.33: (a) Angular displacement range (b) Power consumption and working temperature versus actuator/hinge length for $N_a = 2, 4$ and 6 .

The maximum displacement angle range versus actuator/hinge length is reported in Fig. 2.33a. The motion range of 12° is achievable using different combinations of N_a and l_y . In Fig. 2.33b temperatures and power consumption to achieve the final position of the microplate in the actuated state are presented. The system with 2 actuators and hinge length of $900 \mu\text{m}$ uses 250 mW of power to provide the desired motion range. However, this configuration could result in low resonant frequency. The system with 4 actuators needs a hinge of $800 \mu\text{m}$ length for the same motion range but it uses 470 mW of power. Increasing the number of actuators to 6 would increase the power consumption to 690mW and the eigenfrequency of the system, while still needing the same hinge length for a 12° angular range. Therefore, the configuration with 4 actuators and a length of $800 \mu\text{m}$ is chosen as a tradeoff between mechanical performance and power consumption. Simulation results for this configuration are shown in Fig. 2.34.

The final 3D design model for the MEMS actuator system for y direction scanning is presented in Fig. 2.35. The system has 4 actuators, 2 on each side of the deflecting hinge. Also, in this case a $3 \times 3 \mu\text{m}^2$ Si waveguide with a 440 nm thick SiO_2 layer underneath is placed on the top of the hinge and ends with a 45° facet above the Si microlens. The

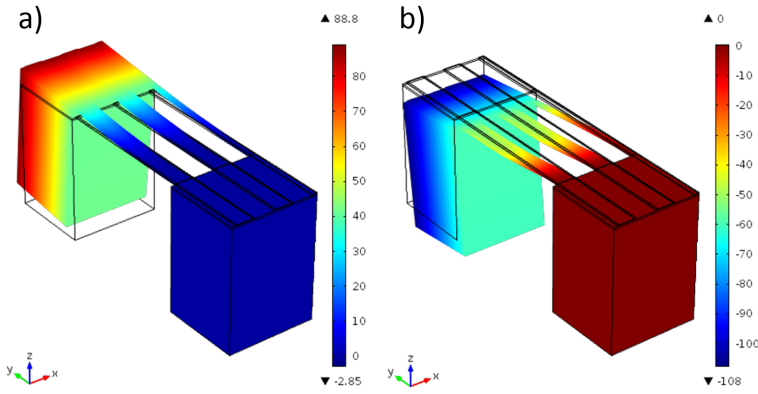


Figure 2.34: (a) Simulation results for $N_a = 4$ and $l_y = 800 \mu\text{m}$: (a) initial microplate position due to pre-stress and (b) final microplate position at 420°C . (Only one half of the system is simulated to save computational time).

system is actuated with an Al heater with the same dimensions as for the x direction scanning. Thus, the resistance of one heater is 28.8Ω . Like for x direction scanning, the heaters are connected in an electrical circuit as illustrated in 2.30. Design parameters and expected operational values are summarized in Table 2.10.

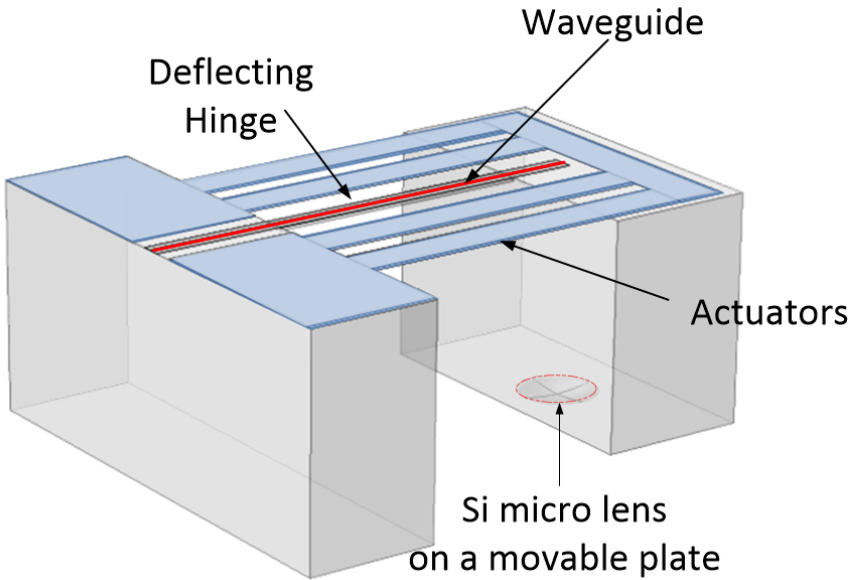


Figure 2.35: Final design of the MEMS actuator system for y direction scanning with optical components for OCT imaging.

Table 2.10: Parameters of the MEMS actuator system for x direction scanning

Parameter	Symbol	Value
Actuator/hinge length	l_y	800 μm
Al layer width	w_{al}	110 μm
Al layer thickness	t_{al}	2 μm
SiO _x layer width	w_{ox}	90 μm
SiO _x layer thickness	t_{ox}	2 μm
Number of actuators per side	N_a	4
Gap between actuators	g_a	115 μm
Hinge thickness	t_h	10 μm
Hinge width	w_h	60 μm
Microplate width	w_p	800 μm
Microplate length	l_p	450 μm
Maximum angular displacement	α_{max}	$\pm 6^\circ$
Maximum power consumption	P_{max}	470 mW
Average working temperature	T	420 $^\circ\text{C}$
Resonant frequency	f_r	463 Hz

2.3. THE FULL SYSTEM LAYOUT

NOW, that all components of the integrated OCT system have been determined and their expected performance simulated, the final layout can be designed. In Fig. 2.36 is presented a mask layout of all major components of the system: the lens, waveguide circuitry, bimorph layers, heater and hinge opening. Figure 2.36a-b presents the layout of 1D x and y integrated OCT scanners respectively while in 2.36c a 2D optical scanner is given which consist for one x and two y MEMS actuator systems, a waveguide with 45° facet and a lens. The total footprint of each design is 5×10 mm with possibilities for further reduction by optimization of the design for the heater interconnects (red and green area) and openings for the hinge definition (gray area).

All system components are designed to meet the requirements given in Table 1.1. The photonic circuit design is provided by Medlumics and it is based on VTT thick SOI waveguide technology. The Si has to collimate the light coming out of presented waveguide/mirror system and through the substrate thickness 700 μm . This requires a Si surface radius of curvature to be 500 μm . The microlens is designed to have the lowest possible top to bottom height which can be achieved with diameter of 150 μm .

The MEMS actuator systems are designed to provide motion range of 12° using low Al-SiO_x bimorph beams. Two systems, for x and y direction scanning are designed to be fully compatible to be integrated in one 2D scanning device (Fig. 2.36c). The attention during the system design is put to mechanical motion. The estimated working temperature shows it is possible to use Al as a heating material as well and hence, the electrothermal optimization is not included in this work.

In the next three chapters the fabrication process and device characterization for optical components, MEMS actuators and integrated OCT system is presented.

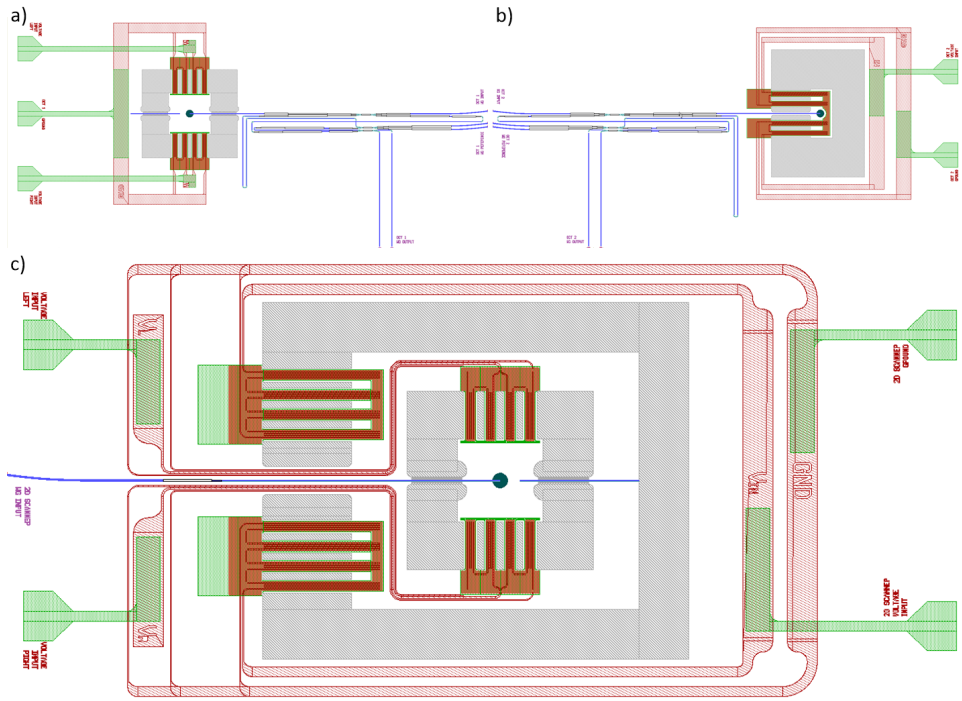


Figure 2.36: The layout for one dimensional integrated OCT system of (a) x and (b) y direction scanning. (c) The layout for 2D optical scanner. In blue color Si waveguides are presented while the dark green circle represents the lens. Bimorph layers are shown with orange (SiO_x) and green (Al). The heater and its interconnects are depicted using red color. Also, the bimorph Al layer is used as an interconnect between heater and electrical bond pads.

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3

OPTICAL COMPONENTS FABRICATION AND CHARACTERIZATION

In order for the light to shine so brightly, the darkness must be present.

Francis Bacon

The optical path of the OCT system presented in the previous chapter guides the light from the source towards the scanning sample and the photodetector. In this chapter I present the process flow development for the optical components, namely the Si microlens, the mirror and the waveguide, fabrication. All three components are finally integrated in one photonic device and optically characterized. This integration is an important step forward towards the fabrication of monolithically integrated single-chip OCT system.

Parts of this chapter have been published in "Fabrication process of Si microlenses for OCT systems", *Micro-Optics* 2016 **9888**, 98880C (2016) and in "An Integrated Photonic Platform for A Single-Chip MEMS-Based Optical Coherent Tomography Scanner", *Micromachines*, Under Review.

3.1. SI MICROLENS

SPHERICAL silicon microlenses whose design parameters are determined in Chapter 2 of this thesis, can be realized using different techniques, such as binary optics, grayscale lithography and photoresist reflow. Each technique aims at the realization of a spherical silicon surface using photoresist as a mask and reactive ion etching to transfer the mask geometry into the silicon substrate.

Binary optics is a technology based on optical diffraction, which uses planar geometry to define the phase profile of the light beam. Sometimes, multilevel binary optical lenses are used to improve their focusing properties. The multilevel approach can be implemented to create spherical lenses [1], as illustrated in Fig. 3.1. Unfortunately, it is a time-consuming technique due to the many lithography and reactive ion etching steps needed [1]. Furthermore, this approach gives a stepped profile (Fig. 3.1a) determined by the etch process steps employed. Hence, to achieve a smoother surface, i.e. without visible steps, the number of lithography/etching steps becomes very high and even unpractical (Fig. 3.1b).

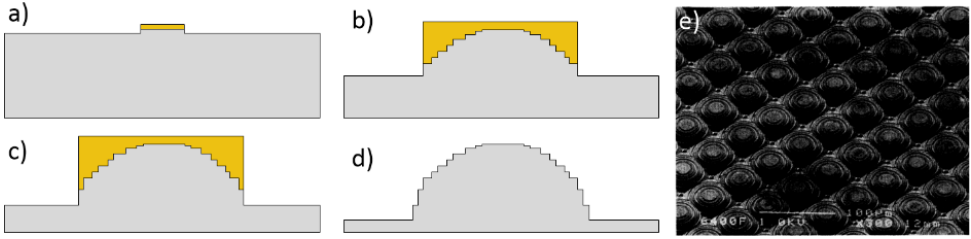


Figure 3.1: Schematic illustration of Si lens fabrication using the binary optics technique: (a) first mask and etching step. (b) n^{th} litho-etch step (c) $(n+1)^{th}$ litho-etch step (d) Final shape of the fabricated lens. (e) SEM image of a binary optics microlens array presented in [1].

Lens fabrication using grayscale lithography is straightforward in terms of fabrication steps, somewhat less with respect to the design. It employs a classic lithography process (photoresist coating, photoresist exposure and photoresist development) and reactive ion etching. The gray scale mask is made from pixels smaller than the exposure tool resolution [2]. Each pixel has a defined transparency allowing only a certain percentage of the light to go through and partially expose the photoresist. For example, if the pixel allows 70% of the light to go through, then 70% of the photoresist will be exposed and removed during the subsequent development step (Fig. 3.2a). In this way, it is possible to create different slopes and steps in the photoresist (Fig. 3.2b) which will be then transferred by etching into the substrate. However, establishing correctly the lithography process parameters and accurately designing the required photolithography mask is a complex and time-consuming operation [3,4]. Due to the pixelated image, the surface roughness of the resist is high. This roughness will be transferred into Si after etching [5]. If the photoresist to silicon selectivity is high, the roughness will be further increased, possibly to the point when the thick thermal oxidation cannot improve the surface quality. Also, a designed pixelated mask defined by exposure tool parameters cannot be easily transferred to another IC fabrication facility and it would require

re-definition of the process, pixel and mask design, thus making this method less transferable.

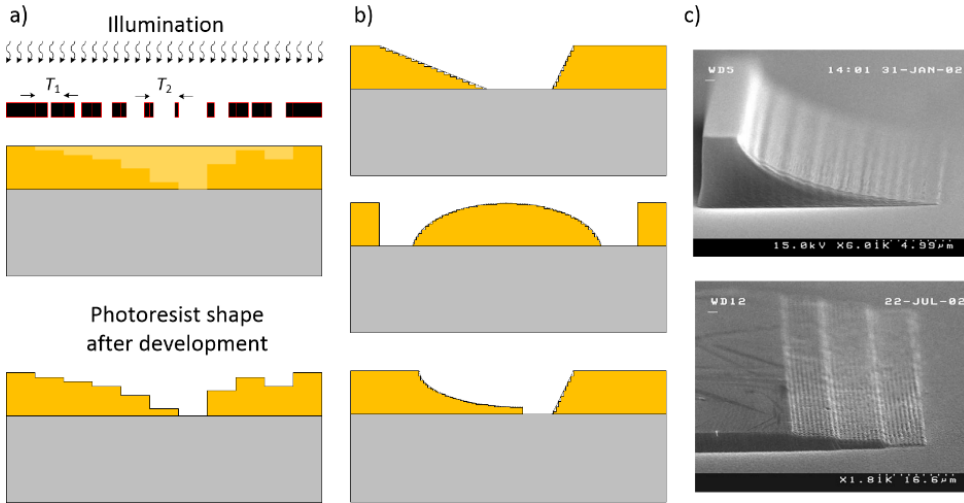


Figure 3.2: (a) Grayscale lithography exposure principle. Each pixel has a pre-defined transparency T to allow only a certain percentage of the light to go through the mask and (partially) expose the photoresist. (b) Different slopes which can be created by grayscale lithography. The smallest step height depends on the pixel size. (c) An example of a photoresist profile created with grayscale lithography (top) and rough profile after transfer into the silicon substrate (bottom) [5].

The photoresist reflow technique is also a straightforward processing technique, like grayscale lithography. Unlike grayscale lithography, it cannot be used to fabricate any nonplanar Si surface geometry. However, it is ideal for spherical surfaces and thus microlens fabrication. Spherical photoresist ball caps are formed by thermal or chemical treatment of photoresist cylinders defined by standard lithography and then transferred into the substrate by dry etching. Therefore, this approach does not require any special mask design, or multiple lithography steps, making it more convenient than binary optics and grayscale lithography.

Chemical photoresist reflow is mainly used in saturated vapor solvent atmosphere at room temperature [6]. Thanks to the diffusion process, which is enhanced by surrounding solvent atmosphere, a photoresist cylinder shape (Fig. 3.3a) can be transformed into a ball cap (Fig. 3.3b). A disadvantage is that the lens diameter is not constant during the reflow process, due to the increased surface wetting by solvent presence [6]. Thermal photoresist reflow is a well-known technique which is based on the partial melting of non-crosslinked photoresist [7] (Fig. 3.3c). If the photoresist is brought to above its glass transition temperature T_g then the photoresist cylinder becomes soft allowing itself to change shape to minimize its surface energy [8]. The drawback of the process is that the initial photoresist volume needs to be carefully chosen as it should be higher than the critical resist thickness which allows the formation of the spherical ball cap [9] (Fig. 3.3d).

As optically transparent material, thermally reflowed photoresist ball cap can be used

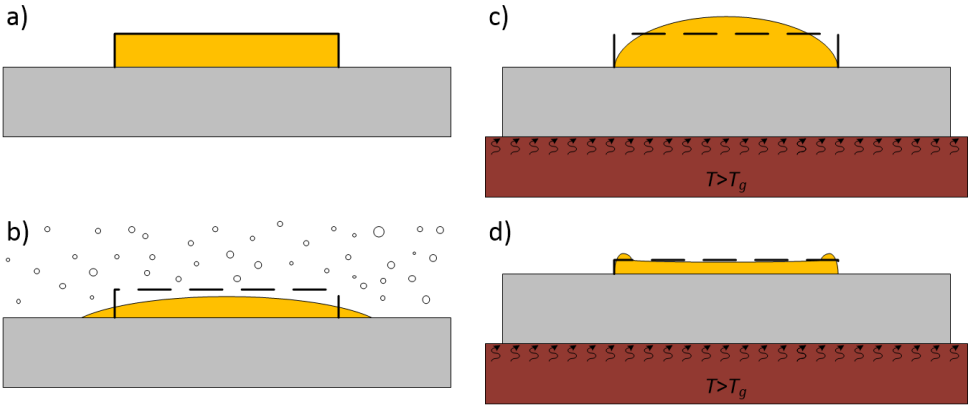


Figure 3.3: Main steps of the photoresist reflow technique: (a) Initial photoresist cylinder definition by conventional optical lithography (b) Chemical photoresist reflow process. (c) Thermal photoresist reflow process with sufficiently thick photoresist and (d) with not sufficiently thick photoresist. The dash line (b-d) represents the initial photoresist shape.

as lens even without any transfer into Si, for applications in the visible and near-infrared spectrum. Different diameter ($25\text{ }\mu\text{m} - 150\text{ }\mu\text{m}$) photoresist lenses presented in [10] achieved different focal lengths from $73\text{ }\mu\text{m}$ up to $1550\text{ }\mu\text{m}$. The focal length can be also tuned with the upside-down baking approach presented in [11] where wafers are baked on a hotplate with photoresist cylinders facing the hotplate. Thus, the photoresist deforms during the reflow with an additional contribution from gravity. Using the thermal reflow it is possible to fabricate dense microlens arrays with a fill factor up to 90% [12]. After creating the desired photoresist ball cap, the shape is transferred to the substrate like quartz [12], diamond [9] and silicon [13-15]. By controlling the selectivity of photoresist to silicon etching, it is possible to create ball caps in silicon with bigger or smaller radius of curvature than the initial photoresist geometry. A large, $280\text{ }\mu\text{m}$ high and 2.5 mm diameter Si lens for THz application was fabricated using thermal reflow technique and a high photoresist to silicon etching selectivity [13]. The mid-infrared Si collimated lenses presented in [14] are $120\text{ }\mu\text{m}$ high and 1.6 mm in diameter and present a low roughness of 450 nm . Using the same approach, it is possible to fabricate small and much smoother lenses of $30\text{ }\mu\text{m}$ in diameter and $3\text{ }\mu\text{m}$ high with only 30 nm surface roughness [15].

Table 3.1: Comparison of the microlens fabrication techniques

	Design flexibility	Mask design	Process development	Surface roughness
Binary optics	High	Complex	Simple	High
Grayscale lithography	High	Complex	Complex	High
Photoresist reflow	Low	Simple	Simple	Low

The three lens fabrication approaches described have been compared to evaluate

advantages and disadvantages as summarized in Table 3.1. Comparison parameters of these techniques are: design flexibility, mask design complexity, process development complexity, photoresist (and thus lens) surface roughness. The possibility to have low roughness of the Si surface, different lens sizes and the simplicity of resist ball cap formation, make thermal reflow the best choice for the Si microlens fabrication for the system presented in Chapter 2.

3.2. SI MICROLENSSES PROCESS FLOW

3.2.1. PHOTORESIST BALL CAP FORMATION

Defining the right size photoresist ball cap by thermal reflow is one of the two most important steps in Si microlens fabrication. To determine the initial photoresist thickness, first the thermal reflow process must be optimized. The two parameters that are important in this process are the final ball cap size, which directly defines the Si microlens shape, and the resist chemical and thermal stability, which ensures a stable etching process. As we aim at a wafer scale, reproducible fabrication process, it is preferable to use a type of photoresist available in most silicon microfabrication laboratories. We selected the *Microchemicals* AZ9260, which is one of the main photoresist used in the automatic coater/developer track EVG120 in our laboratory and which has the biggest possible thickness range for microlens size tuning.

During the resist bake for thermal reflow, two physical mechanisms can be observed: the photoresist transition into spherical ball cap and the photoresist solvent evaporation. Therefore, the final ball cap size depends on the initial photoresist volume and the evaporated solvent amount. To achieve chemical stability of the photoresist, the thermal reflow bake should be sufficiently long for all solvents to evaporate, but also at a not too high temperature to prevent photoresist from cracking due increased mechanical stress in the layer [16].

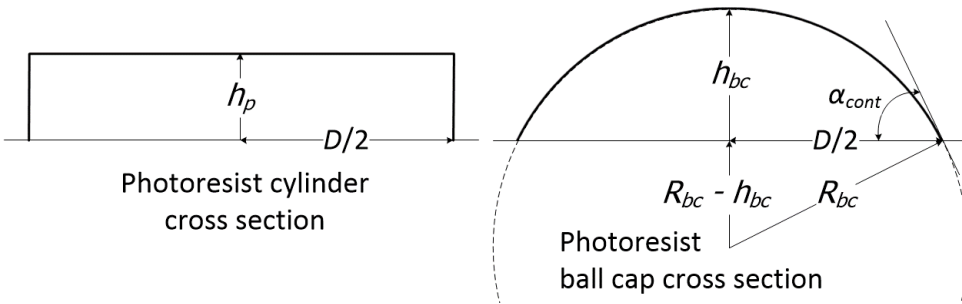


Figure 3.4: Photoresist cylinder and corresponding ball cap parameters.

Any photoresist coating begins with the application of an adhesion promoter, mainly hexamethyldisilane (HMDS). If the photoresist to silicon adhesion is good and with the support of the results presented in [8-16], it is safe to assume that the ball cap diameter will be equal to the initial cylinder diameter. Let us first exclude the effect of solvent

evaporation. Then the initial ball cap volume is equal to the cylinder volume:

$$V_{cylinder} = h_p \cdot \left(\frac{D}{2}\right)^2 \cdot \pi = \frac{1}{6} h_{bc} \cdot \left(3 \cdot \left(\frac{D}{2}\right)^2 + h_{bc}^2\right) \quad (3.1)$$

where h_p is the initial photoresist thickness, h_{bc} is the top to bottom ball cap height and D is ball cap/cylinder diameter. The ball cap and cylinder parameters are illustrated in Fig. 3.4. Following Eq. (3.1) we get a cubic equation with unknown parameter h_{bc} :

$$h_{bc}^3 + 3 \cdot \left(\frac{D}{2}\right)^2 \cdot h_{bc} = 6 \cdot \left(\frac{D}{2}\right)^2 \cdot h_p \quad (3.2)$$

As the ball cap height cannot be smaller than 0, by applying Vieta's substitution in Eq. (3.2), the solution for the ball cap height is:

$$h_{bc} = \frac{D}{2} \cdot \left(\sqrt[3]{\frac{6 \cdot h_p}{D} \cdot \left(1 + \sqrt{1 + \left(\frac{D}{6 \cdot h_p}\right)^2}\right)} - \frac{1}{\sqrt[3]{\frac{6 \cdot h_p}{D} \cdot \left(1 + \sqrt{1 + \left(\frac{D}{6 \cdot h_p}\right)^2}\right)}} \right) \quad (3.3)$$

From Fig. 3.4, the contact angle can be expressed as:

$$\alpha = \frac{\pi}{2} - \arcsin\left(\frac{R_{bc} - h_{bc}}{R_{bc}}\right) \quad (3.4)$$

where R_{bc} can be calculated following Pythagoras's theorem:

$$(R_{bc} - h_{bc})^2 + \left(\frac{D}{2}\right)^2 = R_{bc}^2 \quad (3.5)$$

$$R_{bc} = \frac{4 \cdot h_{bc}^2 + D^2}{8 \cdot h_{bc}} \quad (3.6)$$

Based on the material properties of the selected photoresist and using the theoretical analysis given in [9, 17-20] we can find the minimum cylinder height for which transformation into the ball cap with the required diameter of 150 μm is possible. The thicknesses that can be achieved with single coating are summarized in Table 3.2. For each photoresist thickness the maximum ball cap height and corresponding contact angle are calculated using Eq. 3.3 and 3.4.

To initiate the reflow process, the photoresist needs to be brought at temperatures above the glass transition temperature T_g . Further, to ensure chemical stability of the resist, all solvents must evaporate and the diazonaphthoquinone (DNQ) chain must be broken. A DNQ chain can break if the resist temperature is above the photoactivation temperature T_{pa} . Based on the material data provided by the photoresist manufacturer for *Microchemical* AZ9260 photoresist, the reflow temperature T_r is fixed at 160 $^{\circ}\text{C}$. This temperature is 30 $^{\circ}\text{C}$ higher than T_g and 15 $^{\circ}\text{C}$ higher than T_{pa} , thus satisfying both criteria. The reflow process is done in a *Memmert* vacuum oven to increase the speed of

Table 3.2: AZ9260 photoresist thickness and corresponding ball cap parameters

Thickness	h_{bc} [μm]	α [$^\circ$]
6.0	11.9	18.0
8.0	15.8	23.7
12.0	23.3	34.5

solvent evaporation. The faster diffusion process in vacuum as compared to a hotplate bake at atmospheric pressure results in faster evaporation of the solvent. To achieve 5.67 μm high Si ball cap, all initial thicknesses presented in Table 3.2 will require a higher photoresist to Si selectivity, i.e. a higher photoresist etch rate than the Si etch rate. Next, we need to optimize the defined dry etching process for ball cap transfer into silicon. This optimization can be performed on any resist thickness and we set it to 8 μm , the intermediate value among those tested.

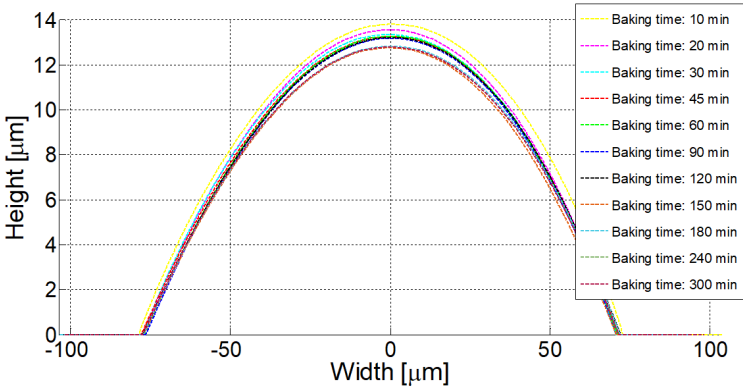


Figure 3.5: Photoresist ball cap cross section profile after a reflow time ranging from 10 min to 300 min.

The ball cap shape change is monitored during a 5 hour reflow. The profile of the cross section of the photoresist ball cap during reflow is shown in Fig. 3.5, while the height versus reflow time is reported in Fig 3.6. The profile is obtained using a *Veeco Dektak 8* stylus surface profilometer with vertical resolution of 10 nm and minimum lateral resolution of 1 μm . The initial thickness after the lithography step is 8.0 μm . The ball cap height after 10 minutes of thermal reflow at 160 $^\circ\text{C}$ is 13.8 μm . On the other hand, equation 3.3 gives a ball cap height of 15.7 μm for the initial thickness of 8.0 μm . However, Eq. 3.3, and thus the results in Table 3.2, do not include the effect of volume reduction due to solvent evaporation, which has a high impact on the ball cap final size. The size of the ball cap decreases with the reflow time and saturates after 2.5 – 3 hours of baking.

Based on the measurements reported in Fig. 3.6, the ball cap volume is calculated using the following Eq. 3.1. and presented in Fig. 3.7. Also, in this figure, the ball cap volume reduction is given. The solvent evaporation stops after 2.5 hours of baking at 160 $^\circ\text{C}$. During this process, the resist loses about 20% of its volume.

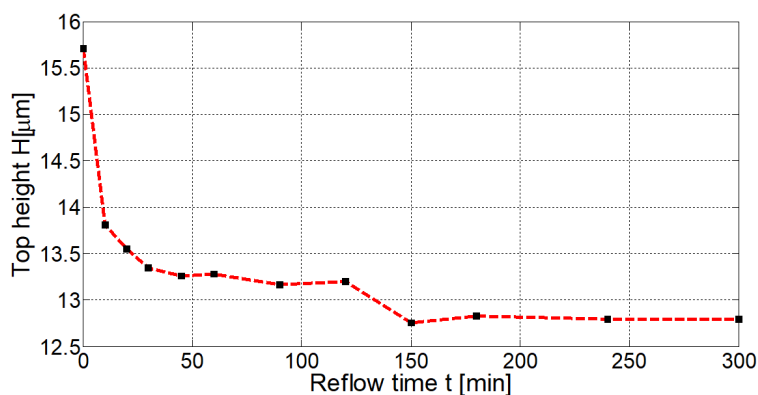


Figure 3.6: Height of the ball cap versus reflow time. The measurement error is 10 nm.

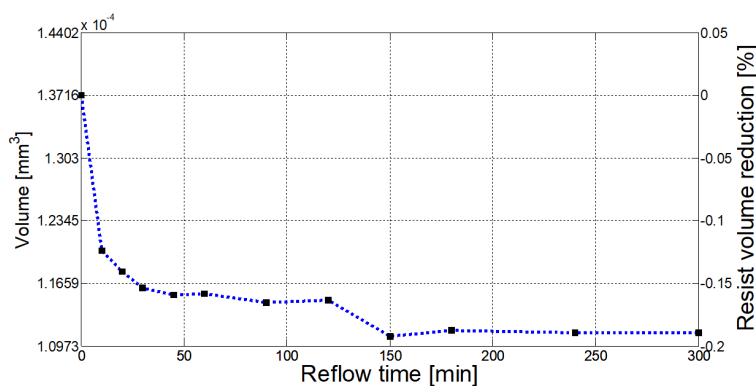


Figure 3.7: The ball cap volume and volume reduction versus reflow time.

3.2.2. BALL CAP TRANSFER TO SI

Once the chemical stability of the photoresist ball cap is reached, i.e. the solvent is completely evaporated, the ball cap shape of the photoresist needs to be transferred onto the Si surface. A dedicate etch recipe needs to be developed which preserves the shape, while giving a smooth final surface (below 38 nm, see Chapter 2). As starting point we consider the values reported in [15] and a mixture of SF_6 and O_2 plasma is used in a *Trikon Omega* ICP dry etcher. The influence of platen temperature and power, gas flow, and pressure on etch profile and surface roughness is investigated.

Table 3.3 reports the surface roughness of the silicon lens surface when gas flow ratios are changed, while the other parameters are kept constant. Since the pressure of the etching process is controlled by the turbo pump, the actual gas flows are not of significant importance. In fact, the gas flow ratio defines partial pressure of each gas inside the plasma reactor. However, gas flows can give an indication on how often plasma is refreshed, thus reducing the etching effect by free radicals and producing a more chemically stable etching. The results are presented in descriptive terms where S stand for

smooth surface, *R* for rough surface. For the etching conditions resulting in a smooth surface, the etching selectivity is measured as well.

Table 3.3: Gas flow ratio in etching recipe on surface roughness

Parameter		Value							
ICP power [W]		500							
Platen power [W]		50 W							
Platen temperature [°C]		25							
Process pressure [mTorr]		50							
O ₂ flow [sccm]	20	25	26	27	28	30	40	50	
SF ₆ flow [sccm]	20	14	13	12	28	10	10	20	
Ratio O ₂ /SF ₆	1	1.67	1.86	2.08	2.33	3	4	2.5	
Surface quality	S	S	R	R	S/R	S/R	S	S	
Selectivity PR:Si	0.04	10.31	-	-	2.32	14.4	4	3.04	
Etching time [min]		2							

For a gas flow ratio of 2.5, the measured Si etch rate is 120 ± 10 nm/min and the photoresist etch rate is 380 ± 10 nm/min. These gas flow parameters were used to observe the influence of the platen temperature change on the photoresist to silicon selectivity. Lowering the temperature to 10 °C resulted in low photoresist to silicon selectivity, with almost no photoresist etched.

Table 3.4: Platen power influence on surface roughness and etching selectivity

Parameter		Value							
ICP power [W]		500							
Platen temperature [°C]		25							
Process pressure [mTorr]		50							
O ₂ flow [sccm]		50							
SF ₆ flow [sccm]		20							
Ratio O ₂ /SF ₆		2.5							
Platen power [W]	0	5	10	20	30	40	50	60	
Reflected power [W]	0	1±1	2±2	3±3	20±5	25±5	30±2	40±2	
Effective power [W]	0	4±1	8±2	17±3	10±5	15±5	20±2	20±2	
Surface quality	S	S	R	R	S/R	S/R	S	S	
PR etch rate [nm/min]	0	220	300	375	305	340	380	390	
Si etch rate [nm/min]	0	140	125	120	130	125	130	130	
Selectivity PR:Si	-	1.57	2.4	3.12	2.35	2.72	2.92	3.0	
Etching time [min]		20							

The influence of platen power is presented in Table 3.4. The platen power was varied between 0 and 60 W with steps of 10 W. Descriptive results of the resulting surface roughness are given in a similar way as for Table 3.3. Increasing the bias power resulted in increased selectivity. However, for 30 W and 40 W, a drop in selectivity is observed, while for 50 W and 60 W almost the same value as for 20 W is obtained. During these tests, high

values of reflected power were observed, resulting in lower effective bias power.

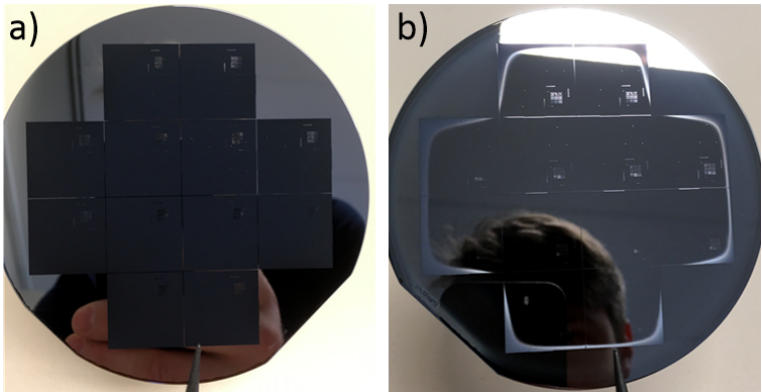


Figure 3.8: The ball cap volume and volume reduction versus reflow time.

The reason for the rough surface obtained with lower effective bias power etching, lays in the local formation of sub nm-thick SiO_2 which is highly selective to SF_6 etching when concentration of O_2^+ ions is high. Hence, a local micro mask is formed. Since this process is stochastic over the wafer surface and over time, the etching can produce black silicon [22,23]. The formation of black Si with 5 W of platen power is shown in Fig. 3.8a, while with 20 W of effective platen power the wafer surface is smooth and uniform (Fig. 3.8b).

Table 3.5: Pressure influence on surface roughness and etching selectivity

Parameter	Value	
ICP power [W]	500	
Platen temperature [°C]	25	
Process pressure [mTorr]	50	10
O_2 flow [sccm]	50	25
SF_6 flow [sccm]	20	10
Ratio O_2/SF_6	2.5	
Platen power [W]	50	50
Reflected power [W]	30	0
Effective power [W]	20	50
Surface quality	S	S
Etching time [min]	20	

The influence of pressure on the etching properties is studied at two pressure values, 50 mTorr and 10 mTorr (Table 3.5). The gas flows for the lower pressure process is reduced while the ratio is kept the same. At the lower pressure, the turbo pump must pump out gasses at a higher rate, thus lowering the flows reduces the work load of the pump. This ensures that the etching process will not be disrupted due to pumping error and make a more stable plasma during the etching process. Lowering the pressure

results in successful matching of the process reflected power. In both cases the etched surface is smooth.

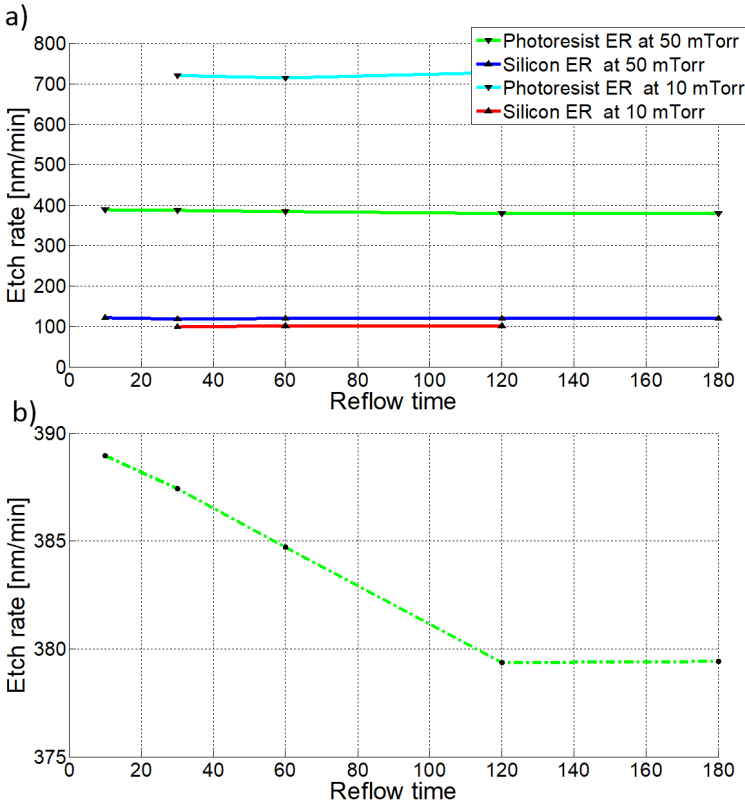


Figure 3.9: (a) Photoresist and Si etch rates versus resist reflow time at 10 mTorr and 50 mTorr; (b) zoom in on the photoresist etch rate at 50 mTorr.

To investigate chemical stability of the reflowed photoresist, the etch rate of both photoresist and Si at 50 mTorr and 10 mTorr versus thermal reflow time is given in Fig. 3.9a. As expected, the Si etch rate is not influenced by the photoresist reflow time. At 50 mTorr the etch rate is 120 ± 10 nm/min, while at 10 mTorr decreases to 100 ± 10 nm/min which is about 17% lower. Surprisingly, the photoresist etch rate drastically increases from ~ 380 nm/min to ~ 720 nm/min when pressure is lowered from 50 to 10 mTorr which is probably caused by an increased effective bias power.

Although the photoresist etch rate at 50 mTorr looks like it is not affected by the thermal reflow time, a slight decrease is visible when the reflow time increases (Fig. 3.9b). Photoresist etching results (Fig. 3.9b) shows that for $8 \mu\text{m}$ of initial resist thickness, the reflow time of 2 hours at 160°C is sufficient to achieve chemical stability for the dry etching process, since the etch rate goes into saturation. Any further thermal reflow will not influence the etching process and is therefore unnecessary.

Figure 3.10 reports the photoresist to Si selectivity for both pressure values versus

different reflow times. Using the 10 mTorr recipe to achieve $5.67\text{ }\mu\text{m}$ high Si microlens would require $40.82\text{ }\mu\text{m}$ of photoresist ball cap height and 57 minutes of etching. With 50 mTorr recipe and selectivity of 3.15, the initial ball cap height should be $17.86\text{ }\mu\text{m}$ and 45 minutes of etching would be required. Therefore, the 50 mTorr recipe is chosen as process recipe for the shorter etching time and smaller initial photoresist thickness needed for the reflow step.

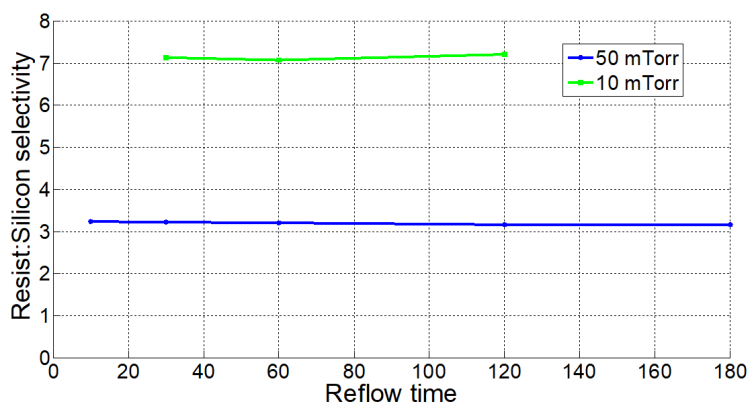


Figure 3.10: The Photoresist to Si etching selectivity at 10 mTorr and 50 mTorr.

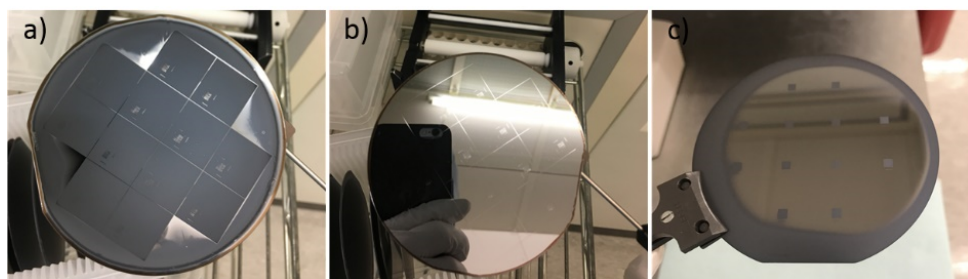


Figure 3.11: Influence of chamber cleanliness and exposed area on surface quality: (a) Before chamber wet cleaning - black Si formation during etching. (b) After chamber wet cleaning - good surface quality. The exposed area in this case is 85% (c) Clear effect of mask open area on surface quality: a 10% exposed area results in poor surface quality as compared to result for 85% exposed area.

A few other points of attention for a stable and reproducible process are the etching tool chamber conditions and the mask layout (% of exposed area) [24]. In Fig. 3.11a an image of a wafer after the lens etching process before wet cleaning of the reactor chamber is shown. The result after reactor wet cleaning is presented in Fig. 3.11b. The processed wafer in the first image has poor surface quality. The wafer is textured and there is not optical reflection from the wafer surface. In the second image, the processed wafer has a smooth surface and high optical reflection (the image of the phone used for the picture is clearly visible). Finally, in Fig. 3.11c the surface quality for a wafer etched with the same process but with a 10% dark field mask (10% open are) is shown. The surface

quality is much lower compared to the result achieved with a bright field mask (85% open area) reported in Fig. 3.11b.

3.2.3. SURFACE ROUGHNESS REDUCTION

The final step in the Si microlens fabrication process is the reduction of the surface roughness. This is done by oxidizing the silicon surface after the ICP etching (wet thermal oxidation [26,26]) and the subsequent removal of the grown SiO_2 layer using a BHF 1:7 solution at room temperature. To find the minimum SiO_2 thickness needed to achieve the lowest possible roughness several oxide thickness values have been tested. Figure 3.12 reports the root mean square value of the surface roughness, R_{RMS} , measured relative to ideal shape, versus grown SiO_2 thickness. A big improvement is observed after the removal of 1000 nm SiO_2 and the R_{RMS} continues to decrease with further increase of the oxide thickness, although in a less pronounced way, and after the removal of 2000 nm of grown SiO_2 no additional improvement in surface roughness is measured.

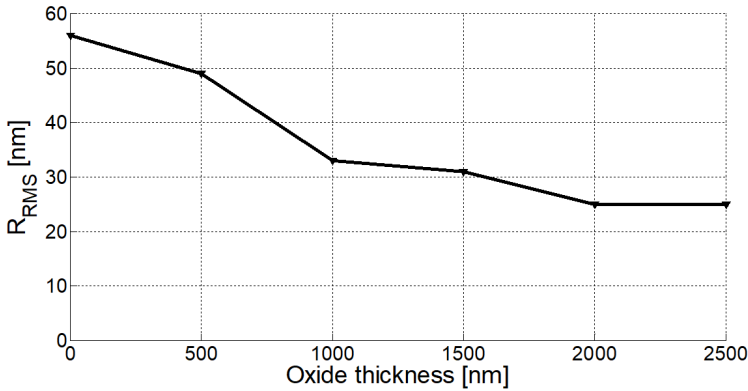


Figure 3.12: Root mean square value of roughness versus grown silicon dioxide thickness.

3.2.4. PROCESS FLOW OPTIMIZATION

After all process steps are investigated and individually optimized, Si microlenses are fabricated and tested utilizing the optimal sub-steps developed and described above. The diameter D of the microlenses is defined using standard lithography: photoresist coating, UV exposure and development. To ensure the photoresist adhesion to the Si surface, a hexamethyldisilazane (HMDS) adhesion promoter is applied. Then, *Micro-Chemicals* AZ9260 positive photoresist is dispensed, spun over the wafer and soft baked to get a 8 μm thick layer. Photoresist cylinders with diameter D are defined with ultra violet light exposure and photoresist development (Fig. 3.13a) using wafer stepper exposure tool.

The thermal reflow step to transform the cylinder into the ball cap (Fig. 3.13b) is done in an oven at 160 $^{\circ}\text{C}$, in vacuum, for 2 hours. The transfer of the photoresist ball cap into the silicon substrate is performed using the dry etching parameters reported in table 3.5 corresponding to a pressure of 50 mTorr for 35 minutes (Fig. 3.13c). After the etching

step (Fig. 3.13d) the wafers are cleaned and then oxidized (wet oxidation) to grow a 2.5 μm -thick layer of SiO_2 (Fig. 3.13e). The layer is then stripped in BHF 1:7 solution (Fig. 3.13f). A surface roughness reduction from 56 nm to 25 nm is measured. Details of the fabrication process are given in Appendix B.1.

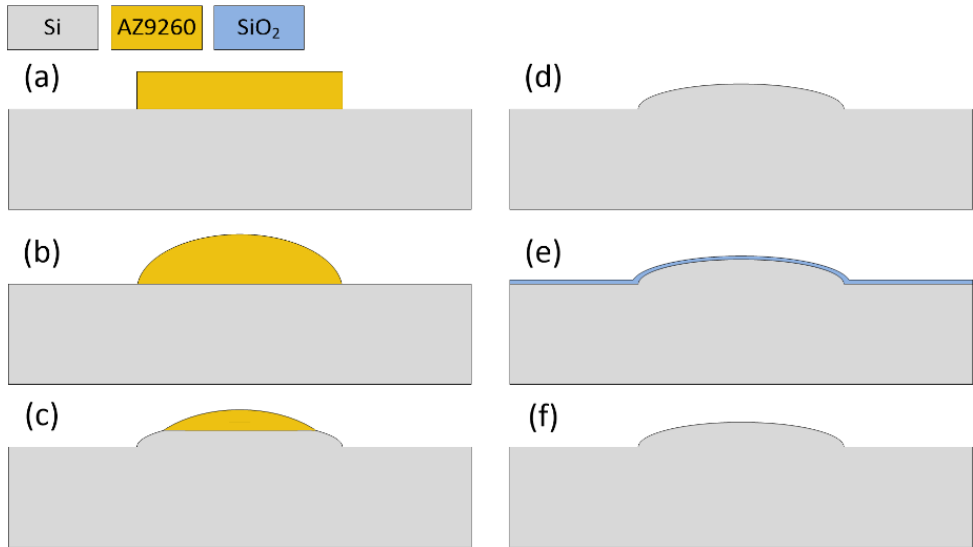


Figure 3.13: Main process steps for microlens fabrication: (a) UV lithography lens definition. (b) Thermal reflow of photoresist. (c) Lens formation during dry etching. (d) Si microlens after dry etching (e) Thermal oxidation for surface polishing. (f) Si microlens after oxide removal.

The process results are presented in Fig. 3.14. Figure 3.14a shows the SEM image of a Si microlens with a diameter of 150 μm , while in Fig. 3.14b a cross section of the lens is shown. The achieved radius of curvature R is 682 μm giving a focal length f of 955 μm and a numerical aperture NA of 0.27.

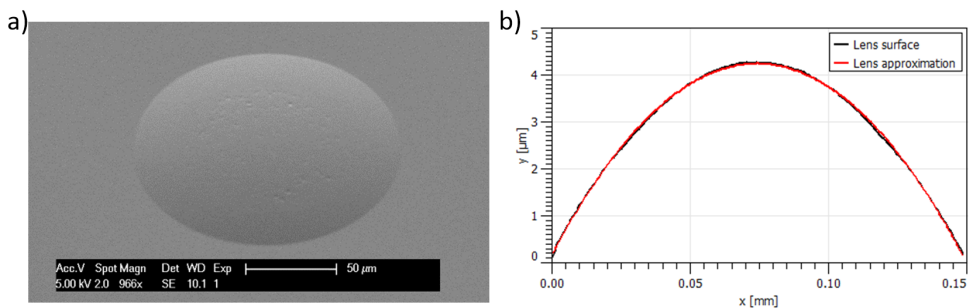


Figure 3.14: The fabrication of microlenses: (a) SEM image of a Si microlens with a diameter of 150 μm and a low surface roughness of 25 nm. (b) Microlens cross section and its approximation.

A comparison between calculated and measured values of lens radius of curvature for three different lens diameters is given in Table 3.6. The calculation of R_c is based

on the photoresist ball cap shape and experimental results of etching selectivity of the process given in Table 3.5 at 50 mTorr and for a reflow time of 2 h. The radius of curvature R_c is calculated according to the following formula:

$$R_c = \frac{S}{2 \cdot h_{bc}} \left(\frac{1}{4} D^2 + \frac{h_{bc}^2}{S^2} \right) \quad (3.7)$$

The results indicate the developed fabrication process is sufficiently optimized to fabricate lenses with the desired parameters. For all three lens diameters tested, the measured radius of curvature is within 5% from the calculated value.

Table 3.6: Comparison of calculated and measured lens radius of curvature for different lens diameters

Diameter D [μm]	Calculated radius R_c [μm]	Measured radius R_m [μm]	Error [%]
80	201	207	3.3
100	305	308	0.8
150	671	682	1.7

As mentioned in Chapter 2, the Si microlens must have a focal length equal to the wafer thickness, namely 700 μm , which corresponds to 500 μm radius of curvature. With a defined diameter of 150 μm , the top to bottom lens height h_s is 5.67 μm . Considering the selectivity values of 3.10 ± 0.1 for the etching process at 50 mTorr presented in Table 3.5, the initial photoresist ball cap height h_{bc} should be 17.6 ± 0.6 μm . From Eq. 1.1 and taking into account that around 20% of the photoresist volume will evaporate during the thermal reflow process, the initial photoresist thickness should be 10.9 ± 0.3 μm .

To obtain an initial photoresist thickness as close as possible to the desired value of 10.9 μm , a test was done to determine the optimal spinning speed. Test wafers were coated using spinning speeds ranging from 1050 rpm to 1200 rpm with an increment of 50 rpm. After coating, wafers were soft baked following the same baking steps and conditions in the automated coating/development track: 90 s at 100 °C and 120 s at 115 °C. However, wafers were not taken out of the light-controlled environment for thickness measurement. Instead, they are exposed with the mask of the designed lens patterns using ultra violet light to define cylinders with a diameter of 150 μm . After development, the wafers are baked for 4 h at 160 °C to allow the photoresist cylinders to reflow into spherical ball caps. The reflow time is intentionally set to be longer than the linear approximation based on the results for the 8 μm photoresist tests to ensure photoresist chemical stability. Finally, the wafers were dry etched (Table 3.5, 50 mTorr process) for 50 minutes. Using the *Dektak* stylus profiler, the Si microlens height is measured and results are summarized in Table 3.7.

Table 3.7: Final lens height versus resist spinning speed

Parameter	Values			
Spinning speed [rpm]	1050	1100	1150	1200
h_s [μm]	5.74	5.66	5.5	5.4

The lens surface roughness is then reduced with the above described oxidation procedure (2 μm of wet thermal oxidation at 1100 $^{\circ}\text{C}$ and oxide removal) and additionally, a 165 nm-thick SiN layer is deposited as an anti reflective coating. The geometry of the fabricated Si microlens is characterized using a white light interferometer (WLI) *Bruker* 3D microscope. The white light image of the lens with a diameter of 150 μm , is given in Fig. 3.15a, while in Fig. 3.15b the lens cross-section. Surface waviness due to Newton's rings, a consequence of light interference on SiN ARC layer, was observed. The spherical approximation of the lens geometry gives a radius of curvature $R_s = 520 \pm 10 \mu\text{m}$, which corresponds to a $730 \pm 30 \mu\text{m}$ focal length. The measured surface roughness is below 30 nm, which agrees with previously achieved results presented in this chapter. The calculated divergent angle is only $0.25 \pm 0.13^{\circ}$. Needless, this value will not diverge light significantly and the whole system will provide sufficient light focusing at the selected working distance of 5 cm.

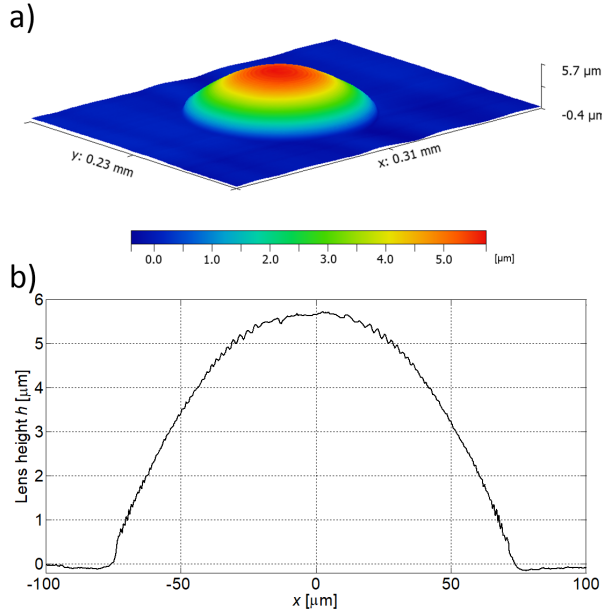


Figure 3.15: The fabricated Si micro lens: (a) WLI image (b) Lens cross-section.

3.3. WAVEGUIDE FABRICATION

THE photonic circuit built in the device layer of the SOI wafer is presented in Chapter 2. For the fabrication, a process initially developed by VTT [26-31] is transferred to our laboratory to be implemented in the same SOI platform with the lens and the actuators. First, test waveguide structures which consist of S-bends, rib-to-ridge converters, multi modal interferometers (MMIs) and waveguide crossings, are processed. A reference straight waveguide includes 2 ridge-to-rib converters and a straight rib waveguide. Waveguides with several Euler or S-bends, 3 1×2 MMIs: with no bends (MMI-2), S band

(MMI-3) and Euler bend (MMI-4); and one system of 2 1×2 MMIs in series with 3 outputs at the end (MMI-5) are included as well to test the propagation losses of the photonic circuit. Some test waveguides are designed to terminate with a 45° mirror facet. The layout of these test structures is shown in Fig. 3.16.

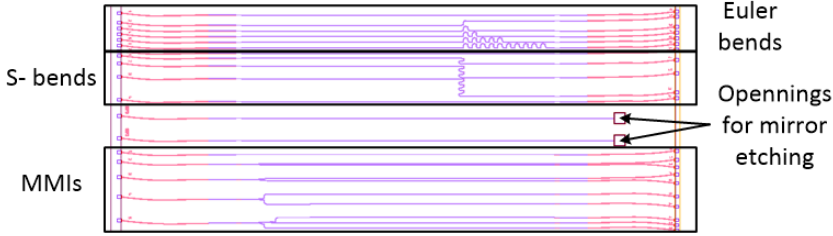


Figure 3.16: The mask layout containing test structures.

The main part of the waveguide fabrication is a two-step Si etching which defines the waveguide geometry. First, a PECVD silicon oxide hard mask is deposited and patterned using dry etching to define the top Si part of the rib and ridge waveguides (Fig. 3.17a). Next, a photoresist mask is added to define rib waveguides (Fig. 3.17b). The total height of the rib waveguide is $3 \mu\text{m}$ while for the ridge is $1.2 \mu\text{m}$. Therefore, the first Si dry etching, using the photoresist mask, is $1.8 \mu\text{m}$, while the remaining $1.2 \mu\text{m}$ is etched using silicon oxide as a masking layer (Fig. 3.17b-c). Next, similarly as for the lens surface roughness smoothening, waveguides sidewalls are smoothened using 500 nm thick thermal oxidation process and subsequent SiO_2 wet etch removal in buffered 1:7 HF solution (Fig. 3.17d-e). To provide good light coupling at entry facet, a 160 nm -thick LPCVD SiN antireflective coating is added and patterned, with silicon oxide as hard mask layer, using wet etching (Fig. 3.17f-g). Proper light confinement is ensured by a 240 nm -thick LPCVD SiO_x cladding layer definition (3.17h). All layers must provide uniform and sufficient sidewall coverage to withstand the isotropic characteristics of the subsequent wet etching. Finally, a $100 \mu\text{m}$ deep trench is etched next to the entry facet to provide space for a fiber butt coupling (3.17i). A detailed fabrication process flow is presented in Appendix B.2.

The main step of the two-step waveguide Si etching is done using a Bosch deep reactive ion etching (RIE) process with short cycles [30]. The idea behind is to avoid scattering losses induced by sidewall roughness created by normal ICP or RIE etching. Standard ICP or RIE dry etching process creates sidewall roughness which is perpendicular to the light propagation and it is responsible for scattering losses in waveguides. Instead, the Bosch process creates scallops which are in line with the light propagation. Thus, the scallops do not create any obstacle for the light propagation along the optical path. The parameters of the developed recipe for the waveguide etching process are given in Table 3.8.

The result obtained with 9 cycles of this etching process is shown in Fig. 3.18. The total height divided by the number of cycles gives a scallop size of approximately 170 nm . However, measurements show a scallop size of $200 - 210 \text{ nm}$ height and a total of 8 scallops where the first scallop is only around 100 nm height. The etching gas, SF_6 is

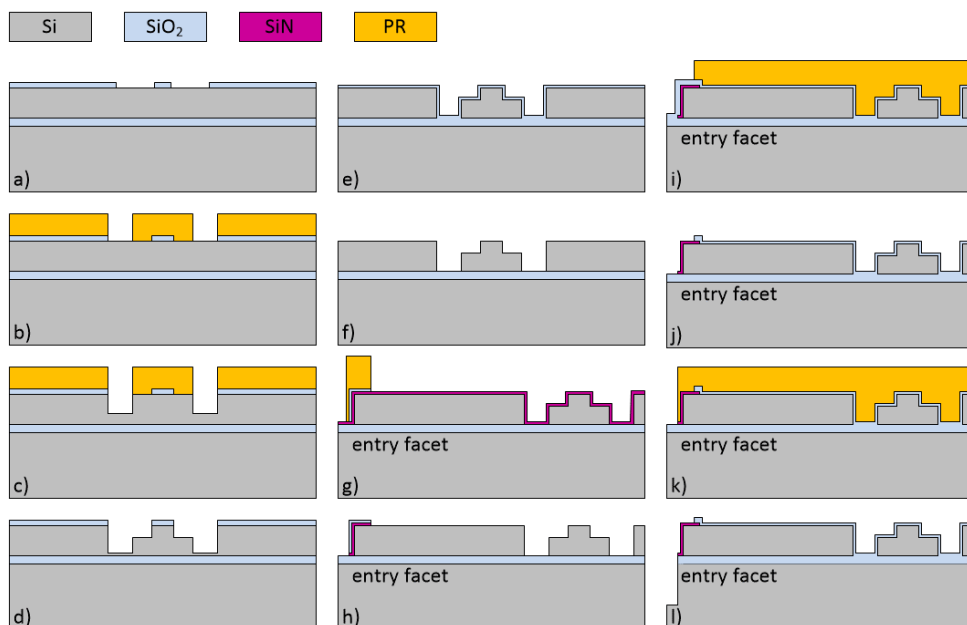


Figure 3.17: Waveguide fabrication process flow: (a) Silicon oxide hard mask definition for top rib and ridge waveguide definition. (b) Photoresist mask for rib waveguide definition. (c) First 1.8 μm deep Si etching step. (d) Photoresist removal and second 1.2 μm deep Si etching step. (e) Thermal oxidation for waveguide sidewall roughness reduction. (f) Oxide removal using wet etching. (g) Antireflective coating deposition and hard mask definition. (h) Antireflective coating patterning. (i) Cladding layer deposition and photoresist mask definition. (j) Cladding layer patterning and photoresist removal. (k) End facet definition. (l) End facet patterning.

Table 3.8: Final lens height versus resist spinning speed

Parameter	Passivation	Etch
Time [s]	1.2	1.8
Pressure [mTorr]	45	25
Source power [W]	2200	
C ₄ F ₈ [sccm]	280	0
SF ₆ [sccm]	0	350
Platen power [W]	0	80
Duty cycle	20 %	
Platen temperature [°C]	20	

highly selective to SiO₂. Since there is always the formation of native SiO₂ on the wafer surface [31], the first and part of the second cycle are used to break through the native SiO₂ which results in a lower step height with respect to the subsequent cycles.

To overcome this problem, an etch in 0.55% HF solution for 4 minutes is introduced to remove the native oxide and passivate the Si surface just before any DRIE process for waveguides fabrication takes place. The vertical cross-section of the rib-to-ridge converter etched in two steps of 9 and 6 cycles, respectively, with native oxide removal prior

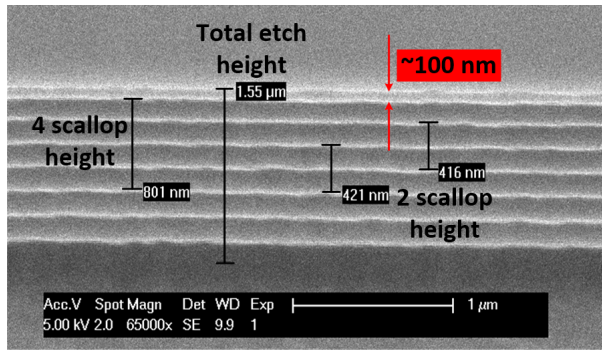


Figure 3.18: SEM image of the waveguide sidewall after etching without native oxide removal prior to etching.

to etching, is presented in Fig. 3.19a. The targeted depth of $3 \pm 0.1 \mu\text{m}$ is achieved with a total of 15 cycles, each 200 nm in depth. In Fig. 3.19b and In Fig. 3.19c cross over of two waveguides before and after the 500 nm thermal oxidation process and subsequent oxide removal, are shown. As expected, the waveguide width and height are reduced due to silicon consumption during SiO_2 growth. Figure 3.19d shows the waveguide entry facet with antireflective coating and cladding layer in front of the facet. Finally, a deep trench in front of the entry facet is etched to define the end facet for fiber coupling.

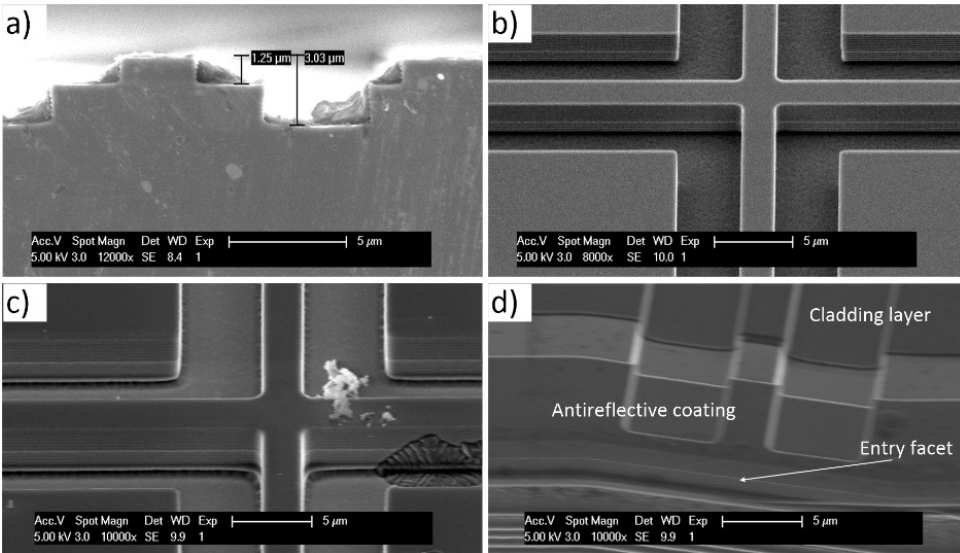


Figure 3.19: Waveguide fabrication results: (a) Vertical cross section of the rib-to-ridge waveguide converter. (b) Waveguide cross over before smoothing process. (c) Waveguide cross over after finished fabrication. (d) Waveguide entry facet with cladding layer and antireflective coating.

The fabricated test waveguides are characterized at Medlumics S.L. facility in Madrid, Spain using the setup depicted in Fig. 3.20. Light coming out of the $1.3 \mu\text{m}$ super lumi-

nescent diode (SLED) is coupled to the waveguide using lensed fiber. At the waveguide end is decoupled to the fiber again and reaches the photodetector. The measured total waveguide losses are summarized in Table 3.9. These results indicate that there are almost no losses through Euler bends while S-bends measurements showed a large deviation from mean values. Multimodal interferometers with one input and two outputs are used as beam splitters. Hence, it is expected to have at least 3 dB of additional optical losses at each output. Measurements show a total loss of 8 dB, which causes an additional 4 dB per output. Measurements results for MMI-5 are in line with values observed on a single 1×2 MMIs.

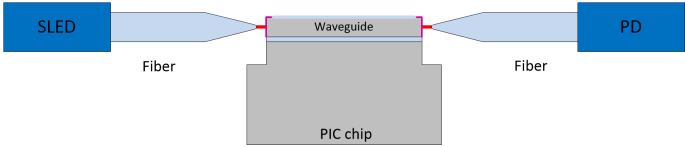


Figure 3.20: SEM image of the waveguide sidewall after etching without native oxide removal prior to etching.

Table 3.9: Total waveguide losses

Waveguide type	Total optical losses [dB]
Straight waveguide	3.0 ± 0.6
1 Euler bend	2.9 ± 0.1
4 Euler bends	3.1 ± 0.7
10 Euler bends	3.2 ± 1.0
20 Euler bends	2.9 ± 0.4
2 S-bends	4.3 ± 2.6
4 S-bends	3.4 ± 0.7
6 S-bends	3.9 ± 1.7
MMI-2 output 1	7.8 ± 0.8
MMI-2 output 2	7.7 ± 0.8
MMI-3 output 1	8.0 ± 0.9
MMI-3 output 2	8.1 ± 1.0
MMI-4 output 1	7.7 ± 0.1
MMI-4 output 2	8.1 ± 0.6
MMI-5 output 1	13.1 ± 0.2
MMI-5 output 2	12.4 ± 0.3
MMI-5 output 3	9.6 ± 0.7

The measured losses are slightly higher (1-2 dB in average) than in commercially available passive optical circuitry. The beam splitters (1×2 MMIs) used for interferometer introduce only 1 dB additional losses. Therefore, the optical quality of the presented process flow for photonic interferometer fabrication is suitable for the development of the first ‘single-chip’ OCT scanner.

3.4. MIRROR FABRICATION

THE light from the waveguide must be deflected towards the Si microlens at the back-side of the chip. Thus, the waveguide must finish with a 45° facet as explained in Chapter 2. Total internal reflection provides no optical losses. However, a rough facet surface can induce scattering losses and deteriorate the signal. Thus, a combination of grayscale lithography and dry etching process cannot be used (Fig. 3.2). An alternative is the use of silicon wet anisotropic etching in alkaline solution, in which the etch rate for each silicon crystal plane is different [32].

The use of $\langle 110 \rangle$ plane Si micromirrors is reported in [33-40]. All of them, are fabricated using either potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAOH) based solutions. Mainly, 45° facets in Si are used for micro optical benches in combination with fibers [35-38] for sensing applications or as a waveguide reflector integrated on a SOI based micro optical bench for interconnect transmitter application [40].

KOH, and TMAOH based solutions are often used due to their selectivity to $\langle 111 \rangle$ Si planes while the etch rate of $\langle 100 \rangle$ plane, the most common crystal orientation for Si wafers in IC manufacturing technology, is high. The other two main planes, $\langle 110 \rangle$ and $\langle \bar{1}\bar{1}0 \rangle$, are oriented at 45° and 54.7° with respect to the $\langle 100 \rangle$ plane. Usually, lithography patterns are mainly oriented in the $\langle 110 \rangle$ direction due to $\langle 110 \rangle$ primary flat orientation. Thus, etching will result in exposure of $\langle 111 \rangle$ plane (Fig. 3.21a) [33,34]. If the mask opening is rotated 45° , it is oriented in the $\langle 100 \rangle$ direction and etching will expose $\langle 110 \rangle$ planes which form a 45° angle with $\langle 100 \rangle$ surface plane (Fig. 3.21b) [33,34].

Anisotropic etching with alkaline based solution usually gives a rough silicon surface. Application of additional surfactants can reduce surface roughness of $\langle 110 \rangle$ and $\langle 100 \rangle$ planes [33,34, 36-38]. Different etching properties of KOH and TMAOH with isopropanol are compared in [36], while in [37] the influence of Triton-X-100 surfactant on surface roughness and anisotropy is studied. The study in [37] showed that for more than 10 ppm of Triton-X-100 concentration in 25% TMAOH, no significant improvement in surface quality is observed. Thus, a 25% TMAOH etching solution with 50 ppm of Triton-X-100 at 85°C is used here.

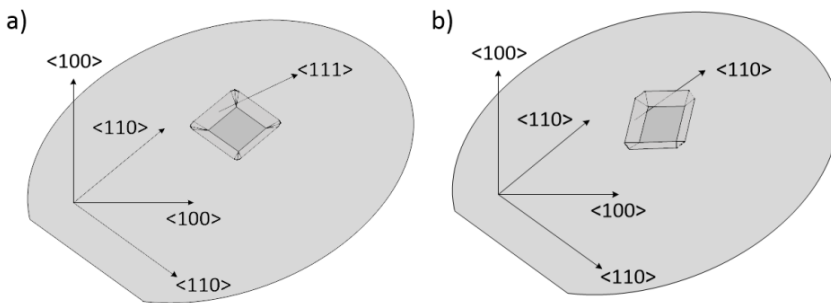


Figure 3.21: Exposed crystal planes during KOH and TMAOH anisotropic etching: (a) Opening oriented to $\langle 110 \rangle$ plane, standard orientation of mask opening compared to primary flat in IC fabrication. (b) Opening oriented to $\langle 100 \rangle$ plane, 45° rotation compared to standard mask alignment.

According to [38] the etch rate of $\langle 100 \rangle$ plane is around $0.55 \mu\text{m}$ per minute, while the etch rate of $\langle 110 \rangle$ plane is 4 times slower. Therefore, a test etch of 30 minutes is performed after adding 50 ppm of Triton-X-100. A 200 nm of LPCVD silicon oxide was patterned as a hard mask for mirror fabrication. A passivation of the Si surface is done using 4 min HF etching and Marangoni drying to avoid native oxide formation. The etching results are presented in Fig. 3.22. A detailed process flow is given in Appendix B.3.

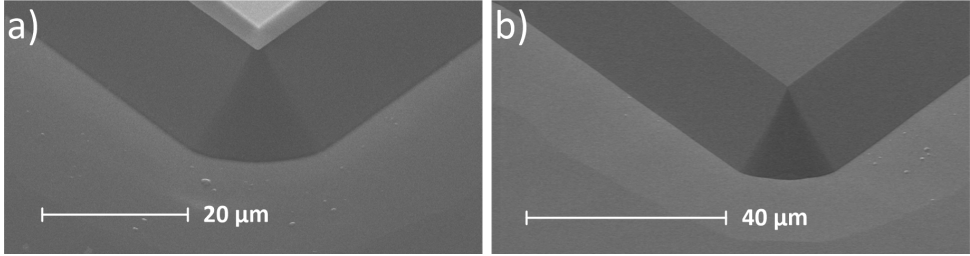


Figure 3.22: The Si mirror: (a) 45° facet after etching. The oxide hard mask is still there and (b) 45° facet after hard mask removal.

3.5. INTEGRATION OF ALL OPTICAL COMPONENTS

THE next step towards fully integrated OCT system is to combine all optical components in one device. From the fabrication point of view, this means that the three process flows described in this chapter for the lens, the waveguides and the mirror, need to be merged in a single process flow. First, the main steps of integration are discussed and then the fabrication and characterization of the ‘single-chip’ with all optical components is presented.

3.5.1. CONSIDERATIONS ON ORDER AND MERGING OF FABRICATION STEPS

First, we need to define the best order of components fabrication and, at the same time, which fabrication steps, common to more than one component, can be combined. The optical alignment of the components is guaranteed by the exposure tool, so no special measures are needed for that, and it is thus within 100 nm. The full device layout is rotated 45° with respect to the wafer primary flat to fabricate the 45° mirror facets (Fig. 3.21). This has no influence on the fabrication of the lens and waveguides.

The Si microlens fabrication process is developed on the polished side of a wafer. The photonic circuitry is built in the device layer of a $700 \mu\text{m}$ -thick SOI wafer, with a 400 nm-thick buried oxide layer and a $3 \mu\text{m}$ device layer. Since the lens is placed on the backside of the chip, the starting material must be a double side polished (DSP) SOI wafer. The thickness of the device layer is quite sensitive to any thermal oxidation process which consumes silicon. Therefore, the starting device layer is determined considering all oxidation steps necessary throughout the fabrication process.

The waveguide fabrication process contains a 500 nm-thick thermal oxidation step for sidewall surface quality improvement (Appendix B.2). Unlike waveguides, the 45°

mirror facet does not require any smoothening step (Appendix B.3) and thus it will not cause additional consumption of the silicon device layer. The remaining optical component which needs to be integrated is the Si microlens. The fabrication flow for the lens has a 2500 nm thermal oxidation step for surface quality improvement (Appendix B.1). The total silicon consumption for both oxidation steps is 1350 nm (225 for waveguides and 1125 for the lens). This brings to a total silicon device layer starting thickness of 4350 nm.

Once the starting material parameters are defined, the order of component integration must be established. Although the mirror fabrication does not require any smoothening step, it can be fabricated after the two-step waveguide etching and before the thermal oxidation (Fig. 3.17d and Fig. 3.17e, Appendix B.2.). This way, the mirror surface quality would either stay the same or it will improve. The remaining component, the Si microlens can be added after waveguide and mirror fabrication. In that case, there will be significant Si consumption below the SiO_x cladding layer. To prevent that, the lens must be fabricated as the first component in the integrated system.

All optical components require an antireflective coating (ARC), namely a 165 nm-thick SiN. Deposition of one ARC layer for the lens and one for waveguides would require unnecessary deposition and removal of additional protection layers. Thus, to optimize the fabrication process the depositions of the ARC SiN will be done only once, for both components and thus moved later in the process flow, namely after the waveguide side-wall surface quality improvement step.

In conclusion, the starting material must be a double-polished SOI wafer with a 4350 nm-thick device layer, a 400 nm buried oxide layer and a total thickness of 700 μm . The above-mentioned considerations determine the order of optical component fabrication: first the microlens, then the waveguides, followed by the mirror and finalized with the surface smoothening oxidation. In the end, margining all antireflective coating deposition in one single step simplifies the fabrication process.

3.5.2. FABRICATION OF ALL OPTICAL COMPONENTS

The fabrication process starts with the deposition of 1 μm -thick PECVD SiO_x layer on the front side of the wafer as scratch protection during the microlens fabrication (Fig. 3.23a) at the wafer backside. For the Si microlens the process described in section 3.1.4 is used. The scratch protection SiO_x layer must be removed using wet etching before the lens smoothening step (Fig. 3.13e) to accurately control the Si device layer consumption during the 2.5 μm -thick thermal oxidation.

An additional step, a 1 μm -thick PECVD SiN scratch protection layer, is now required to protect the lens during the following process steps. But, the device layer on the front side before this SiN deposition must be protected as well. For this purpose, the 2.5 μm -thick thermal SiO_2 for lens surface quality improvement can be used. The front side of the wafer is coated with photoresist and then, the thermal silicon dioxide is removed, using wet etching in HF solution, only from the wafer back side, i.e. lens surface (Fig. 3.23b).

A 1 μm -thick PECVD SiN scratch protection layer is now deposited on the wafer backside and the oxide layer at the front side can be stripped, clearing the device layer surface (Fig. 3.23c). At this point, the wafer is ready for the waveguide and mirror fabrication.

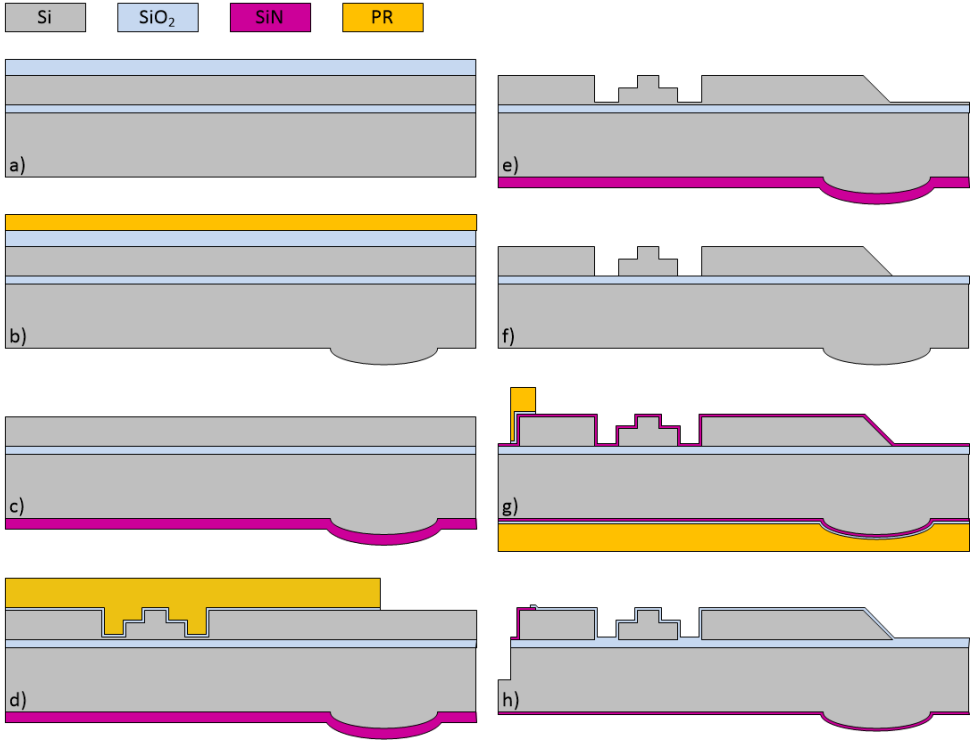


Figure 3.23: Main process steps for the integration of all optical components: (a) PECVD SiO_x as device layer scratch protection (b) Lens formation and surface quality improvement by oxidation and subsequent oxide removal. (c) Lens scratch protection PECVD SiN deposition (d) Two-step etching for waveguide definition and hard mask definition for mirror etching. (e) Mirror etching and hard mask removal. (f) SiN scratch protection removal and thermal oxidation for surface quality improvement. (g) Additional photoresist coating for the backside antireflective coating protection. (h) Final view of the chip cross section with all optical components.

The next step is waveguide fabrication using the two-step etching described in section 3.2. (Fig. 3.17a-d, Appendix B.2). After hard mask removal, a 300 nm of LPCVD SiO_x is deposited and patterned as a hard mask for the mirror fabrication (Fig. 3.23d). Then, the 45° facet is fabricated by 6 min etching in TMAOH based solution (section 3.3) after which the hard mask is removed (Fig. 3.23e). To continue with the rest of processing steps for waveguide fabrication (thermal oxidation, antireflective and cladding layer deposition etc.), the lens protective SiN must be removed using H_3PO_4 solution at 157°C (Fig. 3.23f).

From this point on, the process flow follows the sequence developed for waveguide fabrication (Appendix B.2) up to the hard mask for antireflection coating definition (Fig. 3.17g). Here, the antireflective coating must be protected also on the lens surface. Thus, additional photoresist coating on the backside is needed to protect the LPCVD SiO_x hard mask layer (Fig. 3.23g). The fabrication is finished by repeating the steps described in Fig. 3.17h-l, where antireflective coating, cladding layer and entry facet are defined (Fig. 3.23h). Details of the fabrication process flow are given in Appendix C.

Fabrication results are illustrated in Fig. 3.24. In Fig. 3.24a the SEM image of an integrated 45° mirror facet at the end of the waveguide is shown. The slope length showed in this SEM image is 3 μm long. Also, the step height measurement using stylus profilometer gives a total height of 3 μm as expected. Thus, the facet is indeed at 45°. In Fig. 3.24b a 3D topography image of a Si microlens obtained with white light interferometry is reported. The radius of curvature of the microlens is $567 \pm 2 \mu\text{m}$, which corresponds to a focal length of $794 \pm 3 \mu\text{m}$ which will theoretically in beam divergence of 0.75°.

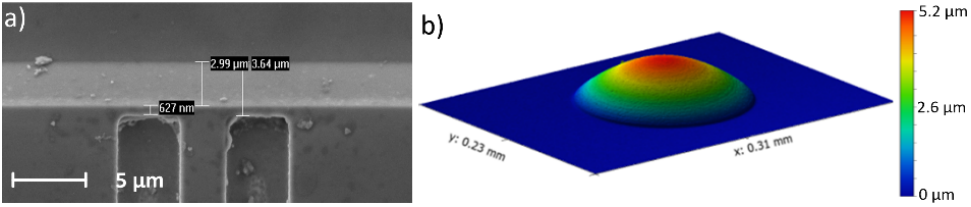


Figure 3.24: Fabrication results of integrated process flow: (a) Top view SEM image of 45° waveguide ending facet. (b) WLI profile image of Si microlens.

Table 3.10: Total waveguide losses

Waveguide type	Total optical losses [dB]
Straight waveguide	6.1
1 Euler bend	5.3
4 Euler bends	5.7
10 Euler bends	5.8
20 Euler bends	6.1
2 S-bends	8.0
4 S-bends	6.2
6 S-bends	7.2
MMI-2 output 1	9.6
MMI-2 output 2	9.4
MMI-3 output 1	9.5
MMI-3 output 2	9.5
MMI-4 output 1	10.2
MMI-4 output 2	10.1
MMI-5 output 1	18.0
MMI-5 output 2	9.6
MMI-5 output 3	9.6
Waveguide + Mirror 1	4.8
Waveguide + Mirror 2	4.8
Waveguide + Mirror 3	5.7
Standard deviation	2.9

The total optical losses of the waveguides and integrated waveguide and mirror are presented in Table 3.10. Measurements are performed at Medlumics S.L using the setup in Fig. 3.20. Optical losses are on average 3 dB higher compared to the result given in Table 3.9. However, as the error in these measurements is almost 3 dB as well, we cannot draw conclusions about the influence of additional processing steps in integrated flow compared to the process used for waveguide fabrication only (Section 3.2). The reason for the large measurement error could be polymer residues at the waveguide entry facet. The residues are the result of the end facet definition step where the deep trench is etched using a Bosch process. Another source of the measurement uncertainty could be the fiber coupling (Fig. 3.20). If one of the lensed fibers is damaged at the coupling lens surface, then this could introduce additional scattering losses in the total optical path.

To measure the mirror losses, the setup from Fig. 3.20 was modified and only one lensed fiber was used to couple the light in the system. The light was detected with a large surface area photodetector placed below the chip. Measured optical losses for waveguide with 45° end facet showed approximately 1 dB better values than straight waveguides. Since in this system only one waveguide entry facet is used, this can be an indication that there are large coupling losses. Assuming a 1 dB of additional coupling losses at entry facet, the total losses of the waveguide with mirror should be around 4 dB. Comparison of the results for straight waveguides from Table 3.9 with this value, suggests the mirror optical losses to be below 1 dB. However, due to large measurement uncertainty, the optical performance of the mirror should be taken just as an indication and better characterization is needed to verify it. Nevertheless, optical test of the waveguide with mirror and the lens showed no additional signal degradation.

3.6. CONCLUSION

IN this chapter the fabrication process for the optical components of the integrated OCT system were described and discussed. First, the fabrication process for Si microlenses was developed and optimized. Then, the waveguide fabrication process was transferred from VTT to our laboratory and fabricated test waveguides were characterized at Medlumics S.L. to validate the successful transfer of the technology. The mirror fabrication was implemented based on data and reports from literature. In the end, all components are integrated in one chip thus, finalizing the first step of the envisioned monolithically integrated OCT system.

The analysis of thermal reflow process of AZ9260 showed it is possible to control and optimize the photoresist ball cap size for Si lens fabrication. Since the base of the ball cap is a circle, naturally, the cylinder will turn into the ball cap to minimize the surface tension. By changing initial photoresist thickness and with the evaporating of all solvents from the resist, the total volume of the ball cap can be controlled.

The photoresist ball cap was successfully transferred into Si using reactive ion etching. Once the ball cap size is fixed, the final lens shape can also be changed by changing the gas flow ratio, pressure, temperature or bias power of the etch process. This step was optimized for the most important parameter, namely the surface smoothness. The final Si microlens has the targeted height of 5.67 μm with a surface roughness of 56 nm. A thermal oxidation step of 2.5 μm was implemented to improve the surface quality and the roughness is reduced to only 25 nm.

The thick Si waveguides technology was successfully transferred from VTT and adapted to the etching capabilities available in our laboratory. Optical characterization of test structures, performed at Medlumics S.L., showed only 1 dB difference compared to the commercially available technology offered by VTT. The difference probably comes from non-optimized waveguide etching. Even the roughness is reduced with thermal oxidation, there is probably still surface waviness which may introduce additional scattering losses at the facet.

The integration process of all photonic components is based on the combination of the developed 3 optical modules: microlens, waveguides and mirror. The system design and the order of component fabrication in the integrated flow determines the initial device layer thickness of the DSP SOI wafers.

Optical propagation measurements on test structures showed unexpectedly higher optical losses compared to the first run. Analyzing the measurement results of the waveguide mirror system, it can be assumed the main source for higher losses is related to the waveguide entry facet. With this assumption, the integrated mirror adds less than 1 dB of losses to the system. The waveguide-mirror-lens integrated structure showed no additional optical signal degradation.

All components and their fabrication processes should be further improved to reach the optimal optical performance of the integrated chip. However, the goal of this work is to demonstrate a fully integrated OCT system and for a first proof of principle the presented optical performance of waveguide-mirror-lens chip is acceptable. In the next chapter the fabrication of the MEMS actuators to be integrated within this optical chip will be reported.

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4

ACTUATOR SYSTEM FABRICATION AND CHARACTERIZATION

Brain is better than brawn

Folk proverb

The MEMS actuator systems for x and y direction scanning presented in Chapter 2 is to be integrated with the optical components on the same platform to be combined in one device. The fabrication must therefore be compatible with the process previously developed for the fabrication of the optical components. In the first part of this chapter the wafer-level fabrication flow for the MEMS actuator systems is described and the critical steps are discussed. In the second part, the electro-mechanical characterization of the fabricated devices is presented.

Parts of this chapter have been published in "A MEMS Actuator System for an Integrated 3-D Optical Coherent Tomography Scanner", *Journal of Microelectromechanical Systems* **27**(2), 259-268 (2018).

4.1. ACTUATOR FABRICATION PROCESS

THE bimorph beam actuators presented in Chapter 2 are made from aluminum and silicone oxide. Since the optical circuitry fabrication flow uses process steps at temperatures above the melting point of aluminum, the MEMS actuator fabrication must take place on the already finished photonic platform. The waveguide system for the Si-based photonic interferometer for the OCT scanner utilizes the device layer of a silicon-on-insulator (SOI) wafer. As this layer is only 3 μm thick, for a fully integrated chip, the mechanical hinges need to be built in the bulk silicon. Both x and y actuator systems use aluminum and silicon oxide layers of the same thickness. Also, the torsional and deflecting hinges have the same thickness as well. This makes it possible to fabricate both actuator systems with the same process flow. The process flow can be separated into two modules: the bimorph definition and the hinge definition. For the development of the MEMS actuator process flow, single side polished 525 μm -thick Si wafers are first used as starting material. The defined process flow will be later integrated in the process flow developed for the optical components on SOI wafers.

4.1.1. BIMORPHS DEFINITION

The first step in the fabrication of the MEMS actuator system is the deposition of a sacrificial layer, which will be later removed for the final device release. PECVD silicon oxide is chosen as sacrificial layer. This layer must be thick enough to cover the 3 μm -high Si waveguides, which need to be protected during actuators fabrication. Thus, a 4 μm silicon oxide layer is used. The next steps must define the bimorph actuator. Ideally, the heater should be placed between the two bimorph layers to minimize heat losses. According to the system design given in Chapter 2, the bimorph bottom layer is aluminum and it must be isolated from the heater, made of a thin aluminum layer. This can be done by depositing an insulating layer in between them. However, as the bimorph aluminum layer is quite thick (2 μm), the resulting topography causes poor sidewall coverage of the thin sputtered aluminum heater layer (Fig. 4.1a). Another option is to place the thin Al heater layer directly on the aluminum bimorph layer, so that no topography is there (Fig. 4.1b). However, the thin insulation layer will be damaged during wire bonding, causing short circuit problems. The possibilities to place the heater in between the bimorph layers and to overcome the step coverage and wire bonding problems are to add another interconnect Al layer (Fig. 4.1c) or to include a planarization step for the insulation layer (Fig. 4.1d). Both solutions require additional processing steps which would increase the complexity of the fabrication. Also, the additional interconnect layer (Fig. 4.1c) must be thick enough to overcome the high topography of the bimorph beam which further increases wafer topography, with possible problems in subsequent steps.

As all presented options have issues or increase fabrication complexity, we chose to place the heater below the entire bimorph beam. Thus, the 300 nm-thick aluminum layer for the heater is sputtered directly on top of the sacrificial layer and patterned using wet etching (Fig. 4.2). This approach significantly simplifies the fabrication process as at this point the wafer surface is still flat. The drawback is the reduction of the bimorph heating efficacy since the bottom surface of the heater is later exposed to air.

The sacrificial layer also serves as an electrical insulation between the Si substrate and the metal heater. Therefore, the sacrificial layer needs to be patterned to define

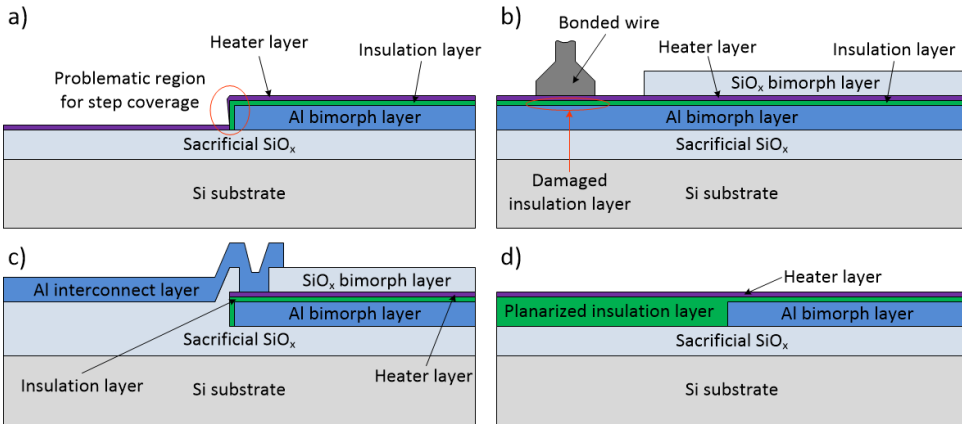


Figure 4.1: Possible configurations of heater placement: (a) Deposition of heater layer above patterned aluminum bimorph; (b) Using aluminum bimorph layer as a planar surface for the heater; (c) Using an additional thick aluminum interconnect layer; (d) Using a planarization process to reduce wafer topography.



Figure 4.2: The first steps of the MEMS actuator fabrication: Sacrificial layer deposition and Al heater definition by sputtering and wet etching.

the area which serves as an anchor for the actuators and the one needed as insulator for the heater. Since the same layer is used as sacrificial layer and insulation, the areas intended as insulation must be protected during the final device release step. In surface and bulk micromachining, sacrificial oxide is usually removed using HF as a wet solution or as vapor. Using wet chemistry for actuator release can introduce bimorph stiction to the Si substrate, which will negatively affect the performance of the actuator system. As etching in vapor HF prevents stiction, we selected this method for the release of the actuators. This implies that the silicon oxide insulation layer must be protected with a masking layer which is highly selective to vapor HF etching. According to Primaxx uEtch tool support information, aluminum oxide has high resistance to HF vapor and can be used as protective layer during the vapor HF release step.

Patterning of the oxide sacrificial layer using only anisotropic dry etching will create steep sidewalls and it may require the deposition of a thick protective layer to ensure good coverage of the corners. Therefore, the insulating and sacrificial area definition should be done using wet etching of silicon oxide. On the other hand, long wet etching in a HF solution may influence photoresist adhesion to the silicon oxide, which results in unwanted photoresist peeling off and, consequently, under etching of the silicon oxide layer (Fig. 4.3). Therefore, the sacrificial layer patterning is done using a combination

of dry plasma and wet etching to create a slope and so facilitate step coverage of the subsequent deposited layer, the protective 100 nm-thick Al_2O_3 , while avoiding peeling off of the resist.

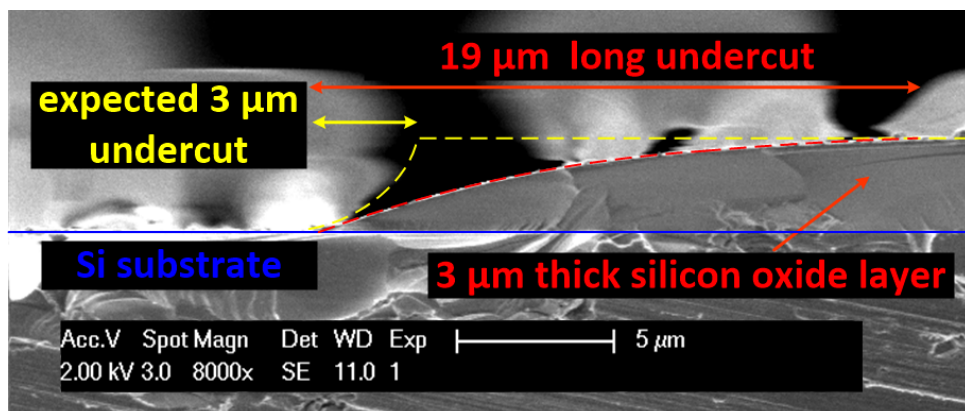


Figure 4.3: Severe undercut observed in a 15 min long etching step, with bad adhesion of the photoresist layer to the 3 μm thick silicon oxide layer. The etching resulted in 19 μm instead of the expected 3 μm long undercut.

The protective layer, atomic layer deposited (ALD), also serves as an electrical insulation between the heater and the bimorph layers. Hence, the thickness of the protective layer is chosen to ensure a good electrical insulation as well. This stage of the process ends with the opening of windows in the Al_2O_3 layer to allow electrical connection to the heater. Since both wet and dry chemistry for aluminum oxide etching also attack aluminum, the contacts are opened by dry etching in F-based chemistry which etches both layers with the same etch rate. This implies a certain consumption of the heater layer at the contact openings which can be minimized by limiting over etch time. These steps are illustrated in Fig. 4.4.

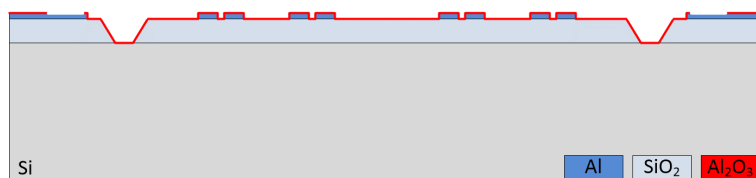


Figure 4.4: Sacrificial layer definition: Silicon oxide sacrificial layer patterning and Al_2O_3 protective layer deposition. The Al_2O_3 layer is patterned to open contact windows to the heater.

The bimorph formation starts with a 2 μm -thick aluminum layer sputtered at 350 $^{\circ}\text{C}$. Then, 2 μm -thick silane-based PECVD silicon oxide layer is deposited at 400 $^{\circ}\text{C}$ (Fig. 4.5a). These are the same layers used for the stress modeling of the actuator design presented in Chapter 2. To optimize the number of processing steps, the interconnect to the heater bond pads will be defined in the aluminum bimorph layer as well.

The silicon oxide bimorph layer is patterned by dry etching in F-based chemistry, which is highly selective to Al. After patterning, the bimorph silicon oxide must be pro-

tected from vapor HF during device release. Also, in this case ALD aluminum oxide is used (Fig.4.5b). The protective layer must be thick enough to ensure coverage of the silicon oxide sidewalls and of the edge of the aluminum/silicon oxide interface. Due to surface roughness of the aluminum layer and rough sidewalls of the patterned silicon oxide, a 100 nm-thick ALD aluminum oxide is now not enough to ensure full sidewall coverage of the silicon oxide (Fig. 4.6). To fully protect the bimorph silicon oxide layer, the aluminum oxide thickness is increased to 200 nm (Fig. 4.7).

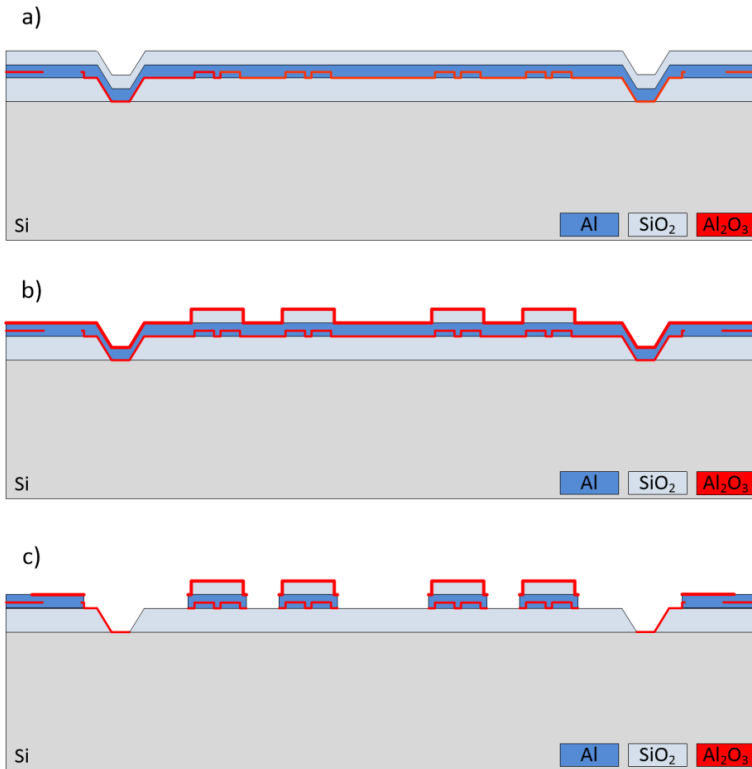


Figure 4.5: First part of bimorph formation: (a) Aluminum and silicon oxide deposition; (b) Bimorph silicon oxide patterning and ALD aluminum oxide deposition for vapor HF protection; (c) patterning of aluminum oxide layer.

The final part of bimorph layer definition is the bimorph aluminum layer patterning. The 200 nm-thick protective aluminum oxide is removed using dry etching in F-based chemistry and landing on the aluminum layer. Then, using a dry etching process in Cl-based chemistry, the bimorph beam is defined. The actuators are finished with removal of unnecessary aluminum oxide to reveal the sacrificial silicon oxide and to open the bond pads for electrical connection. These steps are summarized in Fig. 4.5c.

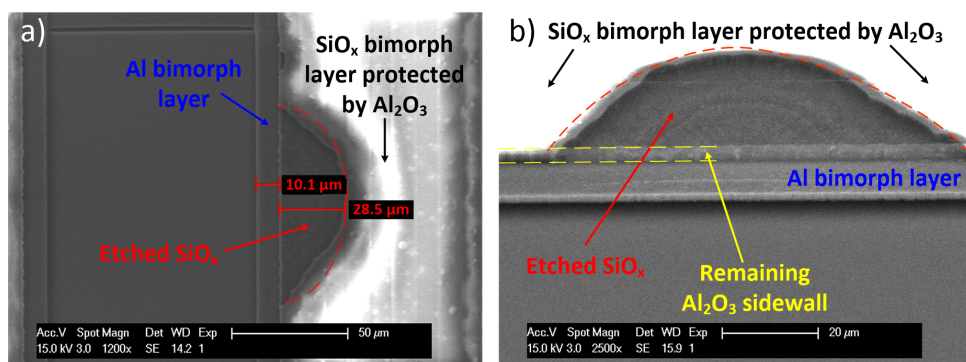


Figure 4.6: Insufficient protection of the bimorph oxide layer with 100 nm-thick ALD Al₂O₃: Top (a) and side (b) view of the unwanted etch of the SiO_x layer

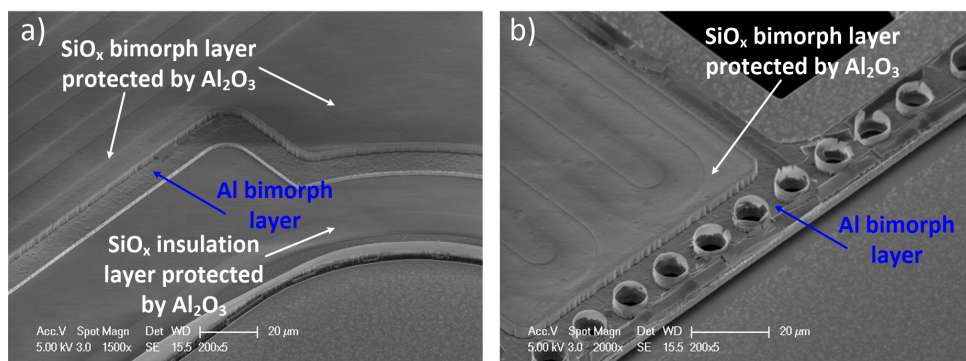


Figure 4.7: Effective protection of the bimorph oxide layer with 200-nm thick ALD Al₂O₃: (a) Bimorph layers of y direction scanning actuator anchored to the microplate. (b) Tip of the x direction scanning actuator.

4.1.2. HINGES DEFINITION

The second part of actuator system fabrication is the definition of both torsional and deflecting hinges. The process flow is based on the one developed for the test hinges given in Chapter 2. First, the sacrificial layer is removed to expose the silicon substrate to be etched from the front side. A 15 μm-deep silicon etch, using a deep reactive ion etching (DRIE) Bosch process, defines the hinges geometry. Then, a low-stress (40 MPa), 5 μm-thick PECVD SiO_x is added as stop layer for the etching from the backside. These steps are depicted in Fig. 4.8a.

The backside processing starts with the patterning of a thick silicon oxide hard mask layer for DRIE of the silicon substrate (Fig. 4.8b). While for the test hinges run only one backside etching step was required as no actuators were included, now we need to divide it into two steps. The hinge definition step (Fig. 4.8a) also leaves unwanted Si below the actuators. Therefore, an initial 50 μm-deep etching step using photoresist as a mask, is introduced to consume Si in areas below the actuators, while leaving a Si buffer below the hinge (Fig. 4.8c).

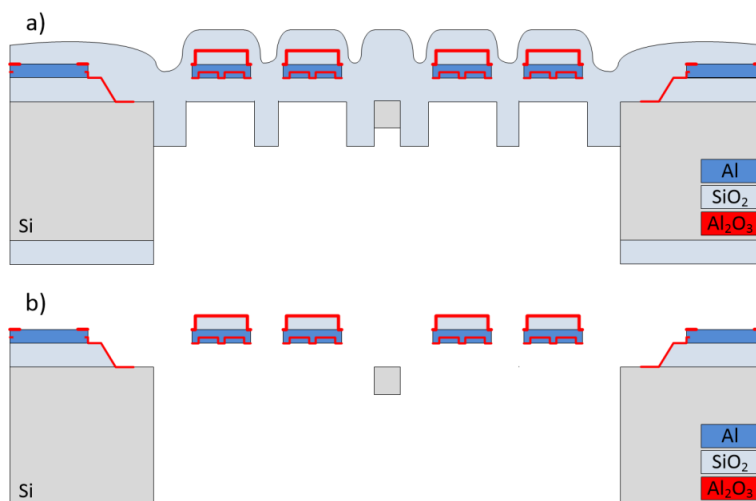


Figure 4.9: Final MEMS actuator steps: (a) Second DRIE backside etching. (b) Final device release.

and thus preventing possible stiction of the bimorph to the microplate (Fig. 4.9b). The detailed flowchart for the MEMS actuator fabrication is presented in Appendix D.

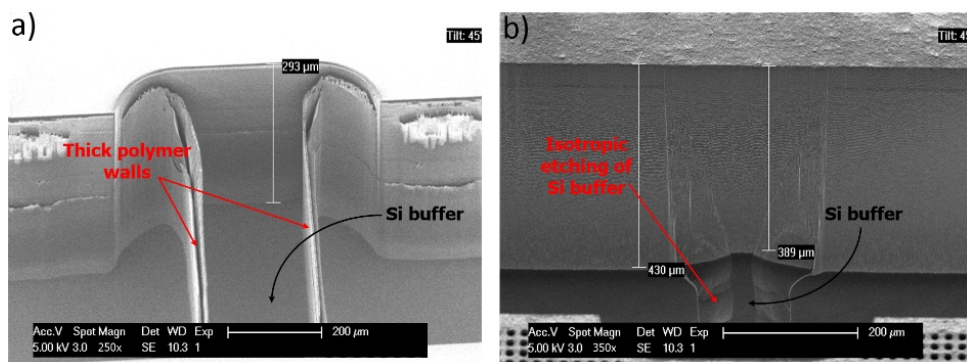


Figure 4.10: Examples of non-optimized backside second DRIE step: (a) Polymer wall formation due to excessive passivation. (b) Poor protection of Si buffer due to insufficient sidewall passivation.

Images of the fabricated wafer before dicing and final device release are shown in Fig. 4.11. The layout has 12 dies (Fig. 4.11a) where each die has 2 actuator systems for x direction scanning, 2 actuator systems for y direction scanning and one 2D MEMS actuator system (Fig. 4.11b). Figures 4.11c and 4.11d are SEM images of the MEMS actuator system for x and y direction, respectively, prior to the final release of the device.

Optical images of final devices, after release, are presented in Fig. 4.12. Due to the initial deflection, these images are not in focus over the entire device area. The protective layers for the bimorph and the sacrificial silicon oxide are pinhole free and withstand the release step as expected. However, residues of the Si buffer are visible around the

mechanical hinges as can be seen in Fig. 4.12c and Fig. 4.12d, where SEM images of a torsional hinge for x direction scanning, and y direction system with deflecting hinge are shown. The Si buffer residue is a consequence of rounding off the bottom cavity surface during DRIE etching, creating a non-uniformly thick mechanical hinge. This non-uniformity and different effective length will affect the mechanical properties of the MEMS actuator systems. However, a good optimization of the DRIE etching process can reduce the Si buffer block non-uniformity, while the front side hinge definition and first back side etching depth optimization can reduce the buffer residues around the hinge.

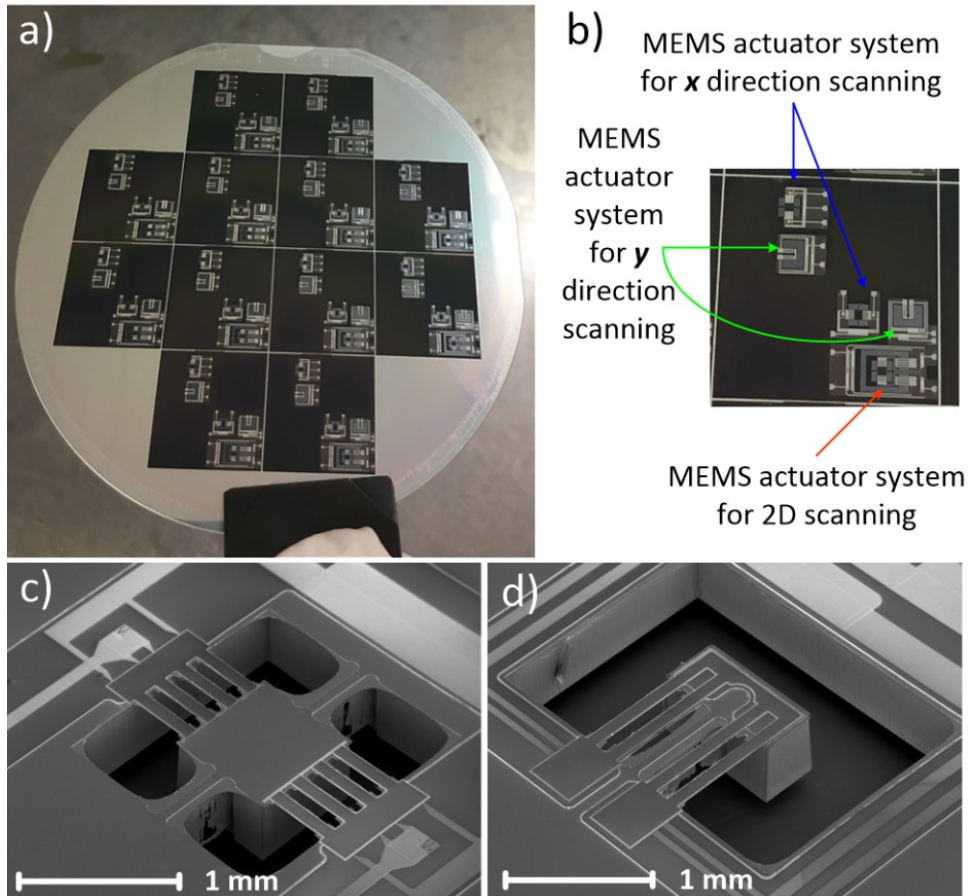


Figure 4.11: The fabricated actuator systems before final device release: Optical images of (a) a processed wafer before dicing and (b) close-up of a single die. SEM images of (c) x direction and (d) y direction scanning MEMS actuator systems.

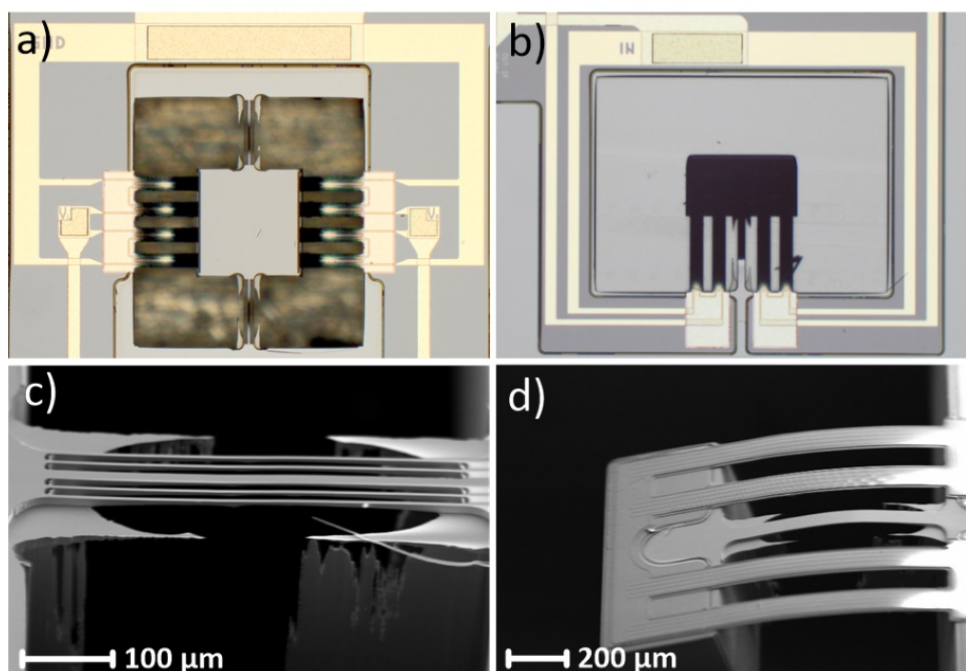


Figure 4.12: The released actuators: Optical images of MEMS actuator system for (a) x direction scanner and (b) y direction scanner. SEM images of (c) torsional and (d) deflective hinge.

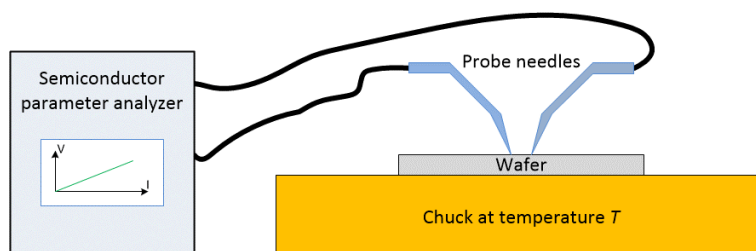


Figure 4.13: Measurement setup for TCR characterization.

4.2. MEMS ACTUATORS CHARACTERIZATION

4.2.1. ELECTRO-THERMAL CHARACTERIZATION

The numerical simulations indicated that the MEMS actuators systems for x and for y direction scanning should reach 260 °C and 420 °C respectively, to achieve the maximum intended scanning range. To evaluate the bimorph temperature during static operation, first the thermal coefficient of resistance (TCR) of the bimorph heater is characterized for each actuator system in the 25 °C to 200 °C temperature range.

A dedicated test wafer is used for the thermal characterization of the heater. This wafer is processed together with the device wafers until the contact opening step (Fig.

4.11) A probe station with a thermal chuck with a maximum heating temperature of 200 °C, is used (Fig. 4.13). For each resistance measurement at a given temperature, the sample was kept for 30 minutes on the hotplate to ensure thermal equilibrium. Then current was swept from 0 to 0.1 mA to minimize self-heating of the resistor. The measurement results for both x and y scanner designs are presented in Fig. 4.14. As expected, both characteristics show a linear behavior. The temperature coefficient of resistivity is calculated to be $4.45 \pm 0.05 \times 10^{-3} \text{ }^{\circ}\text{C}^{-1}$.

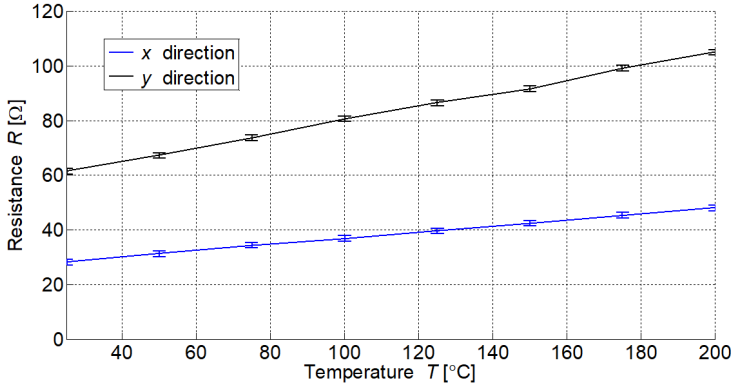


Figure 4.14: Heater resistance versus temperature for both x and y actuator systems.

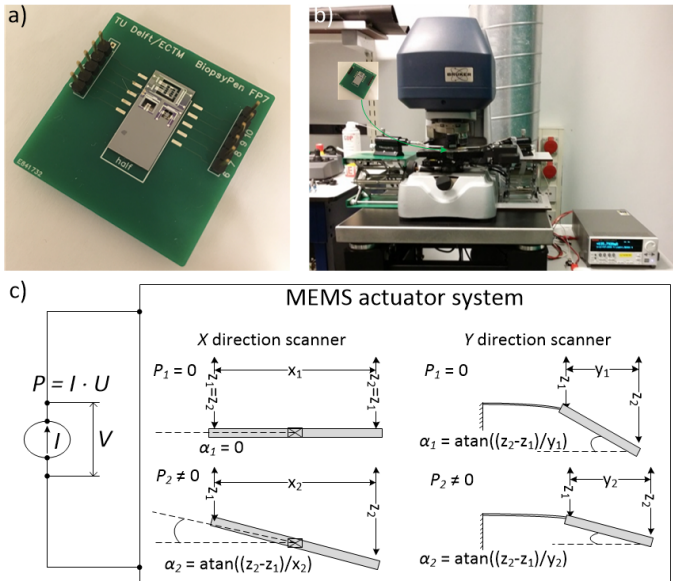


Figure 4.15: Electro-Mechanical characterization: (a) the fabricated chip wire-bonded to a PCB; (b) WLI measurement set up; (c) Angular displacement measurement principle.

4.2.2. ELECTRO-MECHANICAL CHARACTERIZATION

The static response and maximal angular displacement are characterized using white light interferometry. The fabricated chips are wire bonded to a printed circuit board (PCB) (Fig. 4.15a). The PCB is fixed to a movable stage of a *Brooker* white light interferometer. Electrical input to the actuator system was provided using a 4-channel *Keithley* power supply which gives voltage, current, resistance and power readout. The setup is shown in Fig. 4.15b. The angular displacement measurement principle is illustrated in Fig. 4.15c. For an input power P , using the white light surface profile of the chip, the vertical and horizontal distance between two points of the microplate were measured. Based on these measurements, the angular displacement is calculated.

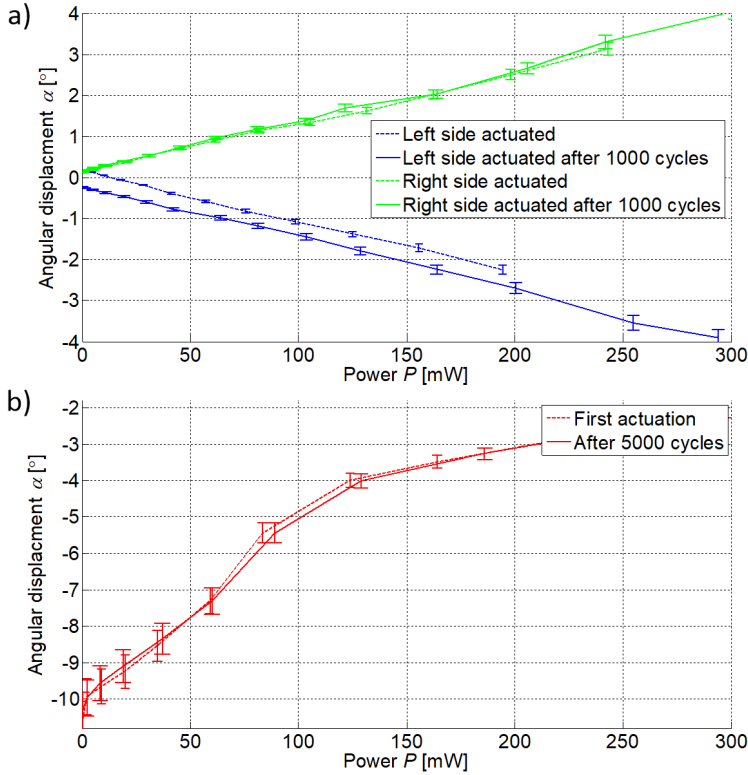


Figure 4.16: Angular displacement static response for (a) x and (b) y direction scanning MEMS actuator systems.

Measurement results for both x and y direction actuator systems are presented in Fig. 4.16. For the x direction scanner, a tilting range of 8° is achieved, with an average power consumption of 150 mW. A 0.1 s long power sweep from 0 to 300 mW as repeated for 1000 times and no detectable change in performance was observed. For the y direction scanner, the same range is achieved with an average power consumption of 200 mW. In this case, the system was cycled for more than 5000 times with the same input signal and

no significant changes were observed over time.

Based on simulations, the plate rotation of the actuator system for y scanning should be at the junction of the hinge and the plate. The initial angular displacement differs from the expected value due to the hinge thickness non-uniformity. Effectively, the hinge length is lower than designed and the hinge is thicker at its ends and thinner in the middle. However, a good optimization of the etching process can reduce hinge non-uniformity and accurately reproduce the designed parameters into the fabricated device.

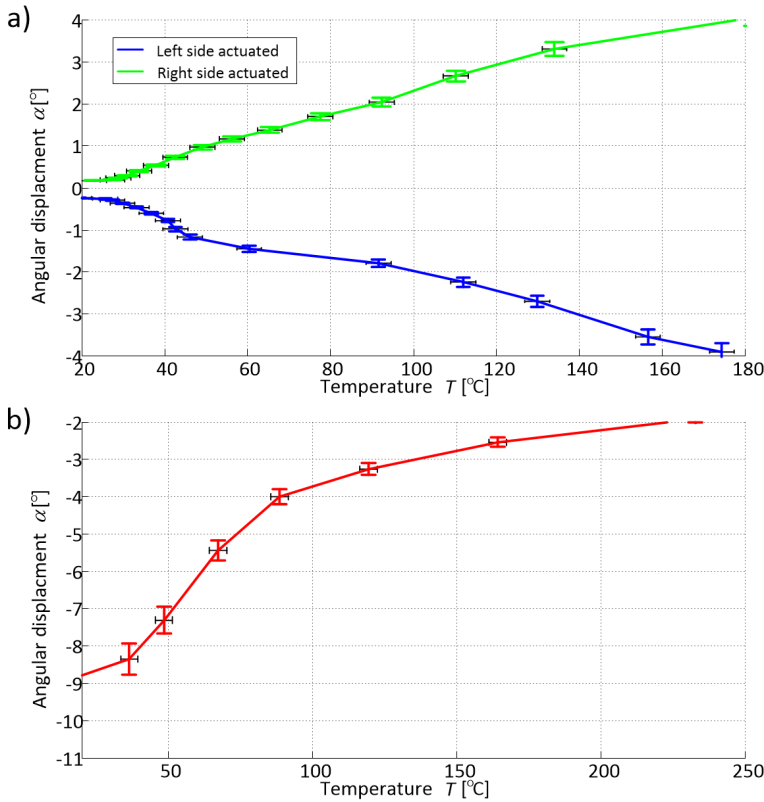


Figure 4.17: Angular displacement static response for (a) x and (b) y direction scanning MEMS actuator systems.

Knowing the initial resistance of the actuators heater, the resistance value during the actuator static operation and the thermal coefficient of resistivity, it is possible to correlate the power consumption of the MEMS actuator system with the operating temperature. The angular displacement versus calculated operating temperature for both systems is given in Fig. 4.17. This plot shows that the actuators did not reach the expected operating temperature. For the x direction scanner, the achieved temperature is 80 °C while for the y direction system it is 170 °C i.e. respectively 30% and 40% lower than calculated.

The heater resistivity is $0.036 \Omega/\mu\text{m}$. For the x direction scanning system, the heater resistance for one actuator is 18Ω . A power of 300 mW is generated using an input current of 70 mA. Following the electrical schematic circuit given in Fig. 2.30, and including resistance change due to self-heating, the total generated power on each set of actuators is only 162 mW. The rest is lost as joule heating of interconnections, bonding wires etc. Supplying more than 70 mA of electrical current damaged the actuator heater. The impossibility to achieve higher temperature during the first actuation, i.e. giving higher power, results in lower initial residual stress in the beams, thus giving lower initial deflection. As a result, the actuators force F_0 is lower than expected, resulting in a lower angular displacement than predicted. Increasing the force F_0 will require a higher initial temperature, thus a 280W power must be generated (see numerical results presented in Chapter 2, section 2.2.2.) for each actuator set. To overcome this problem, different materials (Ti, TiN, Mo, poly-Si etc.) and design optimization for the heater implementation must be considered.

4.2.3. FREQUENCY RESPONSE

Dynamic characteristics for both actuator systems are measured in the range 50 Hz - 4 kHz using a *Polytec* Laser Doppler Vibrometer (LDV). Frequencies lower than 50 Hz were not measured to exclude electrical noise from the power supply. Results are presented in Fig. 4.18 The first resonant mode for the actuator systems is at 668 Hz and 297 Hz, respectively, with corresponding Q factors of 126.1 and 151.5. The higher eigenfrequency for the x direction system indicates a higher torsional stiffness. This can also explain the lower angular displacement the device has compared to the simulated value. On the other side, the deflected hinge-based system has a lower frequency than calculated. The reason can be that the hinge is thinner in the middle (Fig. 4.12d), thus having a lower effective coefficient of elasticity. Nevertheless, the desired scanning speed for both devices is 10 Hz and therefore both scanners satisfy the dynamic requirement as indicated in Chapter 1, namely being a 10-fold higher than the first mode resonant frequency.

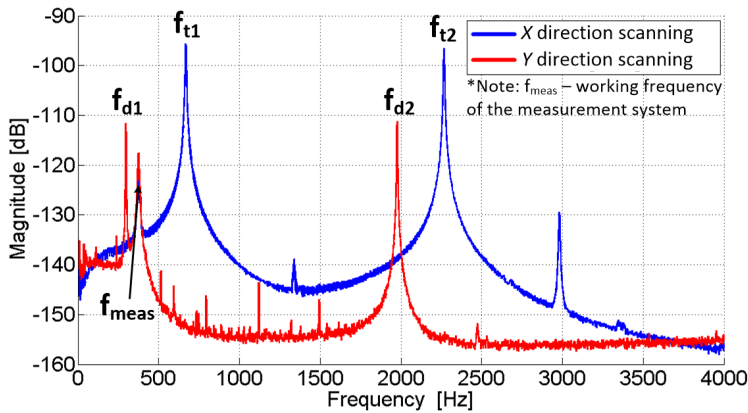


Figure 4.18: Frequency response for the fabricated MEMS actuator systems.

4.3. CONCLUSION

THIS chapter gives an overview of the fabrication process and characterization of the MEMS actuators. Particular attention is paid to critical steps to identify potential issues and explore alternatives.

The MEMS bimorph actuator systems displacement has a 33% lower range than the estimated values presented in Chapter 2. The main reason for the lower than expected motion range is the insufficient generated Joule heating. The maximum generated temperature was lower than expected. This resulted in lower residual stress and therefore lower generated force F_0 . Also, the final hinge geometry differs from the nominal value due to the non-optimized DRIE etching process used.

Static measurements of the fabricated devices showed it is possible to achieve 8° of angular motion range, a value representing 67% of the defined specifications given in Table 1.1. Although the measurements showed a maximum power consumption of 300 mW, TCR analysis indicated that only 162 mW are delivered to the actuators, while the rest is lost in electrical connections. Heater optimization, in terms of material used and layout, will allow reaching the required temperature during actuator operation.

The fabrication flow is developed to be fully compatible with the process for the optical components presented in Chapter 3 of this thesis. It does not require any high temperature processing steps (the total thermal budget is kept under 400 °C), which could affect the quality of the optical layers (antireflective and cladding layer), and consequently their properties. In the next chapter, the MEMS actuator systems will be integrated with the Si microlens and photonic circuitry to realize a fully integrated OCT scanning system.

5

THE INTEGRATED MOEMS OCT SYSTEM

The two most powerful warriors are patience and time.

Leo Tolstoy

This chapter describes the integration of all OCT components into a single device. The integrated OCT system consisting of the Si photonic interferometer, mirror, lens and actuators, is first characterized electromechanically and then optically. Finally, the optical setup is prepared, and the capability of the system to scan a surface is demonstrated.

Parts of this chapter have been published in "An Integrated Photonic Platform for A Single-Chip MEMS-Based Optical Coherent Tomography Scanner", *Micromachines*, Under Review, and "A Monolithically Integrated MOEMS Scanner for A Single-Chip OCT imaging Solution", To be submitted to *Journal of Microelectromechanical Systems*.

5.1. DEVICE FABRICATION

IN the previous two chapters we have already successfully demonstrated the integration of optical components into one Si block and the fabrication of MEMS actuators which are specially designed considering their integration with the optical components. Both process flows are thus conceived to be mutually compatible. Even so, the MEMS actuators cannot be directly added on the top of the photonic platform, but their fabrication should be interwoven with it. The main points that must thus be addressed are:

- Which parts and which layers of the PIC must be protected during the actuators fabrication?
- Which processing steps could be combined to reduce the number of steps and optimize the fabrication flow?
- Does any layer need to be locally removed to allow for correct placement of another component?

5

5.1.1. FABRICATION OPTIMIZATION

The final step of the MEMS actuators fabrication is the release in HF. Since the actuators are built on top of the photonic circuit, the cladding layer and the antireflective coating must be **protected from the vapor HF**. A pinhole free, atomic layer deposited, Al_2O_3 film is used for this purpose. Based on data available from the HF dry etch system (*SPTS Pri-maxx uEtch*) manufacturer, a thickness of 20 nm is chosen as the minimum thickness required to effectively protect the SiO_x cladding layer and the SiN antireflective coating. Also, a **scratch protection** layer on all optical components must be applied to prevent mechanical damage during the MEMS actuators fabrication. For this, a 4 μm -thick PECVD SiO_x layer is used.

The final step of the photonic circuit fabrication is the end facet definition (Fig. 3.23) which is a 100 μm deep Si trench. This creates a big wafer topography which complicates subsequent lithography process steps needed for the actuators fabrication. So, the positioning of this step in the overall process flow should be reconsidered.

In addition, as shown in the previous chapter, the 15 μm deep front side etching used for hinge layout definition (Fig. 4.8) resulted in Si buffer residues around the hinge (Fig. 4.12). To eliminate this problem, a deeper front side hinge etch must be performed. Therefore, **the end facet definition and the front side hinge etching could be combined** into a single step to optimize the process flow and make additional lithography on a high topography surface unnecessary.

Another way to contribute to process optimization is the use of a single layer for multiple purposes. For example, as the photonic components must be protected during the actuators fabrication, the SiO_x sacrificial layer can be used also to protect the front side of the wafer. Similarly, the SiO_x hard mask layer deposited on the backside for the DRIE etching can be used at the same time to protect the lens from any mechanical damage.

The actuator system must now be implemented in the SOI substrate used for the PIC. Thus, the area where the actuators will be built (Fig. 5.1) must be cleared from any material down to the bulk Si. In Fig. 5.1a the layout of the system is shown together with

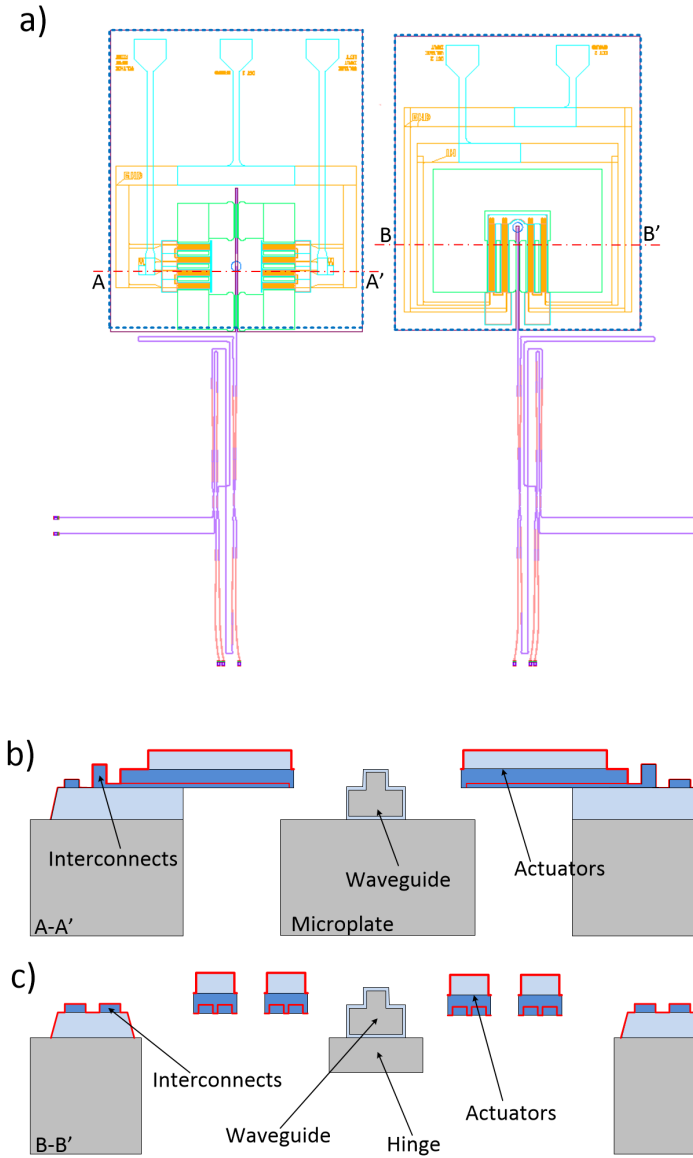


Figure 5.1: Preparation of a wafer with PIC for MEMS integration – device layer removal: (a) The frame (dashed line) indicates the area where all layers must be removed down to bulk Si. (b) Cross section A-A' of MEMS actuator system for x direction scanning. (c) Cross section B-B' of MEMS actuator system for y direction scanning.

the cross sections (A-A', B-B') for both actuator systems, revealing that only the waveguide uses the device layer and the buried oxide of the SOI wafer. The Si top layer could be removed during the waveguide definition or during mirror etching. In any case, all photolithography steps during the MEMS actuator fabrication would face at least a $3\text{ }\mu\text{m}$

high topography. Unlike the two-step waveguide etching, the 45° mirror facet etching does not leave sharp edges, thus ensuring better photoresist coverage. Hence it is better to remove the silicon device layer on the area for the actuators fabrication during the mirror definition.

The wafer cross section after the fabrication of optical components is presented in Fig. 5.2a. To reach the bulk Si for the actuators fabrication, the buried oxide must be removed as well, as illustrated in Fig. 5.2b. In addition, both cladding and antireflective coating must be preserved during the final device release in vapor HF. Thus, they should be protected with an atomic layer deposited Al_2O_3 coating.

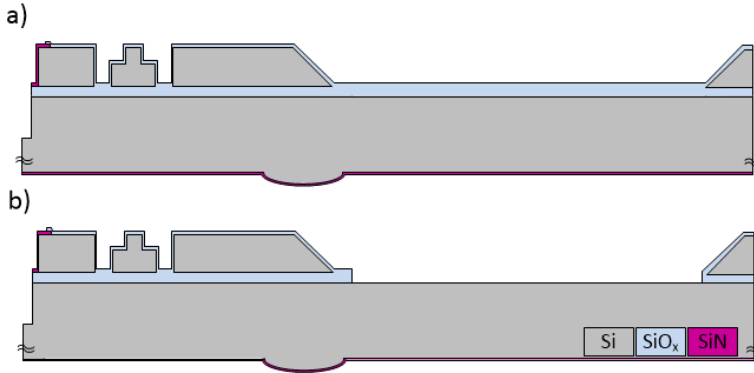


Figure 5.2: Optical components and functional layers (not to scale): (a) Device cross section after finalization of optical components integration. (b) Device cross section after buried oxide removal for integration of MEMS actuators.

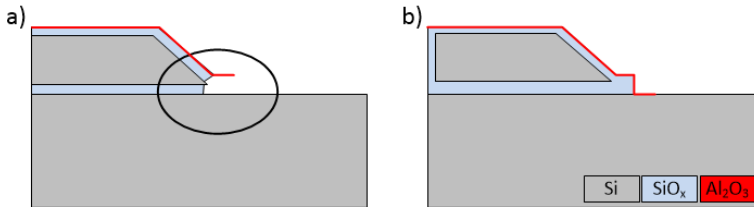


Figure 5.3: Buried oxide removal for MEMS actuators integration on a wafer with PIC: (b) Direct etching – bad protection from vapor HF (c) Two-step approach – good protection from vapor HF.

The straightforward approach is to deposit the protective layer first (Fig. 5.3a). Then all layers must be directly etched down to the bare Si. In this case, there will be unprotected SiO_x as indicated in Fig. 3a. This will result in cladding and buried oxide layer removal during the release step, since the sidewalls of the buried oxide are exposed. However, if the protective ALD Al_2O_3 is added after etching the buried oxide layer, the sidewalls will be protected as well (Fig. 5.3b). Thus, this more cautious approach is preferred for the MEMS actuators integration. The drawback is that it requires an additional patterning of the protective layer.

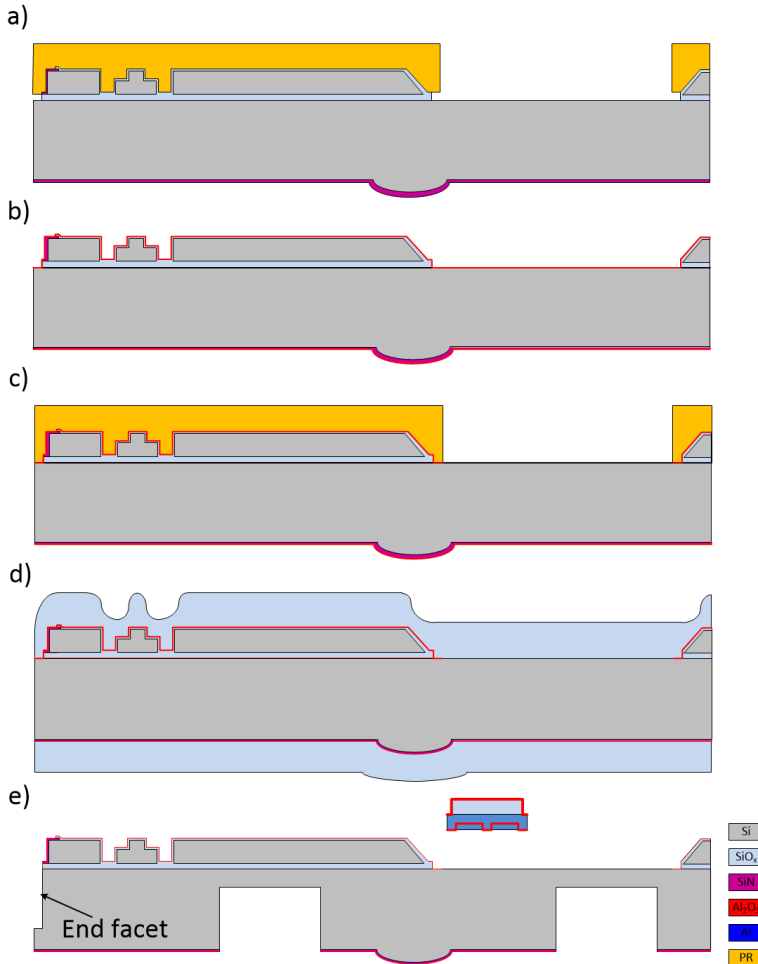


Figure 5.4: Main (additional) steps for the integration of MEMS actuators with optical components: (a) Removal of buried SiO₂ layer in pre-defined areas outside the PIC. End facet trench not yet defined in the process. (b) ALD Al₂O₃ deposition (c) Patterning of protective Al₂O₃ to open the same pre-defined area. (d) Sacrificial and hard mask layer deposition for MEMS actuators fabrication and as protective layers for optical components. (e) MEMS actuator system fabrication with end facet definition included.

Further optimization of the fabrication process can be achieved using the same mask layer for both SiO₂ and Al₂O₃ patterning. To ensure sufficient overlay of Al₂O₃ over the SiO₂ sidewall, the buried oxide is isotopically etched using a HF based solution with sufficient over etch time (Fig. 5.4a) to create at least 200 nm of undercut. The minimum undercut length is defined based on the maximum overlay error guaranteed by the exposure tool used. Then, the wafers are coated with a 20 nm-thick ALD Al₂O₃ (Fig. 5.4b) and the same mask is used to anisotropically remove this layer in CHF₃ – CF₄ based plasma (Fig. 5.4c).

The wafer preparation for the MEMS actuators fabrication is finalized by adding a 4 μm and 7 μm -thick protective PECVD SiO_x layers on the front and the backside, respectively (Fig. 5.4d). The top layer serves as a sacrificial layer for the MEMS actuators release, while the bottom one is used as a backside hard mask for DRIE etching and as protection layer for the lens. Then, the MEMS actuators fabrication process flow as outlined in Chapter 4 is followed (Fig. 5.4e), with the difference that now a single 100 μm -deep front side etch step is used for both facet and front side hinge definition. Full fabrication process is described in Appendix E.

5.1.2. HINGE DEFINITION IMPROVEMENTS

Special attention was given to the optimization of the backside DRIE Bosch process to achieve uniform mechanical hinges. Two points had to be addressed during this process optimization:

1. Uniformity of the bottom surface after the first backside DRIE step
2. Accurate control of the passivation layer thickness during the etching

The surface bottom uniformity is needed to have a uniform hinge thickness. Sufficient thickness of the passivation layer must be maintained during the Bosch process to ensure preservation of the Si buffer blocks but at the same time excessive passivation must be removed so that an unwanted polymer wall is not formed (Fig. 4.10a). Thus, the passivation layer deposition must be accurately controlled.

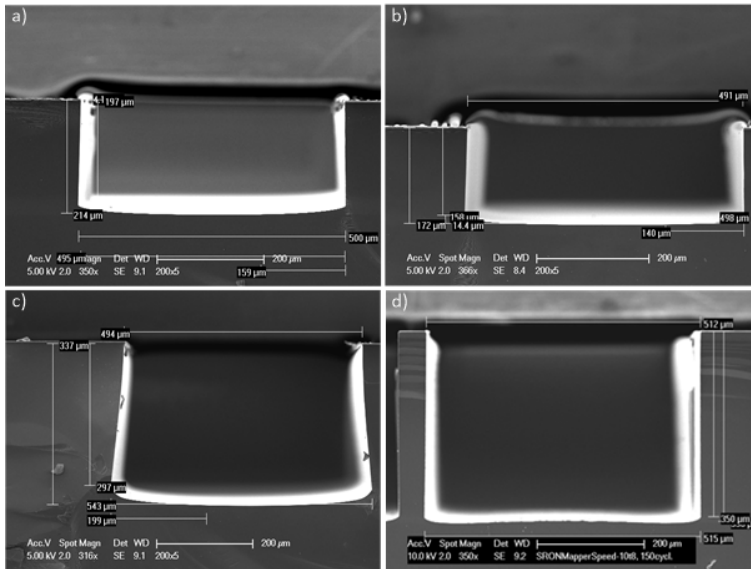


Figure 5.5: The silicon cavity profile after a 200 cycle DRIE Bosch process varying passivation thickness (CF deposition time) and process pressure: (a) 2 s and 35 mTorr (b) 2s and 15 mTorr (c) 2 s and 60 mTorr (d) 3 s and 60 mTorr. The etch time is set to 5 s.

The Bosch process consists of two steps, CF passivation layer deposition and etching of Si using SF_6 plasma. Due to the increased bias power, the ions flux is directed downwards, and the CF layer is sputtered from the bottom, but it is still preserved on the sidewalls of the substrate. After the removal of CF layer, isotropic etching of Si starts. Due to the nature of isotropic etching, the surface bottom will be rounded, causing the hinge non-uniformity observed in Fig. 4.12. In Fig. 5 the influence of pressure in the etching step is presented.

In Fig. 5.5a the result of a 200 cycle Bosch process at 35 mTorr is shown. In general, pressure reduction influences ions flux making the angular distribution closer to 0° . This improves etching anisotropy but reduces the etch rate. The result of a same cycle but at

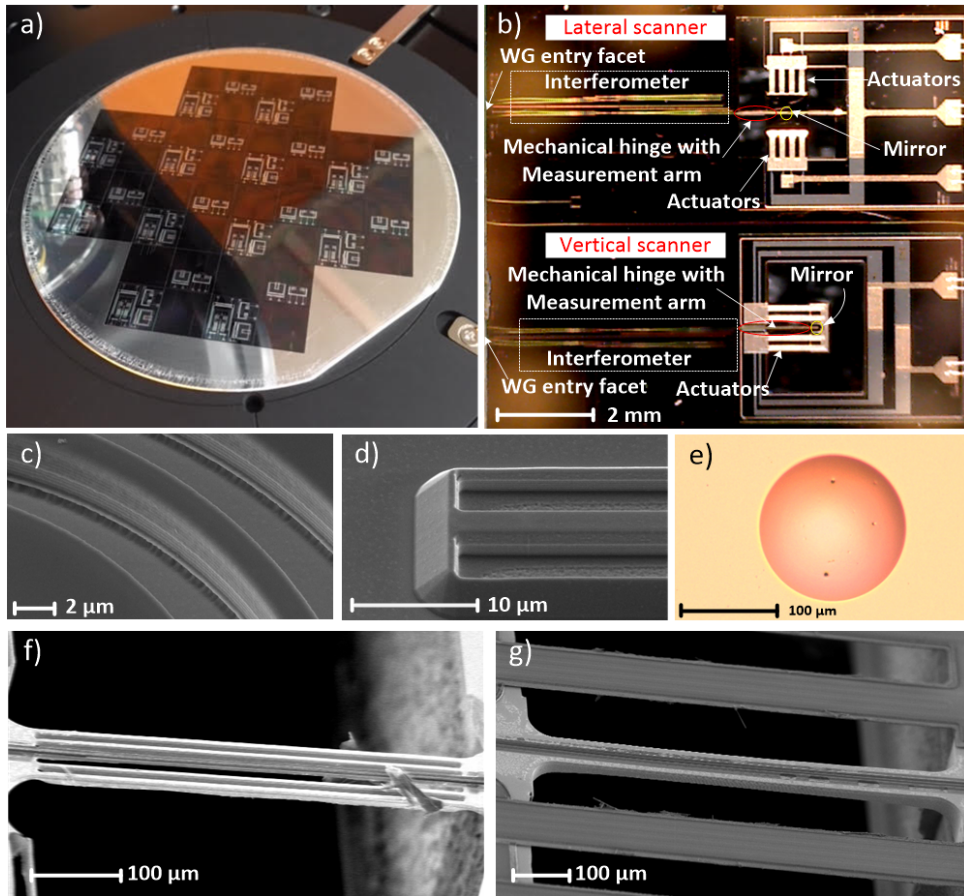


Figure 5.6: The fully integrated OCT system: (a) Optical image of a full wafer after completion of the integrated MEMS actuators system and photonic components fabrication. (b) Optical image of a single OCT chip with all optical components and MEMS actuators system. SEM images of (c) the interferometer S-bend waveguide and (d) the interferometer measurement arm finished with the 45° mirror facet. (e) Optical image of the Si microlens coated with SiN and Al_2O_3 antireflective and protective layers. SEM images of (f) torsional and (g) deflecting hinge with the interferometer measurement arm waveguide.

15 mTorr is given in Fig. 5.5b. A slight improvement of the surface rounding can be noticed, but it is not sufficient to provide a flat, uniform bottom.

Increasing the etching pressure makes ion distribution less directional and thus the etching more isotropic. The effect of further increasing pressure (60 mTorr) is shown in Fig. 5.5c. The taper angle is more than 4.5° and the height difference on the bottom is $40\text{ }\mu\text{m}$. This process cannot be considered as a good DRIE Bosch process. To improve the taper angle, the CF passivation layer during one cycle must be increased. The thicker CF layer improved the sidewall angle and consequently the bottom profile (Fig. 5.5d).

5.1.3. FABRICATION RESULTS

Images of the fabricated fully integrated system are presented in Fig. 5.6. A wafer with integrated optical components and MEMS actuators is shown in Fig. 5.6a, indicating that up to 60 devices can be extracted from a 4" wafer. In Fig. 5.6b an optical image of a single OCT chip with one x and one y direction integrated MEMS scanner can be seen. A SEM image of the OCT interferometer S-bend is given in Fig. 5.6c. The measurement arm of the interferometer runs along the mechanical hinges of the MEMS actuator systems (Fig. 5.6b) and finishes with a 45° mirror facet (Fig. 5.6d). An optical image of the Si collimating lens with antireflective coating, placed at the backside of the chip, is visible in Fig. 5.6e. A SEM image of two torsional hinges with the measurement arm waveguide is presented in Fig. 5.6f while a deflecting hinge is shown in Fig. 5.6g. These hinges have uniform thickness over their length and no silicon residues nor polymer walls can be observed around the hinges.

5.2. ACTUATORS CHARACTERIZATION

IN this section we present the characterization of both x and y direction integrated scanners. These devices are chosen as the most suitable devices based on an optical inspection of numerous dies. So, the presented x and y integrated scanners are not fabricated at the same time. These same devices are the optically characterized as described in the next section.

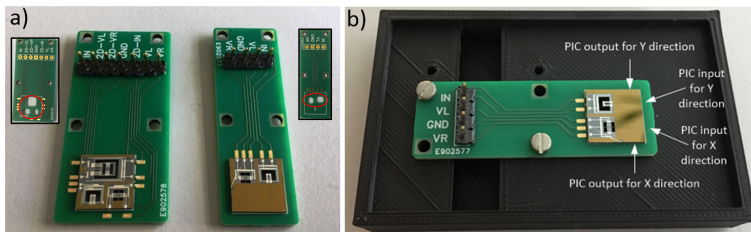


Figure 5.7: Packaged integrated OCT and MOEMS scanner devices: (a) Devices mounted on a custom-made PCB. Red circles on PCBs indicate the opening for the light signal coming from the lens. (b) Packaged device mounted on a special transport carrier for electromechanical characterization.

The integrated micro-opto-electromechanical scanners and integrated OCT systems are packaged using specially designed printed circuit boards (PCB) to perform both electromechanical and optomechanical characterization. Packaged devices are shown in

Fig. 5.7a. Each PCB has opening holes (Fig. 5.7a) for optical signal output and to provide free space for the microplate motion. The packaged device is then mounted on a specially designed carrier to ensure mechanical stability during device characterization (Fig. 5.7b).

5.2.1. ELECTRO-THERMAL CHARACTERIZATION

The fabricated devices are first electromechanically characterized using the same techniques and setups as described in Chapter 4. The first step is the TCR characterization of the heaters to correlate the beam temperature with the mechanical motion. The measurement results are reported in Fig. 5.8. As expected, the same linear behavior is observed as in Chapter 4, and the coefficient of temperature dependence is calculated to be $4.5 \pm 0.05 \times 10^{-3} \text{ }^{\circ}\text{C}^{-1}$.

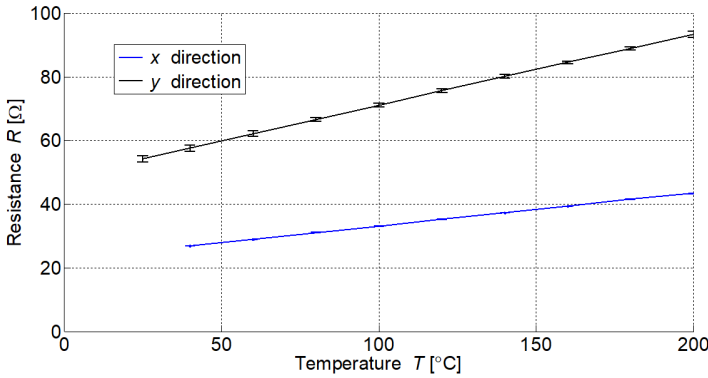


Figure 5.8: Temperature coefficient of resistance measurement: Resistance versus heater temperature for x direction (blue line) and y direction (black line) scanner.

5.2.2. ELECTRO-MECHANICAL CHARACTERIZATION

The angular displacement is characterized using the white light interferometry setup described in Chapter 4, Fig. 4.15. The static response of the x and y direction scanners is presented in Fig. 5.9. The angular displacement versus input electrical power, supplied using constant electrical current, is shown in Fig. 5.9a-b. In Fig. 5.9c-d the angular displacement versus input current is given. These results will be later used for the optical characterization to link the surface scanning range to the angular displacement.

A comparison of the measurement results for the integrated system given in Fig. 5.9 with the achieved angular displacement for the actuator system reported in Fig. 4.16, indicates a lower power consumption for the integrated system. The biggest difference between the integrated system and the actuator system alone is in the wire bonding. The actuator system chips described in Chapter 4 are wire bonded using thermal paste and single Al wire. To reduce unwanted resistance, now the integrated system chips are bonded using double bond wires for each pad and gold-plated PCB bond pads. This results in a contact and wire resistance reduction of $17 \text{ } \Omega$ per set of actuators, which reduces the total power consumption by $\sim 30\%$ for both x and y direction scanning systems.

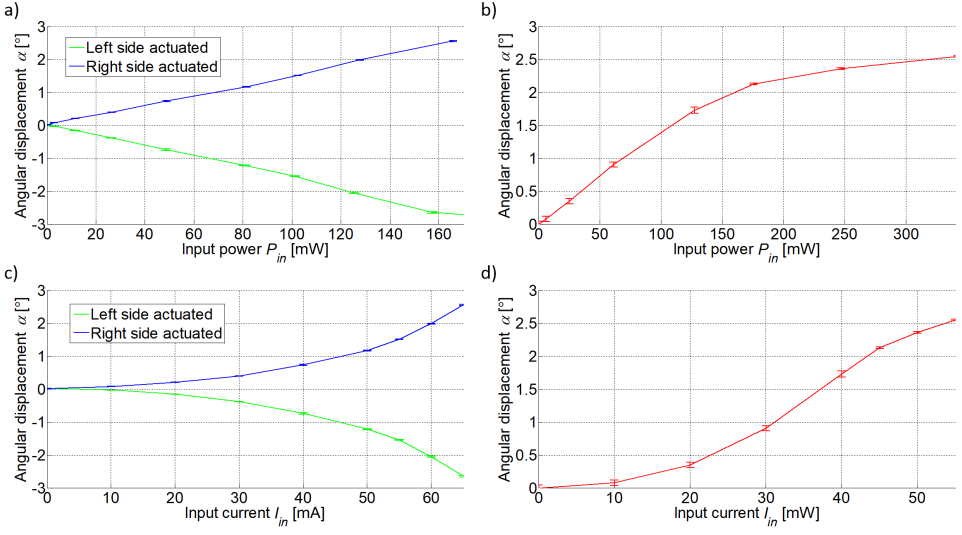


Figure 5.9: Electromechanical characterization: Angular displacement versus electrical input power for (a) x direction scanner and (b) y direction scanner. Angular displacement versus electrical input current for (c) x direction scanner and (d) y direction scanner.

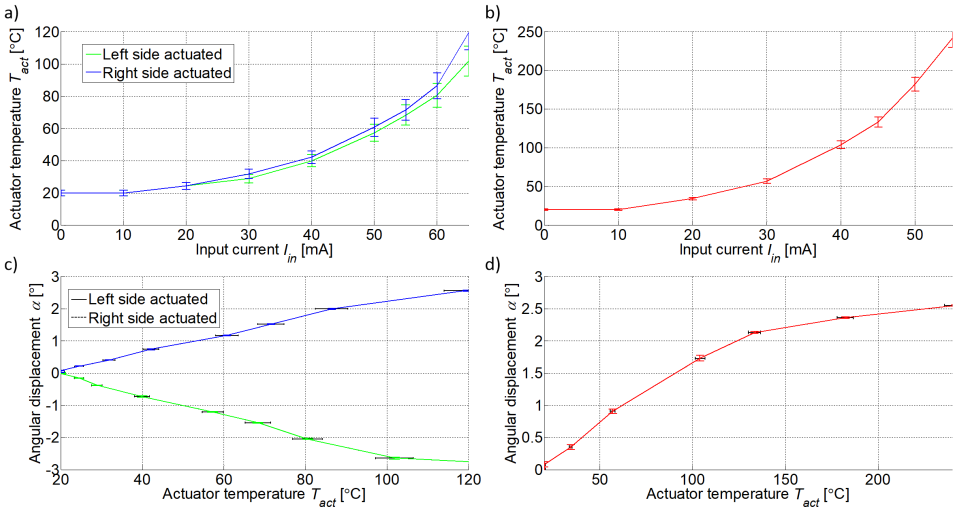


Figure 5.10: Thermo-mechanical characterization: Actuator temperature versus electrical input current for the (a) x direction scanner and (b) y direction scanner. Angular displacement versus actuator temperature for the (c) x direction scanner and (d) y direction scanner.

Results of the thermal characterization of the integrated OCT scanners are presented in Fig. 5.10. The actuator temperature is calculated based on the TCR characterization (Fig. 5.7) and heater resistance values during actuation. The actuator self-heated tem-

perature versus input current is presented in Fig. 5.10a-b. Then, the actuator temperature is linked to the angular displacement of the system and the results are given in Fig. 5.10c-d.

The results presented in Fig. 5.10 show a lower maximum generated temperature than for the actuator system alone given in Fig. 4.17. The estimated temperature for the integrated x and y direction scanner is $\sim 33\%$ and $\sim 36\%$ lower, respectively, than for the x and y actuator systems presented in Chapter 4. The self-heating effect of the interconnects was then not included and can be a reason for the higher estimated temperature. Since the interconnect resistance for the integrated system is much lower than for the actuator system alone, the estimated temperature for the integrated system provides a more accurate overall thermal performance of the actuator.

Finally, the torsional and deflective hinge (5.6f-g) definition has been improved and they have now a better geometrical uniformity compared to the actuator systems presented in Chapter 4. The fabricated x direction scanner has torsional hinges with a thickness of $10.5 \pm 1 \mu\text{m}$ which matches the designed values. However, it can generate only 50% of the desired motion range. The presented y direction scanner has $21 \pm 1 \mu\text{m}$ thick deflective hinge. A simulation result for y direction scanning system with $21 \mu\text{m}$ -thick hinge shows that the motion range should be 63% of the target value (12°). But, the measured motion range is only 21% of the expected value. Thus, while the uniformity of the hinges is improved, the limit in reaching higher temperatures in the heater, which is largely responsible for the lower than designed motion range, is not overcome. A suggested solution for this problem is provided in Chapter 6, Section 6.2 with the rest of recommendations for further improvements and future work.

5.2.3. DYNAMIC CHARACTERIZATION

Dynamic characterization of the integrated devices is preformed using a *Polytec MSA 400* laser doppler vibrometer (LDV) following the same procedure as reported for the actuators system in Chapter 4. The total scanning range is from 50 Hz to 5 kHz, where the first 50 Hz is filtered out to remove electrical noise. In Fig. 5.11 the frequency response for both x and y integrated scanners is shown.

The first resonant mode for the x direction integrated scanner is at 551 Hz, which is only 3% higher than the simulated value. A good comparison between measured and simulated values is also an indication that the fabricated hinge geometry matches the designed values. Due to two times higher deflection hinge thickness of the y direction scanner, the first resonant frequency mode is expected to be higher than 463 Hz. The measured resonant frequency is 1503 Hz and matches simulation value for y direction system with $21 \mu\text{m}$ -thick hinge. The quality factors of the fabricated integrated scanners are 78 and 578, respectively. Both systems have high Q factors making them good resonators. The higher Q factor of the y direction scanner is expected, since the actuators in this system also serves as the mechanical support to the bulk Si microplate, while in the x direction scanning system one set of actuators always acts as dumping springs.

Both x and y integrated scanners are tested with a triangle input signal of 10 Hz using the available signal generator of the *Polytec MSA 400* laser doppler vibrometer. In Fig. 5.12 measurement results for both systems are shown (the dashed line illustrates the shape of the input signal). The input signal for the x direction scanner is applied

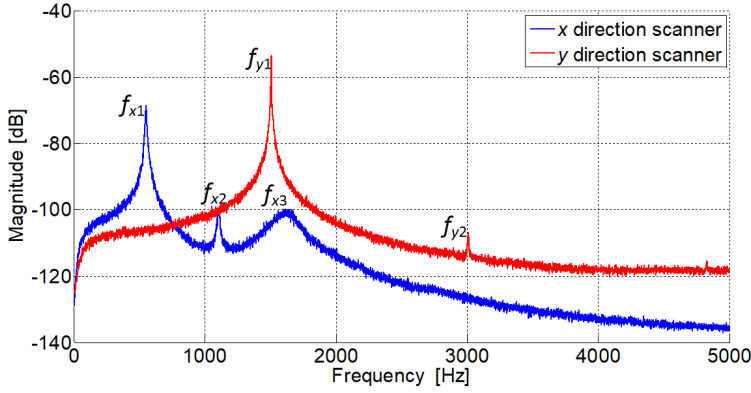


Figure 5.11: Dynamic characterization of integrated system: x direction scanner (blue line) y direction scanner (red line).

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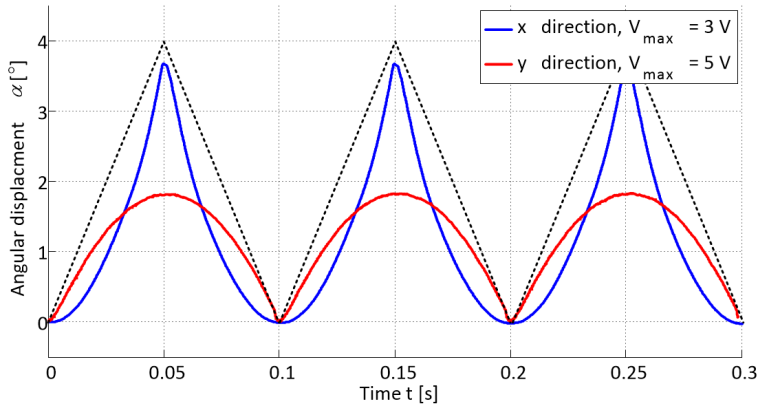


Figure 5.12: Angular displacement range for a 10 Hz triangular voltage signal. Blue line: One side of x direction scanner actuated with a 3 V amplitude and 1.5 V offset signal. Red line: Angular displacement for y direction scanner with a 5 V amplitude and 2.5 V offset signal.

only to one set of actuators. This means the presented angular displacement (blue line) is only half of the scanning range. For the y direction scanner (red line) full angular displacement for the input signal is measured. All presented measured values have an uncertainty of $\pm 5\%$.

The achieved voltage of ~ 2.5 V for the x direction scanning during static characterization for an input current of 65 mA corresponds to a rather low power consumption of ~ 160 mW. Therefore, to see if the integrated system can generate higher temperature, i.e. achieve higher displacement range, a higher amplitude signal (3 V; offset 1.5 V) was applied. The maximum achieved displacement range on each side is 3.65° , which should give a total range of 7.3° . The value of 2.5 V is considered for comparison with the static response (Fig. 5.9a and c). When the triangular input signal has this value, the angular displacement is 2.5° which is in line with the results presented in Fig. 5.9a and c.

The electrical measurements for the y direction scanner showed that when a power of the 350 mW is generated, the heaters can be damaged. Hence, the amplitude for the dynamic response on the triangular signal is set to 5 V with 2.5 V offset, which corresponds to 50 mA input current during static characterization of the integrated systems (Fig. 5.9b and d). The maximum achieved angular displacement is 1.81° which is $\sim 20\%$ lower than in the static regime. This means the fabricated y direction integrated system has a much longer response time than expected. Nevertheless, the system has enough time to cool down and to return to its initial state.

In Fig. 5.13 the angular displacement response for a triangular signal of the same amplitude but with frequency of 100 Hz is reported. The angular displacement range for the x direction scanner when one side is actuated is only 2.42° which is $\sim 33\%$ lower than what is achieved for the 10 Hz input signal. The y direction scanner is only 1.33° which is $\sim 26\%$ lower than in the case of 10 Hz input signal. Also, the presented plot shows that at 100 Hz input signal the devices do not have enough time to cool down to room temperature. Based on the estimated temperature in static regime (Fig. 5.10), the temperature of the x direction scanner during 100 Hz actuation will not go below 24°C while for the y direction scanner, the system temperature will not be below 43°C . This means that these devices are not able to follow changes of the input signal smaller than 0.1 s.

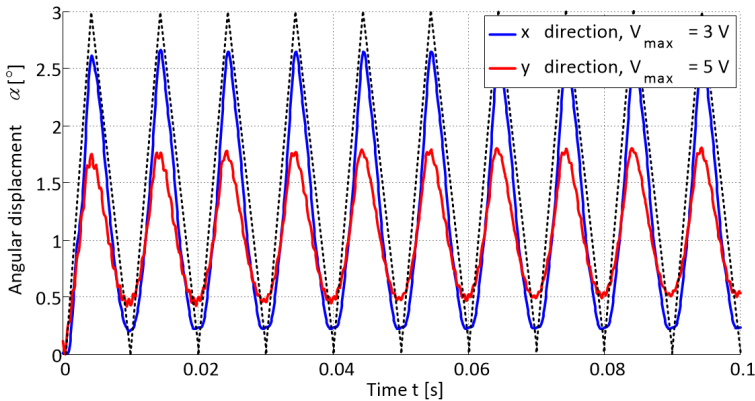


Figure 5.13: Angular displacement range for a 100 Hz triangular voltage signal. Blue line: One side of x direction scanner actuated with a 3 V amplitude and 1.5 V offset signal. Red line: Angular displacement for y direction scanner with a 5 V amplitude and 2.5 V offset signal.

Both integrated systems showed a slower response than expected. Using a 10 Hz triangular input signal, the integrated system for y direction can achieve only 80% of the possible angular displacement. Nevertheless, the system has enough time to cool down to room temperature and go back to its initial position. The x direction integrated system can achieve full range of angular displacement and is able to go back to its initial position. For an input signal of 100 Hz, both systems cannot cool down fast enough and they do not go back to the initial state. But, the x direction scanner is closer to the 0 position than the y direction system. The main reason for the faster response of the x direction scanner compared to the y direction scanner is the shorter actuator and heater.

Moreover, the y direction scanning system design presented in Chapter 2 shows that the bimorph beams are also anchored to the Si microplate with the lens which acts as a heat sink.

The frequency response for both devices satisfies the system requirements given in Chapter 1. The resonant frequency for the x direction scanning matches the simulated values since the targeted hinge thickness is achieved. But due to the large thickness of the deflecting hinge, the system for y direction scanning has a much higher resonant frequency. Both devices have a high Q factor making it possible to actuate them at resonant frequency with low actuation electrical power.

5.3. SURFACE SCANNING DEMONSTRATION

THE main purpose of the integrated optical scanners is to guide the light over the surface to be scanned. Hence, the optical scanning must be demonstrated. The system is designed to work with a broadband light source of $1.3\ \mu\text{m}$ wavelength. Thus, to characterize the system, the measurement setup needs a super luminescent diode (SLED) light source. Since $1.3\ \mu\text{m}$ wavelength is not visible to the human eye, the measurement system is equipped with a CCD camera to detect the light spot and be able to track it. The light needs to be coupled to the integrated OCT chip using a lensed coupling fiber.

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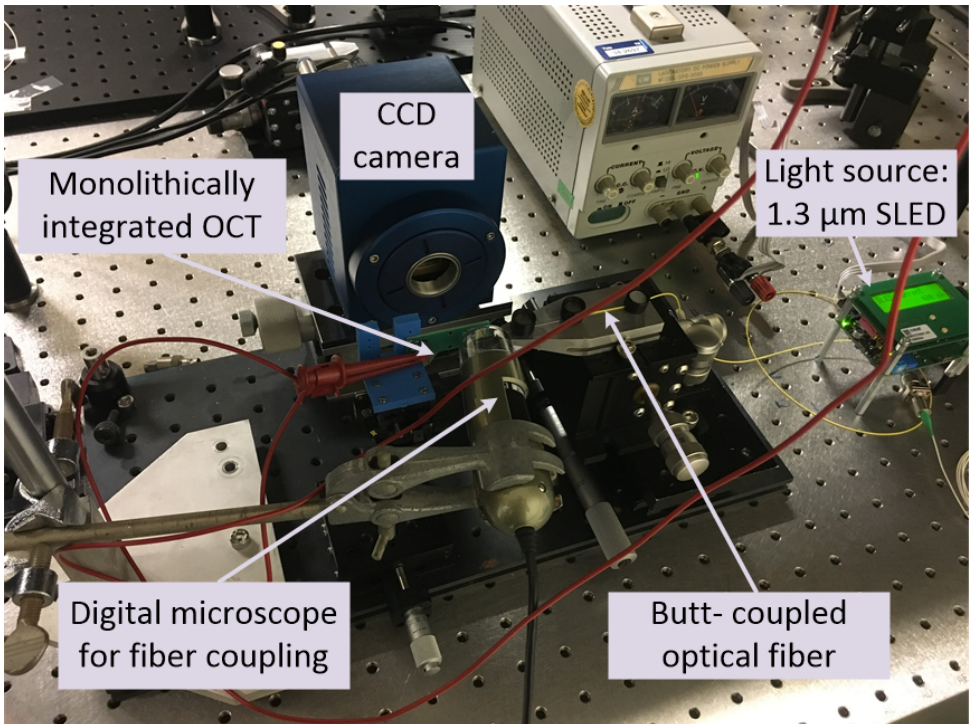


Figure 5.14: Angular displacement range for a 100 Hz triangular voltage signal. Blue line: One side of x direction scanner actuated with a 3 V amplitude and 1.5 V offset signal. Red line: Angular displacement for y direction scanner with a 5 V amplitude and 2.5 V offset signal.

The measurement setup is depicted in Fig. 5.14. It consists of an Exalos SLED source of $1.3\mu\text{m}$ wavelength and 80 nm bandwidth, followed by a coupling optical fiber mounted on a fiber aligner. Using the fiber aligner, the light is butt-coupled into the integrated OCT chip. The wire bonded chip (Fig. 5.8) is mounted on a specially designed holder which places the chip at 90° relative to the light propagation direction. This way, the light from the collimated lens is directed towards a 640×512 -pixel resolution CCD camera with $20\mu\text{m}$ pitch size. Finally, the measurement setup uses a power source to actuate the integrated system.

5.3.1. SURFACE SCANNING WITH THE INTEGRATED SYSTEM

In this subsection, results of the surface scanning range, not light spot characteristics, are reported. Using the setup described in the previous section, both systems are actuated with constant current. A CCD image was taken for a single input current value. So, the measured displacement corresponds to the system static response. CCD images of the output light spot from the integrated systems are presented in Figs 5.15 and 5.16.

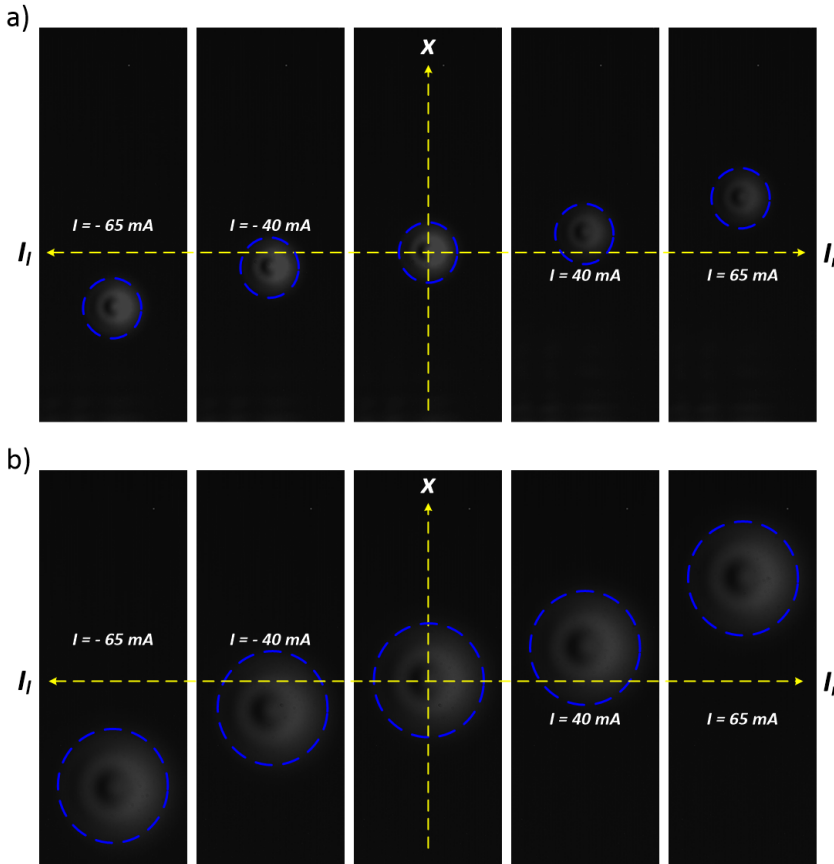


Figure 5.15: Surface scanning in x direction at working distance of about (a) 3 cm and (b) 6 cm.

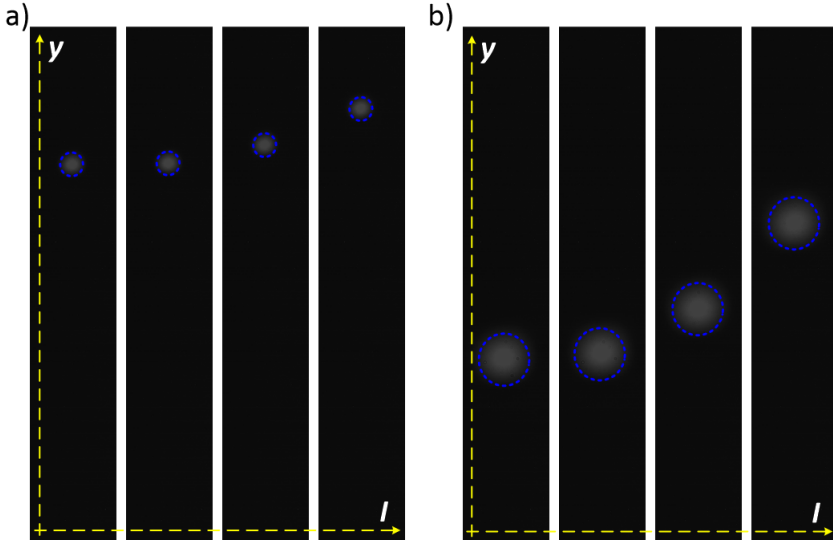


Figure 5.16: Surface scanning in y direction at working distance of about (a) 3 cm and (b) 8 cm.

The x direction integrated scanning system is actuated using constant current in the range from 0 to 65 mA. The first measurement was performed placing the CCD camera at a ~ 3 cm working distance (Fig. 5.15a) and the second one at a ~ 6 cm (Fig. 5.15b) working distance. With the captured CCD images shown, the center of the light spot is tracked and its position versus input current is reported in Fig. 5.17. Based on the angular displacement (Fig. 5.9) and light spot position, the working distance is calculated to be $z = 31 \pm 3$ mm for the first measurement and $z = 61 \pm 6$ mm for the second measurement. As expected, a longer working distance provides a larger surface scanning. Namely, the total scanning range increased from 2.74 ± 0.01 mm to 5.38 ± 0.01 mm.

The y direction integrated scanning system is actuated using constant current in the range from 0 to 60 mA at a ~ 3 cm (Fig. 5.16a) and ~ 8 cm (Fig. 5.16b) working distance. Again, the position of the light spot center is measured versus input current and the results are presented in Fig. 5.18. Using the same considerations, the working distance between CCD camera and the device is calculated to be $z = 33 \pm 5$ mm in the first measurement and $z = 81 \pm 12$ mm in the second measurement. The total surface displacement range in the y direction at ~ 3 cm is 1.58 ± 0.01 mm, while at ~ 8 cm is 3.90 ± 0.01 mm was reached.

The mechanical characterization given in the previous section already shows the system cannot achieve the desired angular displacement. Therefore, only 5×2 mm² instead of targeted 10×10 mm² area cannot be scanned. To increase the scanning range, a right temperature should be provided to the actuators. Nevertheless, the surface scanning capabilities of the new developed integrated systems are demonstrated. These initial tests show that the scanning range can be increased by increasing the working distance. Based on the total intensity of CCD images, no additional optical signal attenuation is observed during both x and y integrated system actuation.

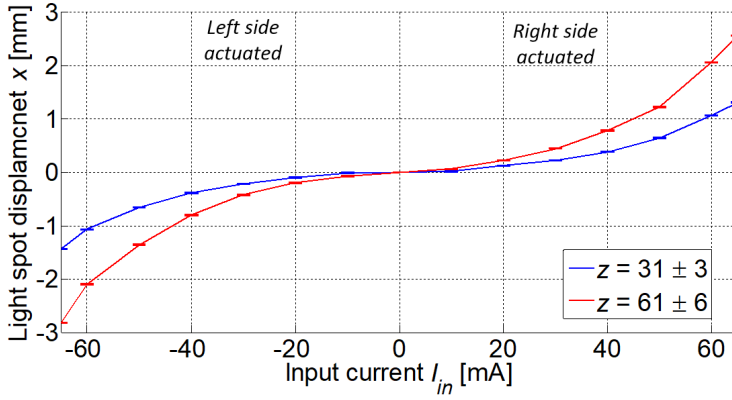


Figure 5.17: Light spot position of x direction scanner versus input current for the two working distances tested: 31 mm (red line) and 61 mm (blue line). The negative sign for the current indicates actuation of the left side while the positive current is related to the right-side actuation.

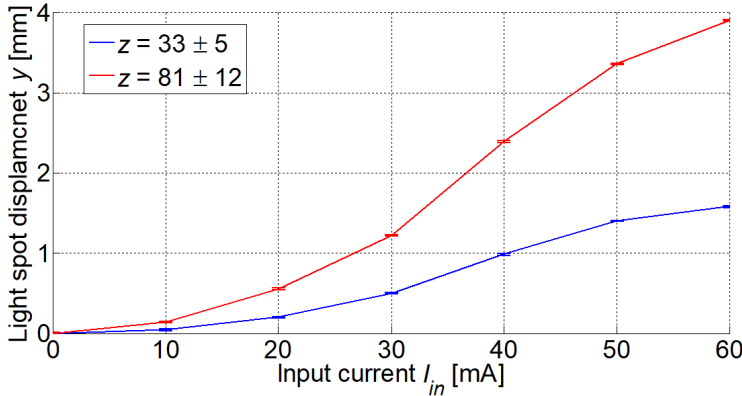


Figure 5.18: Light spot position of y direction scanner versus input current at two working distances of 33 mm (red line) and 81 mm (blue line).

5.3.2. SPOT SIZE CHARACTERIZATION

The integrated OCT system is designed to have a collimated beam at the chip output. This means, the light spot should have a size of around $150 \mu\text{m}$, which is the diameter of the collimating lens (Chapter 2). The spot size diameter should be constant independently of the working distance. However, for both presented devices, the CCD images show (Fig. 5.15 and Fig. 5.16) the light spot has a larger diameter at the longer working distance. This means, both x and y direction scanner have divergent light beam at the system output.

Figure 5.19 illustrates the relation between the light spot diameter and the working distance. The light spot at the output of the chip has a diameter D_0 which should be equal or smaller than the lens diameter ($150 \mu\text{m}$). At the working distances z_1 and z_2 , the

spot diameter is D_1 and D_2 , respectively. The divergent angle is defined as:

$$\tan \alpha = \frac{D_2 - D_1}{2 \cdot \Delta z_{21}} = \frac{D_2 - D_1}{2 \cdot (z_2 - z_1)} \quad (5.1)$$

where Δz_{21} is difference of the two working distances.

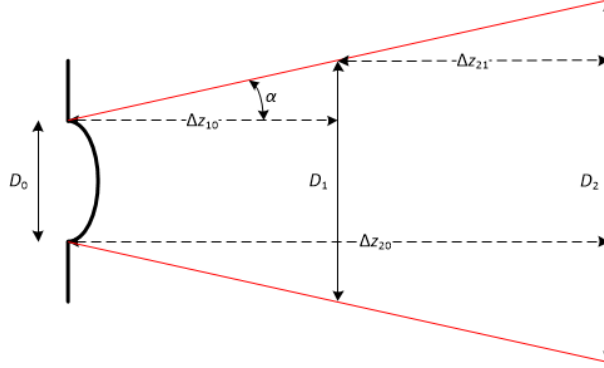


Figure 5.19: Diverged light spot diameter at two different working distances.

The light beam profiles at both working distances are presented in Fig. 5.20. Figures 5.20a-b show the relative intensity profile of the x direction scanner at 31 mm (Fig. 5.20a) and 61 mm (Fig. 5.20b), while Fig. 5.20c-d show the profiles of the y direction scanners at 33 mm (Fig. 5.20c) and 81 mm (5.20d). No Gaussian profile, although expected, is obtained. The x direction scanner has 3 maximum intensity peaks, which indicates there are some problems with the lens. The y direction scanner reaches the maximum intensity value of the CCD camera, due to too long acquisition time for the image formation (50 μ s). Nevertheless, the diameter of the light spot can be extracted from all 4 images.

In the Table 5.1 are summarized light spot diameter values at different working distances. The spot diameter measurement is indicated in Fig. 5.20. Based on presented results the divergence angle is calculated for x direction scanner $\alpha_x = 2.2 \pm 0.6^\circ$ and for y direction scanner $\alpha_y = 0.63 \pm 0.13^\circ$. The x scanning system divergence angle has much higher value than expected while y scanning system divergence angle is comparable compared to the value of 0.75° given in Chapter 3.

Table 5.1: The light spot diameter D and divergence angle α

x direction scanner		y direction scanner	
z [mm]	D [mm]	z [mm]	D [mm]
31 ± 3	2.12 ± 0.05	33 ± 5	0.86 ± 0.05
61 ± 6	4.43 ± 0.05	81 ± 12	1.91 ± 0.05
$\alpha_x = 2.20 \pm 0.60^\circ$		$\alpha_y = 0.63 \pm 0.13^\circ$	

To investigate the reason for such high divergence angle for the x direction scanner, an additional 3D surface profile scan of the lens is done on an already packaged device.

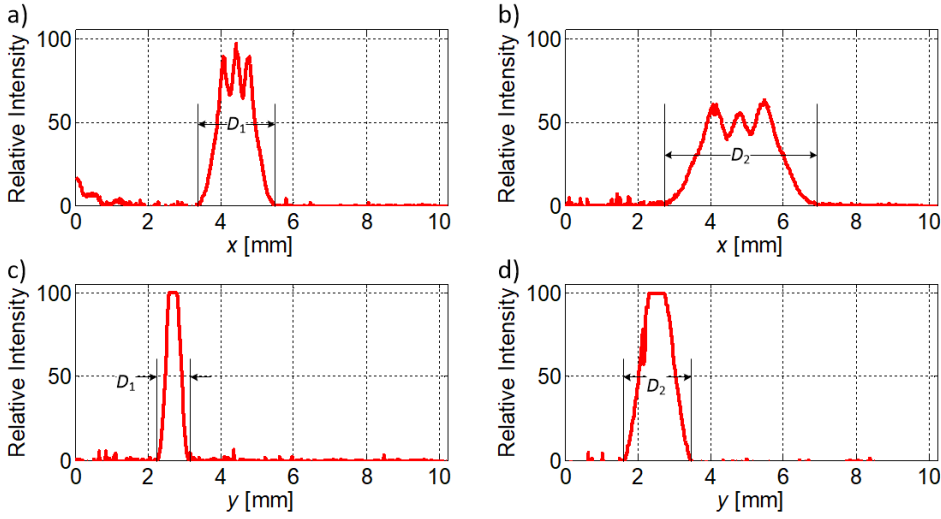


Figure 5.20: Divergent light spot diameter of: x direction scanner at (a) ~ 3 cm and (b) ~ 6 cm and y direction scanner at (c) ~ 3 and (d) ~ 8 cm working distance.

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Due to the PCB board thickness (1.55 mm) and the 3D microscope measurement lens working distance, the magnification is limited to 20, which gives a resolution of only 30 nm. Nevertheless, even such coarse profile gives an indication of lens geometry. In Fig. 5.21 a cross section of the x direction scanner lens is given.

It is clear that the lens profile does not have the right geometry compared to the results given in Chapter 3. First, the lens top to bottom height is much higher than expected. The segment fitted with the dashed red line in Fig. 5.21 has a radius of curvature $R = 850 \pm 50 \mu\text{m}$. Using Eq. 2.7 and 2.11, the calculated divergence angle is $2.4 \pm 0.3^\circ$ which is in agreement with the result obtained using CCD images. Also, big waviness of the surface (green dashed line) resulted in the non-Gaussian light profile in Fig. 20a-b.

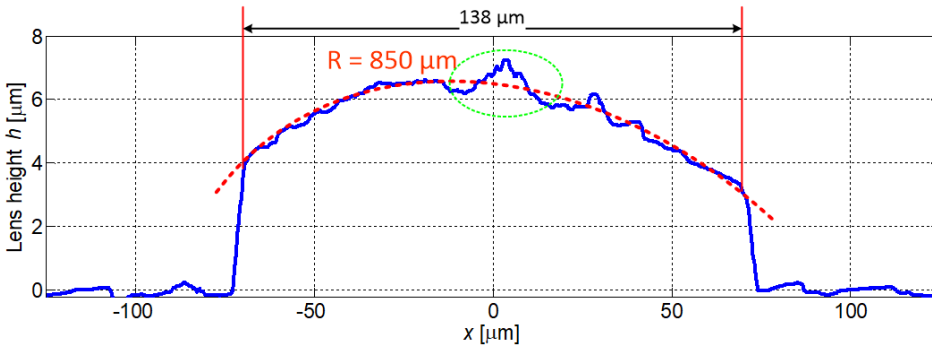


Figure 5.21: Scanning profile (cross section) of the Si microlens of the x direction scanner.

The Si microlens of x or y direction scanning system are made using the same fabrication process and there should not be any differences in the lens profile. To confirm this, the surface of 10 randomly picked Si microlenses of both x and y unpackaged scanners is measured. The measured lens radius of curvature varies between 520 to 590 μm , which complies with the results reported in Chapter 3. Therefore, the bad profile (Fig. 5.21) of the tested device is most likely caused by an incidental scratch during wafer handling before scratch layer deposition or during assembly.

Figure 5.22a shows the CCD image of the light spot at 81 mm working distance with acquisition time of 50 μs . Such long acquisition time gives good contrast and a bright image. However, the CCD camera pixel intensity reaches the maximum and therefore cannot be used to extract the light beam profile (Fig. 5.20b). Thus, the CCD acquisition time is reduced to 5 μs giving a low contrast, barely visible, light spot (Fig. 5.22b). However, with this low acquisition time there is no saturation of the image intensity and the light spot intensity profile can be extracted. The relative light spot intensity from the y direction scanner output is presented in Fig. 5.22c. The presented profile has a good Gaussian fit.

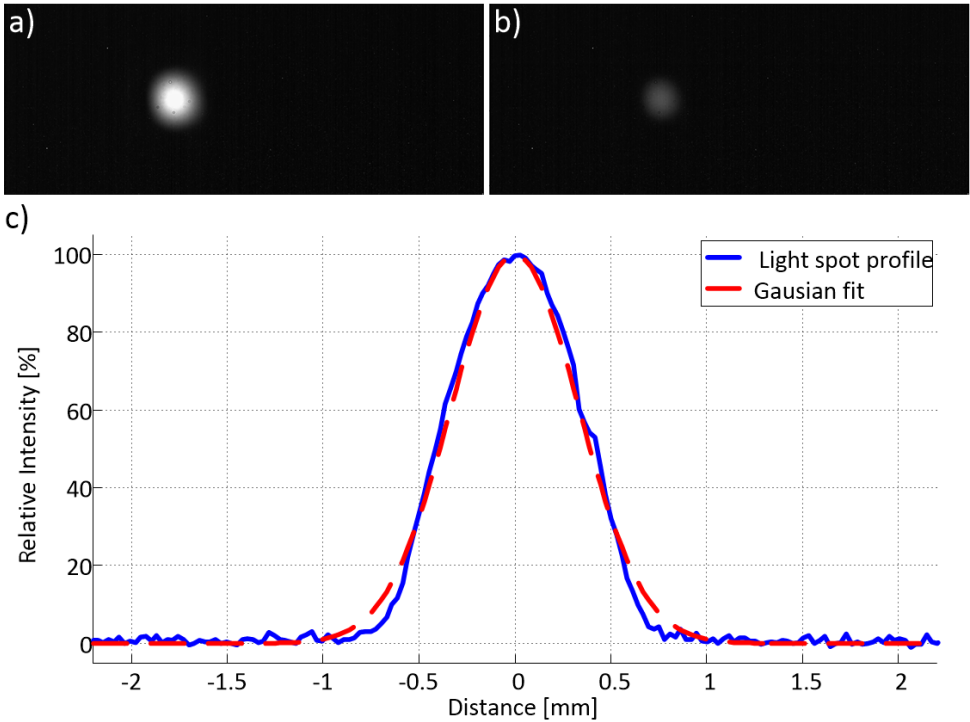


Figure 5.22: (a) High intensity and high contrast CCD image of the light spot. (b) Low intensity and low contrast CCD image of the light spot. (c) Extracted light beam intensity profile and its gaussian fit.

5.4. CONCLUSION

IN this chapter we show how to integrate the photonic platform for the OCT interferometer presented in Chapter 3 with the MEMS actuator systems described in Chapter 4. The main problems with integration are addressed and possibilities for optimization of the fabrication flow are explored. Electro-Mechanical characterization on the fabricated integrated devices is performed. Finally, the optical surface scanning is demonstrated using a CCD camera, thus proving the feasibility of realizing a single chip OCT system.

Electro-Mechanical characterization showed a 50% lower displacement range than expected for the x direction scanner and 75% lower for the y direction scanner. The integrated devices have experienced an improved packaging and wire bonding compared to the stand-alone actuator systems. Consequently, the estimated temperature using TCR characteristics of the Al heater is now more precise compared to what was given in Chapter 4. The torsional hinge thickness of the x direction scanner matches the designed value, but the generated displacement range is lower. The main reason for the lower angular range is the lower maximum generated temperature during static actuation. In the case of the y direction scanner, in addition to the temperature limit, the higher hinge thickness (21 μm) contributes to a lower displacement range.

Dynamic characterization showed the resonant frequency of x direction scanner matches the simulated values presented in Chapter 2. This was expected since the torsional hinge geometry matches the design. Also, the expected high y direction integrated system resonant frequency is observed.

Using 10 Hz and 100 Hz triangular input signal, devices are tested in dynamic regime. For an input signal of 10 Hz, the x direction integrated systems can achieve the same angular displacement as in static regime. Even more, the amplitude was increased up to 3 V which allowed the system to generate higher temperature resulting in a higher total displacement range (7.3°). However, the y direction scanner cannot achieve the maximum temperature probably due to the lower response time. In case of a 100 Hz input signal, both devices could not achieve the values obtained in static regime. The heater response time was not measured and to analyze this problem it would require additional tests for the heater dynamic characterization. This will show what is the fastest temperature change which the Al heaters can follow. Further dynamic characterization with different input signal shapes, actuation in resonant regime etc., will provide more information, which is needed for the MEMS actuator system optimization.

The presented optical characterization is a proof of concept for the optical surface scanning capability using the developed integrated MOEMS devices. Using the presented measurement setup with CCD camera, both scanning range and lens properties are analyzed. The total demonstrated scanning range is ~2.7 mm in x and ~1.6 mm in y direction. Increasing the working distance provides a proportional increase of the scanning range. Although the collimating lens still diverges light and needs further process tuning, the presented results show it is possible to improve the imaging area while keeping the same mechanical performance.

6

CONCLUSION

Education is the most powerful weapon you can use to change the world.

Nelson Mandela

The first single-chip micro-opto-electromechanical system for OCT imaging is presented in this work. Two different MEMS actuator systems for x and y direction surface scanning are designed to be compatible with a commercially available photonic platform. The fabrication process for the integration of all optical components is presented and a compatible process flow for the MEMS actuator system is developed. Finally, these two technologies are combined to produce to the best of author knowledge the first fully integrated self-aligned single-chip MOEMS system.

6.1. MAIN CONCLUSIONS

THE main motivation for this work is to provide an economically viable, high performance alternative technology to the existing OCT imaging systems which are constructed using several discrete components. The presented new approach overcomes complicated and time-consuming packaging solutions, provides a better alignment of optical components and at the same time reduces the overall device footprint. The main idea for solving these problems is the integration of all components into a single-chip device. In this work, the author demonstrates:

- To author's knowledge, the first integrated photonic interferometer with mechanical scanning capabilities for OCT imaging.
- A novel MEMS actuators system realized with a wafer level fabrication process compatible with existing commercially available photonic circuit.
- A working concept for increasing the scanning range by increasing the working distance.

This work is divided in 4 parts: design, optical integration, actuators fabrication and system integration.

Design

The design of the overall system is dictated by the application requirements given in Table 1.1. The main criteria for the design of the supporting hinge is a trade-off between vertical stiffness (as high as possible) and torsional stiffness (as low as possible). The supporting hinge design further dictates the choice of the actuation principle and the actuators design is a compromise between output force, small device footprint and low power consumption. The chosen Al-SiO_x bimorph beam actuators satisfy the low power consumption (<1 W) requirement, have a small footprint and in combination with the properly designed supporting hinges can achieve a system angular displacement of 12° in both directions.

Integration of all optical components

The integration of all optical components is the first step towards the single-chip MOEMS system for OCT imaging. It consists of the fabrication of a silicon microlens and an integrated interferometer as one device. The Si waveguide technology was transferred from VTT to our laboratory (TUD-EKL). The fabricated test waveguides, realized without any dedicated optimization, showed total 1 dB higher optical losses compared to commercially available waveguides. The origin probably comes from facet waviness which introduces additional scattering losses.

The Si microlens is fabricated using thermal photoresist reflow and subsequent dry etching using SF₆/O₂ plasma. The photoresist reflow process showed to be easily controllable. The photoresist ball cap transfer into Si showed the etching selectivity of photoresist to Si etching can be tuned, thus giving more freedom in lens fabrication process definition. However, the surface quality of the final Si lens is sensitive to the process

parameters. Yet, to some extent, it can be improved by thermal oxidation of the lens surface.

The process flow for the integration of all optical modules (lens, mirror and waveguides) must be carefully defined, paying attention to the order of module fabrication to on one hand optimize the overall process flow, and on the other hand, prevent that each module optical properties are negatively affected.

The new MEMS actuators system

The new MEMS actuators system is developed based on the design given in Chapter 2. The fabrication process flow is fully compatible with the process used for the photonic components and has a total thermal budget below 400 °C. Two crucial steps in the fabrication process are identified: Al₂O₃ atomic layer deposition for SiO_x protection and backside DRIE etching for hinge definition.

The first fabrication run (Chapter 4) resulted in working devices with angular displacement of 8° instead of the targeted 12°. Electro-mechanical characterization showed the actuators cannot reach the desired temperature (calculated in Chapter 2), due to burning out of the heater, which is the main reason for the lower displacement range. Also, the supporting hinge geometry was not optimal and resulted in a lower resonant frequency than expected.

In the second run (Chapter 5, Section 5.2), the devices are improved from both packaging and fabrication point of view. The backside etching process improvement resulted in uniform hinge thickness (10%). The *x* direction scanner geometry matched the design values but the achieved displacement range is only 50% of the targeted one, which confirms that Al heater is not sufficiently robust to withstand the higher temperatures needed to fully actuate this device. The *y* direction scanner has a thicker deflecting hinge due to not enough long etching time. The thicker hinge and inefficient Al heater are responsible for the angular range of only 25% of the targeted specifications given in Table 1.1.

The resonant frequency of both devices matched the simulation results corresponding to the fabricated value of hinge thickness. Further dynamic characterization of both devices showed they have a slow response time and at higher frequencies and above 100 Hz they cannot return to the initial state. The *x* direction actuator system has a faster response compared to the *y* direction actuator system and is able to reach the maximum displacement range for an input signal of 10 Hz. Since the *y* direction scanning system has longer actuators, the observed slower thermal response was expected. Also, it could only reach 80% of the expected displacement range compared to static response.

Integration of all components

The second run for the actuators system is done on wafers in which all optical components are already integrated. To enable the integration of the MEMS actuators, the right order of deposition of protective layers is vital to preserve proper functionalities of all components. The result is a monolithically integrated MOEMS chip.

The MOEMS chip demonstrated scanning capabilities using static actuation. A total

scanning range of 2.7 mm in x and 1.6 mm in y direction was achieved with working distance of 3 cm. This demonstrated that using a small angle displacement it is possible to achieve large scanning ranges and that this range can be further extended by increasing the working distance.

6.2. RECOMMENDATIONS FOR FUTURE WORK

THE presented concept is based on the integration of photonic components with Al-SiO_x bimorph beam actuators and its capabilities are demonstrated, to the author's best knowledge, for the first time. Despite the encouraging initial results achieved, further development and optimization of the system are required to reach the targeted optical and mechanical performance and fully benefit from the novel concept introduced. The main improvements to be considered are related:

- Fabrication process optimization.
- Microheater development.
- System design improvement.

Fabrication process optimization

In this thesis, a first level of process optimization has been carried out and extensively described. However, there is still room for further improvement. In the future, additional optimization is needed for:

- Lens process fabrication – The Si lens surface quality is sensitive to the stability of the etching process. Therefore, the etching process must be made more robust to small variations of the main process parameters. Also, the effect of chamber cleanness on the stability and uniformity of the process should be identified and controlled.
- Mirror fabrication – Although the mirror fabrication did not show any significant problem, some consideration should be made related to possible variation due to the very short etch time used. The wet etch process at 85 °C is short (6 min 30 sec) and the time for the wafer to heat up from room temperature to 85 °C while immersed in the solution, might influence the etching uniformity. Possible etching alternatives or a better set up should be explored.
- Waveguide fabrication – To achieve the same optical performance as the commercially available photonic platform from VTT, the Bosch process must be improved to further reduce sidewall roughness.
- MEMS actuator system fabrication – The hinge is fabricated using 100 μm deep front side etch and two-step backside etch (100 μm and 690 μm). Such deep frontside etch is not ideal for PECVD SiO_x etch stop layer deposition. Hence, optimization of front and backside etch depth is needed to improve stop layer robustness.

Microheater development

The driving unit of any electrothermal bimorph beam actuator is its microheater. The calculated maximum temperature in Chapter 2 indicated that Al can be used as a heating material. Unfortunately, the test results showed it is not possible to supply more than 40 mA of current into the heater and thus provide the right temperature to the actuator system. Therefore, a new microheater must be developed to achieve the desired displacement range. The new microheater must satisfy the following requirements:

- Be thermo-mechanically robust to withstand material deflection at higher temperature (up to 500 °C).
- Operate with voltages below 12 V.
- Consume less than 1 W power.
- Have a faster dynamic response than 0.1 s.

The new microheater should be made from a different, mechanically stronger, CMOS compatible, material such as Mo, Ti, TiN, in-situ doped SiC, highly doped poly-Si or similar. Once the right material is chosen, a proper design must be investigated to satisfy the requirements mentioned above.

System design improvements

This work focuses more on technology development than on device characterization. In order to make further improvements in the design it is important to have more information on the system performance. In particular:

- Optical performance of mirror-lens interface– The wet etch time for 45° facet fabrication is short and thus a slight over etch might introduce misalignment of the mirror relative to the lens. Once the temperature influence at the beginning of the etching process of the 45° facet is investigated, the layout should be corrected to insure a more stable etching process.
- Dynamic performance of MEMS actuator systems – To improve the design of the actuators and hinges, further dynamic characterization is needed to better understand drawbacks of the current design.
- Total thermal losses in the system - Based on the presented results, the first design improvement must include the microheater placed between the two bimorph layers. Currently, the microheater is placed below the actuator and one side is exposed to the air. Hence, there are big thermal losses. Next, the heater of the y direction scanner is much longer than the actuator itself. In the current design, the heater also sits on the Si block with the lens and therefore also heating the Si block. As Si is good thermal conductor, this block behaves as a heatsink and contributes to the thermal losses observed.

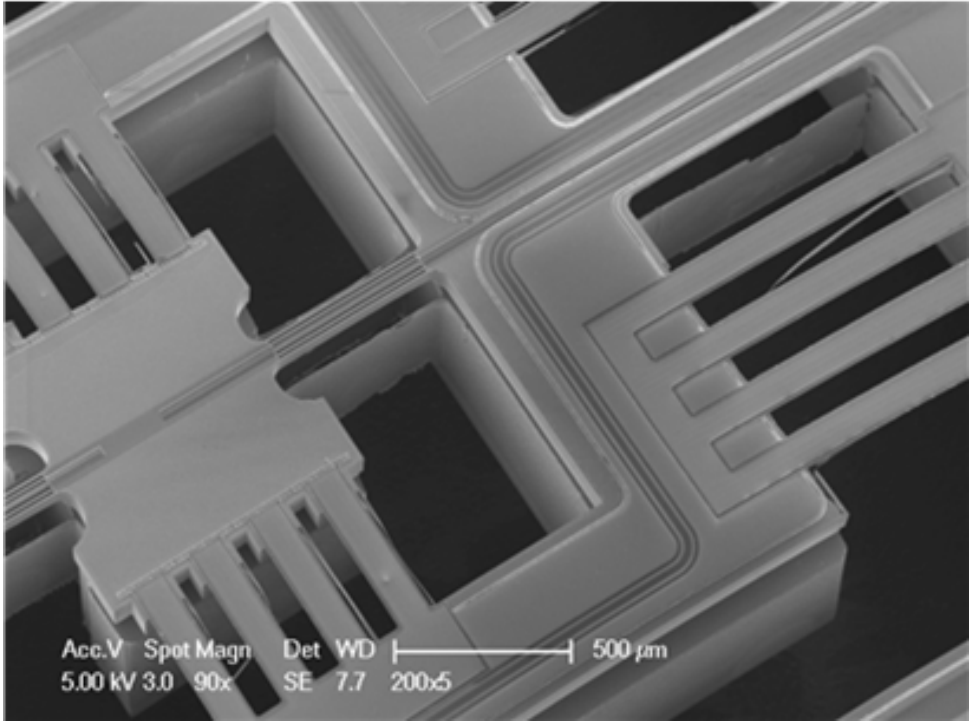


Figure 6.1: A SEM image of a fabricated monolithically integrated 2D MOEMS scanning system.

Naturally, the last recommendation is related to the fabrication of a 2D scanning system. In Fig. 6.1 a fabricated 2D scanning system is shown. Unfortunately, the hinge definition and device release were not optimum resulting in low angular displacement ranges (below 1°). The fabrication process needs to be fine-tuned to overcome these problems. Once the x and y direction scanners are optimized following above mentioned recommendations, the monolithically integrated 2D MOEMS scanning system can be successfully fabricated and implemented in hand-held OCT imaging device as it was the main goal of BiopsyPen project.

APPENDIX A

A.1 TEST HINGES FABRICATION PROCESS

THIS section gives detailed fabrication process for torsional hinge test structures presented in Chapter 2. The process flow corresponds to Fig. 2.17. Fabrication steps are grouped in functional blocks while critical parts are explained in more details. The mask set is designed for full wafer exposure tool. The starting material is a 525 μm -thick single side polished Si wafer with alignment markers for full wafer exposure.

1. Hinge geometry definition

- (a) *Lithography for hinge geometry definition*: Photoresist coating process; full wafer exposure using HNG mask and corresponding light energy; Photoresist development process.
- (b) *Front side hinge etching*: 20 μm deep Si etching using Bosch process.
- (c) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.
- (d) *Stop layer deposition*: 5 μm thick PECVD silicon oxide deposition on the wafer front side

2. Backside etching and hinge release

- (a) *Wafer cleaning*: Standard wafer cleaning.
- (b) *Hard mask layer deposition*: 5 μm thick PECVD silicon oxide deposition on the wafer back side
- (c) *Lithography for backside opening*: Photoresist coating process; Full wafer exposure using BSE mask and corresponding light energy; Photoresist development process.
- (d) *Hard mask opening*: 20 μm deep silicon etching using Bosch process.
- (e) *Back side mask etching*: 5 μm thick PECVD silicon oxide using plasma dry etching process.
- (f) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.
- (g) *Back side etching*: 515 μm deep back side silicon etching using Bosch process
- (h) *Device release*: Stop layer and hard mask silicon oxide layer removal using vapor HF.

A.2 TEST BIMORPH BEAMS FABRICATION PROCESS

THIS section gives detailed fabrication process for bimorph cantilever test structures introduced in Chapter 2. Fabrication steps are grouped in functional blocks while critical parts are explained in more details. The mask set is designed for stepper exposure tool. The starting material is a 525 μm -thick single side polished Si wafer with dedicated alignment markers for available stepper exposure tool.

1. Layer depositions

- (a) *Wafer cleaning*: Standard wafer cleaning.

- (b) *Silicon oxide deposition*: 2 μm -thick silicon oxide deposition using thermal oxidation, LPCVD TEOS deposition, PECVD TEOS or silane PECVD deposition. For each deposition technique use 3 wafers.
- (c) *Aluminum deposition*: 2 μm -thick Al1%Si sputter coating at 25°C, 50°C and 350°C. For each deposition temperature use 4 wafers with different silicon oxide.

2. Bimorph definition

- (a) *Lithography*: Photoresist coating process; Stepper exposure using COLD LAYER mask and corresponding light energy; Photoresist development process.
- (b) *Aluminum etching*: 2 μm -thick dry aluminum etching using Cl-based plasma at 25°C and landing on silicon oxide.
- (c) *Oxide etching*: 2 μm -thick dry silicon oxide etching using CHF₃-based plasma at 20°C and landing on silicon oxide.
- (d) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.
- (e) *Cantilever release*: Isotropic dry silicon etching using SF₆ plasma at 20°C.

APPENDIX B

B.1 SI MICROLENS FABRICATION PROCESS

THIS section gives detailed fabrication process for silicon microlenses presented in Chapter 3. The process flow corresponds to Fig. 3.13. Fabrication steps are grouped in functional blocks while critical parts are explained in more details. The mask set is designed for stepper exposure tool. The starting material is a 525 μm -thick single side polished Si wafer with dedicated alignment markers for available stepper exposure tool.

1. Ball cap formation

- (a) *Diameter definition*: 90 s long HMDS treatment at 130°C; 8 μm -thick Microchemicals AZ9260 photoresist coating; 90 s long soft bake at 95°C; 120 s long soft bake at 115°C; UV exposure using LNS stepper mask and corresponding energy (wait 30 minutes before exposure); Photoresist development process (wait 30 minutes before development).
- (b) *Photoresist reflow*: 2.5 hours bake in vacuum furnace at 160°C.

2. Microlens etching

- (a) *Etching*: Silicon microlens dry etching using SF_6 - O_2 plasma. The etching process is defined in Chapter 3, Section 3.2.2.
- (b) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.

3. Surface roughness reduction

- (a) *Thermal oxidation*: 2.5 μm -thick wet thermal oxidation.
- (b) *Silicon oxide removal*: 35 minutes long etching in buffered HF solution (1:7).

B.2 SI WAVEGUIDES FABRICATION PROCESS

THIS section gives detailed fabrication process for Si waveguides presented in Chapter 3. The process flow corresponds to Fig. 3.17. Fabrication steps are grouped in functional blocks while critical parts are explained in more details. The mask set is designed for stepper exposure tool. The starting material is a double side polished 700 μm -thick SOI wafer with 3225 nm-thick device layer and 440 nm thick BOX oxide layer with dedicated alignment markers for available stepper exposure tool.

1. Waveguide definition

- (a) *Hard mask deposition*: 200 nm-thick silane PECVD oxide deposition.
- (b) *Hard mask definition*: Photoresist coating process; Stepper wafer exposure using WG1 mask and corresponding light energy; Photoresist development process.
- (c) *Hard mask patterning*: Silicon oxide dry etching using CHF_3 -based plasma at 20°C.
- (d) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.

- (e) *Soft mask definition*: Photoresist coating process; Stepper wafer exposure using WG2 mask and corresponding light energy; Photoresist development process.
- (f) *First step etching*: 4 minute long 0.55% HF dip for native oxide removal; 9 cycle long Bosch process etching using recipe given in Table 3.8
- (g) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.
- (h) *Second step etching*: 4 minute long 0.55% HF dip for native oxide removal; 6 cycle long Bosch process etching using recipe given in Table 3.8
- (i) *Hard mask removal*: Silicon oxide mask removal in buffered HF solution (1:7).

2. Sidewall roughness reduction

- (a) *Wafer cleaning*: Standard wafer cleaning.
- (b) *Thermal oxidation*: 500 nm-thick wet thermal oxidation.
- (c) *Oxide removal*: 500 nm-thick silicon oxide removal in buffered HF solution (1:7). BOX layer must not be etched away and etching time must be calculated precisely based on previous test etch.

3. Anti reflection coating definition

- (a) *Wafer cleaning*: Standard wafer cleaning.
- (b) *Silicon nitride layer deposition*: 165 nm-thick LPCVD silicon nitride deposition.
- (c) *Hard mask deposition*: 100 nm-thick LPCVD TEOS silicon oxide deposition.
- (d) *Hard mask definition*: Photoresist coating process for high topography surface; Stepper wafer exposure using ARC mask and corresponding light energy; Photoresist development process.
- (e) *Hard mask patterning*: 100 nm-thick silicon oxide removal in buffered HF solution (1:7). No significant over etch is expected.
- (f) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.
- (g) *ACR patterning*: 165 nm-thick silicon nitride removal in phosphoric acid at 157°C.

4. Cladding layer definition

- (a) *Wafer cleaning*: Standard wafer cleaning.
- (b) *Cladding deposition*: 240 nm-thick LPCVD TEOS silicon oxide deposition.
- (c) *Lithography*: Photoresist coating process for high topography surface; Stepper wafer exposure using CLD mask and corresponding light energy; Photoresist development process.
- (d) *Oxide etching*: 340 nm-thick silicon oxide removal in buffered HF solution (1:7). No significant over etch is expected.
- (e) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.

5. End facet definition

- (a) *Mask definition*: Photoresist coating process; Stepper wafer exposure using EFD mask and corresponding light energy and focus; Photoresist development process.
- (b) *BOX removal*: Silicon oxide dry etching using CHF₃-based plasma at 20°C.
- (c) *Trench etching*: 100 µm-deep silicon etching using Bosch process.
- (d) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.

B.3 45° FACET FABRICATION PROCESS

THIS section gives detailed fabrication process for formation of 45° facets presented in Chapter 3. Section 3.4. Fabrication steps are grouped in functional blocks while critical parts are explained in more details. The mask set is designed for full wafer exposure tool. The starting material is a <100> 525 µm-thick single side polished Si wafer with alignment markers for full wafer exposure. All lithography images must be oriented for 45° compared to wafer primary flat.

1. Hard mask definition

- (a) *Hard mask deposition*: 200 nm-thick LPCVD TEOS oxide deposition
- (b) *Lithography*: Photoresist coating process; Stepper wafer exposure using MIR mask and corresponding light energy; Photoresist development process.
- (c) *Hard mask patterning*: Silicon oxide dry etching using CHF₃-based plasma at 20°C.
- (d) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.

2. Mirror formation

- (a) *Surface passivation*: 4 minute long 0.55% HF dip with subsequent Maragoni drying.
- (b) *Mirror etching*: 30 minute long Si wet etching in 25% TMAH solution with additional 50 ppm of Triton-X at 85°C.
- (c) *Hard mask removal*: Silicon oxide mask removal in buffered HF solution (1:7).
- (d) *Wafer cleaning*: Standard wafer cleaning.

APPENDIX C

THIS chapter gives detailed fabrication process for integrated optical chip with all OCT components Chapter 3, Section 3.5.2. The process flow corresponds to Fig. 3.23. Fabrication steps are grouped in functional blocks while critical parts are explained in more details. The mask set is designed for stepper exposure tool. The starting material is a <100> double side polished 700 μm -thick SOI wafer with 4350 nm-thick device layer and 440 nm thick BOX oxide layer with dedicated alignment markers for available stepper exposure tool on both front and backside of the wafer. All lithography images must be oriented for 45° compared to wafer primary flat.

1. Ball cap formation

- (a) *Front side scratch protection*: 5 μm -thick silane PECVD silicon oxide deposition.
- (b) *Backside lithography*: 90 s long HMDS treatment at 130°C; Microchemical AZ92600 photoresist coating with 1100 rpm; 90 s long soft bake at 95°C; 120 s long soft bake at 115°C; UV exposure using LNS stepper mask and corresponding energy (wait 30 minutes before exposure); Photoresist development process (wait 30 minutes before development).
- (c) *Photoresist reflow*: 4 hours bake in vacuum furnace at 160°C.

2. Microlens etching

- (a) *Etching*: 50 minute long silicon microlens dry etching using SF_6 - O_2 plasma. The etching process is defined in Chapter 3, Section 3.2.2.
- (b) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.

3. Surface roughness reduction and back side protection

- (a) *Thermal oxidation*: 2.5 μm -thick wet thermal oxidation.
- (b) *Front side coating*: 90 s long HMDS treatment at 130°C; 1.4 μm -thick photoresist coating;
- (c) *Silicon oxide removal*: 35 minutes long etching in buffered HF solution (1:7).
- (d) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.
- (e) *Back side scratch protection*: 1 μm -thick PECVD silicon nitride deposition.
- (f) *Silicon oxide removal*: 35 minutes long etching in buffered HF solution (1:7).
- (g) *Wafer cleaning*: Standard wafer cleaning.

4. Waveguide definition

- (a) *Hard mask deposition*: 200 nm-thick silane PECVD oxide deposition.
- (b) *Hard mask definition* Photoresist coating process; Stepper wafer exposure using WG1 mask and corresponding light energy; Photoresist development process.
- (c) *Hard mask patterning*: Silicon oxide dry etching using CHF_3 -based plasma at 20°C.
- (d) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.

- (e) *Soft mask definition*: Photoresist coating process; Stepper wafer exposure using WG2 mask and corresponding light energy; Photoresist development process.
- (f) *First step etching*: 4 minute long 0.55% HF dip for native oxide removal; 9 cycle long Bosch process etching using recipe given in Table 3.8
- (g) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.
- (h) *Second step etching*: 4 minute long 0.55% HF dip for native oxide removal; 6 cycle long Bosch process etching using recipe given in Table 3.8
- (i) *Hard mask removal*: Silicon oxide mask removal in buffered HF solution (1:7).

5. 45° mirror fabrication

- (a) *Hard mask deposition*: 200 nm-thick LPCVD TEOS oxide deposition
- (b) *Lithography*: Photoresist coating process for wafers with high topography; Stepper wafer exposure using MIR mask and corresponding light energy; Photoresist development process.
- (c) *Hard mask patterning*: Silicon oxide dry etching using CHF₃-based plasma at 20°C.
- (d) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.
- (e) *Surface passivation*: 4 minute long 0.55% HF dip with subsequent Maragoni drying.
- (f) *Mirror etching*: 6 min 10 s long Si wet etching in 25% TMAH solution with additional 50 ppm of Triton-X at 85°C.
- (g) *Hard mask removal*: Silicon oxide mask removal in buffered HF solution (1:7).

6. Sidewall surface reduction

- (a) *Wafer cleaning*: Standard wafer cleaning.
- (b) *Backside scratch protection removal*: 1 µm-thick PECVD silicon nitride removal in phosphoric acid at 157°C.
- (c) *Wafer cleaning*: Standard wafer cleaning.
- (d) *Thermal oxidation*: 500 nm-thick wet thermal oxidation.
- (e) *Oxide removal*: 500 nm-thick silicon oxide removal in buffered HF solution (1:7). BOX layer must not be etched away and etching time must be calculated precisely based on previous test etch.

7. Anti reflection coating definition

- (a) *Wafer cleaning*: Standard wafer cleaning.
- (b) *Silicon nitride layer deposition*: 165 nm-thick LPCVD silicon nitride deposition.
- (c) *Hard mask deposition*: 100 nm-thick LPCVD TEOS silicon oxide deposition.
- (d) *Hard mask definition*: Photoresist coating process for high topography surface; Stepper wafer exposure using ARC mask and corresponding light energy; Photoresist development process.
- (e) *Backside hard mask protection*: Manual HMDS treatment at room temperature for 10 minutes; 8 µm-thick photoresist manual wafer coating; 30 min long soft bake in furnace at 100°C.
- (f) *Hard mask patterning*: 100 nm-thick silicon oxide removal in buffered HF solution (1:7). No significant over etch is expected.
- (g) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.
- (h) *ACR patterning*: 165 nm-thick silicon nitride removal in phosphoric acid at 157°C.

8. Cladding layer definition

- (a) *Wafer cleaning*: Standard wafer cleaning.
- (b) *Cladding deposition*: 240 nm-thick LPCVD TEOS silicon oxide deposition.
- (c) *Lithography*: Photoresist coating process for high topography surface; Stepper wafer exposure using CLD mask and corresponding light energy; Photoresist development process.
- (d) *Oxide etching*: 340 nm-thick silicon oxide removal in buffered HF solution (1:7). No significant over etch is expected.
- (e) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.

9. End facet definition

- (a) *Mask definition*: Photoresist coating process; Stepper wafer exposure using EFD mask and corresponding light energy and focus; Photoresist development process.
- (b) *BOX removal*: Silicon oxide dry etching using CHF₃-based plasma at 20°C.
- (c) *Trench etching*: 100 µm-deep silicon etching using Bosch process.
- (d) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.

APPENDIX D

THIS chapter gives detailed fabrication process for MEMS actuators fully described in Chapter 4. Fabrication steps are grouped in functional blocks while critical parts are explained in more details. The mask set is designed for stepper exposure tool. The starting material is a single side polished 525 μm -thick wafer with dedicated alignment markers for available stepper exposure tool.

1. Microheater definition

- (a) *Insulation/sacrificial layer deposition*: 3 μm -thick silane PECVD oxide deposition.
- (b) *Aluminum deposition*: 300 nm-thick Al2%Si sputter coating at 350°C.
- (c) *Heater definition* Photoresist coating process; Stepper wafer exposure using HTR mask and corresponding light energy; Photoresist development process.
- (d) *Heater patterning*: 300 nm-thick dry aluminum etching using Cl-based plasma at 25°C and landing on silicon oxide.
- (e) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.

2. Trench definition

- (a) *Trench definition*: Photoresist coating process; Stepper wafer exposure using TRN mask and corresponding light energy; Photoresist development process.
- (b) *First etch*: 4 minute long 0.55% HF dip for native oxide removal; 9 cycle long Bosch process etching using recipe given in Table 3.8
- (c) *First etch*: 1.5 μm -thick dry silicon oxide etching using CHF₃-based plasma at 20°C and landing on silicon oxide.
- (d) *Second etch*: 1.5 μm -thick wet etch using buffer HF solution (1:7).
- (e) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.

3. Electrical insulation

- (a) *ALD alumina*: 100 nm-thick ALD alumina deposition at 300°C.
- (b) *Contact opening definition* Photoresist coating process; Stepper wafer exposure using CTO mask and corresponding light energy; Photoresist development process.
- (c) *Contact opening patterning*: 100 nm-thick dry alumina etching using F-based plasma at 25°C and landing on aluminum. Add 50% overetch. Etching recipe must have selectivity towards aluminum better than 1.
- (d) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.

4. Bimorph definition

- (a) *Aluminum deposition*: 2 μm -thick Al2%Si sputter coating at 350°C.
- (b) *Silicon oxide layer deposition*: 2 μm -thick silane PECVD oxide deposition.
- (c) *Silicon oxide definition*: Photoresist coating process for high topography surface; Stepper wafer exposure using OXL mask and corresponding light energy; Photoresist development process.

- (d) *Silicon oxide patterning* : 2 μm -thick dry silicon oxide etching using CHF_3 -based plasma at 20°C and landing on silicon oxide.
- (e) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.
- (f) *ALD alumina*: 200 nm-thick ALD alumina deposition at 300°C .
- (g) *Aluminum definition*: Photoresist coating process; Stepper wafer exposure using ALL mask and corresponding light energy; Photoresist development process.
- (h) *Alumina etching*: 200 nm-thick dry alumina etching using F-based plasma at 25°C and landing on aluminum. Add 50% overetch. Etching recipe must have selectivity towards aluminum better than 1.
- (i) *Aluminum etching*: 2 μm -thick dry aluminum etching using Cl-based plasma at 25°C and landing on 100 nm-thick alumina. Overetch must not have high bias not to introduce significant damage to 100 nm-thick alumina.
- (j) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.
- (k) *Alumina definition*: Photoresist coating process; Stepper wafer exposure using ALO mask and corresponding light energy; Photoresist development process.
- (l) *Alumina etching*: 200 nm-thick dry alumina etching using F-based plasma at 25°C and landing on aluminum and silicon oxide. Add 50% overetch. Etching recipe must have selectivity towards aluminum better than 1.
- (m) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.

5. Front side hinge definition

- (a) *Hinge definition*: Photoresist coating process; Stepper wafer exposure using HNG mask and corresponding light energy and focus; Photoresist development process.
- (b) *Front side hinge etch*: 20 μm -deep silicon etching using Bosch process.
- (c) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.
- (d) *Stop layer deposition*: 5 μm -thick silane PECVD silicon oxide deposition

6. Backside hinge definition and device release

- (a) *Backside alumina etching*: 300 nm-thick dry alumina etching using F-based plasma at 25°C and landing on silicon.
- (b) *Wafer cleaning*: Standard wafer cleaning.
- (c) *Hard mask deposition*: 5 μm -thick silane PECVD silicon oxide deposition
- (d) *Hard mask definition*: Photoresist coating process; Stepper wafer exposure using BSE mask and corresponding light energy and focus; Photoresist development process.
- (e) *Hard mask etching*: Silicon oxide dry etching using CHF_3 -based plasma at 20°C and landing on silicon.
- (f) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.
- (g) *Soft mask definition*: Photoresist coating process; Stepper wafer exposure using FBE mask and corresponding light energy and focus; Photoresist development process.
- (h) *First backside etching*: 50 μm -deep silicon etching using Bosch process.
- (i) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.
- (j) *Second backside etching*: 515 μm -deep silicon etching using Bosch process.
- (k) *Device release*: Device release in vapor HF. It is advisable to dice wafer first and do release on die level.
- (l) *Device bake*: Hotplate bake at 200°C of devices to remove residues of PECVD oxide vapor HF etching.

APPENDIX E

THIS chapter gives detailed fabrication process for monolithically integrated MOEMS system presented in Chapter 5. The fabrication process corresponds to Fig. 5.4 Fabrication steps are grouped in functional blocks while critical parts are explained in more details. The mask set is designed for stepper exposure tool. The starting material is a <100> double side polished 700 μm -thick SOI wafer with 4350 nm-thick device layer and 440 nm thick BOX oxide layer with dedicated alignment markers for available stepper exposure tool on both front and backside of the wafer. All lithography images must be oriented for 45° compared to wafer primary flat.

1. Ball cap formation

- (a) *Front side scratch protection*: 5 μm -thick silane PECVD silicon oxide deposition.
- (b) *Backside lithography*: 90 s long HMDS treatment at 130°C; Microchemical AZ92600 photoresist coating with 1100 rpm; 90 s long soft bake at 95°C; 120 s long soft bake at 115°C; UV exposure using LNS stepper mask and corresponding energy (wait 30 minutes before exposure); Photoresist development process (wait 30 minutes before development).
- (c) *Photoresist reflow*: 4 hours bake in vacuum furnace at 160°C.

2. Microlens etching

- (a) *Etching*: 50 minute long silicon microlens dry etching using SF_6 - O_2 plasma. The etching process is defined in Chapter 3, Section 3.2.2.
- (b) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.

3. Surface roughness reduction and back side protection

- (a) *Thermal oxidation*: 2.5 μm -thick wet thermal oxidation.
- (b) Front side coating: 90 s long HMDS treatment at 130°C; 1.4 μm -thick photoresist coating;
- (c) *Silicon oxide removal*: 35 minutes long etching in buffered HF solution (1:7).
- (d) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.
- (e) *Back side scratch protection*: 1 μm -thick PECVD silicon nitride deposition.
- (f) *Silicon oxide removal*: 35 minutes long etching in buffered HF solution (1:7).
- (g) *Wafer cleaning*: Standard wafer cleaning.

4. Waveguide definition

- (a) *Hard mask deposition*: 200 nm-thick silane PECVD oxide deposition.
- (b) *Hard mask definition* Photoresist coating process; Stepper wafer exposure using WG1 mask and corresponding light energy; Photoresist development process.
- (c) *Hard mask patterning*: Silicon oxide dry etching using CHF_3 -based plasma at 20°C.
- (d) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.

- (e) *Soft mask definition*: Photoresist coating process; Stepper wafer exposure using WG2 mask and corresponding light energy; Photoresist development process.
- (f) *First step etching*: 4 minute long 0.55% HF dip for native oxide removal; 9 cycle long Bosch process etching using recipe given in Table 3.8
- (g) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.
- (h) *Second step etching*: 4 minute long 0.55% HF dip for native oxide removal; 6 cycle long Bosch process etching using recipe given in Table 3.8
- (i) *Hard mask removal*: Silicon oxide mask removal in buffered HF solution (1:7).

5. 45° mirror fabrication

- (a) *Hard mask deposition*: 200 nm-thick LPCVD TEOS oxide deposition
- (b) *Lithography*: Photoresist coating process for wafers with high topography; Stepper wafer exposure using MIR mask and corresponding light energy; Photoresist development process.
- (c) *Hard mask patterning*: Silicon oxide dry etching using CHF₃-based plasma at 20°C.
- (d) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.
- (e) *Surface passivation*: 4 minute long 0.55% HF dip with subsequent Maragoni drying.
- (f) *Mirror etching*: 6 min 10 s long Si wet etching in 25% TMAH solution with additional 50 ppm of Triton-X at 85°C.
- (g) *Hard mask removal*: Silicon oxide mask removal in buffered HF solution (1:7).

6. Sidewall surface reduction

- (a) *Wafer cleaning*: Standard wafer cleaning.
- (b) *Backside scratch protection removal*: 1 µm-thick PECVD silicon nitride removal in phosphoric acid at 157°C.
- (c) *Wafer cleaning*: Standard wafer cleaning.
- (d) *Thermal oxidation*: 500 nm-thick wet thermal oxidation.
- (e) *Oxide removal*: 500 nm-thick silicon oxide removal in buffered HF solution (1:7). BOX layer must not be etched away and etching time must be calculated precisely based on previous test etch.

7. Anti reflection coating definition

- (a) *Wafer cleaning*: Standard wafer cleaning.
- (b) *Silicon nitride layer deposition*: 165 nm-thick LPCVD silicon nitride deposition.
- (c) *Hard mask deposition*: 100 nm-thick LPCVD TEOS silicon oxide deposition.
- (d) *Hard mask definition*: Photoresist coating process for high topography surface; Stepper wafer exposure using ARC mask and corresponding light energy; Photoresist development process.
- (e) *Backside hard mask protection*: Manual HMDS treatment at room temperature for 10 minutes; 8 µm-thick photoresist manual wafer coating; 30 min long soft bake in furnace at 100°C.
- (f) *Hard mask patterning*: 100 nm-thick silicon oxide removal in buffered HF solution (1:7). No significant over etch is expected.
- (g) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.
- (h) *ACR patterning*: 165 nm-thick silicon nitride removal in phosphoric acid at 157°C.

8. Cladding layer definition

- (a) *Wafer cleaning*: Standard wafer cleaning.
- (b) *Cladding deposition*: 220 nm-thick LPCVD TEOS silicon oxide deposition.
- (c) *Lithography*: Photoresist coating process for high topography surface; Stepper wafer exposure using CLD mask and corresponding light energy; Photoresist development process.
- (d) *Oxide etching*: 320 nm-thick silicon oxide removal in buffered HF solution (1:7). No significant over etch is expected.
- (e) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.

9. Actuator fabrication preparation

- (a) *Lithography*: Photoresist coating process for high topography surface; Stepper wafer exposure using PLL mask and corresponding light energy; Photoresist development process.
- (b) *Oxide etching*: 680 nm-thick silicon oxide removal in buffered HF solution (1:7). Add 50% overetch to create bigger undercut.
- (c) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.
- (d) *Alumina protection*: 20 nm-thick ALD alumina deposition at 300°C.
- (e) *Lithography*: Photoresist coating process for high topography surface; Stepper wafer exposure using PLL mask and corresponding light energy; Photoresist development process.
- (f) *Alumina etch*: 20 nm-thick dry alumina etching using CHF₃-based plasma at 20°C and landing on silicon.
- (g) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.
- (h) *Insulation/sacrificial layer deposition*: 5 µm-thick silane PECVD oxide deposition.
- (i) *Backside protection*: 10 µm-thick silane PECVD oxide deposition.

10. Microheater definition

- (a) *Aluminum deposition*: 300 nm-thick Al₂Si sputter coating at 350°C.
- (b) *Heater definition*: Photoresist coating process; Stepper wafer exposure using HTR mask and corresponding light energy; Photoresist development process.
- (c) *Heater patterning*: 300 nm-thick dry aluminum etching using Cl-based plasma at 25°C and landing on silicon oxide.
- (d) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.

11. Trench definition

- (a) *Trench definition*: Photoresist coating process; Stepper wafer exposure using TRN mask and corresponding light energy; Photoresist development process.
- (b) *First etch*: 4 minute long 0.55% HF dip for native oxide removal; 9 cycle long Bosch process etching using recipe given in Table 3.8
- (c) *First etch*: 2.5 µm-thick dry silicon oxide etching using CHF₃-based plasma at 20°C and landing on silicon oxide.
- (d) *Second etch*: 2.5 µm-thick wet etch using buffer HF solution (1:7).
- (e) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.

12. Electrical insulation

- (a) *ALD alumina*: 100 nm-thick ALD alumina deposition at 300°C.
- (b) *Contact opening definition*: Photoresist coating process; Stepper wafer exposure using CTO mask and corresponding light energy; Photoresist development process.
- (c) *Contact opening patterning*: 100 nm-thick dry alumina etching using F-based plasma at 25°C and landing on aluminum. Add 50% overetch. Etching recipe must have selectivity towards aluminum better than 1.
- (d) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.

13. Bimorph definition

- (a) *Aluminum deposition*: 2 µm-thick Al₂Si sputter coating at 350°C.
- (b) *Silicon oxide layer deposition*: 2 µm-thick silane PECVD oxide deposition.
- (c) *Silicon oxide definition*: Photoresist coating process for high topography surface; Stepper wafer exposure using OXL mask and corresponding light energy; Photoresist development process.
- (d) *Silicon oxide patterning*: 2 µm-thick dry silicon oxide etching using CHF₃-based plasma at 20°C and landing on silicon oxide.
- (e) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.
- (f) *ALD alumina*: 200 nm-thick ALD alumina deposition at 300°C.
- (g) *Aluminum definition*: Photoresist coating process; Stepper wafer exposure using ALL mask and corresponding light energy; Photoresist development process.
- (h) *Alumina etching*: 200 nm-thick dry alumina etching using F-based plasma at 25°C and landing on aluminum. Add 50% overetch. Etching recipe must have selectivity towards aluminum better than 1.
- (i) *Aluminum etching*: 2 µm-thick dry aluminum etching using Cl-based plasma at 25°C and landing on 100 nm-thick alumina. Overetch must not have high bias not to introduce significant damage to 100 nm-thick alumina.
- (j) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.
- (k) *Alumina definition*: Photoresist coating process; Stepper wafer exposure using ALO mask and corresponding light energy; Photoresist development process.
- (l) *Alumina etching*: 200 nm-thick dry alumina etching using F-based plasma at 25°C and landing on aluminum and silicon oxide. Add 50% overetch. Etching recipe must have selectivity towards aluminum better than 1.
- (m) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.

14. Front side and end facet hinge definition

- (a) *Hinge and end facet definition*: Photoresist coating process for wafer with high topography; 2 mask stepper wafer exposure using HNG and EFD mask and corresponding light energy and focus; Photoresist development process.
- (b) *sacrificial layer removal*: Silicon oxide dry etching using CHF₃-based plasma at 20°C.
- (c) *Front side hinge etch*: 100 µm-deep silicon etching using Bosch process.
- (d) *Wafer cleaning*: Photoresist removal using O₂ plasma and standard wafer cleaning.
- (e) *Stop layer deposition*: 5 µm-thick silane PECVD silicon oxide deposition

15. Backside hinge definition and device release

- (a) *Backside alumina etching*: 300 nm-thick dry alumina etching using F-based plasma at 25°C and landing on silicon oxide.

- (b) *Wafer cleaning*: Standard wafer cleaning.
- (c) *Hard mask definition*: Photoresist coating process; Stepper wafer exposure using BSE mask and corresponding light energy and focus; Photoresist development process.
- (d) *Hard mask etching*: Silicon oxide dry etching using CHF_3 -based plasma at 20°C and landing on silicon.
- (e) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.
- (f) *Soft mask definition*: Photoresist coating process; Stepper wafer exposure using FBE mask and corresponding light energy and focus; Photoresist development process.
- (g) *First backside etching*: $50\text{ }\mu\text{m}$ -deep silicon etching using Bosch process.
- (h) *Wafer cleaning*: Photoresist removal using O_2 plasma and standard wafer cleaning.
- (i) *Second backside etching*: $690\text{ }\mu\text{m}$ -deep silicon etching using Bosch process.
- (j) *Device release*: Device release in vapor HF. It is advisable to dice wafer first and do release on die level.
- (k) *Device bake*: Hotplate bake at 200°C of devices to remove residues of PECVD oxide vapor HF etching.

ACKNOWLEDGMENTS

A good story is a combination of drama and excitement. Personally, I like action movies when the main character is running against the clock to save the world. To be honest, I also like when stories have happy endings. Thus, I am very glad my 4 and a bit more (and a bit more) year long PhD story is finished as I like. Often, it had moments with a lot of drama, disappointments, last minute finishes and a lot of excitement. But, the most of all, my story had its heroes and this chapter is dedicated to them!

The first hero of my story is my supervisor and promotor Prof. Lina Sarro. She was brave enough to accept me as a PhD student after only one Skype meeting. Working with her, I always felt completely independent from the start. However, she was always there when I needed support whenever I was aware of it or not. As a chairman of the group, Lina makes sure that everyone feels well accepted. She is a dedicated supervisor and always is there to share the burden of young researchers. Lina, you are a true mentor and I am grateful for your support and a lot of patience you had for me (especially when it comes to writing). With your guidance, I have grown as a scientist and as a person.

The boss of all bosses, Dr. Gregory Pandraud, my daily supervisor who spent most of the time with me, both in the cleanroom and on all BiopsyPen meetings. He is one of the most enthusiastic people I have met. He taught me the first lesson of doing research: Learn from your failure! Gregory, thank you for your support and motivation ("It is life!" ☺).

Although, they were not part of my story until the very end, as university professors they are heroes and role models to many other students and researchers like me. Dear comity members, thank you for your time and eagerness to participate in this ceremony. Prof. Kraft, Prof. den Toonder, Prof. Hendriks, Prof. French and Prof. Serdijn, I hope will be a part of many more defense ceremonies and to continue contributing in creation of future scientists.

A brave startup Medlumics, S.L. led by Dr. Eduardo Margallo created an opportunity to work on such interesting concept within BiopsyPen project. I would like to thank the whole Medlumics team, especially Eduardo, Jose, Kirill, Pedro, Juan and Nuria for having a faith in me, at that moment an inexperienced guy, to work on something which was never done before. Also, I would like to thank all BiopsyPen members who participated in our meetings. Mateo, Marcus, Wolfgang, Maria, Andres, Bill and William, it was a pleasure collaborating and moreover, learning from you. It was an honor to part of the team.

We all love movies. Naturally, we always focus on actors. But we should never forget about the crew behind the scenes. Marian and Bianca, thank you for dealing with all our bureaucratic problems. Mario, thanks for teaching me everything you know about etching, I still have a lot to learn. Henk, I hope I will one day catch you as a litho guru but I will never reach your 3D printing design skills. Joost Koos, Robert, Loek, Tom, Wim, Johannes and Alex, Hugo, Cassan, Giles, Ruud, Johan, Jan Cornelis, Jan, Vinod, Ron thanks

for keeping the cleanroom running all these years and trying to translate our dreams into reality. After being a user for so long, I am happy to be your colleague now and I will try to match up. Casper, Silvana, Gregory and Paul, thanks for recognizing me as a suitable member to EKL team. You, as leading team of EKL had a brave decision to bring young guys on such responsible positions. Paolo and Hitham, you are great roommates and you bring much fun and joy in our office and it is a great pleasure to work with you.

During my PhD years I had an honor to spend time with amazing people. Moreover, it is awesome when some of them become your friends. Sten, is my Dutch guide! He taught me, everything I need to know about Delft: where to have a beer, where to go for a gig, where to buy screwdrivers, how to deal with administration and much more. Though, he could not transfer his love for C. Alongside with Ha, he also became house market advisor to both Amir and me. Sten, you have always been a role model to students and I know you will be great mentor.

Amir, I am happy we became such good friends. Even more, we will soon be neighbors. You are now part of TNO, but we are always happy when you are joining our lunch. Also, jealous when you are at QuTech. Even long boring movies are fun to watch with you. Although, people think you are there only to bring smiles, not much know how careful and supportive you can be.

Bruno, was my real cleanroom teacher. He took me by my hand (figuratively speaking) and taught me how to do things right. He gave me tips, showed me tricks and contributed a lot for development of my working skills. Daddy cool, as long as you are here, I will be coming for brainstorming sessions (and for questions about car problems).

Being a member of ECTM group I spent time with people coming from all around the globe. The first person who greeted me, Xueming (and asked to water his flowers) was awesome roommate. Cinzia was my Las Vegas guardian angel. Now, with Niko and William, she guards their startup BI/OND. Aslihan, thanks for the coffee pot. Miki, I hope we practiced Serbian enough. Hong Wah, we had a nice time during our road trip in US. Marta, I believe you will manage to find time for a good gig. Luke, thanks a lot for doing translation of my summary. Manju, you are our measurement room expert. Ronald and Shivani, thanks for fun time in Budapest. Massimo, a burden of reading all my things fell on you as well and I am grateful for your help in writing this book. Our silent genius Rene, thanks for advices on mechanics. Jia, thanks for always finding time to for me. Robert, hope to see you soon in Delft. Giuseppe, Andrea, Jin, Gianluca, Gianpaolo, Joost, Pengfei, Lin, Franchesco, Shinnosuke, Daniel, Jing, Pan, Zhara, Hang, Juan, Paolo, Filiberto, Boyao, Zhen, Yelena, Jian, Brahim, Joosts, Tianyi, Amir 2, Pelin, Xin, Ifigenia, Levar, Sarat, Salvatore, Paolo Firestarter and others, thanks for creating nice and lovely working atmosphere in and outside the cleanroom. I cannot forget colleagues from other departments, Fede, Alkisti, Jaap and Tjite-Jelte from PME and Kefei from ImPhys, thanks for help to characterize my device.

Special heroes during my PhD are Sotiris and Toshi. Sotiris, thanks for having a lot of patience while being my master student. You made all my crazy ideas working. Moreover, while being your supervisor, I had to become better researcher myself in order to be able to supervise you. Thanks for that! Together with Toshi, you managed to push my research forward and because of you we manage to succeed. Toshi, I hope your idea will come to life and it will save many lives.

Dealing with a lot of different people is a tough job. However, for Locus crew it is easy since they create always a friendly atmosphere. Alex, Jim, Bart, Nicko and Thijs, thanks for being always welcoming.

A Bulgarian hero who now fights air pollution brought me back to karate again. Petar, thanks for encouraging me to start training after a long time. At Yoroshi, I met wonderful people. Linda, Merel, Ruben, Shruti, Dhruv, Julius, Robert, Richard, Diego, Tessa, Kevin, Malden it was amazing training with you under our wonderful sensei Dik. Alongside karate, I started kickboxing and met more awesome guys. Eline, Erik, Nam, Deb, Merle, Nick, Natalia and Simon, we had great time with our coach Robert.

Moving from a Serbia to Netherlands is not that hard from me. There was a large Serbian community in Delft and some of these guys were here among the first. Their experience made our accommodation to Delft very easy. First of all, I must thank our hero Marko for introducing me to Lina, even we did not know each other. He is responsible for organizing our community and making good atmosphere whenever he shows up (with few hours delay). Marko, you are unique person and hope you will never change. The biggest scientist between us, Stevan, is a role model to all our young physicist. I hope one day I will tell everyone how I had fun with a Nobel prize winner. Our JNA hero, Stevo aka Rudonja is an example of party-work balance. Rudo, you are an incredible guy and you know when I nag you, I do that because I care.

A couple which brakes the prejudice about partners working together are Maldena and Branko. Guys I am proud of you as parents to Luka. Dmitrije, we miss you since you went back to Serbia. There is none to force us to eat ginger when we are ill. Somići, you are a wonderful family, and everyone feels welcomed at your place. Marija and Patrick, I am looking forward to your wedding. Andrija and Aleksandra, it was an amazing evening in Niš. Pavlovići, Dudo, Lazo, Beške i Nato, I am glad I have met you. Igore, (tata) Nikola, Vlado, Stojane i Jovana, we had and amazing time here in Delft.

Officially we are speaking different language but somehow, we understand each other ☺. Ranko, I know I am not the best friend when it comes to going to your concerts but you know I am there for you when needed. I also met a lot of cool people hanging out with you and dearest of all are Dejan and Nandini. While being in Delft I also met my Dutch Balkaneros. Ivar, Deniz, Vahid, Antonio, Mirza and Ante, thanks for reminding me what good cevapi are. If anyone is wondering how paradise on Earth looks like, ask Ante. He will show you his Žirje. Antiša, I am always happy to have philosophical talks with your home-made beer!

Living in the same student housing bonds people. Our paths went same ways, but in different countries. Steka and Nikola (with long accent on o) are story package which always goes together. For a long time, you were a special duo. Luckily, we all grow up, and things are changing. Now, Nikola and his soul mate Nevena are proud parents of a cute little and very energetic girl Tijana. Guys, I miss you a lot and I appreciate every time we see each other.

During my university days in Serbia I meet people with who I become also very close. Aleksandra, Jelena, Tanja, Mixa and others. Thanks for making my visits to Belgrade joyful. Director Marko, you know you have a special place in my hart. I hope you are proud how your first student turned out.

My math teacher said friendship from high school stays forever. As teenagers we do

not appreciate our teachers at that moment. Few years later we finally understand their wisdom. Marija, thanks for pushing my decision PhD in the right direction. Strahinja, we are always prepared for your visit to the Netherlands (waiting you with herrings). Dr Džoni, I miss discussing deep thoughts with you.

Being roommates at such early age, we learned almost everything about each other. We were next to each other while growing from young province boys to grown up men. You know me as good as my family. Momčilo, after so much years of our friendship you gave me the honor to be the best man to you and Hristina.

I don't know how many people are lucky to have their closest friends close to them once they move from their countries. Žarko is a person with who I did almost everything during my university. We almost ended up doing a PhD at the same place. Although you were in Eindhoven, we never felt the one-and-a-half-hour distance. You were one of my biggest support in past few years.

A man on who I can always relay. He was my right hand in Belgrade whenever I needed him, and he is the same now in Delft. I could not express how happy I have been when Uroš decided to start his masters at TUD. Uroš, you are like a brother me and I am glad you decided to stay around.

New places bring us new people in our life. It is natural. Funny thing is I had to move to Delft to gain a new friend who in fact was just around the corner while being in Belgrade. My buddy was here for me when I had hardest time and with who I share a lot of nice memories in past years. Violeta, I am thankful for always telling me directly when I was making stupid decisions and supporting smart ones.

Because of her devotion to students, we consider her as our hero. She is the one who keeps our lab in place. I don't know if I should consider her as a second mom or as a friend. I learned a lot from her how to process in the cleanroom. But the best lessons I got from Silvana were how to understand people. Silvana you are lovely person and I am happy you found a space for me in your hart.

While working on BiopsyPen project, I gain a lot of experience. The nice part was also visiting project partners around Europe. It is fair to say that my PhD also brought Katarina into my life. Her bravery to leave everything in Vienna and come to Delft made my life meaningful. She is the one who I share everything with. She is the one who hugs me when I am sad. She is the one who makes every morning joyful. She is the one who puts smile on my face. She is the one who makes me a better person. Knowing my personality, she is my everyday hero who knows how to be with me. She is my Queen of the Universe! I love you!

My dear brother is an example how people can overcome the hardest things in their life. His focus, dedication and will is an example to everyone who want to get up after the fall. Vlado, it is amazing how you manage to continue where you stopped after all this time. People should know your story because they need real life heroes to look up to.

The biggest heroes of my story are my parents. When everyone doubted their decision to let me go to high school in Belgrade at age of 15, they were determined. They let me make my own mistakes, so I could learn. They build up my confidence. They convinced me I can achieve anything if I am dedicated. They taught me to be independent. They taught me how to stand still and be realistic. They taught me how to dream. Mom and Dad, I love you and I am grateful you raised me a man who I become.

LIST OF PUBLICATIONS

Journal publications

4. **A. Jović**, T. Uto, K. Hei, J. Sancho, N. Sanchez, K. Zinoviev, J. L. Rubio, E. Margallo, G. Pandraud and P. M. Sarro, *A Monolithically Integrated MOEMS Scanner for A Single-Chip OCT imaging Solution*, To be submitted to *Journal of Microelectromechanical Systems*.
3. **A. Jović**, J. Sancho, N. Sanchez, K. Zinoviev, J. L. Rubio, E. Margallo, M. Mastrangli G. Pandraud and P. M. Sarro, *An Integrated Photonic Platform for a Single-Chip MEMS-Based Optical Coherent Tomography Scanner*, *Micromachines*, Under Review.
2. C. Silvestri, M. Riccio, R. H. Poelma, **A. Jovic**, B. Morana, S. Vollebregt, A. Irace, G. Q. Zhang, P. M. Sarro, *Effects of Conformal Nanoscale Coatings on Thermal Performance of Vertically Aligned Carbon Nanotubes*, *Small*, **14**(20) 1800614, 2018.
1. **A. Jović**, G. Pandraud, N. Sanchez, J. Sancho, K. Zinoviev, J. L. Rubio, E. Margallo and P. M. Sarro, *A MEMS Actuator System for an Integrated 3-D Optical Coherent Tomography Scanner*, *Journal of Microelectromechanical Systems* **27**(2), 259, 2018.

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7. **A. Jović**, T. Uto, K. Hei, J. Sancho, N. Sanchez, K. Zinoviev, J. L. Rubio, E. Margallo, G. Pandraud and P. M. Sarro, *Towards fully integrated, low cost optical coherence tomography system*, 31st IEEE Micro Electro Mechanical Systems (MEMS), 25-28, January 21-25, Belfast, United Kingdom, 2018.
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CURRICULUM VITÆ

Aleksandar JOVIĆ

04-10-1989 Born in Bor, Serbia.

EDUCATION

1996–2004 Elementary School
3. Oktobar, Bor, Serbia

2004–2008 High School
Mathematical Grammar School, Belgrade, Serbia

2008–2012 Bachelor of Science (BSc) in Electrical Engineering and Computer Science
University of Belgrade, Belgrade, Serbia

Thesis: Optimization of Polarization Insensitive Rib Waveguide

Promotor: Prof. dr. D. Gvozdić

2012–2013 Master of Science (MSc) in Electrical Engineering and Computer Science
University of Belgrade, Belgrade, Serbia

Thesis: Statistical Analysis of Optical Packet Switch With Output Buffers

Promotor: Prof. dr. P. Ivaniš

2014–2019 Doctor of Philosophy (PhD) in Electrical Engineering
Delft University of technology

Thesis: A Single-Chip Micro-Opto-Electro-Mechanical System for Optical Coherence Tomography Imaging

Promotor: Prof. dr. ir. P. M. Sarro

INTERNSHIPS

2012 Republic Telecommunication Agency (RATEL), Department for Management of RF spectrum

2013 VIP mobile, Department for Core Network Management and Planning

WORK EXPERIENCE

2013 Microsoft, Serbia: Data Collecting and Labeling Assistant

2010–2013 Lab course assistant at University of Belgrade