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A 5:1 Connected Slot Array Loaded with Artificial Dielectric Layers

(invited paper)

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Abstract—We propose a radiation concept to realize phased arrays with wideband and wide-scanning performance. The array is based on connected-slot elements that radiate in the presence of artificial dielectric superstrates. The array can be implemented with a single multi-layer printed circuit board. Artificial dielectrics are used in place of real dielectrics to minimize the losses due to surface waves and avoid the occurrence of scan blindness over a wide scan range. The achievable bandwidth depends on the number of layers composing the artificial dielectric. A design example is shown that achieves a bandwidth (VSWR < 2.5) of about 5:1 when scanning up to 50° in all azimuth planes. Both single- and dual-polarization designs can be implemented.

Keywords—Artificial dielectric, connected arrays, wideband arrays, wide-scan arrays.

I. INTRODUCTION

Wideband, wide-scanning arrays have been receiving great attention in the last few decades for both commercial and military applications, such as satellite communications, radioastronomy and multifunction radars. One category of arrays with such characteristics is represented by connected arrays: they consist of arrays of either slots or dipoles that are electrically connected [1] or tightly coupled [2] to achieve broadband properties.

Several designs have been presented in the literature and shown to achieve wide bandwidths within a large scan range and low cross-polarization [3]–[6]. Many of these designs were based on a costly three-dimensional assembly, where the array elements were realized on vertical printed circuit boards and arranged in an egg-crate configuration [4]. A planar implementation of connected dipole arrays was proposed in [7], with the advantage of cheaper and simpler manufacturing. More recently, the present authors proposed an alternative planar concept based on slot elements in [8]. This design consists of a connected array of slots loaded with artificial dielectric layers (ADLs). A schematic unit cell structure is shown in Fig. 1. The ADL superstrates can be engineered to obtain an effective dielectric constant higher than that of the medium hosting the metallic inclusions [9], [10]. Such types of superstrate can increase the front-to-back ratio without introducing surface-wave losses, unlike standard homogenous dielectric slabs. A singly polarized array design with three

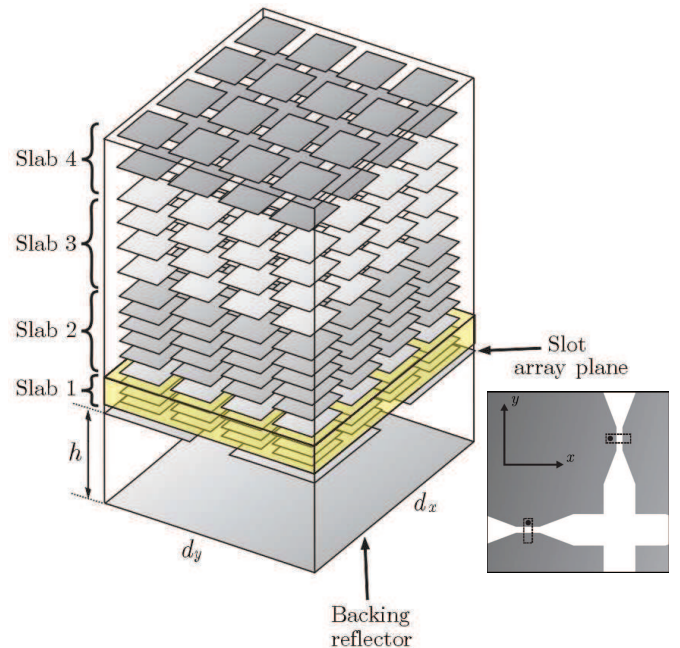


Fig. 1. Geometry of the array unitcell.

ADL superstrates was presented in [8], and it was shown by simulations to achieve a bandwidth exceeding one octave for scanning up to 50° for all the azimuths. The manufacturing of a prototype based on the design in [8] is planned for the next months and we expect to be able to present experimental results by the time of the conference.

In this work, we investigate designs based on the same antenna concept, but targeting wider bandwidths. Only by increasing the number of ADLs, a 5:1 bandwidth (VSWR < 2.5) is achieved for scanning up to 50° , both for single- and for dual-polarized operation. Simulations based on infinite-array analysis are reported to assess the array performance. It is also shown that including a series capacitance in the feeding lines helps to further increase the bandwidth. The purpose of the series capacitance is to tune out the inductive effects of the ground plane at lower frequencies, similarly to the inter-element capacitance in tightly-coupled dipole arrays [2].

II. ARRAY CONCEPT AND ANALYSIS METHOD

Figure 1 depicts the array unit cell, consisting of a connected array of slots in the presence of a backing reflector and loaded with ADLs. ADLs are composed by a cascade of arrays of electrically small metal patches included in a dielectric host medium to enhance its equivalent relative permittivity. Therefore, when loaded with a single or multiple ADL slabs, the array ‘feels’ less the presence of the backing reflector, which can be located closer to it without strongly degrading the impedance matching properties. This reduced distance between the array and the backing reflector allows the implementation of the feed structure by means of standard via-hole technology, e.g. for a 3 to 15 GHz design. Consequently, the proposed solution enables the implementation of the array with a single multi-layer printed circuit board (PCB).

Simulating a unit cell like the one in Fig. 1 using commercial electromagnetic solvers is not a simple or fast process, due to the large number of layers composing the entire stack and the electrically small geometrical features that require very fine meshes. Moreover, a high number of such simulations are needed for the optimization of the total structure, rendering the design impractical. For these reasons, we developed in [8] a spectral method to estimate the performance of the connected array of slots loaded with the ADLs. The method is used to predict the active impedance of the array unit cell, with negligible computational costs.

III. ARRAY DESIGN

As a design example, we consider an array with four ADL slabs. The geometrical parameters are defined in Fig. 2. The array periods are $a = b = 9$ mm and the overall array height is 15 mm, which correspond to 0.45λ and 0.75λ at the highest frequency of operation, respectively. The four slabs are used to realize a multiple quarter-wave section transformer. After optimization of the geometrical parameters, performed with the aid of the analytical models available for the structure under investigation, we selected the values reported in Table I. The feed in the slot element is assumed to be an ideal lumped port of dimension δ . A more realistic feed that leads to the same results can be obtained by tapering the slots in the center and coupling a microstrip feeding line, as depicted in the inset of Fig. 1. The slab separating the slot from the ground plane is characterized by relative permittivity of $\epsilon_{r,back} = 1.4$. Such a low dielectric constant can be realized by means of a perforated dielectric grid [8], that can also host the vias needed for the vertical connections with the PCB coaxial connectors.

A. Array Performance

The active VSWR of a single-pol design is presented in Fig. 3, calculated with both our method [8] and CST Microwave Studio. The array achieves a bandwidth (VSWR < 2.5) of about 5:1 when scanning up to 50° in all azimuth planes. Also a dual polarized cell has been simulated in CST and exhibit similar matching performance (Fig. 4).

The cross-polarization (X-pol) level simulated for the dual polarized case is shown in Fig. 5, for scanning to 50° in the diagonal plane. It is apparent that the X-pol increases with frequencies and reaches high values in the high end of the operative bandwidth. This effect is due to the presence of

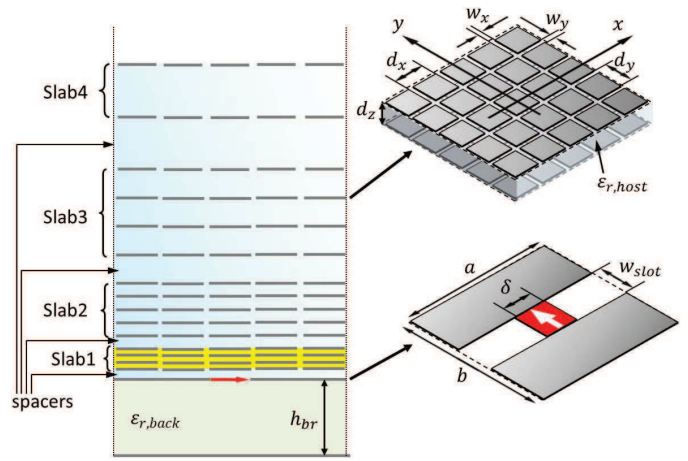


Fig. 2. Definition of the unit cell geometrical and electrical parameters.

TABLE I. ARRAY DIMENSIONS (IN mm), AS DEFINED IN FIG. 2

	Slab1	Slab 2	Slab 3	Slab 4	
$d_x = d_y$	1.8	1.8	1.8	1.8	$a = b$
$w_x = w_y$	0.11	0.08	0.1	0.19	w_{slot}
d_z	0.254	0.508	1.1	1.1	δ
spacer	0.5	0.508	1.1	1.1	h_{br}
$\epsilon_{r,host}$	1.96	1	1	1	$\epsilon_{r,back}$
					1.4

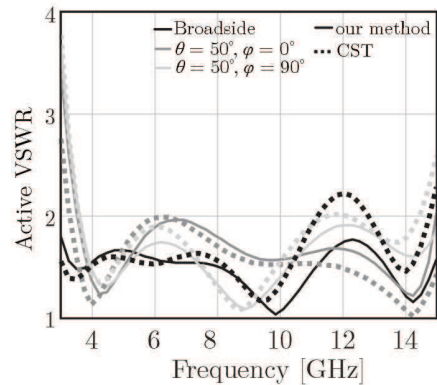


Fig. 3. Active VSWR for a single-pol array configuration.

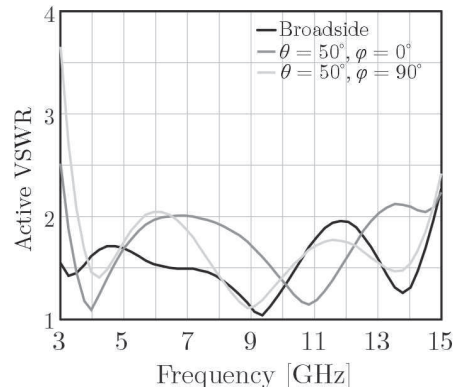


Fig. 4. Active VSWR for a dual-pol array configuration.

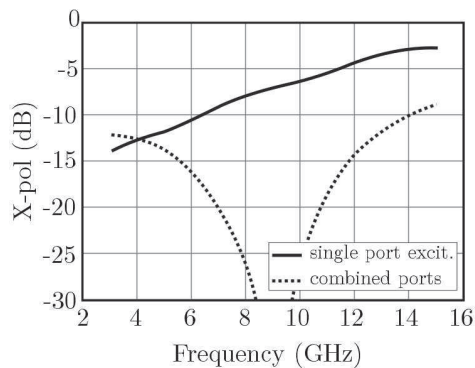


Fig. 5. Cross-polarization level for scanning to 50 degrees on the diagonal plane, with and without ad-hoc combination of the two orthogonal ports.

the dielectric superstrate that is known to yield increased X-pol for linearly polarized radiators [11], due to the different reflection properties of transverse electric and transverse magnetic components. However, thanks to the low isolation between the two slots, the two ports can be combined so that the cross-polarization is perfectly cancelled at a specific frequency and is strongly reduced over a wide bandwidth. Figure 5 shows the reduced cross-pol obtained by combining the two port with the weights ($1\angle 0^\circ$) and ($0.45\angle 139.42^\circ$). The weight are determined by observing the complex amplitudes of the two components of the radiated field in the direction of scanning. It is important to note that similar cancellations can be obtained only over very narrow bandwidth when the cross-polarization is caused by common-mode resonances within the feeding lines [12]. Since the feed structure for the slot element does not support common-mode propagation, one set of weights for the two orthogonal ports leads to cross-polarization lower than -10 dB over a large frequency band.

B. Approach for Enhanced Bandwidth

The matching bandwidth of the array shown in Fig. 2 is limited by two main aspects: the upper limit is due to the inter-element spacing, which should be smaller than half a wavelength at the highest frequency of operation; the lower limit is determined by the ground plane, which becomes strongly inductive in the lower end of the frequency band.

For connected dipole elements, a capacitance is often introduced between elements to improve the low-frequency performance [2], by compensating for the strong inductance of the ground plane. For connected slots, an equivalent series capacitance between elements is not straightforward to implement. However, such series capacitance can be easily introduced in the feeding transmission line of the element, e.g. as shown in Fig 6.

The active VSWR obtained by including a 0.9 pF capacitance in series with the feed is show in Fig. 7. The geometrical parameters are the same as in the Table I, except for the distance from the ground plane, that is set as $h_{br} = 6$ mm. A bandwidth of 8.5 to 1 is obtained with VSWR lower than 3, for scanning to 45° .

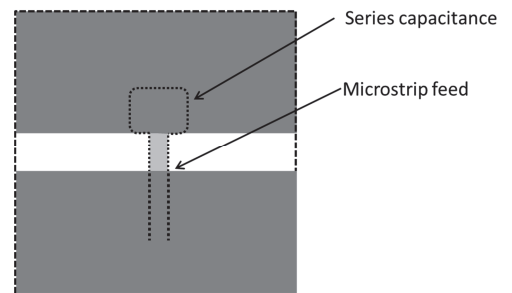


Fig. 6. Feeding microstrip for the connected slot element, with a series capacitance.

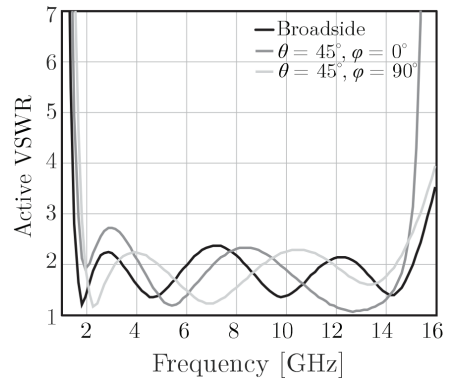


Fig. 7. Active VSWR for a single-pol array configuration.

IV. CONCLUSIONS

We have proposed an antenna concept for phased array applications with wideband and wide-scan capability. The array elements consist of connected slots that radiate in the presence of artificial dielectric superstrates. A design example was shown that achieves a bandwidth (VSWR < 2.5) of about 5:1 when scanning up to 50° in all azimuth planes, both for single- and dual-polarized configurations. Although the polarization purity degrades because of the presence of the superstrate, it was shown that the two orthogonal elements can be easily combined with appropriate weights to reduce the cross-pol over the entire bandwidth of operation.

An approach to further widen the matching bandwidth has also been discussed and involves the inclusion of a series capacitor in the feed structure.

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