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Proefschrift

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Front & Back: Inspired by the painting in EWI building of TUDelft and drawn by Yu Xin.

Printed in the Netherlands

To my wife, Yan Jin

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Introduction

This dissertation describes the research into design and realization of energy-efficient bridge readout integrated circuits (ROICs) for Wheatstone bridge (WhB) sensors. The associated design techniques are progressively explored at both the system and circuit levels. In this chapter, the motivation, objectives and challenges of this work are described. At the end of this chapter, the highlights and structure of the dissertation are presented.

1.1 Motivation

Nowadays, sensors extend human capabilities in many different ways and are all around us, in smartphones, in Internet of Things (IoT) gadgets, high-tech industrial machines, and even in our bodies. Many of these sensors are based on Wheatstone bridge sensors, which convert the variation of a resistance (or impedance) into a differential output voltage (or current). Although the basic idea is more than 180 years old, Wheatstone bridge sensors are still widely used due to their simplicity, stability, and accuracy [1,2]. Examples include sensors of physical quantities such as pressure, strain, temperature, and magnetic field (Figure 1.1) [3-14].

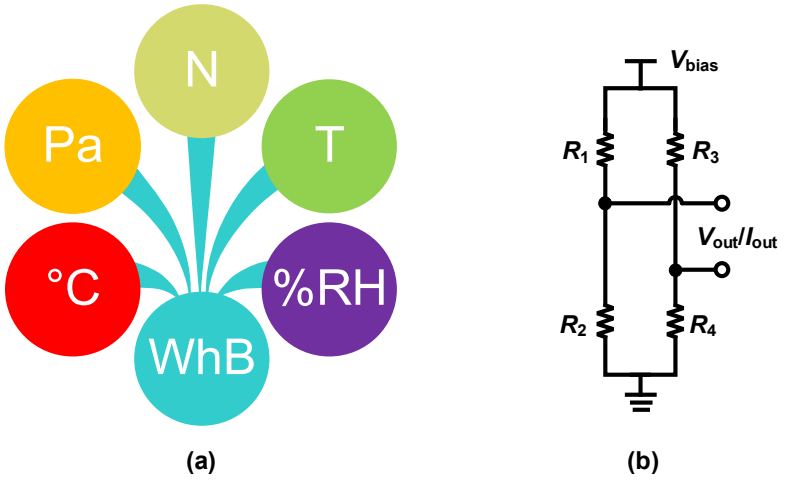

Figure 1.1: WhB sensor: the bridge between the real world and the electrical domain (a); WhB equivalent circuit (b).

1.2 Background and Challenges

In a so-called "full" Wheatstone bridge sensor [2], all four bridge resistances shown in Figure 1. 1.b change in tandem in a manner that maximizes bridge sensitivity [15]. In this case, the output voltage V_{out} is given by

$$V_{out} = \frac{V_{bias} \times r}{R_{bridge}}, \tag{1. 1}$$

where V_{bias} is a DC biasing voltage, R_{bridge} is the nominal bridge resistance and r is the resistance change. So-called "half" bridges are also used, in which two of the resistors are fixed. In this case, V_{out} will be a non-linear function of the ratio r/R_{bridge}

$$V_{out} = \frac{V_{bias} \times r}{2R_{bridge} + r}. \tag{1. 2}$$

However, this ratio will often be less than 1%, and so this non-linearity can be neglected [2]. From (1. 1) and (1. 2), it should be noted that the sensitivity of a bridge sensor is proportional to its biasing voltage.

The output of a Wheatstone bridge sensor will typically be a mV-level differential signal superimposed on a much larger common-mode (CM) voltage, which must then be amplified and digitized by a ROIC to facilitate further digital processing. A conventional Wheatstone ROIC typically consists of a precision instrumentation amplifier (IA) followed by a high-resolution analog-to-digital converter (ADC) as shown in Figure 1.2.

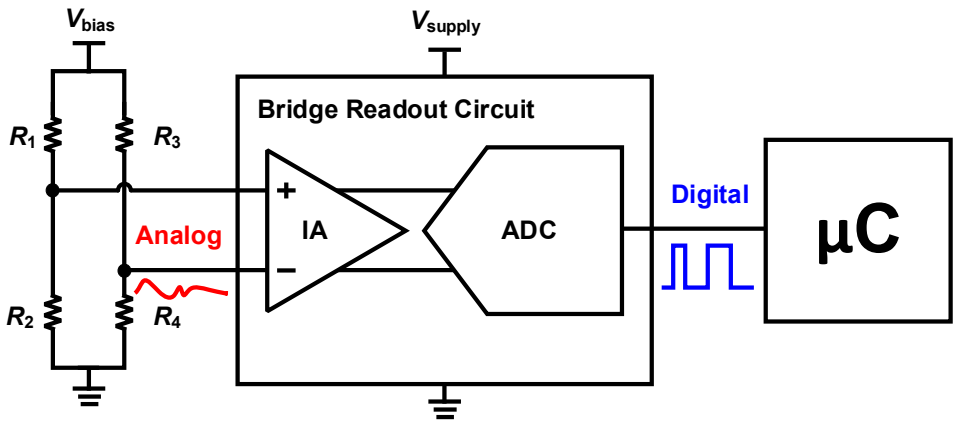

Figure 1.2: Typical bridge sensing system.

To avoid corrupting the bridge output, such ROICs should achieve low input-referred offset, noise, and drift; high input impedance, gain accuracy, stability, and linearity; high immunity to power-supply and common-mode variations; as well as a high energy efficiency.

Low-frequency precision

To precisely handle the small differential signal output by a bridge sensor, input-referred errors such as noise and offset should be much smaller. In most sensing applications, the bandwidth of interest will be in the order of a few kHz. Therefore, $1/f$ noise and offset are usually the dominant error sources. These can both be reduced with the help of dynamic offset cancellation techniques, such as chopping

and auto-zeroing [3-14]. However, the drawbacks of such techniques need to be taken care of [16-20].

Drift

The measurement precision of a sensing system should be maintained even if environmental conditions (e.g., temperature) change, without the need for re-calibration. In typical precision sensing applications, however, the drift of the ROICs cannot be distinguished from the bridge sensor signal. Thus, the drift of such circuits due to temperature and time should be minimized.

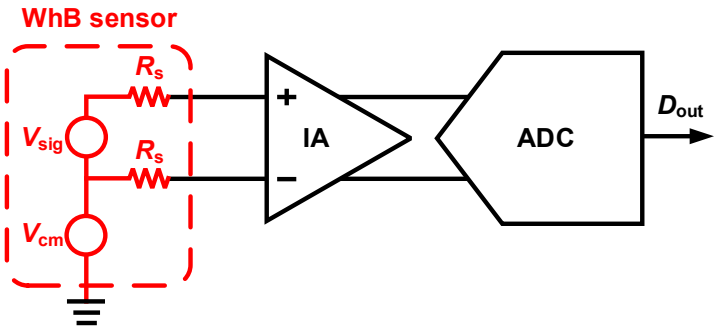

Figure 1.3: Typical ROIC in the bridge sensing system.

Input impedance

As shown in Figure 1.3, the differential source resistance of a bridge sensor is equal to the bridge resistance. Therefore, the input impedance of the ROIC must be much larger than this to avoid signal attenuation.

Linearity

To accurately process the bridge output signal, a ROIC must be more linear than the sensor itself. The typical nonlinearity of a bridge sensor is about several hundred ppm with respect to its full dynamic range [2,15]. This usually results in a trade-off between energy-efficiency and linearity in the design of the ROICs.

Power supply and common-mode variation

To obtain enough sensitivity, the biasing voltage and thus the CM voltage of a bridge sensor will often be two or three orders of magnitude larger than its differential

output signal. The ROIC should have a high power supply rejection ratio (PSRR) as well as high common-mode rejection ratio (CMRR) to cope with the errors caused by the power supply and the common-mode voltage variation.

Energy Efficiency

Another challenge associated with a high bridge bias voltage is a high CM voltage, about half of V_{bias}, which must be handled by the ROICs. This often means that the power supply of the ROICs should be at least higher than the CM level of the WhB sensor [6, 7]. Thus, a high sensitivity with a high bridge biasing voltage usually results in high power dissipation of the ROIC.

Recently, fueled by the proliferation of battery-powered sensing systems, e.g., in mobile and IoT applications, and also, to a lesser extent, the ongoing need to reduce self-heating errors in precision mechatronic systems, considerable efforts have been made to reduce the power dissipation, and therefore, improve the energy efficiency of ROICs, i.e., the amount of energy that they need to achieve a certain input-referred noise level [3-14]. Some of the metrics for evaluating the energy efficiency of IAs and ADCs will be discussed here.

The energy efficiency of IAs in a ROIC is often evaluated by calculating the noise efficiency factor (NEF) [3-14], as given by

$$\mathrm{NEF} = V_{\mathrm{n}} \sqrt{\frac{2I_{\mathrm{tot}}}{\pi \cdot V_{\mathrm{t}} \cdot 4kT \cdot BW}}, \tag{1. 3}$$

where V_{n} is the amplifier's input-referred noise voltage, I_{tot} is the supply current, BW is the bandwidth, and V_{T} is the thermal voltage kT/q. The NEF expresses how an amplifier's noise performance compares to that of a single thermal noise-limited bipolar transistor with the same current consumption [13]. Thus, a smaller NEF corresponds to better energy efficiency. However, since the NEF does not take the IA's supply voltage V_{DD} into account, which is application- and process-dependent, a more accurate metric is the power efficiency factor (PEF), defined as [21]

$$\mathrm{PEF} = \mathrm{NEF}^2 \times V_{\mathrm{DD}}. \tag{1.4}$$

ROICs typically employ high-resolution ADCs for which resolution is thermal-noise limited. For such ADCs, the appropriate metric of energy efficiency is the Schreier figure of merit ($\mathrm{FoM_S}$) [22], which is defined as

$$\mathrm{FoM_S} = DR + 10\log\left(\frac{BW}{Power}\right), \tag{1.5}$$

where *DR* is the ADC dynamic range in dB, *BW* is the ADC's Nyquist bandwidth, and *Power* is the power dissipation. It is often expressed in terms of SNDR, since, in many practical situations, distortion is just as limiting as noise.

It should be noted that the $\mathrm{FoM_S}$ is expressed in terms of relative noise (or distortion) levels. However, ROICs are usually designed to achieve an absolute level of input-referred noise, which should be commensurate with that of the bridge. Furthermore, the IA of a ROIC will typically have a significant gain (> 10), and so will determine its noise performance. As such, when evaluating the energy efficiency of ROICs, the NEF and/or PEF are better metrics than the $\mathrm{FoM_S}$. Thus, in this thesis, we will use both the NEF and PEF as the metrics to quantify and compare the energy efficiency of the ROICs.

State of the Art ROICs

Table 1. 1 gives a survey of precision ROICs up to 2016, which was when this thesis work started. Both stand-alone IAs (3-5) and ROICs [6-9], based on the conventional two-stage architecture, are listed.

Table 1.1 Prior Art of Energy-Efficient Precision Bridge ROIC.

	Stand-alone IA			ROIC			
Reference No.	[3]	[4]	[5]	[6]	[7]	[8]	[9]
Supply voltage (V)	5	1.5	1	5	1.55	3.3	5
Supply current (μA)	230	194	1.8	270	1560**	2000	4300
Input noise density (nV/√Hz)	15	13.5	60	16.2	8.2	6.7	5
DC CMRR (dB)	120	102	136	140	--	--	110
Offset (μV)	5	3.5	1	0.2 *	--	--	1
NEF	8.8	7.2	3.3	10.4	12.5	11.6	12.7
PEF	387.2	77.8	10.9	540.8	242	444	806

* With a system level chopping.
** Only the current consumption of the IA and ADC is considered.

As indicated in Table 1. 1, the IA [5] achieves at best a NEF of 3.3, more than 3× better than the state-of-the-art ROIC [6]. One reason for this energy-efficiency gap between the stand-alone IAs and bridge readouts is that the additional power consumption, noise contribution, and the aliased high-frequency noise of the following ADC stage in the ROICs. However, as discussed earlier, the IA usually determines the noise performance, and thus the energy efficiency, due to its significant gain in the ROIC. This means that there still exist areas for continued development on energy-efficiency. Still, the remaining unbridged gap in the prior art [5,6] indicates its difficulty.

Moreover, owning similar levels of NEF, the PEF of the readout in [7] is about 3× better than that of [9] due to its 3× lower power supplies. However, this also indicates that, compared to [9], the maximum bridge bias voltage is at least 3× lower. However, the bridge sensors' sensitivity is proportional to its biasing voltage.

To conclude, the design of a ROIC with high energy-efficiency, high precision, and high stability is quite challenging.

1.3 Targeted Sensing Application

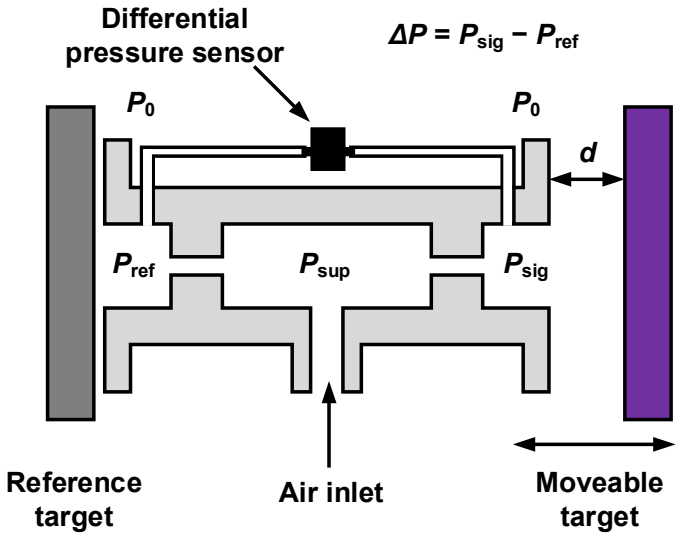

Figure 1.4: Air gauge for precision distance measurement.

The targeted application of this thesis is the readout of a differential pressure sensing system intended for precision distance measurements in low-vacuum environments such as wafer steppers [23]. Known as air gauges, such systems are promising for precision distance measurement due to their high sensitivity and accuracy and the fact that, unlike capacitive or eddy-current sensors, they do not require a conductive target.

The operating principle of a precision air gauge is shown in Figure 1.4. Air flows into an inlet and is distributed between two nozzles, symmetrically located on each side of the inlet. The reference pressure, P_{ref}, then depends on the distance between the

left nozzle and the reference target, while the signal pressure, P_{sig}, depends on the distance d between the right nozzle and the moveable target. This distance can then be accurately determined by measuring the pressure difference ΔP with a differential pressure sensor. By optimizing the pneumatic gain factor of the air gauge, pm-resolution can be achieved [23]. However, this requires both a precision differential pressure sensor and a precision ROIC.

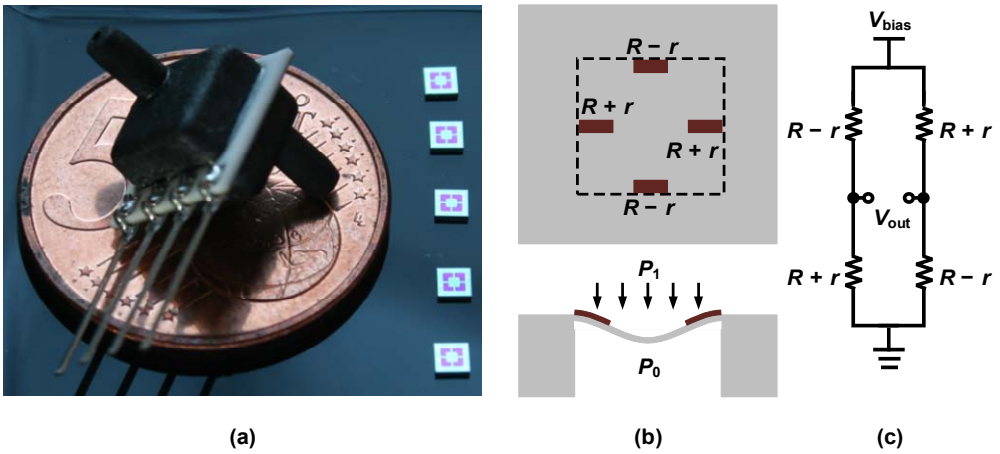

Figure 1.5: MEMS piezoresistive differential pressure sensor (a); piezoresistors that can be used in a full Wheatstone bridge configuration (b); its equivalent circuits (c).

Due to their high resolution, piezoresistive differential pressure sensors are well suited for such applications. To maximize their resolution, such sensors usually employ a full Wheatstone bridge configuration (AC40110 in Figure 1.5) [15]. However, such sensors are also strongly temperature dependent, which often limits their stability. This is exacerbated by the fact that in the near vacuum conditions at which an air gauge works, only limited cooling capability is available. On the other hand, the sensor needs a certain biasing voltage, and thus a certain energy dissipation, to achieve the target resolution. This restricts the energy budget for the ROIC, which is typically located close to the sensor to minimize the possibility of interference pickup.

To enable distance measurements with a pm-level precision, a resolution of 10 mPa (rms) over 1 kHz bandwidth. The biasing voltage of AC4010 should be at least 5 V, thus resulting in a sensitivity of about 45 μV/Pa. To guarantee that the ROIC does

not limit the sensor's performance, it should be designed to meet the specifications in Table 1.2.

Table 1.2. Target Specifications of the ROIC.

Specifications	Value
Input noise density	4 nV/√Hz (~ 1 kΩ)
Signal bandwidth	1 kHz
Input CM level	2.5 V
Input range	± 100 mV (offset), ±10 mV (signal)
Gain	≈ 100
Input impedance	> 370 kΩ (for < 0.1% gain error)
Offset drift	< 10 µ/°C
Power dissapation	< 6.8 mW
INL	< 50 ppm

Besides the general requirements, as discussed in 1.2, two more challenges need to be met by the ROIC: 1) the biasing voltage is 2× higher than the normal power supply of a modern CMOS technology, such as TSMC180nm and TSMC130nm. This limits the energy efficiency of a conventional ROIC, since its input stage should be able to handle the high input CM level. 2) the small bridge signal (about ± 5 mV) will be superimposed on a bridge offset of about 100 mV, due to the mismatch of its piezo-resistive elements (nominally 3.7 kΩ each). This offset often varies with biasing voltage and temperature, and therefore, needs to be stably compensated.

1.4 Main question and methodology

This thesis describes the design and development of ROIC intended for differential pressure sensor in precision mechatronic systems. The main research question is: how this can be done with high energy-efficiency, high precision, and high stability?

In order to answer this question, the following approach was taken. Different bridge readout architectures were reviewed and studied to evaluate their potential regarding energy-efficiency, precision, and stability. The review and evaluation helped to determine the most promising bridge readout architectures with the least amount of noise sources, and thus better energy-efficiency. To further improve energy-

efficiency while enhancing the stability of the ROIC, chopping was applied in noise-critical blocks to reduce the effects of 1/*f* noise and offset. However, chopping is known to cause undesired drawbacks such as decreased input impedance and increased in-band noise [17-19]. With the chosen readout architectures, techniques are proposed to minimize such drawbacks. Two designs based on a standard CMOS technology are evaluated through analysis, simulations, and measurements to demonstrate the effectiveness of the proposed techniques.

1.5 Dissertation Organization

The remainder of this dissertation has been divided into six chapters (Figure 1.6).

Chapter 2 presents a review of energy-efficient ROICs, with the aim of discussing architectural and circuit-level innovations that have advanced the state-of-the-art.

Precision techniques are the key to achieving energy-efficiency as well as stability by reducing in-band 1/*f* noise and offset. However, special care must be taken to address the relevant problems resulting from such techniques in precision applications, as they introduce some secondary effects which might be critical for ROICs. Chapter 3 discusses these problems and proposes solutions.

Chapter 4 describes the architecture, circuit realization, and experimental characterization of a ROIC utilizing conventional bridge readout topology, which consists of a precision IA followed by a high-resolution ADC, with proposed techniques, achieving the state-of-the-art energy efficiency with preserved precision and stability.

Chapter 5 presents a bridge to digital converter which directly digitizes the output of the bridge sensor. Measurement results show that the resulting design achieves state-of-the-art energy efficiency and linearity.

Chapter 6 presents a pressure sensing system built with the ROIC and a differential pressure sensor (AC4010), which achieves 10.1 mPa (1σ) resolution within a 0.5 ms conversion time. The ROIC dissipates about 30% of the power dissipation in the system and contributes about 6% of the noise power.

Chapter 7 concludes this dissertation and provides an outlook for future work.

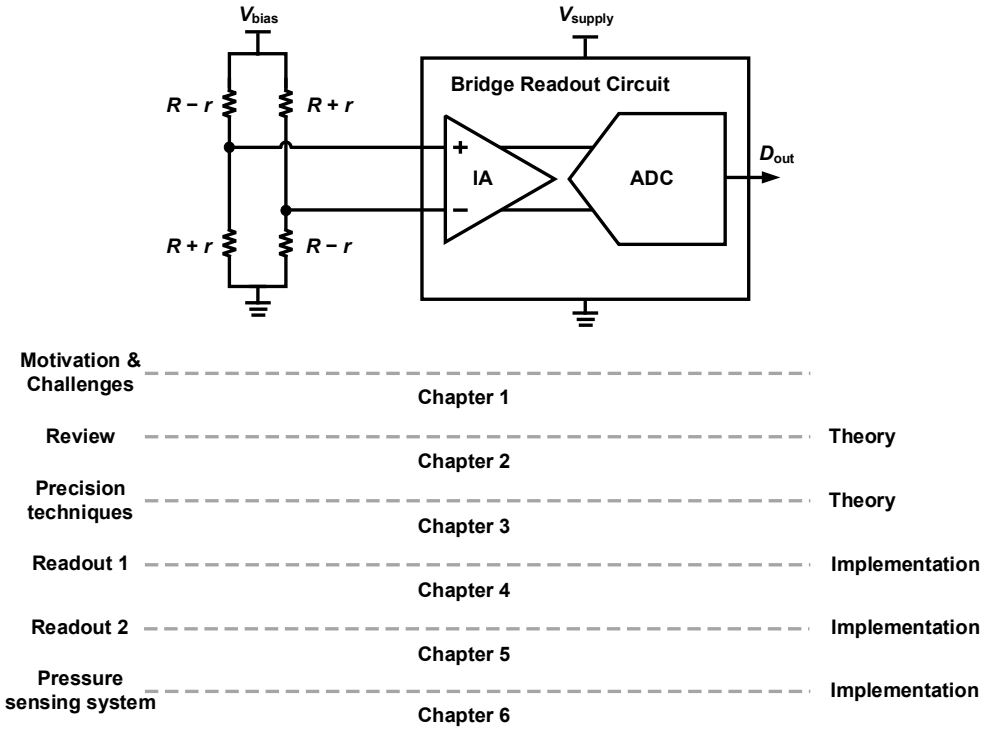

Figure 1.6: Organization of the thesis.

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Energy-Efficient ROICs: A Review

Energy efficiency defines the degree to which a certain performance level can be achieved while consuming minimum energy, within defined operating conditions. In this chapter an overview of energy efficient ROICs will be presented, allowing for a better understanding of the existing design trade-offs. These ROIC designs [1-4] must achieve low input-referred offset, drift, and noise; high gain accuracy, stability, and linearity; as well as high immunity to power-supply and common-mode variations, with the lowest possible energy consumption.

As shown in Figure 2.1a, a conventional ROIC consists of an instrumentation amplifier (IA) followed by an analog-to-digital converter (ADC). The IA boosts the amplitude of the bridge output to levels that are large enough to drive the succeeding ADC. Being the first stage, the IA defines the ROIC's input characteristics and in particular, its input-referred noise, which in turn usually determine its energy efficiency. Therefore, much effort has been devoted to improving the energy efficiency of IAs. The number of high-gain amplifiers required has been reduced from three, as in the classic three opamp IA [1], to one, as in the more recent capacitively-coupled IA (CCIA) [3-5]. Furthermore, chopping has been widely applied to suppress in-band 1/*f* noise [1-8].

This chapter is derived from a conference publication of the authors: H. Jiang and K. A. A. Makinwa, "Energy-efficient bridge-to-digital converters," 2018 IEEE Custom Integrated Circuits Conference (CICC), San Diego, CA, 2018.

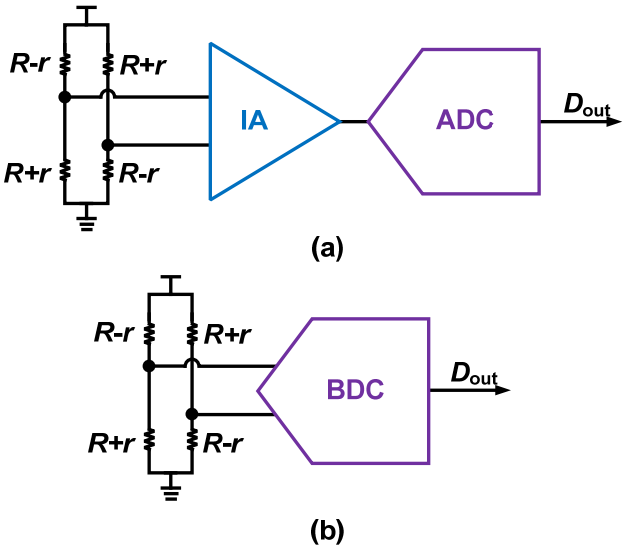

Figure 2.1: Conventional ROICs (a); Direct digital ROICs (b).

Recently, ROICs that eliminate the IA entirely have been proposed [9-15] (Figure 2.1b). The motivation behind those direct ROICs is to eliminate the associated high-gain amplifiers, thus reducing both design complexity and area. To avoid the aliasing and kT/C noise issues of discrete-time ADCs, direct ROICs usually consist of a high-resolution continuous-time (CT) ADC. Then in order to achieve good gain accuracy and stability, as well as low input-referred offset, drift and noise, dynamic compensation techniques such as chopping and dynamic element matching (DEM) are often employed [16].

With the aim of discussing architectural and circuit-level innovations that have advanced the state-of-the-art, this chapter is organized as follows. Some general design considerations to improve ROICs' energy-efficiency in Section 2.2. Section 2.3 discusses the energy efficiency of conventional ROICs while some recent direct digital ROICs are discussed in Section 2.4. Comparisons of state-of-the-art ROICs are given in Section 2.5. Finally, some conclusions are drawn.

2.1 Design Considerations for Energy Efficiency

An IA boosts the amplitude of the bridge output to levels that are large enough to drive the succeeding ADC. Being the first stage, the IA defines the ROIC's input

characteristics and in particular, its input-referred noise, and in turn will usually determine its energy efficiency. Similarly, in terms of energy efficiency, the most critical block of an IA is usually its input stage. This stage will usually have a significant gain, and thus will minimize the noise contribution of succeeding stages.

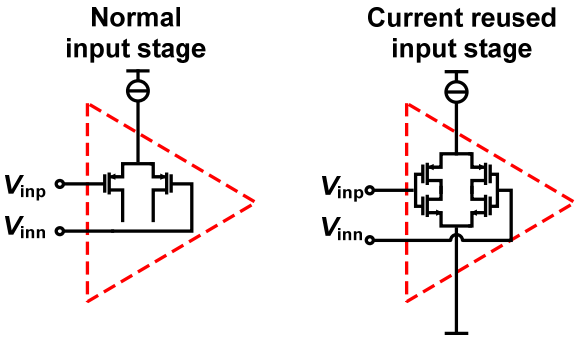

Figure 2.2: Conventional input stage and current-reuse input stage.

As shown in Figure 2.2, current-reuse input stages are more efficient than conventional input stages since they provide roughly double the transconductance for the same supply current [21]. This comes at the expense of less output swing. However, this is usually not a significant drawback in ROICs, since their IAs employ multi-stage topologies for a high open-loop gain and thus high closed-loop gain accuracy [6].

The number of noise-critical input stages in an IA depends on the chosen architecture. For example, the classic 3-Opamp IA [1] and the current feedback IA (CFIA) [2], have two, while the CCIA [3-5] only has one (Figure 2.3). As a result, CCIAs are in general more energy-efficient than either 3-Opamp IAs or CFIAs.

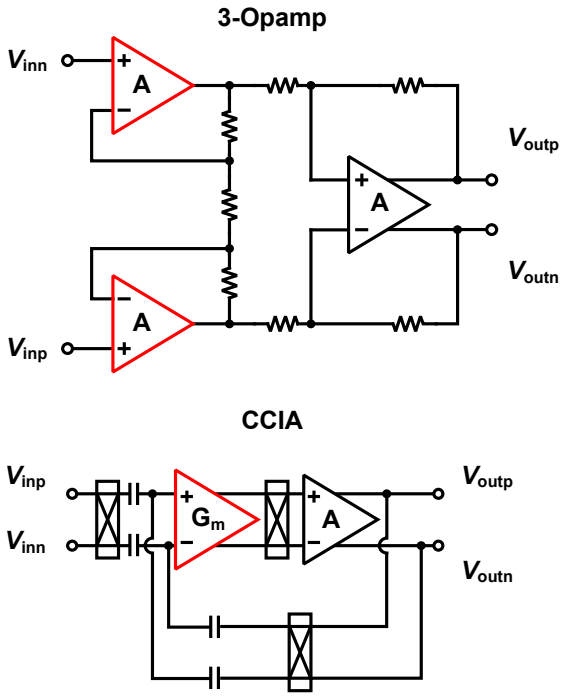

Figure 2.3: Classic 3-Opamp IA and CCIA where noise-critical stages are indicated in red.

However, CCIAs are usually configured as inverting amplifiers, and so their noise gain will be higher than their signal gain, thus degrading their energy efficiency. From Figure 2.4, the signal gain, G_{CCIA}, and the noise gain, NG, of a CCIA can be calculated as follows

$$G_{CCIA} = -\frac{C_{in}}{C_{fb}}, \tag{2. 1}$$

$$NG = -\frac{C_{in} + C_p + C_{fb}}{C_{fb}}, \tag{2. 2}$$

where C_{fb} is the feedback capacitance, C_p is the parasitic capacitance of the input stage and V_n is its input noise. Compared to the input signal V_{in}, the input-referred noise will be amplified by a noise factor, F, which is given by:

$$F = \frac{G_{CCIA}}{NG} = \frac{C_{in} + C_p + C_{fb}}{C_{in}}, \tag{2. 3}$$

For $G_{CCIA} > 10$, C_{in} will be much larger than both C_p and C_{fb}, which means that $F \sim 1$. However, if large input devices are required, e.g. in low-noise applications, C_p may be quite large, thus increasing F and reducing energy efficiency [5].

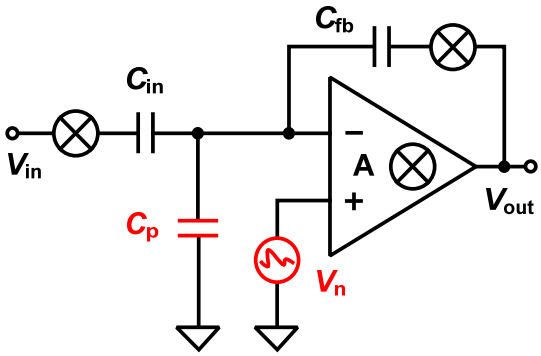

Figure 2.4: Noise analysis of a CCIA.

By definition, $F = 1$ for open-loop amplifiers, meaning they achieve the highest energy efficiencies. However, this comes at the cost of reduced gain accuracy, linearity and stability, making them unsuitable for ROIC applications. In general, improving the energy efficiency of IAs involves reducing the number of noise-critical stages and reducing the effect of feedback and parasitic impedances on the noise factor F, while taking care to preserve other key ROIC specifications.

2.2 Conventional ROICs

A traditional 3-Opamp IA can provide a well-defined gain and high input impedance [1]. However, its energy efficiency is relatively poor because the input stage consists of two high-gain opamps. Moreover, its CM input level is restricted by the output voltage range, making it difficult to sense CM levels close to the supply rails. In ROIC applications, this limits the maximum value of V_{bias}, and, in turn, limits bridge sensitivity. Both CFIAs and CCIAs are much better in this regard.

2.2.1 CFIA-based ROICs

In a CFIA (Figure 2.5), the input and feedback voltages are first converted into currents by transconductors G_{min} and G_{mfb}, respectively. Their difference is then nulled by the overall gain of the amplifier. The voltage gain of the IA can then be expressed in terms of its feedback resistors R_1 and R_2 as

$$A_{Gain} = \frac{G_{min}}{G_{mfb}} \times \frac{R_1 + R_2}{R_2}. \quad (2.4)$$

A CFIA has a higher CMRR and input impedance than a 3-Opamp IA. Its CMRR is mainly determined by the CMRR of G_{mfb} and can often exceed 120 dB [2]. It is also capable of handling input CM voltage that include either of the supply rails [22]. It is also more energy-efficient, since both input stages share a single output stage

The main disadvantage of the CFIA is its limited gain accuracy. Even with precision feedback resistors, this will be limited by the matching of G_{min} and G_{mfb}, which will vary over PVT, as well as in terms of CM voltage, and is limited to about 0.5% [2].

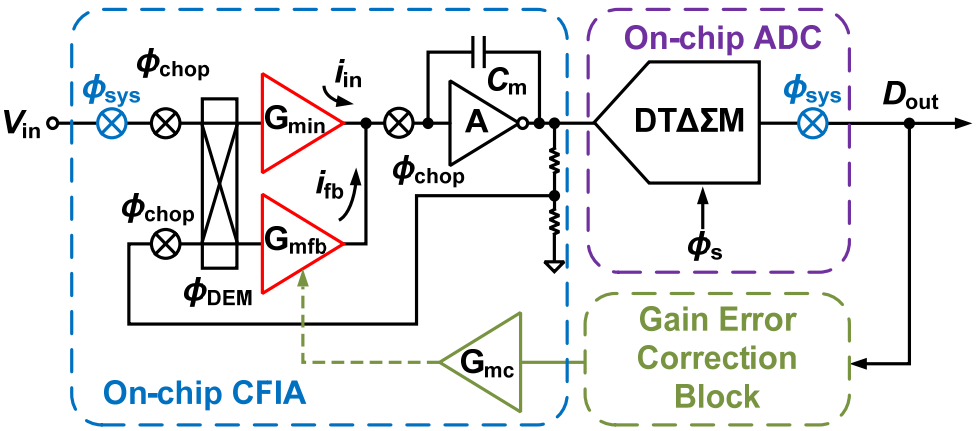

Figure 2.5: ROIC based on a CFIA with a DTADC.

As shown in Figure 2.5, the gain accuracy of a CFIA can be improved with dynamic element matching (DEM) and digitally assisted gain error-correction [2,8]. In this

way, the mismatch between G_{min} and G_{mfb} is averaged out and the CM-dependent gain errors are minimized. In [2], such a CFIA is followed by a SC incremental delta-sigma (ΔΣ) ADC, resulting in 5 ppm INL and a 0.7 ppm/°C gain drift, resulting the best reported NEF for a CFIA-based ROIC, which is about 10.4.

2.2.2 CCIA-based ROICs

As discussed in 2.3, CCIAs are usually more energy-efficient than 3-Opamp IAs and CFIAs [1,2,8,22]. Furthermore, their input capacitors naturally block CM voltage, allowing them to have CM voltage ranges that exceed their own supply rails [5]. Moreover, the gain of a CCIA is set by a ratio of capacitors, rather than resistors, making it usually more stable and accurate.

The main drawback of the CCIA is its limited input impedance. This is because its input capacitances C_{in} are periodically charged/discharged by the chopped input voltage $\pm V_{in}$. The resulting input impedance Z_{in} is proportional to $1/f_{chop}C_{in}$, where f_{chop} is the chopping frequency. Z_{in} is typically in the order of a few mega-Ohms [6], which is somewhat low for a ROIC.

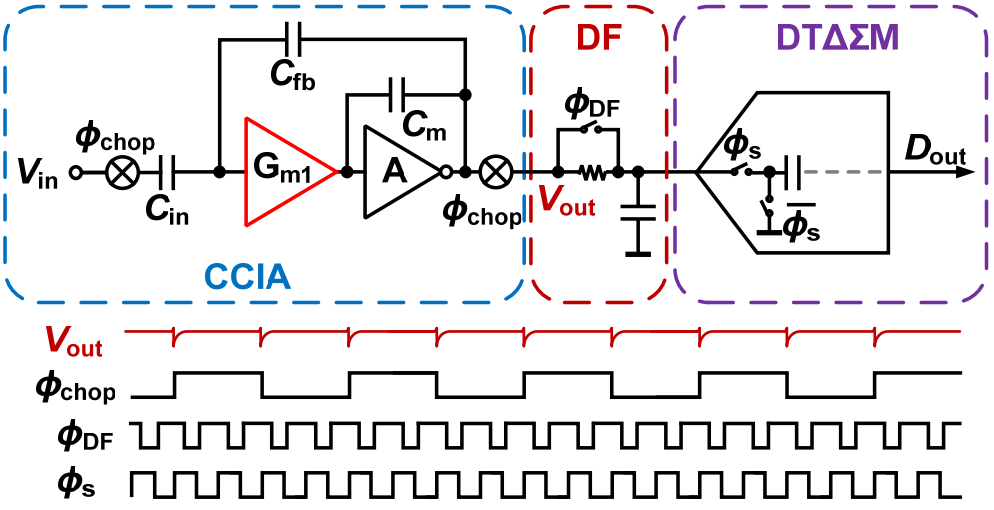

Figure 2.6: ROIC based on a CCIA with a DTADC using a dynamic filter.

Boosting a CCIA's input impedance involves finding ways to ensure that the currents required to charge/discharge C_{in} are not drawn from the input signal V_{in}. In

[5], this is achieved by a capacitively-coupled positive feedback loop, which is driven by the output of the CCIA. In [3], an auxiliary pre-charge buffer is used. The latter solution requires active blocks which cannot operate beyond the supply rails, thus limiting the CCIA's CM input range.

Another drawback of CCIAs is that they generate output spikes at $2f_{chop}$. These are caused by the finite slew rate of their output stages, which cannot instantaneously generate the chopped output voltage $\pm V_{out}$ dictated by the feedback loop and the choppers [5].

To avoid introducing extra offset and non-linearity, the output spikes of a CCIA should not be digitized. In a discrete-time ADC, this can be readily achieved by sampling the output of the CCIA just before the chopping transitions [4,5]. However, the CCIA's bandwidth then needs to be wide enough to ensure complete settling, which leads to an increase in noise aliasing. Furthermore, the ADC's sampling frequency fs is now the same as $2f_{chop}$, which limits design flexibility. In [3], a dynamic filter (DF) is used to limit the noise bandwidth while maintaining the settling accuracy (Figure 2.6). The resulting IA achieves a NEF of 6.4.

2.2.3 Open-loop VCO-based ROICs

Recently, VCO-based ROICs have been proposed. As shown in Figure 2.7, these consist of an input transconductor, G_{min}, whose output current drives a pair of current-controlled oscillators, CCO1,2, whose output phase can then be sampled and differentiated to realize a first-order sigma-delta modulator [23]. The open-loop input Gm stage confers a high input impedance and energy efficiency. In [7], a NEF of 4.6 is achieved with a simple and compact design.

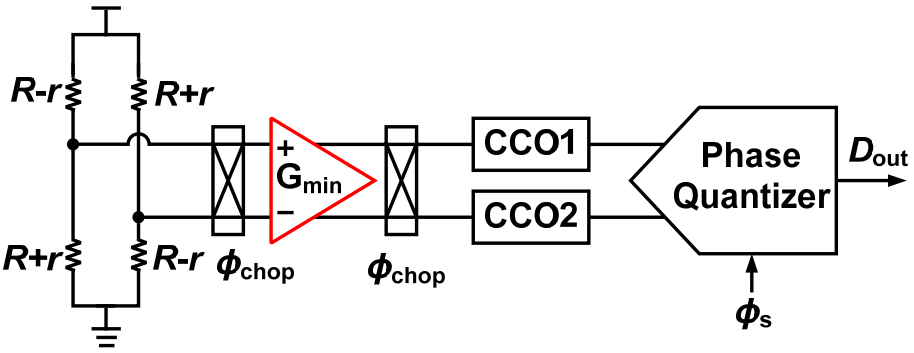

Figure 2.7: Open-loop VCO-based ROIC.

However, the use of an open-loop Gm stage also results in poor gain accuracy and non-linearity (INL of 348 ppm). Moreover, CCO mismatch results in a residual offset of about 50 μV, which is quite large for a ROIC [7].

2.3 Direct digital ROICs

A conventional ROIC requires two feedback loops: one around the IA and the other around the ΔΣ ADC. Each loop should have enough gain to obtain high linearity, which typically requires at least two high gain amplifiers, thus increasing complexity and area. Moreover, the overall gain of the ROIC is defined by at least two resistor/capacitor ratios [1-4], making it twice as hard to achieve sufficient gain accuracy. To address these issues, a number of direct ROIC architectures have been proposed, in which the IA and ADC have been embedded in a single feedback loop.

2.3.1 Closed-loop CFIA-like ROICs

In [9], a CFIA and an ADC are embedded in the feedback loop of a single sigma-delta modulator. The result is shown in Figure 2.8. Matched transconductors (G_{min} and G_{mfb}) are used in both the signal and feedback paths, giving the modulator the high input impedance and CMRR of a CFIA. To accommodate the limited input range of the G_{mfb}, however, the high-amplitude quantization noise generated by the 1-bit digital-to-analog converter (DAC) is first filtered by a second-order RC filter. This in turn requires an extra feedback path to compensate for the extra delay in the feedback path. Compared to a conventional CFIA-based ROIC with a similar

performance [8], the design in [10] requires less area, but achieves a somewhat worse NEF of 12. To save more area, the combination of the 1-bit DAC and an analog filter could be replaced by a FIR filter [24].

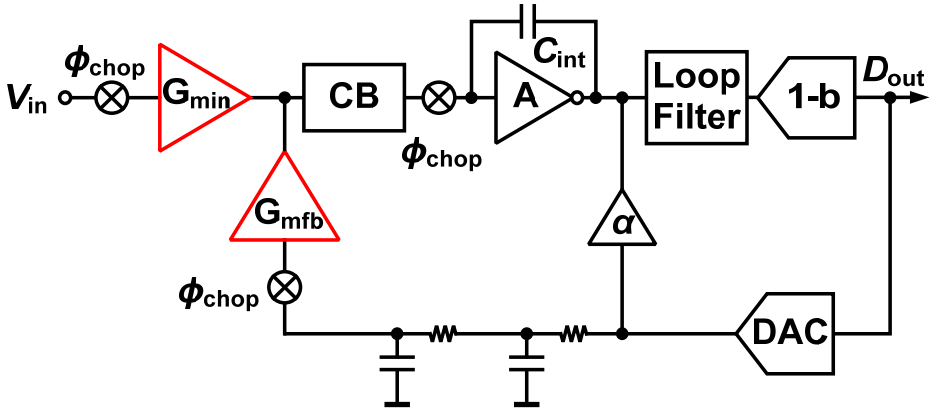

Figure 2.8: Closed-loop CFIA-like ROIC: Gm-C CTΔΣM.

2.3.2 Closed-loop CCIA-like ROICs

A CCIA and an ADC can also be merged into a single sigma-delta modulator by embedding them in a CCIA-like capacitively-coupled feedback loop [25]. Like a CCIA, the resulting ROIC has only a single noise-critical stage and so should inherit both the energy efficiency, as well as input characteristics: a wide input CM range, high gain accuracy, but only moderate input impedance. The latter can be boosted with the same techniques used for CCIAs [3,5]. As in a closed-loop CFIA-like ROIC, however, measures must be taken to ensure that the quantization noise feedback from the modulator DAC does not overload the input stage.

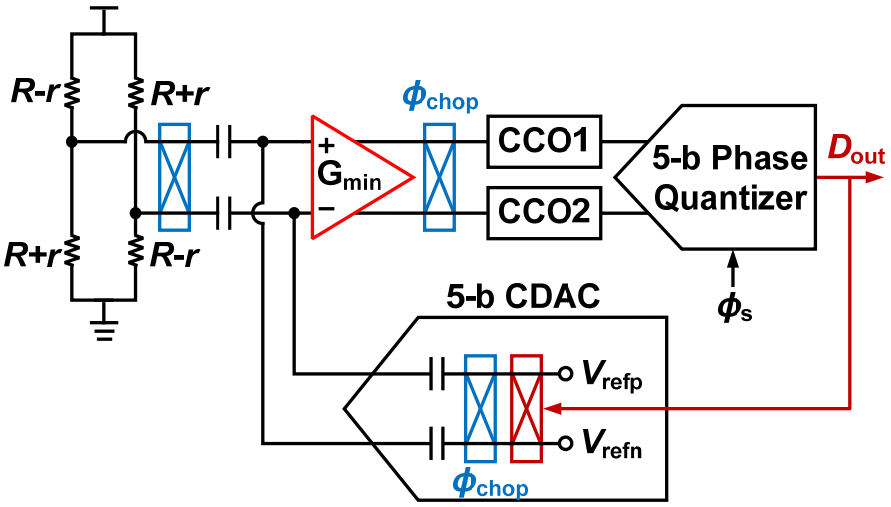

Figure 2.9: Closed-loop CCIA-like ROIC: Closed-loop VCO.

As shown in Figure 2.9, a VCO-based ADC is embedded in a chopped and capacitively coupled feedback loop [13]. A 5-bit DAC is used to ensure that the feedback quantization noise does not overload the input transconductor. Compared to the open-loop VCO-based ROIC in [7], it achieves better linearity and a (10×) larger input range. However, it only achieves a NEF of 22.6, probably due to the non-idealities of its capacitive DAC such as charge injection and non-linearity. Although not intended for ROIC, the design in [26] embeds a Gm-C integrator and a 5-bit SAR into a similar feedback loop. Compared to [13], it achieves better energy efficiency (a NEF of 7.8) but with worse linearity performance.

2.3.3 Current-mode ROICs

Instead of reading out the open-circuit output voltage of a Wheatstone bridge, another approach is to read out its short-circuit output current. One example of this is a current-mode approach. As shown in Figure 2.10, a resistive DAC is used to balance the output of the bridge, thus nulling its short-circuit output current. Balancing the bridge also maximizes its immunity to variations in V_{bias} [14]. In [15], a Wheatstone bridge made from resistors with opposite temperature coefficients was used to realize a CMOS temperature sensor. The bridge is read out by connecting it to the virtual ground formed by the 1st integrator of a CTΔΣM. In the ratiometric

case, i.e. when $V_{refp} = V_{bias}$ and V_{refn} = GND, the modulator's bitstream average μ is given by:

$$\mu = \frac{2r}{R^2 - r^2} R_f . \tag{2. 5}$$

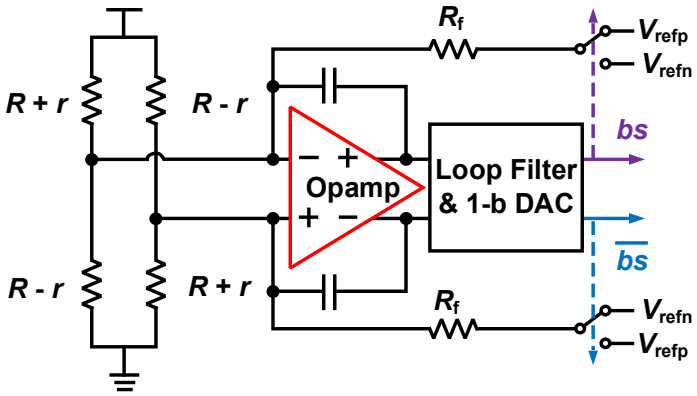

Figure 2.10: Current-mode ROIC.

In [15], the energy efficiency of the CTΔΣM could have been improved by using a more efficient Opamp to realize the 1st integrator. This can be done by using low-noise components [27] or by chopping the Opamp. However, as will be discussed in Chapter 3, special care should then be taken when chopping is implemented in a CTΔΣM.

2.4 Comparison

Table 2.1 State-of-the-Art ROICs.

	[2]	[3]	[4]	[7]	[10]	[13]	[15]
Input stage	PMOS	NMOS	PMOS	PMOS	PMOS	PMOS	PMOS
Technology	0.7 µm	0.18 µm	0.13 µm	40 nm	0.7 µm	40 nm	0.18 µm
Area (mm2)	6	0.531	0.88	0.0145	3	0.06	0.43
Supply voltage (V)	5	3.3	3	1.2	5	1.2	1.5
Supply current (mA)	0.27	0.075[1]	0.326	0.015	0.24	0.0175	0.0355
±Input range (mV)	40	20	--	4	40	50	--
DC CMRR (dB)	140	109	124	91	120	--	--
CM input range (V)	0–2.5	0–3	--	0.15–0.65	0–2.5	--	0.75
INL (ppm)	5	5	--	288[2]	15	79[2]	--
Offset (µV)	0.05	1.8	2.4	50	1	300	--
Input noise density (nV/√Hz)	16.2	19	16	32	20	140	247[3]
NEF	10.4	6.4[1]	11.1	4.8	12	22.6	72[3]

1. Without taking into account the ADC. 2. Estimated from THD. 3. Estimated value.

The performance of some selected ROICs is summarized in Table I. Note that none of them use a current-reuse input stage, and so the differences in their energy efficiency are mainly due to architectural differences.

In general, conventional ROICs achieve better energy efficiency than direct ROICs as well as better accuracy and stability [1,3]. This is because their input stages can be

optimized for efficient and accurate amplification of small DC signals. Although the open-loop VCO-based ROIC demonstrates good technology scalability and state-of-the-art energy efficiency, it suffers from poor gain accuracy and linearity [7]. Direct ROICs are usually simpler and more compact than their conventional counterparts [10,13,15]. However, preserving this advantage, while achieving a competitive trade-off between energy efficiency and other important specifications, remains an unresolved problem.

As discussed in Section 2.2, reducing the number of input stages is one way to improve energy efficiency. For example, although the input stages of [2] and [3] both employ the folded-cascode topology, the CFIA [2] requires two input stages, while the CCIA [3] only requires one. This results in a NEF difference of about 2×.

The noise factor also plays an important role in the energy efficiency of the ROICs. In Table I, the best NEF is achieved with an open-loop design ($F = 1$) [7], while the efficiency of [13], and the closed-loop design of [7], are degraded due to a poor noise factor.

The efficiency of the current-mode ROIC could be improved by using a low $1/f$ noise Opamp at the 1st integrator [15].

Among the selected ROICs, the CCIA-based designs achieve a well-balanced performance in terms of energy efficiency, accuracy, and stability. However, as shown in [4], digitizing the CCIA output signal using $2f_{chop}$ degrades the overall energy efficiency performance of the ROIC. Therefore, efforts must be made to avoid digitizing the CCIA's output spikes and limiting the CCIA's noise bandwidth [3].

2.5 Conclusion

This chapter has presented an overview of several recently developed ROICs that target high energy efficiency, including conventional ROICs which consist of an IA followed by an ADC, as well as direct ROICs which do not have an IA. Among the selected ROICs, the CCIA-based designs [12] achieve a well-balanced performance in terms of energy efficiency, accuracy, and stability. However, to achieve this, efforts must be made to avoid digitizing the CCIA's output spikes. Moreover, the CCIA's input impedance needs to be boosted to properly amplify the bridge signal. Alternatively, the current-mode ROIC could be as energy-efficient as the CCIA-based ROIC without the shortcoming of the CCIA's spikes. However, its precision relies on the DAC resistor, which is hard to stabilize when implemented on an ASIC.

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Chopping in ROICs

Semiconductor devices (especially CMOS transistors) suffer from 1/*f* noise at low frequencies, which is usually within the signal band of bridge sensors. As indicated in Eq. 1.3, this will then degrade the energy efficiency of their ROICs. Moreover, offset and drift will also degrade readout stability. To reduce in-band 1/*f* noise offset and offset drift of the amplifiers, chopping is often applied [1-3]. However, several secondary effects of chopping need to be considered in precision applications, such as reduced bandwidth, output impedance, and input impedance. Moreover, although chopping has been successfully implemented in instrumentation amplifiers and discrete-time ΔΣMs (DTΔΣMs) [1-4], it is known to cause undesirable artefacts when used in continuous-time ΔΣMs (CTΔΣMs) [5-6], namely the fold-back of quantization noise to the signal band.

In this chapter, the use of chopping in ROICs is analysed. Some solutions, which are used in the designs presented in chapter 4 and chapter 5, for preventing quantization noise fold-back in chopped CTΔΣMs are proposed. The rest of the chapter is organized as follows. The principle and secondary effects of chopping are briefly reviewed in Section 3.2. In Section 3.3 an analysis of chopping-related errors in CT-

This chapter is derived from a conference publication of the authors: H. Jiang, B. Gönen, K. A. A. Makinwa and S. Nihitanov, "Chopping in continuous-time sigma-delta modulators," 2017 IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, MD, 2017.

ΔΣMs is made, and previous solutions from the literature are discussed. In Section 3.4 two novel chopping methods based on modified DAC pulse shapes (return-to-zero and exponentially decaying) are proposed. Simulation results showing the effectiveness of the proposed methods are given in Section 3.5. Conclusions are drawn in Section 3.6.

3.1 Chopping in an Amplifier

Chopping is a widely used amplitude modulation technique [8]. Figure 3.1 describes its working principle when it is used in an amplifier with resistive feedback. The input signal V_{in} is modulated by CH_{in} to the chopping frequency, f_{chop}, before being amplified so as to be separated from the $1/f$ noise of the amplifier in the frequency domain. After being processed by Gm, the input signal is modulated back to the signal band by CH_{out}, while the $1/f$ noise is up-modulated to f_{chop} and filtered out by the following low-pass filter, resulting in improved in-band noise performance. Typically, the switches of the chopper can be implemented by using CMOS transistors, therefore, the additional power consumption along with the chopping technique is often negligible. In this way, the energy-efficiency of the amplifier can be greatly improved.

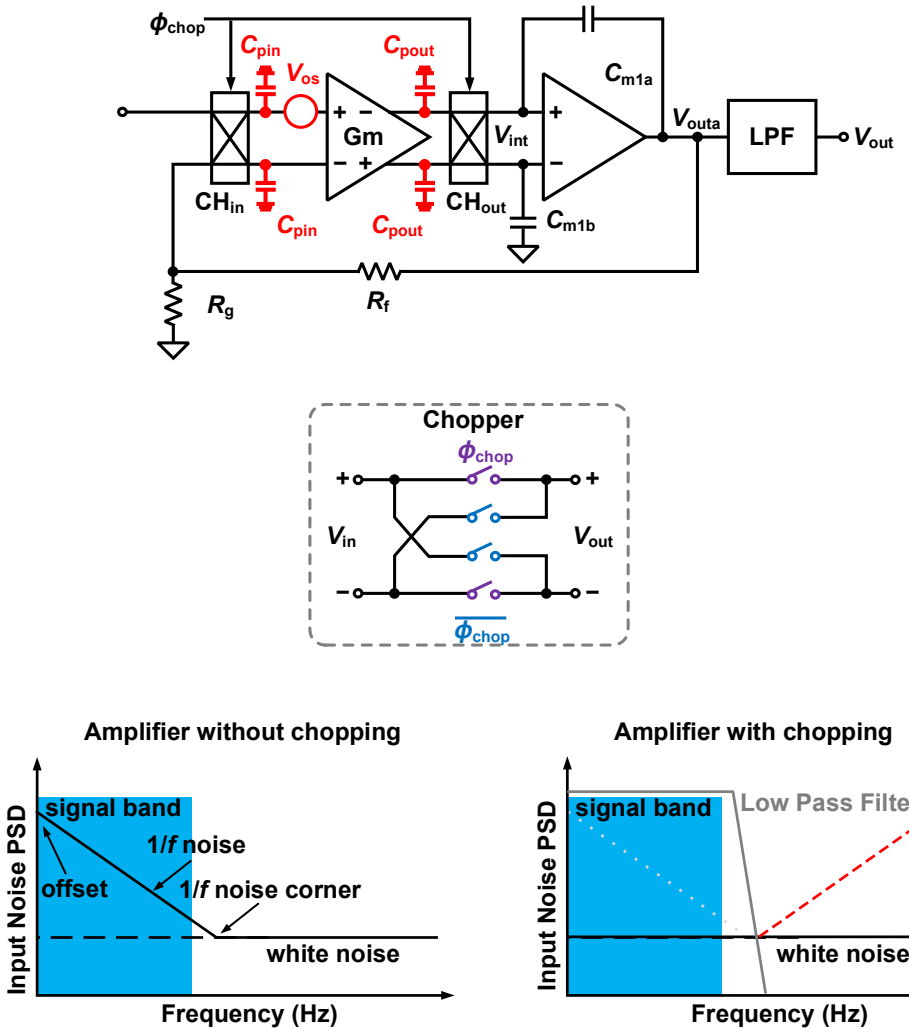

Figure 3.1: Chopped amplifier in a closed-loop.

However, in practical chopped amplifiers, several issues must be considered. These have been well explained in [8-11].

Reduced Bandwidth

The chopping frequency f_{chop} should be at least 2 times higher than the signal bandwidth. To prevent the tail of the $1/f$ noise from appearing in the signal band, f_{chop} should be chosen such that the highest frequency component of the signal ends

up above the 1/*f* corner after being up-converted by the input chopper. In order to process the chopped V_{in}, the Gm stage needs a higher bandwidth compared to the un-chopped ones for a given signal bandwidth. Therefore, for a given input Gm stage, compared to the un-chopped amplifier, the chopped one has a reduced bandwidth for the input signal.

Reduced Input Impedance

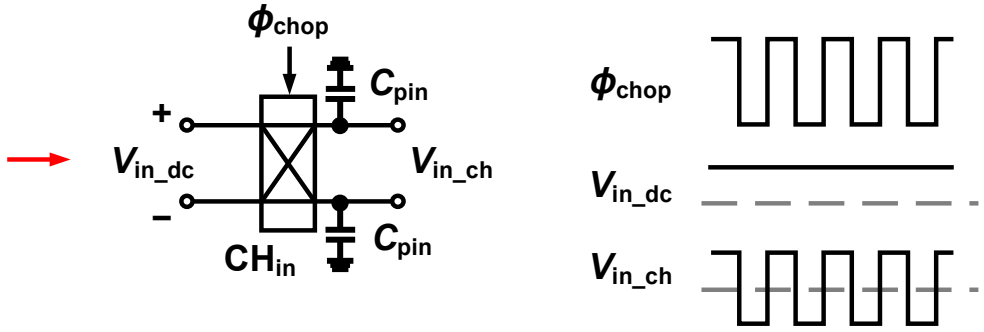

Figure 3.2: Reduced input impedance due to chopping.

The gates of the CMOS transistors are known to have ultra-low input current, and thus high input impedance. However, when chopping is applied to the input of CMOS amplifiers, the input impedance is reduced. As shown in Figure 3.2, this is because the input capacitors of the input transistors, C_{pin}, need to be charged and discharged periodically. This results in input current at the input of the chopped amplifier, leading to a reduced input impedance Z_{in}, given by [9]

$$Z_{in} = \frac{1}{2 f_{chop} C_{pin}}. \tag{3. 1}$$

Reduced Output Impedance

Similarly, as shown in Figure 3.3, since the output parasitic capacitors need to be charged and discharged at every chopping event, the output impedance of the Gm stage is

$$Z_{out} = \frac{1}{2 f_{chop} C_{pout}}. \tag{3.2}$$

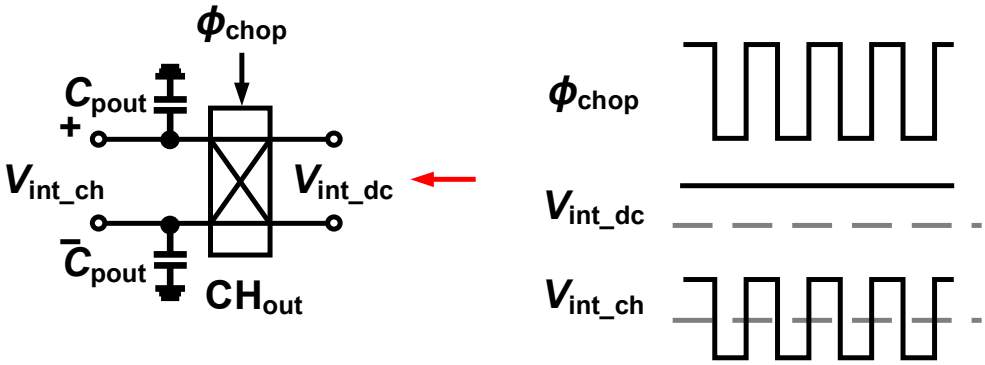

Figure 3.3: Reduced output impedance due to chopping.

Thus, the overall open loop gain of the amplifier is reduced when with a high f_{chop} and large C_{pout}.

3.2 Chopping in a CTΔΣM

CTΔΣMs are attractive for ROICs due to their greater energy efficiency and explicit anti-aliasing behavior compared to their discrete-time counterparts. In ROICs, when the gain of the IA is not high enough to suppress the 1/*f* noise of the CTΔΣM, chopping can also be applied in the CTΔΣM. However, special care must then be taken to deal with possible quantization noise fold-back.

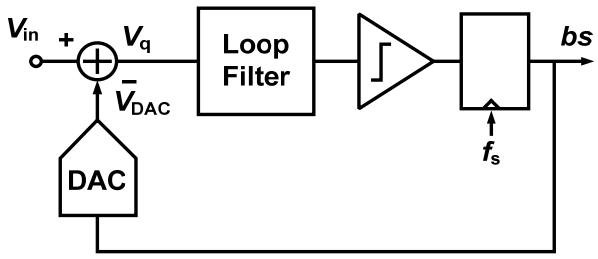

Figure 3.4: Block diagram of a 1-bit CTΔΣM.

Figure 3.4 depicts the block diagram of a 1-bit CTΔΣM. The input signal V_{in} is assumed to be band-limited, and the signal bandwidth is assumed to be much lower than the sampling frequency, f_s. The DAC signal V_{DAC} is a discrete-time signal sampled at f_s with an arbitrary pulse shape. For our analysis, the pulse shape assumed is rectangular (zero-order-hold).

The performance degradation caused by chopping can be attributed to the parasitic sampling of the quantization noise, V_q, present at the input of the loop filter [12, 13]. If this occurs at a frequency which causes aliasing ($|f|<|f_s|$), high-frequency quantization noise may fold-back into the signal band, as will be explained next. Figure 3.4 shows the simplified schematic of a CTΔΣM with a chopped first integrator and a 1-bit resistive DAC, together with its timing diagram. In an OTA-RC integrator, there will be a finite signal swing at its virtual ground "a", which is given by

$$V_a \cong \frac{V_q}{1+g_m \cdot R}, \tag{3. 3}$$

where R is the value of the parallel combination of the input and DAC resistors, and g_m is the transconductance of the OTA. As shown in Figure 3.5, bs (= ±1) is the digital bitstream. V_b is the chopped version of V_a, such that

$$V_b = V_a \cdot \phi_{chop}, \tag{3. 4}$$

where ϕ_{chop} (= ±1) is a square wave with a period of T_{chop} and a 50% duty cycle. When ϕ_{chop} changes state at half periods (1 → -1 or 1 → -1), V_b changes polarity, causing current spikes, I_{bp} and I_{bn}, as the parasitic capacitors C_{p1} at the input of the OTA are charged and discharged (Figure 3.5). The associated differential current I_b (= I_{bp} – I_{bn}) is mostly provided by the OTA via the integration caps, assuming $g_m \gg 1/R$. However, the feedback current I_a (= I_{ap} - I_{an}) is modulated again by ϕ_{chop}. I_a is then integrated onto the integration capacitors, C_{int}, resulting in a sampled input-referred error voltage, V_{err}, with a period of $T_{chop}/2$, given by

$$V_{err} = \frac{2 \cdot C_{p1} \cdot V_q}{C_{int}\left(1 + g_m \cdot R\right)}, \tag{3. 5}$$

where $C_{p1} = C_{p1p} = C_{p1n}$ and $C_{intp} = C_{intp} = C_{intn}$.

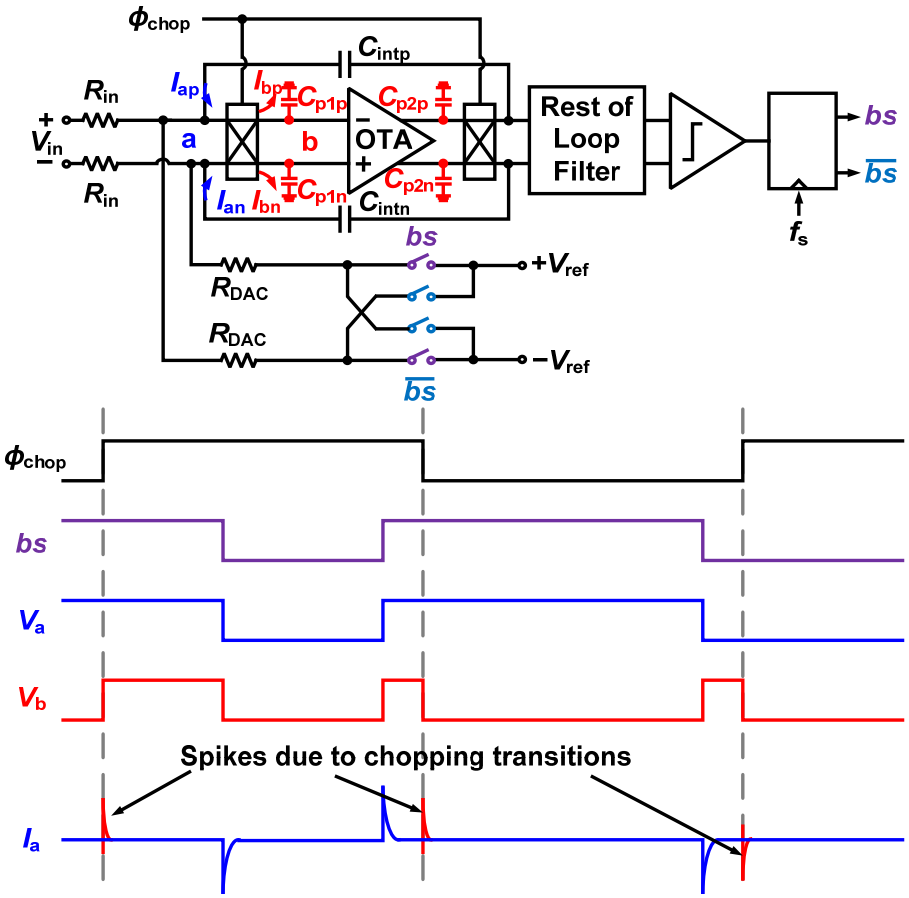

Figure 3.5: Second-order CTΔΣM with chopping with a resistive NRZ-DAC.

This process equivalently samples V_q at $2f_{chop}$. For a rectangular DAC pulse shape, the spectrum of V_q will have notches at f_s and $2f_s$ as shown in Figure 3.6. Therefore, chopping the first integrator at f_s or $f_s/2$ will not cause aliasing (or fold-back) [4, 5]. However, the mismatch error of the parasitic ($C_{p1p} \neq C_{p1n}$) or integration ($C_{intp} \neq C_{intn}$) capacitors will lead to an error sampling at f_{chop}, resulting in V_q also being sampled at f_{chop}. Although such mismatch-induced error is usually much smaller than the error sampled at $2f_{chop}$, for $f_{chop} = f_s/2$ it might still cause significant fold-back of the quantization noise from around $f_s/2$ (where it is largest) to DC.

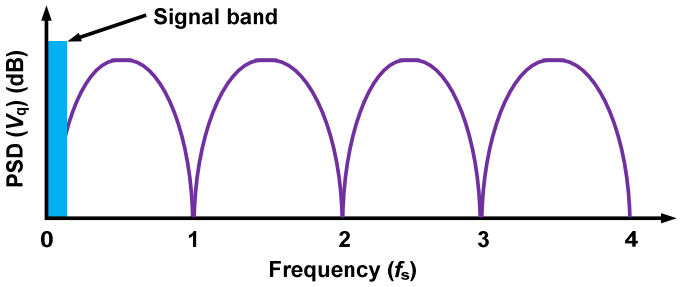

Figure 3.6: The spectrum of V_q.

The output parasitic capacitors, C_{p2p} and C_{p2n}, also cause integrator output voltage to be sampled in a similar manner. However, when the resulting error is referred to the input, it will be first-order high-pass shaped. This makes the output sampling error negligible in most practical cases, provided that the DC gain of the integrator is high. It should be noted that the switched-capacitor resistor due to the switching of C_{p2} may degrade the output impedance of the OTA and reduce the DC gain.

Although chopping at f_s and its integer multiples ($f_{chop} = K{\cdot}f_s$) causes no quantization noise fold-back [6, 7], there are secondary effects, such as discussed lower first integrator's DC gain, higher input referred $1/f$ noise, and higher power consumption, proportional to f_{chop} degrading the performance of the chopped CTΔΣM [6]. Thus, chopping at lower frequencies is preferable, provided that the chosen f_{chop} is above the $1/f$ corner and well within the stop-band of the digital decimation filter.

As can be seen from Eq. 3.4 and Eq. 3.5, the error caused by chopping artifacts can be reduced if the swing at the virtual ground of the OTA is reduced. This can be achieved by increasing the g_m or by adding a low-impedance output stage. Both increase the power consumption, and hence reduce energy efficiency. Observing that the only fold-back prone signal is the output of the DAC (V_{DAC}), previous work has suggested the use of a finite-impulse-response (FIR) DAC to suppress quantization noise around the error-sampling-frequency $2{\cdot}f_{chop}$ [12,13]. Although this is quite effective, the FIR filter design should have notches around $2{\cdot}f_{chop}$ and its harmonics, which may require a large number of taps especially for CTΔΣMs with high OSR. This results in more excess loop delay (ELD) which needs to be compensated by means of additional loops and adds an area overhead which is proportional to the

number of FIR taps, but at the cost of increasing the design complexity. Thus, simpler methods for implementing low-frequency chopping are still needed.

3.3 The Proposed Methods

The previous analysis addresses the problem in the frequency domain and presents a frequency domain filtering solution. However, an alternative approach can be found in the time domain. For a non-return-to-zero (NRZ) DAC, V_{dac} is a zero-order-held version of bs. In practice, the DAC shape can be chosen arbitrarily as long as the total error feedback charge integrated onto C_{int} is kept the same over T_s. If the DAC pulse shape includes a bs-free time window, the sampled error can be reduced if the chopping transition occurs during this time window. The same observation holds for DAC pulse shapes which decay to zero. We propose using a return-to-zero (RZ) or switched-capacitor (SC) DAC in the feedback loop so as to have a bs-free or a reduced-bs time window for the chopping transitions, respectively. This approach can be extended to other DAC pulse shapes with similar properties.

3.3.1 Chopping with RZ-DAC

As shown in Figure 3.7, when ϕ_{RZ} is low, the DAC is connected to the virtual ground of the OTA, and the DAC output current is proportional to bs. When ϕ_{RZ} is high, the DAC is in the RZ phase, meaning the output is zero. This indicates that during the RZ phase no quantization noise from the DAC will appear at the virtual ground node of the OTA. In this case, the virtual ground node signal will be given by

$$V_a \cong \begin{cases} \dfrac{V_q}{1+g_m \cdot R}, & \phi_{RZ}=0 \\ \dfrac{V_{in}}{1+g_m \cdot R}, & \phi_{RZ}=1 \end{cases}. \tag{3.6}$$

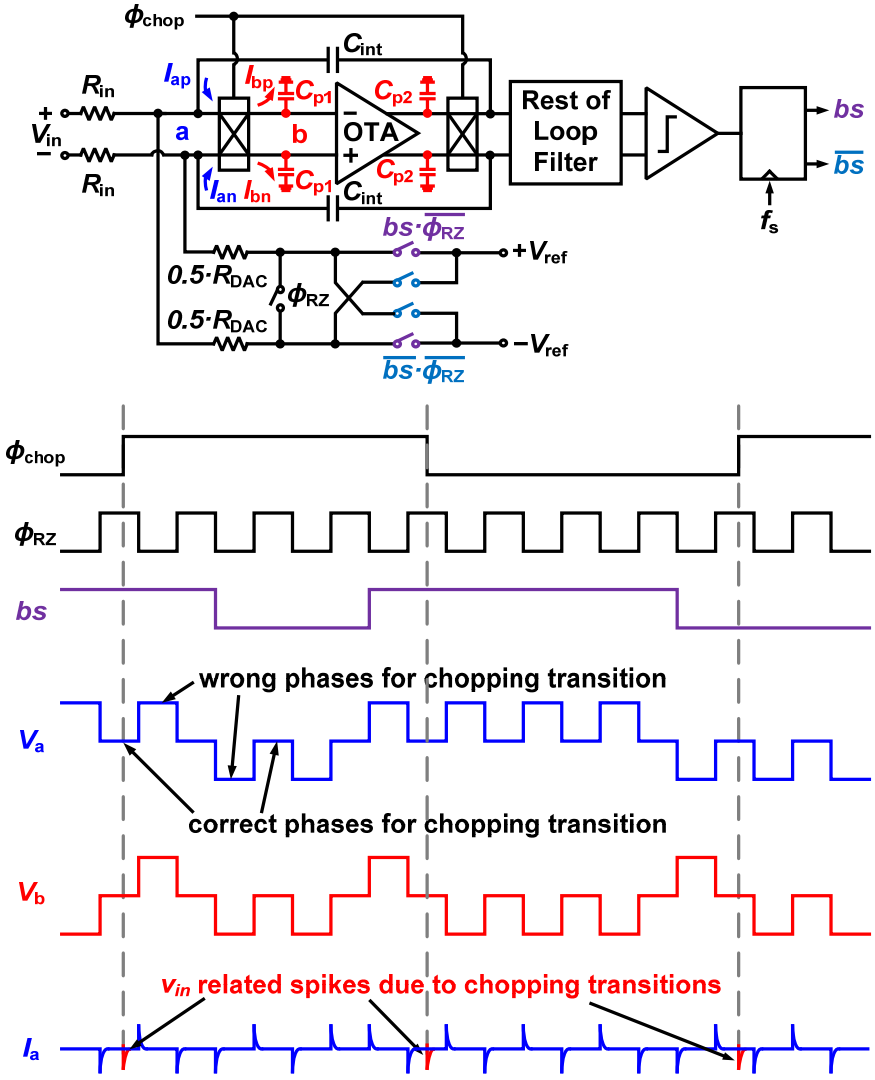

Figure 3.7: Second-order CTΔΣM with chopping with a resistive RZ-DAC.

As shown clearly in Eq. 3.6, if ϕ_{chop} changes state during the RZ phase ($\phi_{RZ} = 1$), i_a and i_b will only be v_{in}-dependent. Thus, the sampled error caused by chopping transitions will not contain the bs related part (V_{DAC}). Hence, the Signal-to-Quantization-Noise Ratio (SQNR) will not be degraded by the aliased quantization noise.

Since RZ-DACs are often used in CTΔΣMs to avoid inter-symbol interference (ISI) due to the finite rise and fall times of the output signal, the proposed method will not increase the complexity of most designs. Moreover, this method allows the first integrator of the modulator to be chopped at frequencies much lower than the sampling frequency. In this way, the input current and noise associated with the charge injection of the chopper switches can be reduced [10]. Furthermore, the degradation of the DC gain of the OTA in the first integrator due to chopping. In turn, this helps to suppress the offset and the 1/*f* noise of the following stages of the loop filter.

3.3.2 Chopping with SC-DAC

SC-DACs are commonly used in CTΔΣMs to reduce jitter sensitivity while also reducing ISI [12]. The error caused by chopping artifacts can also be reduced by selecting the correct chopping moment as shown in Figure 3.8. The DAC capacitor CDAC is charged to $\pm V_{ref}$ during ϕ_{SMP}, and its polarity is determined by bs. During ϕ_{DAC} the sampled charge is integrated onto C_{int}. The virtual ground voltage during this phase has a decaying shape, which is given by

$$V_a \cong \begin{cases} \dfrac{V_{in}}{1+g_m \cdot R} - \dfrac{V_{ref}}{1+g_m \cdot R_{DAC}} e^{-\frac{t}{\tau}}, & \phi_{DAC} = 0 \\ \dfrac{V_{in}}{1+g_m \cdot R}, & \phi_{SMP} = 1 \end{cases}, \tag{3.7}$$

where R_{DAC} is the series resistance of the DAC, and τ is the SC-DAC settling time constant given by

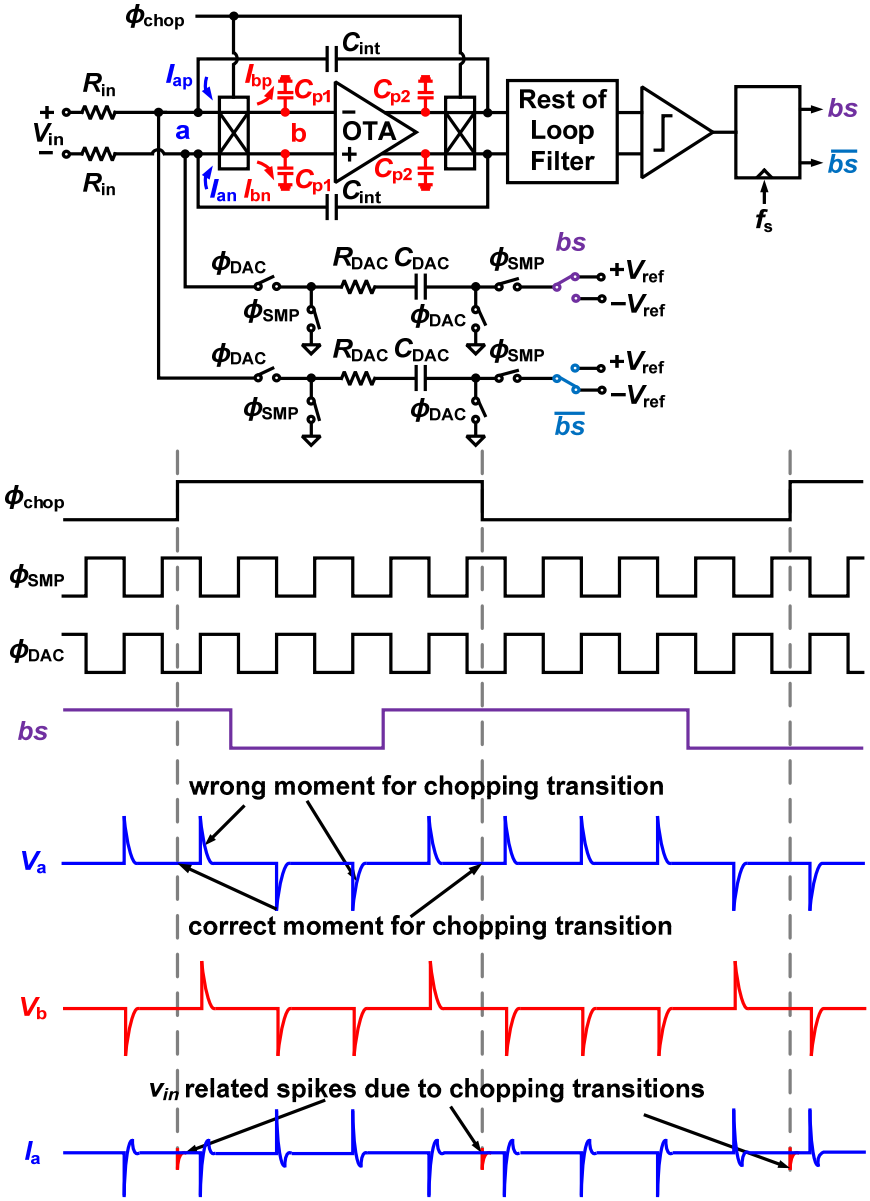

Figure 3.8: Second-order CTΔΣM with chopping with a SC-DAC.

$$\tau \cong \frac{\left(g_m \cdot R_{DAC} + 1\right) \cdot \left(\frac{C_{int} \cdot C_{DAC}}{C_{int} + C_{DAC}}\right)}{g_m}. \tag{3.8}$$

It is evident from Eq. 3.7 that the decaying pulse shape means that chopper transition should occur during ϕ_{SMP} or at the end of ϕ_{DAC} when the bs-related virtual ground components have decayed.

3.4 Simulation Results

To further verify the effectiveness of the proposed techniques, two second-order feed-forward CTΔΣMs have been implemented, one with a resistive RZ-DAC and one with a SC-DAC. The input signal frequency is 500 Hz, the sampling frequency is 2 MHz, and C_{int} is 35 pF for both CTΔΣMs. The OTA in the first integrator has an 80 dB DC gain and 1 mS transconductance. The virtual ground parasitic C_{p1} is 1 pF and the output parasitic C_{p2} is about 100 fF.

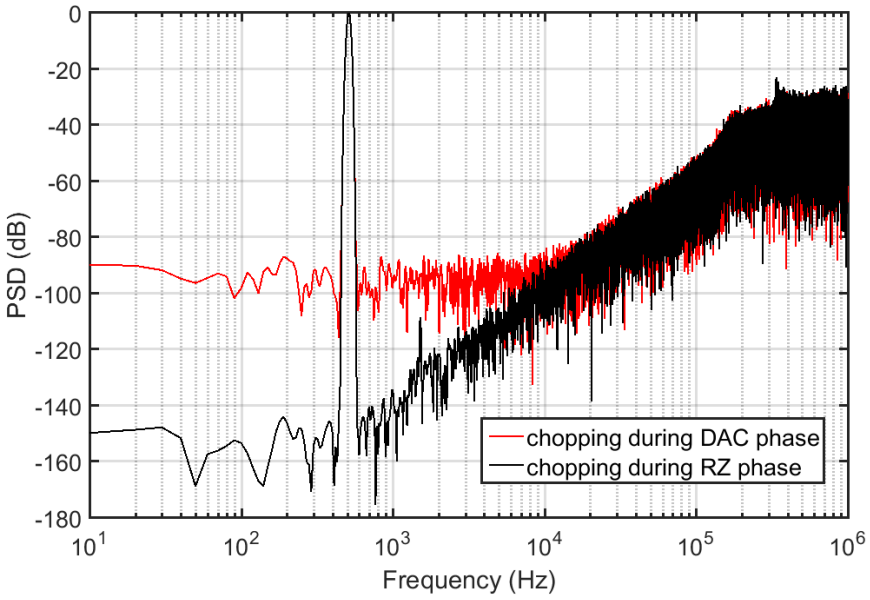

Figure 3.9: Bitstream spectrum of a second-order CTΔΣM with a resistive RZ-DAC, with chopping during the DAC phase (red) at the first integrator, and with chopping during the RZ phase (black) at the first integrator. (2×10^5 samples, Kaiser window)

When chopped at 20kHz, a comparison of the output spectra of the modulator with the RZ-DAC is shown in Figure 3.9 for the correct and incorrect chopping phases, i.e. at $\phi_{RZ} = 1$ and $\phi_{RZ} = 0$, respectively. Chopping during the $\phi_{RZ} = 0$ phase significantly increases the noise floor due to quantization noise fold-back. This is similar to what occurs in NRZ-DACs. Chopping during the $\phi_{RZ} = 1$ phase, however, practically eliminates the effect of quantization noise fold-back.

For further verification, a 3 mV offset and 100 fF parasitic capacitance (C_{p2}) mismatch were added to the OTA used in the first integrator. In order to show the SQNR degradation due to high frequency chopping $f_{chop} = f_s/100 = 20$ kHz, and $f_{chop} = f_s = 2$ MHz are chosen with RZ chopping. As shown in Figure 3.10, the low-frequency noise PSD for $f_{chop} = 2$ MHz is worse than for $f_{chop} = 20$ kHz, even when chopping at ϕ_{RZ}, mainly due to the reduced loop gain caused by chopping and the first integrator OTA's finite bandwidth.

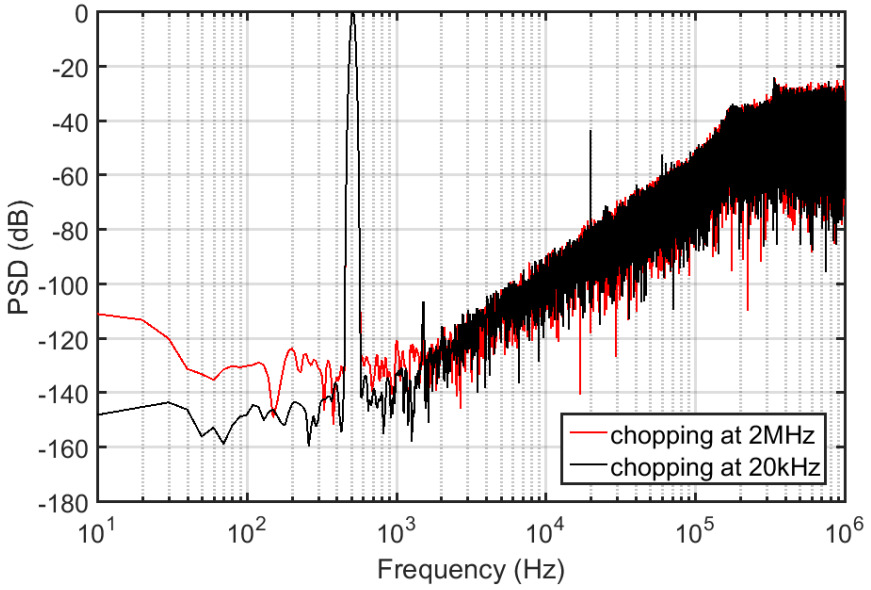

Figure 3.10: Bitstream spectrum of a second-order CTΔΣM with a resistive RZ-DAC, with 2MHz chopping frequency (red) at the first integrator, and with 20kHz chopping frequency (black) at the first integrator. (2×10^5 samples, Kaiser window)

Figure 3.11 shows the output spectra for the CTΔΣM with the SC-DAC when it is chopped at the correct and incorrect moments indicated in Figure 3.8. Although the output of a SC-DAC decays exponentially, the initial amplitude of the bs-related virtual ground signal will be larger than that of a RZ-DAC. Thus, the sampled quantization noise power is dependent on the exact chopping moment. As a result, the simulated PSD corresponding to the incorrect chopping moment (Figure 3.11) has a higher noise floor than that obtained with a RZ-DAC (Figure 3.9).

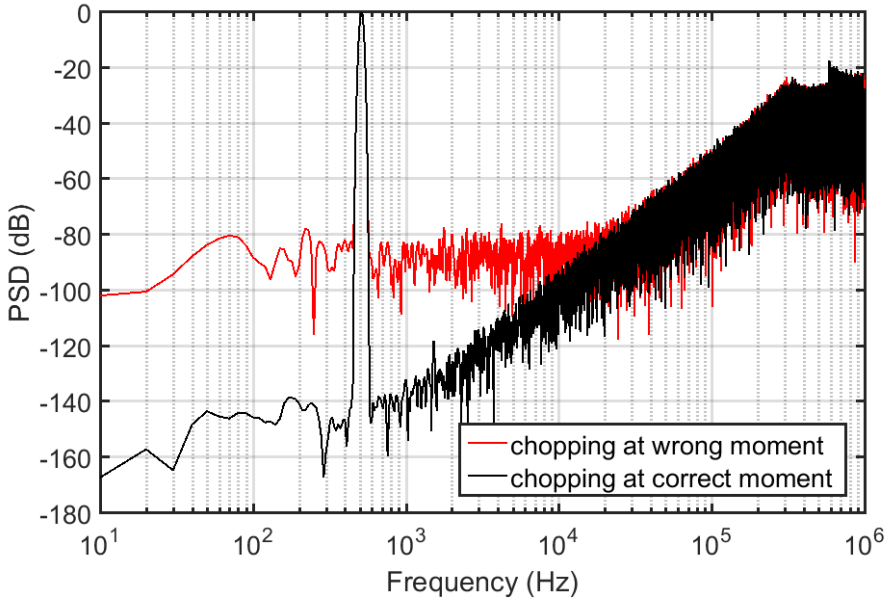

Figure 3.11: Bitstream spectrum of a second-order CTΔΣM with a SC-DAC, with chopping at the incorrect moment (red) at the first integrator, and with chopping at the correct moment (black) at the first integrator. (2×10^5 samples, Kaiser window)

3.5 Conclusion

This chapter has described the theory and implementation problems associated with the use of chopping to reduce offset and 1/*f* noise in ROICs. It is shown that chopping can significantly degrade the noise floor of CTΔΣMs due to the aliasing of high-frequency quantization noise. Two methods are proposed to mitigate quantization-noise aliasing for modulators with RZ-DACs and SC-DACs. Both are based on the DAC pulse shape and the choice of appropriate chopping moments. Analysis and simulations show that these techniques can almost completely eliminate quantization noise fold-back. The proposed methods thus allow the chopping frequency to be flexibly chosen. This is especially valuable in the design of high OSR 1-bit CTΔΣMs where low-frequency chopping is desired to avoid the increased offset and input current associated with high-frequency chopping, e.g. the traditional technique of chopping at the sampling frequency. The proposed methods can be further extended to any DAC shape that exhibits moments when it is zero, open, or decaying. The techniques of this chapter have been applied and verified in the designs of chapter 4 and 5.

3.6 Bibliography

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CCIA Based ROIC

The energy efficiency of a ROIC will usually be determined by its IA, since this sets its input-referred noise (Chapter 2). CCIAs have been shown to be particularly energy-efficient [1]. As shown in Figure 4.1, a CCIA consists of an inverting amplifier with capacitive feedback elements, input and output choppers which modulates and demodulates differential input voltages to a chopping frequency, f_{chop}, allowing them to be amplified. Since they only require one noise-critical input stage, CCIAs are generally more energy-efficient than the chopped 3-Opamp IAs or CFIAs [1-3]. Moreover, their input capacitors naturally block CM input voltages, allowing them to handle CM levels much larger than their supply voltages. In ROIC applications, this means that both the bridge and the ROIC can be powered from different voltage supplies, allowing the supply voltage of the readout to be optimized for energy efficiency. Last but not least, since CCIAs are inherently chopped, their $1/f$ noise and offset are also quite low.

However, a major drawback of CCIAs is that they generate output spikes at their chopping transitions, i.e. at $2f_{chop}$ [1]. This is because C_{in} must be rapidly charged and discharged at the chopping transitions [1,4,5]. These spikes should not be digitized since their amplitude is usually not a linear function of the input signal.

This chapter is derived from a journal publication of the authors: H. Jiang, S. Nihtianov and K. A. A. Makinwa, "An Energy-Efficient 3.7 nV√Hz Bridge Readout IC With a Stable Bridge Offset Compensation Scheme," in IEEE Journal of Solid-State Circuits, vol. 54, no. 3, pp. 856-864, March 2019.

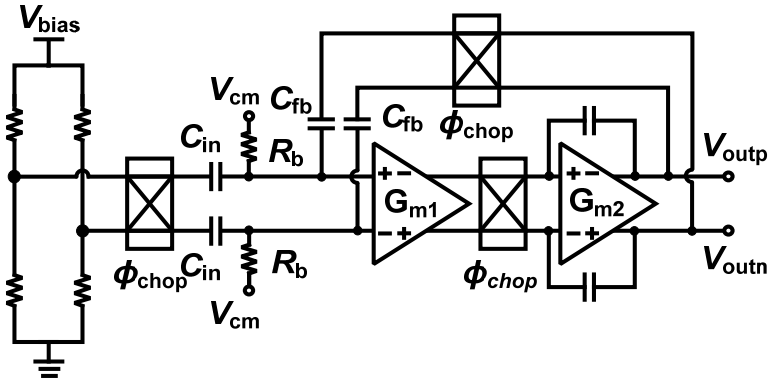

Figure 4.1: ROIC using a CCIA.

This chapter describes an energy-efficient ROIC. The ROIC uses a gated CTΔΣM to digitize the CCIA output while avoiding output spikes. To maximize the CCIA's useful dynamic range, the bridge offset is compensated with a passive DAC referred to the bridge biasing voltage. This ratio metric approach ensures that the compensating signal only depends on capacitor and resistor ratios, making it stable over temperature and bias voltage variations. Implemented in a standard CMOS 180 nm process, the ROIC achieves a state-of-the-art NEF of 5.

The rest of the chapter is organized as follows. Section 4.2 discusses the main techniques used in the ROIC to achieve high energy efficiency and high precision. Section 4.3 describes implementation details of the ROIC, while the experimental results of the ROIC are presented in Section 4.4. The chapter ends with conclusions.

4.1 Energy-efficient Readout Techniques

As discussed in Chapter 1, differential pressure sensors with a range of ±100 Pa are required in air gauges for industrial applications [6]. The AC4010 is a high-resolution bridge-type piezo-resistive pressure sensor that can cover this range [7]. To achieve a resolution of 10 mPa (rms) over a 1 kHz bandwidth, the biasing voltage V_{bias} should be at least 5 V, thus resulting in a sensitivity of about 45 μV/Pa. However, this will be superimposed on a bridge offset of about 100 mV, due to the mismatch of the piezo-resistive elements (nominally 3.7 kΩ each). To ensure that the ROIC does not limit sensor performance, it should be designed to meet the specifications in Table 1.1.

4.1.1 Dual-Supply Sensing System

Conventionally, the supply voltage of a ROIC must be somewhat larger than the bridge's CM level, despite the fact that the bridge output itself is quite small [1-5]. This constraint leads to a trade-off between bridge sensitivity and ROIC power dissipation.

One way of avoiding this trade-off is to exploit the beyond-the-rails capability of a CCIA. As shown in Figure 4.2a, the bridge can then be powered from a 5 V supply, while the ROICs can be powered from a lower, say 1.8 V supply voltage. The only active components exposed to the 2.5 V CM bridge voltage are the switches of the CCIA's input chopper (Figure 4.2b [8]), which can then be realized with DMOS transistors or I/O devices. The input chopper is driven by antiphase chopping clock, which are generated by 1.8 V core circuit. They are capacitively coupled to the gates of four chopping switches via a level shifter composed of two capacitors and a latch. The CCIA's input capacitors can be implemented with metal-insulator-metal (MIM) capacitors, which, in most processes, are capable of handling voltages higher than the core circuits supply voltage (1.8 V).

4.1.2 Compensating the Bridge Offset

Due to bridge mismatch, however, increasing V_{bias} will also increase bridge offset. Since this can be quite large, it may limit the IA's useful output range, and its

maximum closed-loop gain. As a result, the succeeding ADC will require a wider dynamic range and lower input-referred noise, both of which will result in increased power dissipation.

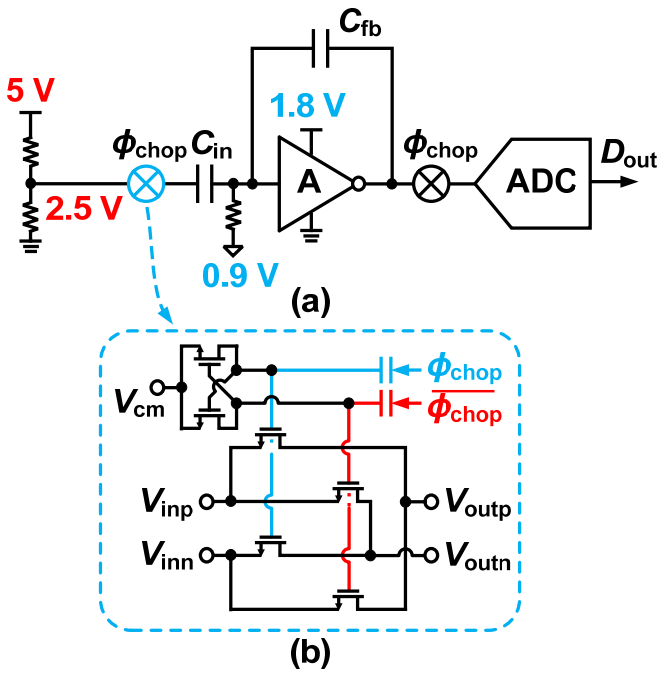

Figure 4.2: (a) The proposed dual-supply sensing system (single-ended representation) and (b) the CCIA's capacitively coupled input chopper.

To avoid this problem, bridge offset should be compensated before amplification. This can be done by: (1) using an external offset compensation network to trim the bridge [9]; or (2) using a current DAC to inject a programmable current into the bridge [10]. However, the bridge and the compensation circuitry will inevitably have different temperature dependencies, leading to significant temperature drift.

In this work, the CCIA is used to implement a ratio-metric offset-compensation scheme (Figure 4.3). The bridge output V_{in} is added to an offset-compensating signal generated by a capacitive DAC (CDAC1), which is referred to V_{bias} via a resistive divider. By implementing both C_{in} (input capacitor of the CCIA) and CDAC1 with MIM capacitors, both the bridge output V_{in}, and the divider output kV_{bias}, will respond in the same way to temperature and V_{bias} variations.

Note that the residual bridge offset and bridge sensitivity will still drift over temperature. This is inherent to the sensor, and can be absorbed by calibrating the overall system. However, the proposed bridge offset compensation minimizes the errors contributed by the ROIC, ensuring that the overall system accuracy is mainly limited by the bridge sensor.

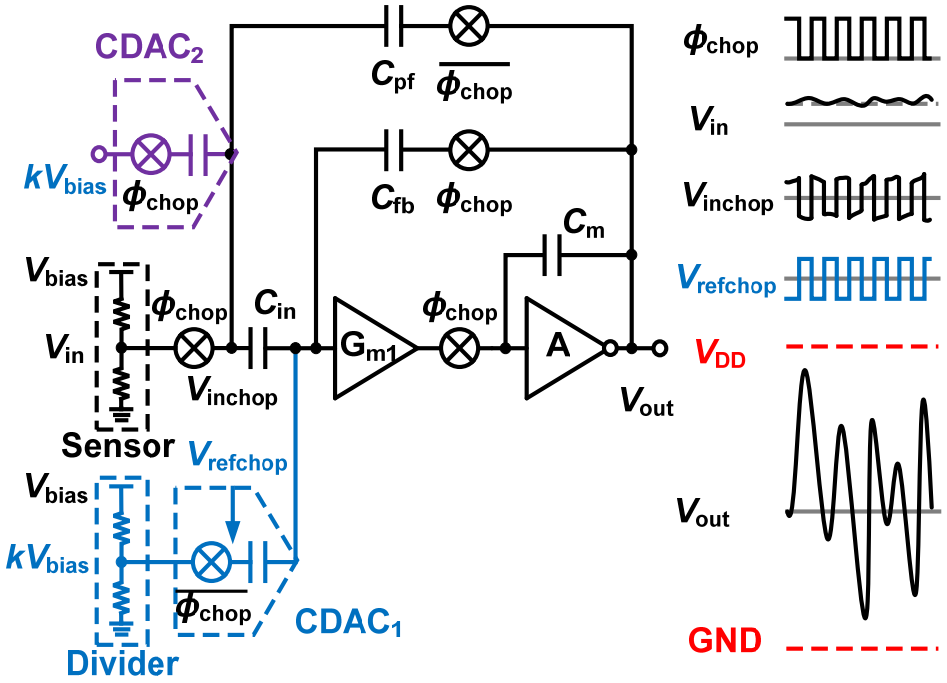

Figure 4.3: Block diagram of the CCIA illustrating the operation of the bridge offset compensation and dual-path input impedance boosting loops.

4.1.3 Dual-Path Impedance Boosting Scheme

A known drawback of CCIAs is that the output spikes at twice the chopping frequency ($2f_{chop}$) [1]. To reduce the amplitude of these spikes, most of the required charge can be provided from the output of the CCIA via a positive feedback path [1], or through an auxiliary pre-charge path [5], which also boosts the CCIA's input impedance. Although the boosting effect of a positive feedback path is limited by parasitic capacitors and stability measures [1], it is an appealing approach in this application, as a pre-charge path requires active buffers which would compromise the CCIA's beyond-the-rails capability.

As shown in Figure 4.3, a positive feedback path can be realized with an extra capacitor C_{pf} which should provide a compensation charge Q_{com} [3], given by:

$$Q_{com} = C_{pf} V_{out} \approx C_{in} V_{in} = Q_{in}, \tag{4.1}$$

where V_{in} consists of two parts: the useful bridge signal, V_{sig}, and the bridge offset, V_{os}. However, in the proposed design (Figure 4.3), V_{os} will be partially canceled by CDAC1 before amplification. To ensure a charge proportional to the compensated offset, a capacitive DAC (CDAC2) is added, and driven by the same code as CDAC1. The total compensation charge is now given by:

$$Q_{com} = C_{pf} V_{out} + Q_{DAC} \approx C_{in} (V_{sig} + V_{off}) = Q_{in}. \tag{4.2}$$

4.1.4 Gating the Output of the CCIA

Residual output spikes in the CCIA can be avoided by using a DTΔΣM to synchronously sample the CCIA output. The modulator's sampling frequency, f_s, will then be equal to $2f_{chop}$, as shown in Figure 4.4a [1,4]. Assuming that the CCIA is a single-pole system without slew rate limitations, a minimum bandwidth, BW, is needed to achieve sufficient settling [11]:

$$BW \geq 2 \cdot (m+1) \cdot f_s \cdot \ln 2 . \tag{4.3}$$

where m is the target resolution of the ROICs in bits. Due to the sampling process, noise within a bandwidth of $\pi/2 \cdot BW$ will fold back to baseband, increasing the in-band noise power density of the CCIA. This significantly decreases the energy efficiency of the ROIC [4]. A dynamic RC filter can be used to limit the noise bandwidth before sampling (Figure 4.4b) but at the expense of increased design complexity [5].

In this design, the CCIA residual spikes are avoided by gating the input of a CTΔΣM. As shown in Figure 4.4c, the input of the CTΔΣM is connected to the CM voltage for the duration of the spikes, after which it is connected to the output of the CCIA. In this way, the errors associated with the CCIA spikes are reduced without noise fold-back. Compared to a switched capacitor (SC) load, the resistive load presented by the modulator significantly relaxes the requirements on the CCIA's driving capability and thus further improves the ROIC's energy efficiency. Since the CCIA output is effectively duty-cycled, these benefits are acquired at the expense of a small reduction (2.5%) in the effective gain.

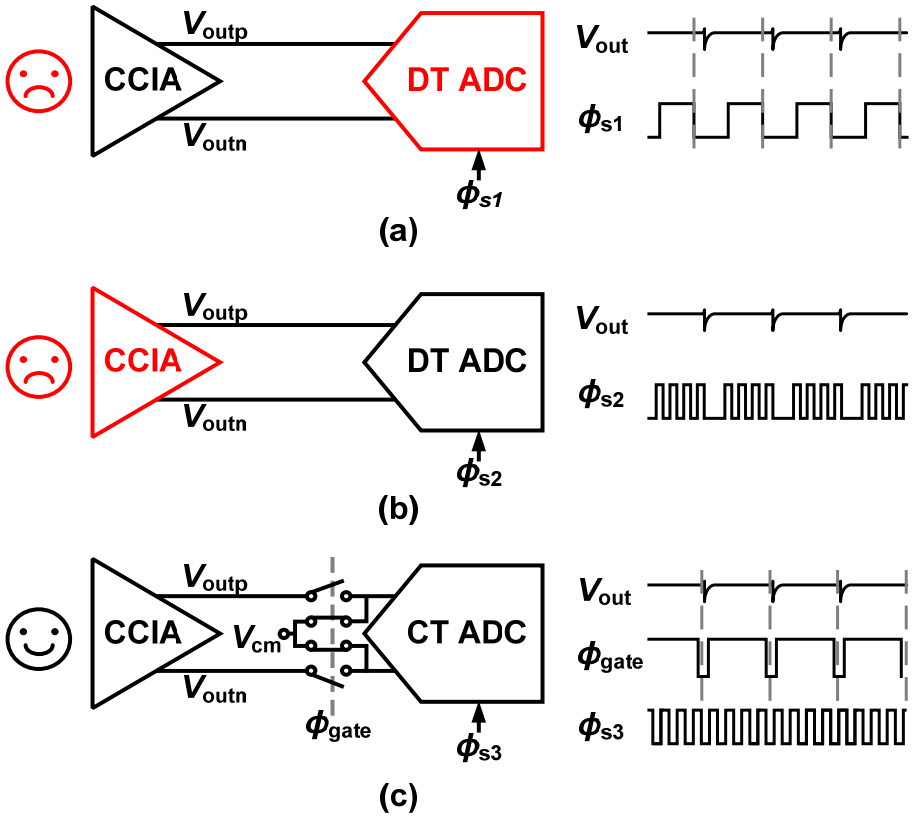

Figure 4.4: Different ways to avoid digitizing the spikes of a CCIA: (a) by using fs = $2f_{chop}$ (b), oversampling at quiet moments and (c) using gated continuous-time integration.

4.2 Circuit Implementation

A simplified circuit diagram of the proposed ROIC is shown in Figure 4.5. It consists of a CCIA with bridge offset-compensation circuitry, and a gated CTΔΣM. In this section the implementation of these blocks will be discussed in detail.

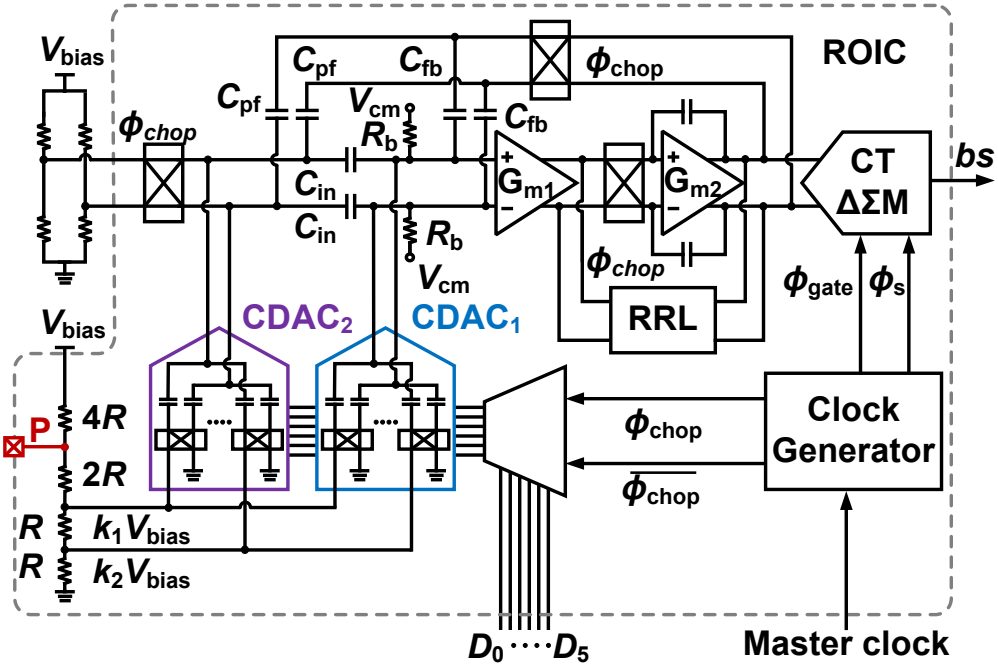

Figure 4.5: Simplified circuit diagram of the ROIC.

4.2.1 CCIA

The gain of the CCIA is set at 40 dB. To achieve high linearity, the CCIA is built around a two-stage Miller compensated opamp, with a DC gain of about 124 dB. The bridge has an equivalent source resistance of 3.7 kΩ, corresponding to a noise density of 7.8 nV/√Hz [7]. The input-referred noise of the CCIA should be lower than this, which is quite challenging. The first stage consists of a chopped folded-cascode amplifier with a very large PMOS input pair (1280 µm/0.2 µm) that is biased in weak inversion to efficiently realize a trans-conductance of about 6.7 mS. Compared to a NMOS or current reused (CMOS) input transistor consuming the same current, PMOS input transistor has a lower input parasitic capacitance as well as a lower inherent 1/*f* noise corner (Figure 4.6). To mitigate the noise gain penalty due to the input pair's parasitic capacitance (1.3 pF), the CCIA's input capacitors C_{in} are set to 10 pF [1]. Meanwhile, a lower 1/*f* noise corner enables the use of a lower chopping frequency, reducing the side effects of higher chopping frequencies (Chapter 3).

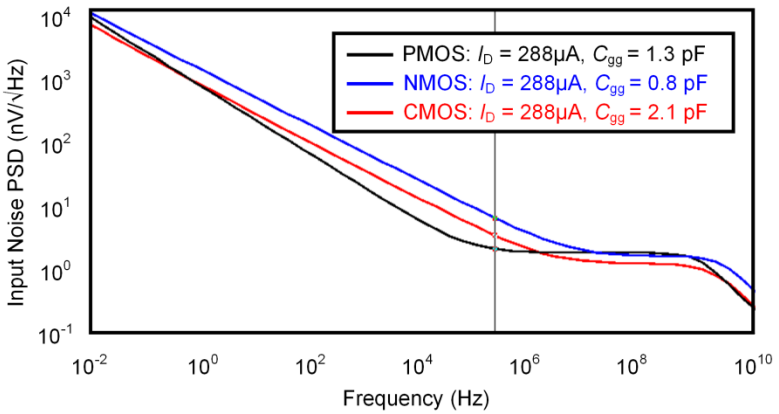

Figure 4.6: Input noise PSD with different types of input transistor.

As shown in Figure 4.7, the opamp draws 870 µA (simulated), with the input pair consuming most of the current. In this design, the offset and 1/*f* noise of the first stage is mitigated with chopping, while that of the second stage is suppressed by the gain of the 1st stage. Often [3,13,14], the demodulating chopper (drawn with dotted lines in Figure 4.7) is located at nodes A, B and C, D. In this case, the cascodes are not chopped and their 1/*f* noise becomes dominant, as shown in Figure 4.8a.

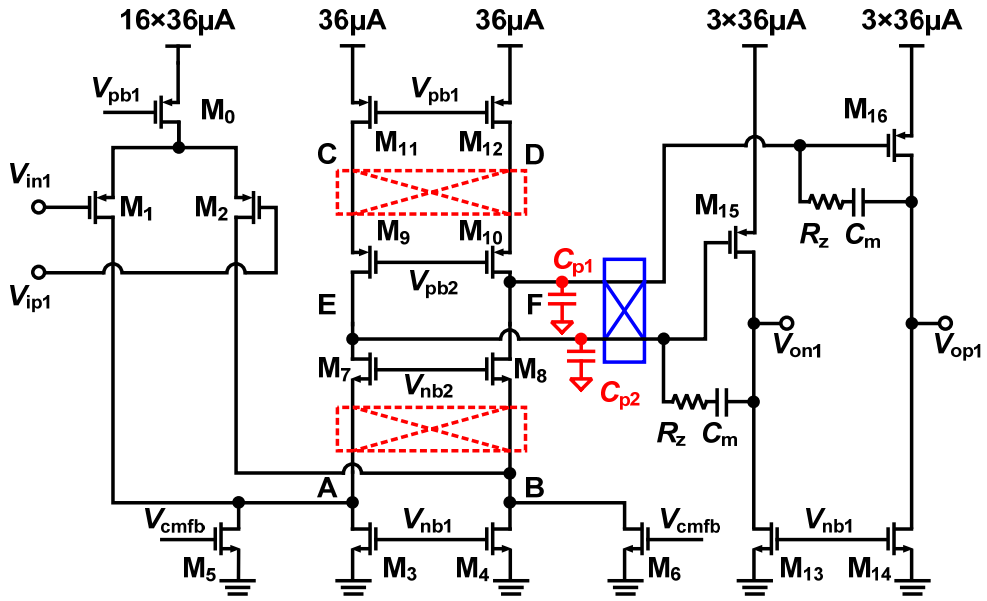

Figure 4.7: Schematic of the CCIA main opamp with demodulating chopper.

This can be resolved by moving the chopper to the output of the first stage, i.e. nodes E and F in Figure 4.7. As shown in Figure 4.8a, chopping at 200kHz results in a simulated 3.2 mHz $1/f$ noise corner. However, the chopped parasitic capacitors ($C_{p1,2}$) at these nodes will form a switched-capacitor resistance, which in turn will reduce the gain of the first stage. To mitigate this, relatively small cascode transistors were designed (M7,8: 24 µm/1.8 µm, M9,10: 60 µm/1.2 µm) and the layout was optimized. In this way, chopping only reduces the open loop gain by 2 dB (Figure 4.8b).

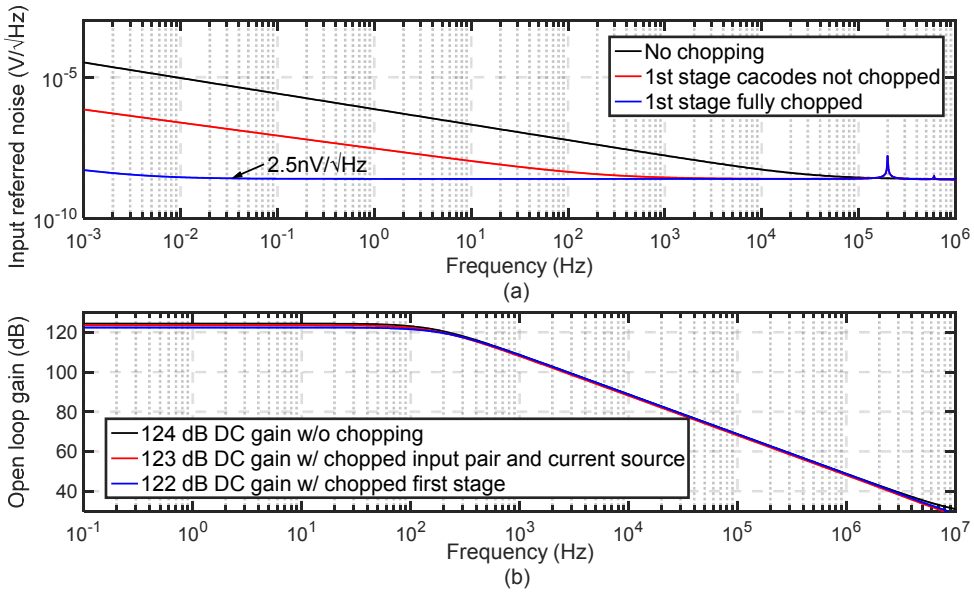

Figure 4.8: Simulation results showing (a) the opamp's input-referred noise PSD and (b) the opamp's open loop gain.

To minimize the noise contribution, the CCIA's bias resistors R_b, should be in excess of 250 MΩ. To conserve area, these resistors are implemented as SC resistors to achieve good linearity and stability over process and temperature variations [8]. The input chopper consists of capacitively driven DMOS transistors, allowing the input of the CCIA to handle bridge CM voltages up to 3.3 V (limited by the ESD-protection diodes) while operating from a 1.8 V supply.

4.2.2 Offset Compensation DAC

The bridge offset-compensation circuit consists of a 5-bit ($D_{5\text{-}1}$) binary weighted DAC with a redundant LSB (D_0) and a bank of chopper switches (Figure 4.9). It is controlled with an external trimming code ($D_{5\text{-}0}$). The DAC compensates the bridge offset by effectively adding a scaled and chopped version of V_{bias} to the output of the bridge.

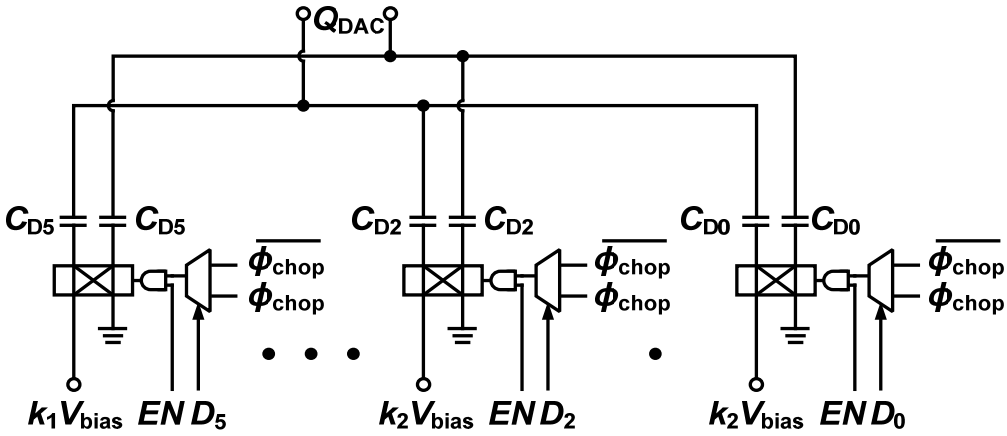

Figure 4.9: Simplified circuit diagram of the offset compensation DAC.

The total DAC capacitance should be kept small to minimize the impact on the CCIA noise gain [8]. With a 5V bias, a ±100mV bridge offset can be expected. To bring the offset into the input range of the CCIA, two references, k_1V_{bias} (1.25 V for $D_{5\text{-}3}$) and k_2V_{bias} (0.625 V for $D_{2\text{-}0}$), are derived from V_{bias} by means of a resistive divider. In this way, the DAC capacitance is reduced from 1.6pF to 0.87pF, 11.4× smaller than C_{in}, ensuring that the divider's noise contribution is much less than that of the CCIA. The unity capacitances are 49.1 fF for $D_{5\text{-}1}$ and 35.6 fF for D_0 (the smallest in the process).

The resistive divider has a total resistance of 36 kΩ, and is composed of polysilicon resistors which can handle bridge bias voltages up to 6.6 V. The chopper switches are protected by connecting node P to an ESD-protected pad to ensure that the chopper gates are not exposed to voltages above the supply (Figure 4.5). The polarity of the

compensating signal can be inverted via the choppers, so that the CCIA output can be expressed as $(V_{in}C_{in} \pm Q_{DAC1})/C_{fb}$. Simulations show that the CCIA, including the DAC, achieves an input-referred noise density of 3.4 nV/√Hz and a 1/*f* noise corner of 18 mHz.

4.2.3 Gated CTΔΣM

As shown in Figure 4.10, the CTΔΣM employs an energy-efficient 2nd-order feedforward topology. It consists of a gated RC integrator (1st stage), a Gm-C integrator (2nd stage), a 1-bit quantizer, and a resistive feedback DAC. The modulator's sampling frequency f_s = 2 MHz is enough to achieve the target resolution.

The 1st integrator, consuming about 190 μA, employs a folded-cascode OTA (A) with an 82 dB DC gain and a trans-conductance of about 0.86 mS. R_{in} and R_{DAC}, each 200 kΩ, are the main thermal noise sources of the CTΔΣM. R_{z1} is added, in series with the C_{int1}, to compensate the right-half plane zero of the OTA based on the RC integrator. The 1st integrator is also chopped to reduce the impact of its 1/*f* noise on the input-referred noise of the ROIC. Its chopping frequency is set at f_s to minimize quantization noise fold-back [15-16]. Although this is much higher than the 1st integrator's 1/*f* corner, the associated drawbacks, such as reduced input impedance, reduced output impedance and increased residual offset, are suppressed by the gain of the preceding CCIA.

The 1st integrator is gated by periodically swapping its input between the CCIA output and the CM voltage. For linearity, the associated switches are located at the virtual ground of the integrator to ensure that the on-resistance is signal-independent. As shown in Figure 4.10, the gating scheme ensures that the CCIA output is always loaded by the input resistors R_{in}, thus minimizing gating transients. In this work, the gating period comprises 2.5% of each chopping phase, resulting in a proportional decrease in the equivalent gain of the CCIA. This gain is quite well-defined since both the gating clock and chopping clock are derived from a 16 MHz external clock.

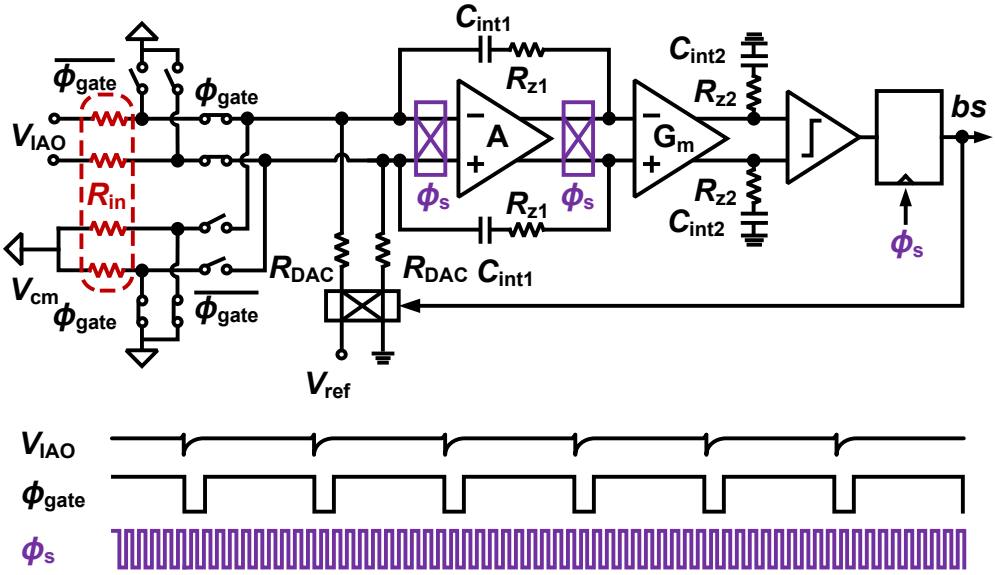

Figure 4.10: Gated 2nd-order CTΔΣM.

As shown in Figure 4.11, the second integrator employs a Gm-C topology based on a source-degenerated OTA (Gm in Figure 4.10). Since the noise of the second integrator will be suppressed by the gain of the 1st, the OTA only draws 20 μA.

The feedforward path of the 2nd-order ΔΣM is realized by adding R_{z2} in series with integration capacitor C_{int2}, with the value of the coefficient being defined by the ratio between the degeneration resistors R_s and the feedforward resistors R_{z2}. Thus, the transfer function, $H(s)$, from the input to the output of the second integrator can be expressed as:

$$H(s) = g_{m2}(R_{z2} + \frac{1}{sC_{int2}}) \approx \frac{R_{z2}}{R_s} + \frac{1}{sR_sC_{int2}}. \tag{4.4}$$

where g_{m2} is the transconductance of Gm in Figure 4.10.

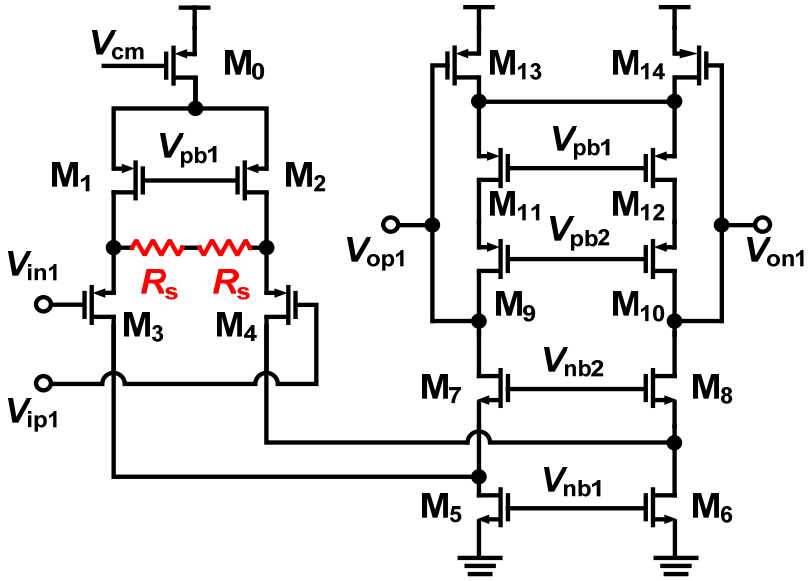

Figure 4.11: Source degenerated OTA of the second integrator.

The jitter of the sampling clock will translate into input-referred noise, thus degrading the signal-to-noise-ratio (*SNR*) of the CTΔΣM. However, the jitter requirement is relaxed by the relatively narrow signal band. The SNR_{jdac} determined by the sampling clock jitter σ_{jdac} is given by [2]:

$$SNR_{jdac} = 10 \cdot \log\left(\frac{1}{16 \cdot OSR \cdot f_b^2 \cdot \sigma_{jdac}^2}\right), \tag{4.5}$$

where *OSR* (over sampling ratio) is 1000 and f_b is 1 kHz. Assuming 10 ps (rms) jitter, SNR_{jdac} is 118 dB, which is sufficient for ROIC. In the worst case, a 42 ps (rms) jitter would result in a noise level close to that of the ROIC. However, this noise power contribution, caused by clock jitter, to the pressure sensing system is less than 6 %.

Similarly, the jitter of the gating clock, σ_{jgate}, in the first integrator also degrades the modulator's in-band noise performance. The SNR_{jgate} determined by this jitter is given by [17]:

$$SNR_{\text{jgate}} = 10 \cdot \log\left(\frac{1}{4 \cdot \left(V_{\text{IAO}} / V_{\text{ref}}\right)^2 \cdot f_{\text{b}} \cdot f_{\text{gate}} \cdot \sigma_{\text{jgate}}^2} \right), \tag{4.6}$$

where V_{IAO} is the CCIA output signal and f_{gate} is 400 kHz. In the worst case, when V_{IAO} is ±1 V, the resulting SNR_{jgate} with 10 ps (rms) jitter is 133 dB, which is 15dB lower than the SNR_{jdac}.

4.3 Measurement Results

The ROIC was implemented in a 180 nm standard CMOS technology, and has an active area of 0.73 mm^2 (Figure 4.12). The core of the ROIC, including the CCIA, CTΔΣM, $CDAC_1$, $CDAC_2$ and clock generator, consumes 1.2 mA from a 1.8 V supply. The on-chip resistive divider is supplied by the bridge bias voltage V_{bias}, which may be as high as 6.6 V.

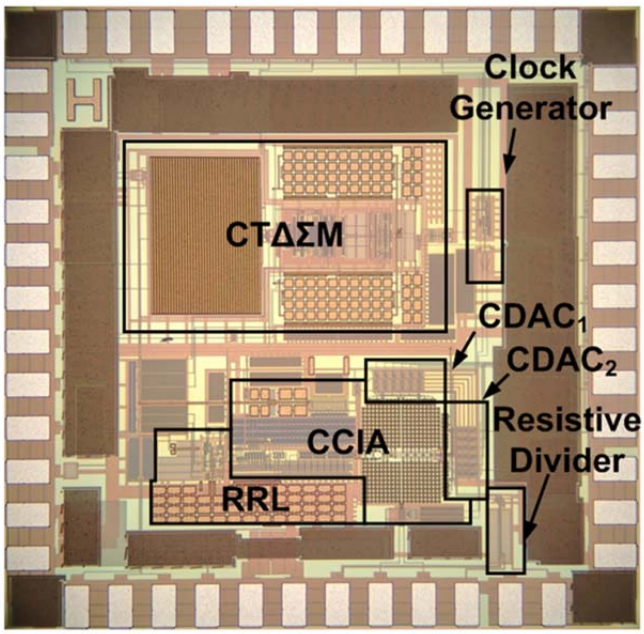

Figure 4.12: Die micrograph of the ROIC.

FFTs of the ROIC output bitstream, based on 2×10^7 samples, are shown in Figure 4.13. It can be seen that the first integrator of the modulator must indeed be chopped to ensure that the ROIC noise spectrum becomes flat from 0.1 Hz to 2 kHz and the spectrum corresponds to a 3.7 nV/√Hz noise level. By decimating the ROIC output with an off-chip sinc3 filter and then acquiring 2×10^8 samples of the filter output over 100 s, the $1/f$ corner frequency was found to be about 0.04 Hz.

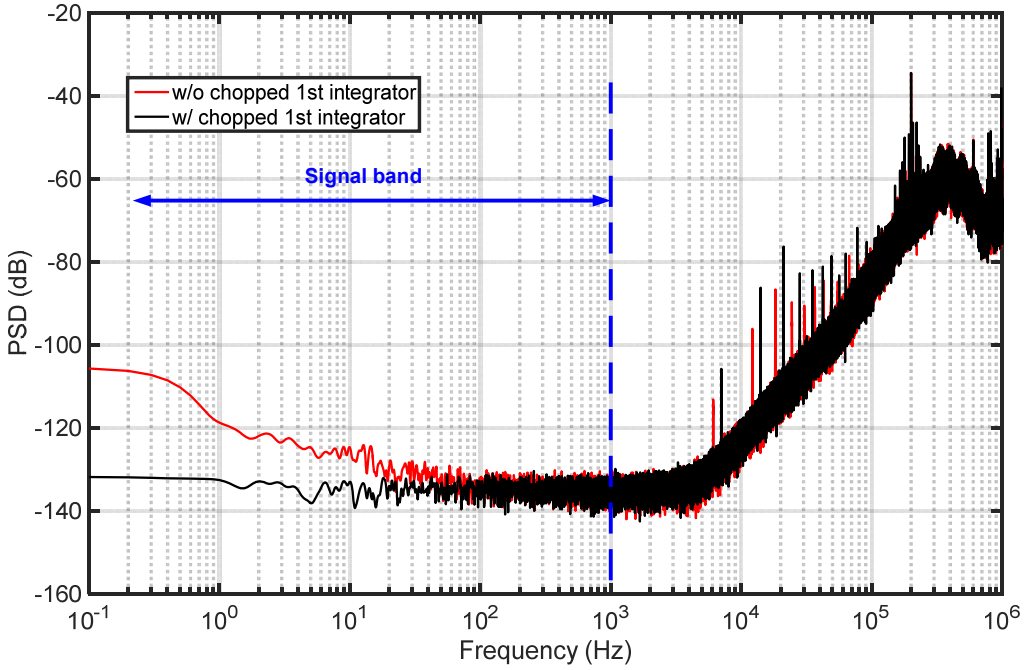

Figure 4.13: Measured PSD of the ROIC bitstream with 2×10^7 samples.

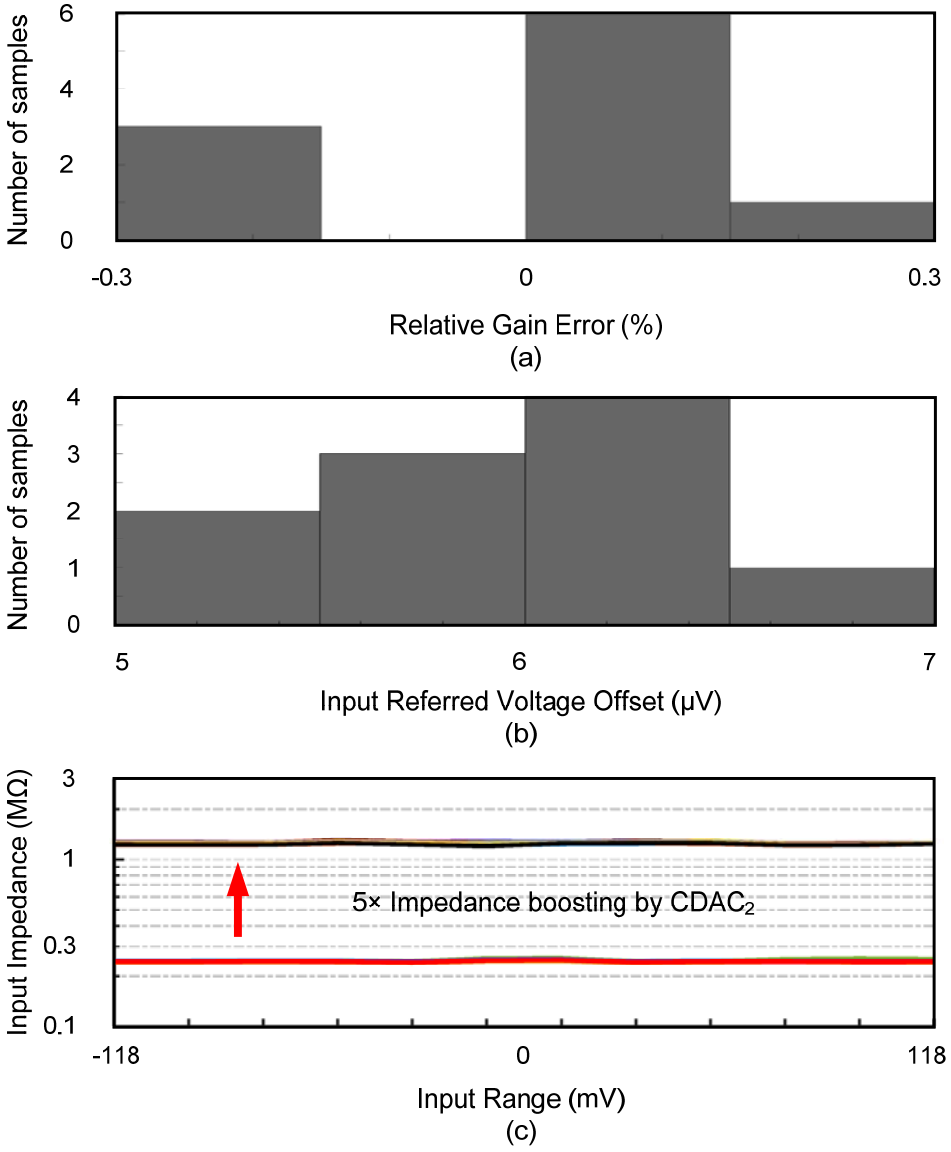

Figure 4.14: Measured relative gain error (a), offset voltage (b), and the input impedance (c) of the ROIC.

Measurements on 10 samples show that the ROIC achieves a 0.3% gain error (Figure 4.14a) and 7 μV voltage offset (Figure 4.14b). Enabling $CDAC_2$ reliably boosts input

impedance by a factor of 5 (Figure 4.14c). The CMRR of the readout is shown in Figure 4.15a.

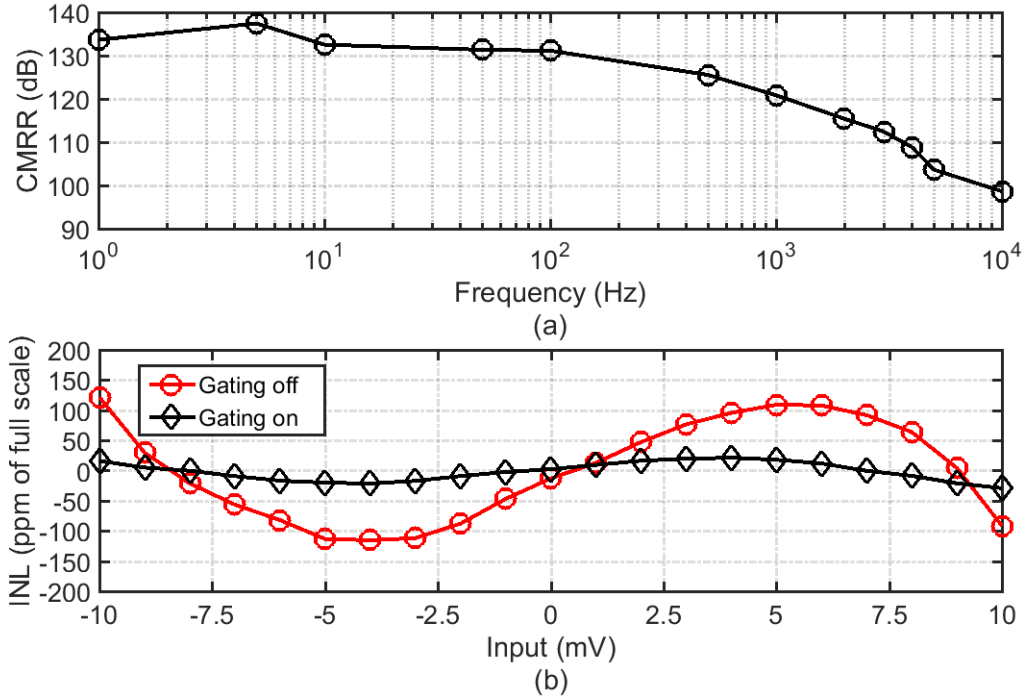

Figure 4.15: Measured CMRR of the ROIC (a) and INL (b).

To test the effectiveness of the gating technique, a 118 mV signal with a 2 kΩ source impedance, was applied to the inputs of the ROIC. Gating the CTΔΣM reduces the gain temperature drift of the ROIC from 74.6 ppm/°C to 8.9 ppm/°C, and reduces offset temperature drift from 105 nV/°C to 12.5 nV/°C. As shown in Figure 4.15b, gating the CTΔΣM also improves the readout INL from 105 ppm to 28 ppm.

The ROIC's performance is summarized in Table 4.1 and compared with the state-of-the-art. It achieves both high accuracy and energy efficiency for ±10 mV bridge signals, while accommodating up to ±118mV bridge offset and up to 3.3 V input common-mode voltage. With a 3.7 nV/√Hz input-referred noise PSD, it achieves a NEF (in [18]) of 5 and a power efficiency factor (PEF) (in [19]) of 44.

Table 4.1. State-of-the-Art ROICs.

	This work	[2]	[3]	[4]	[5]	[20]
Technology (nm)	180 nm	180 nm	700 nm	130 nm	180 nm	40 nm
Supply Voltage (V)	1.8	1.55	5	3	3.3	1.2
Supply Current (mA)	1.2	1.56	0.27	0.326[1]	0.075[2]	0.0175
DC CMRR (dB)	134	--	140	124	109	--
CM Input Range (V)	0–3.3	--	0–2.5	--	0–3	--
INL (ppm)	28	--	5	--	5	79[3]
Gain Drift (ppm/ ^{o}C)	8.9	--	0.7	--	0.81	--
Offset (μV)	7	--	0.05	2.4	1.8	300
Offset Drift (nV/^{o}C)	12.5	--	6	--	70	--
Input Noise Density (nV/√Hz)	3.7	8.2	16.2	16	19	140
NEF/PEF	5.0/44	12.5/242	10.4/541	11.1/372	6.41/136	22.6/613

1. Without taking into account the current consumption from a 1.5V supply.
2. Without taking into account the current consumption of the ADC.
3. Estimated from THD.

4.4 Conclusions

In this chapter, an energy-efficient ROIC for a differential pressure sensing system has been presented. To maximize bridge sensitivity with high energy efficiency, the beyond-the-rails capability of a CCIA is exploited to allow the bridge biasing voltage to exceed the ROIC's supply voltage. A bridge offset compensation is implemented in a ratio-metric manner, which is robust to variations in temperature and bridge biasing voltage. A dual positive feedback path scheme is used to boost the input impedance of the ROIC. A gated-input CTΔΣM is proposed to digitize the amplified signal and avoid the error caused by the output spikes of the CCIA. Measurements show that the ROIC achieves both precision and energy efficiency with a NEF of 5, which represents the state of the art.

4.5 Bibliography

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CC-CTΔΣM Based ROIC

In Chapter 4, the ROIC consists of a CCIA chopped at 200 kHz, and a CTΔΣM which was then chopped at f_s = 2 MHz (Figure 5.1a). Although this approach results in excellent performance, it requires two high-performance circuits and consequently two defining gain factors, which doubles the amount of component matching needed to maintain a given overall accuracy.

Alternatively, a CTΔΣM can be used instead to directly ROIC the bridge sensor. CTΔΣMs can achieve high resolution and energy efficiency, since they do not suffer from the kT/C noise limitations of discrete-time modulators [1]. Since the output of these sensors is often at the mV-level, the modulators also require low offset, 1/*f* noise and drift.

In low bandwidth applications, such as sensor ROIC, both offset and 1/*f* noise can be suppressed by the application of dynamic offset-cancellation techniques such as chopping and auto-zeroing [2,3]. Being a continuous-time technique, chopping can be readily implemented in a CTΔΣM, usually by chopping the first integrator. However, this approach is complicated by the fact that the signal applied to the input

This chapter is derived from a journal publication of the authors: H. Jiang, C. Ligouras, S. Nihtianov and K. A. A. Makinwa, "A 4.5 nV/√Hz Capacitively Coupled Continuous-Time Sigma-Delta Modulator with an Energy-Efficient Chopping Scheme," in IEEE Solid-State Circuits Letters, vol. 1, no. 1, pp. 18-21, Jan. 2018.

chopper consequently contains large amounts of high frequency quantization noise. This noise will be chopped, i.e. multiplied by a square-wave, causing some of it to fold back to low frequencies, and thus degrading the modulator in-band noise, as described in Chapter 2.

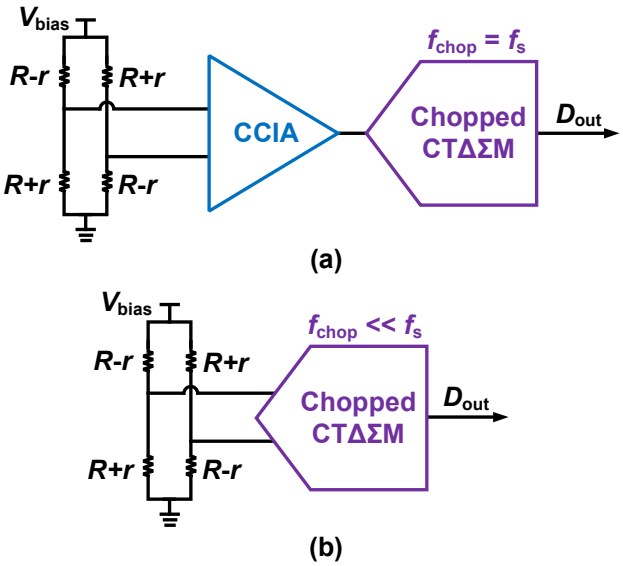

Figure 5.1: ROIC (a) with a CCIA followed by a CTΔΣM chopped at f_s in Chapter 4 and (b) with a stand-alone CTΔΣM and $f_{chop} << f_s$.

To avoid quantization noise fold-back in a chopped CTΔΣM, several approaches have been proposed. The first is to chop the CTΔΣM at the sampling frequency f_s [2]. This is simple and effective, but often means that the chopping frequency f_{chop} will be higher than necessary, i.e. than the modulator's input-referred $1/f$ noise corner. This, in turn, will result in lower input impedance and amplifier gain, as well as higher current noise and residual offset [3,4,5].

An alternative approach is to set $f_{chop} << f_s$ and reduce the quantization noise at the modulator input, either by using a multi-bit digital-to-analog converter (DAC) [7,8], or by filtering the output of a 1-bit DAC with either an analog low-pass filter [1], or a finite impulse response (FIR) filter [9,10]. The ROIC architecture can then be simplified as shown in Figure 5.1b [1,7,8,10]. However, this approach requires a more complex DAC or feedback path, often resulting in lower energy-efficiency [1,7,10] or lower linearity [8] than the designs reported in [2,3]. Moreover, lowering

f_{chop} leads to larger chopper ripple, which may then require a high-order decimation filter or reduce the modulator's useful bandwidth [7,10].

We proposed a simple approach to prevent quantization noise fold-back in a chopped CTΔΣM by arranging the chopping transitions to coincide with the RZ phases of a resistive RZ DAC (Chapter 3). Simulations show that this approach works well and also allows f_{chop} to be flexibly chosen to match the modulator's $1/f$ corner frequency. In this chapter, we extend this approach to a CTΔΣM with an RZ capacitive DAC (CDAC) and present measurement results to demonstrate its effectiveness. The ROIC achieves a wide CM input range by using an embedded CCIA to sum the input signal and the output of the CDAC in the modulator. Measurement results show that compared to other capacitively coupled (CC) CTΔΣMs [7,10], the resulting design achieves state-of-the-art energy efficiency and linearity.

5.1 Chopped CC-CTΔΣM

5.1.1 CCIA inside the CTΔΣM Loop

Open loop integrators, such as Gm-C integrators or the combination of a Gm stage and a current-controlled oscillator (CCO) [1,7,8,10,12], are usually more energy-efficient than closed loop RC integrators. However, they have a much smaller linear range, typically only a few tens of millivolts and so are not compatible with the large output swing of a 1-bit DAC (Figure 5.2a). To reduce this, multi-bit DACs and extra filtering can be used in the feedback path of the modulator [7,8,10,12]. Moreover, the linearity of an open loop Gm stage can be improved through source-degeneration, although this comes at the expense of increased noise, i.e. reduced energy efficiency [1].

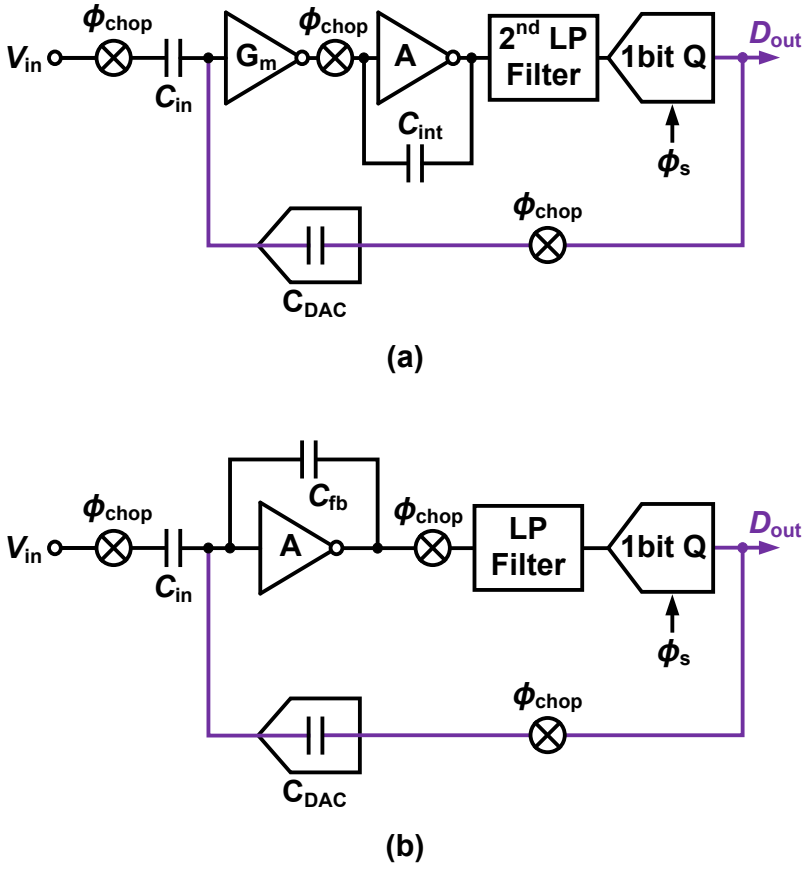

Figure 5.2: (a) CC-CTΔΣM chopped with a Gm-C integrator as the input stage, and (b) CC-CTΔΣM chopped with a CCIA inside the loop as the input stage.

Alternatively, the virtual ground of an energy-efficient CCIA can be used as the continuous-time summing node of the CTΔΣM (Figure 5.2b). Due to the local feedback provided by the CCIA, the voltage swing at its virtual ground will be quite small, and so it is compatible with the use of a 1-bit DAC. The gain of the CCIA will suppress the noise contributed during the succeeding stages of the modulator, and so the modulator's noise will still be dominated by a single stage. The requirements on the CCIA gain accuracy and linearity are quite relaxed, since it is within the modulator's overall feedback loop.

5.1.2 Chopping with a 1-bit RZ CDAC

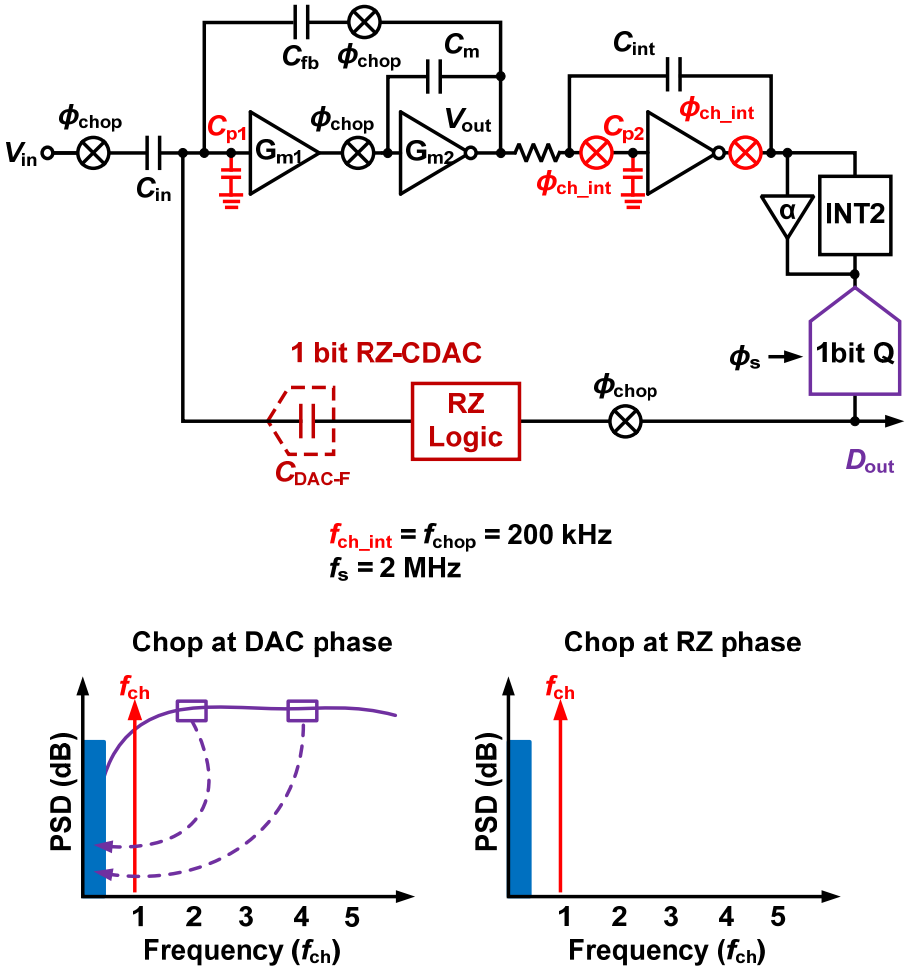

Figure 5.3: Chopping in the CC-CTΔΣM.

For a ROIC, as discussed in Chapter 3, a low frequency chopping of the CCIA is preferred, to avoid the side effects of higher chopping frequencies. Special care must be taken in this CC-CTΔΣM, since the output of the CCIA, V_{out}, contains both the input signal and the shaped quantization noise present in the DAC output. V_{out} is given by:

$$V_{\text{out}} = \frac{C_{\text{in}}V_{\text{in}} + C_{\text{DAC-F}}V_{\text{ref}}}{C_{\text{fb}}}, \tag{5.1}$$

where V_{ref} is the reference of the CDAC. As we know, the CCIA outputs spikes due to the finite output impedance. In a CC-CTΔΣM, these would be demodulated by the chopper at the feedback path, causing charge sampled by the parasitic capacitor at CCIA's virtual ground. Since the sampled charge is bitstream-dependent, this leads to quantization noise fold-back.

Fortunately, the idea proposed in Chapter 3, which breaks the bitstream dependency using an RZ DAC, can avoid such quantization noise fold-back. With an RZ CDAC (in Figure 5.3), the output of the CCIA can be rewritten as:

$$V_{\text{out\_RZ}} \cong \begin{cases} \dfrac{C_{\text{in}}V_{\text{in}} + C_{\text{DAC-F}}V_{\text{ref}}}{C_{\text{fb}}}, & \phi_{\text{RZ}} = 0 \\ \dfrac{C_{\text{in}}V_{\text{in}}}{C_{\text{fb}}}, & \phi_{\text{RZ}} = 1 \end{cases}. \tag{5.2}$$

By ensuring that the chopping transitions only happen during the RZ phase of the CDAC, that $V_{\text{out\_RZ}}$ is free of quantization noise, and thus free of quantization noise fold-back (in Figure 5.3).

Similarly, as discussed in Chapter 3, quantization noise fold-back also occurs because the OTA input capacitors C_{p2} need to be rapidly charged and discharged by V_{sum} whenever the choppers change state, which means that the quantization noise component is effectively sampled at $2f_{\text{ch\_int}}$. For the active OTA-RC integrator (Figure 5.3), the signal at the integrator's summing node is given by:

$$V_{\text{sum}} \cong \begin{cases} \dfrac{C_{\text{in}}/C_{\text{fb}} \times V_{\text{in}} + C_{\text{DAC-F}}/C_{\text{fb}} \times V_{\text{ref}}}{1 + g_{\text{m}} \cdot R_{\text{in}}}, & \phi_{\text{RZ}} = 0 \\ \dfrac{C_{\text{in}}/C_{\text{fb}} \times V_{\text{in}}}{1 + g_{\text{m}} \cdot R_{\text{in}}}, & \phi_{\text{RZ}} = 1 \end{cases}, \tag{5.3}$$

where ϕ_{RZ} = 1 corresponds to the R_Z phase. With this RZ CDAC, the chopping period can now be adjusted in steps of $1/f_s$, allowing f_{ch_int} to be optimally chosen with respect to the OTA's $1/f$ noise corner, optimizing the overall performance of the CC-CTΔΣM.

5.2 Circuit Implementation

Figure 5.4 shows a simplified block diagram of the proposed CTΔΣM. A CCIA is embedded in a 2nd-order CTΔΣM with a 1-bit RZ CDAC and 2 MHz sampling frequency. To suppress $1/f$ noise and offset, both the CCIA and the first integrator are chopped at 200 kHz during the RZ phase of the DAC. As in [2], the CCIA input chopper is driven capacitively, which allows it to handle input common-mode (CM) voltage of up to 3.3 V, even though the CCIA itself is powered from a 1.8 V supply. An extra DAC (C_{DAC1}) compensates for systematic bridge offset, thus maximizing the modulator's useful dynamic range. In an extension of the approach described in [2], a multi-path positive feedback network (C_{pf}, C_{DAC-C} and C_{DAC2}) supplies most of the current required to charge the input capacitors C_{in} of the CCIA, thus boosting the modulator's input impedance.

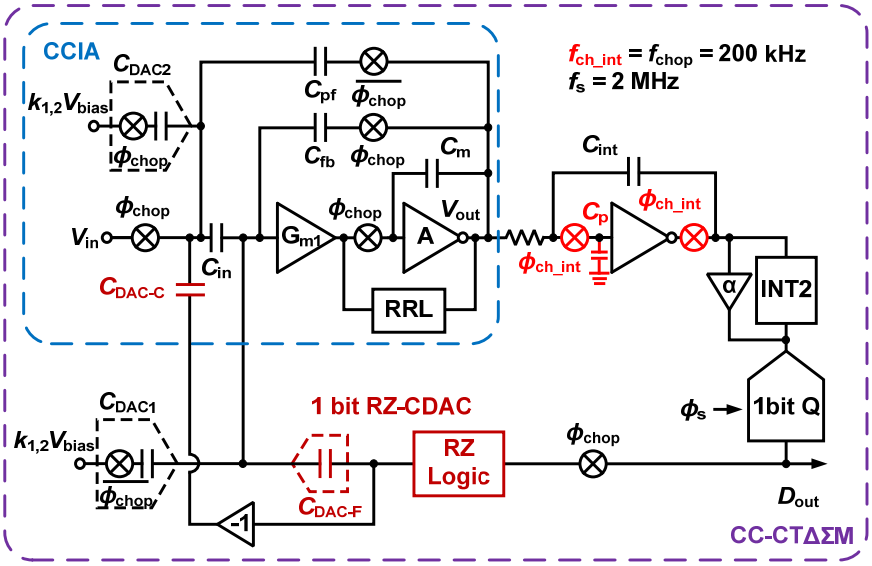

Figure 5.4: Chopping in CTΔΣMs.

5.2.1 CCIA

To drive the resistive load of the first integrator, the CCIA is based on a two-stage Miller-compensated amplifier. It employs a PMOS input pair to achieve a low 1/*f* noise corner (100 kHz). The closed loop gain of the CCIA is set to 50×, providing sufficient suppression of the noise in the modulator's succeeding stages.

Monte Carlo simulations show that the input-referred offset of the amplifier can be as high as 1.5 mV (3σ) without chopping. This offset is comparable to the input signal, and so the resulting chopper ripple may overload the modulator. To prevent this, a ripple-reduction-loop (RRL) is used to suppress the offset ripples [3].

5.2.2 Capacitively Coupled RZ DAC

The operation of the RZ logic is illustrated in Figure 5.5. The DAC output voltage, Vout, is reset to V_{cm} when ϕ_{RZ} is high. When ϕ_{RZ} is low, V_{out} is either pulled up to V_{refp} or pulled down to V_{refn} depending on the chopped bitstream, $\phi_{chop} \cdot bs$. The resulting tri-level voltage is then transferred via $C_{DAC\text{-}F}$ to the virtual ground of the CCIA, counterbalancing the input signal, which is transferred via C_{in}.

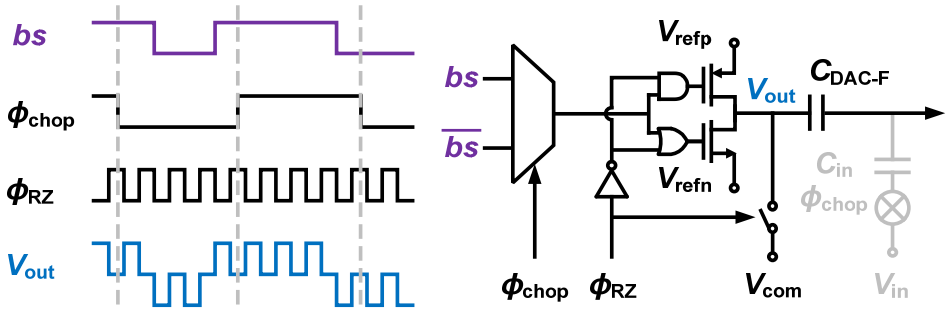

Figure 5.5: Simplified chopped RZ CDAC (single-end) and its timing diagram.

5.2.3 Multipath Impedance Boosting Circuits

Like the CCIA in [2], the input impedance Z_{in} of the CC-CTΔΣM would normally be defined by the switched-capacitor resistance associated with C_{in}, which is a few hundred kilo-Ohms at f_{chop} = 200 kHz. To boost Z_{in}, an auxiliary circuit must supply

the charge *Qin* that is required to charge and discharge C_{in} during every chopping transition. This can be done either by using a capacitively coupled positive feedback path [2,4], or an auxiliary pre-charge path [6]. However, the latter method requires active buffers, which will limit the input CM range of the CC-CTΔΣM and thus negate one of the main advantages of using a CCIA as the input stage.

In a conventional CCIA, a positive feedback path between the input and output can provide the required compensation charge, Q_{com}. This is given by [4]:

$$Q_{com} = C_{pf} V_{out} \approx C_{in} V_{in} = Q_{in} . \tag{5.4}$$

In general, V_{in} consists of two parts: the useful bridge signal, V_{sig} and the unwanted bridge offset, V_{os}. In the proposed modulator (Figure 5.4), V_{os} will be cancelled by C_{DAC1} before amplification and so it cannot be extracted from V_{out}. Moreover, V_{out} contains the additional DAC signal, which should not be fed to the CCIA input.

To generate the required offset compensating charge Q_{os} and DAC charge Q_{DAC}, a multipath input impedance boosting scheme is used. As shown in Figure 5.4, the scheme consists of two extra digital controlled paths (C_{DAC2} and C_{DAC-C}) as well as the conventional analog positive feedback path via C_{pf}. The resulting compensation charge Q_{com} is then given by:

$$Q_{com} = C_{pf} V_{out} + Q_{os} - Q_{DAC} \approx Q_{in} . \tag{5.5}$$

5.3 Measurement Results

The CC-CTΔΣM has been implemented in a 0.18 μm CMOS technology. It occupies an active area of 0.75 mm^2 as shown in Figure 5.6. With f_s = 2 MHz and f_{chop} = 200kHz, it consumes 1.2 mA from a 1.8 V supply.

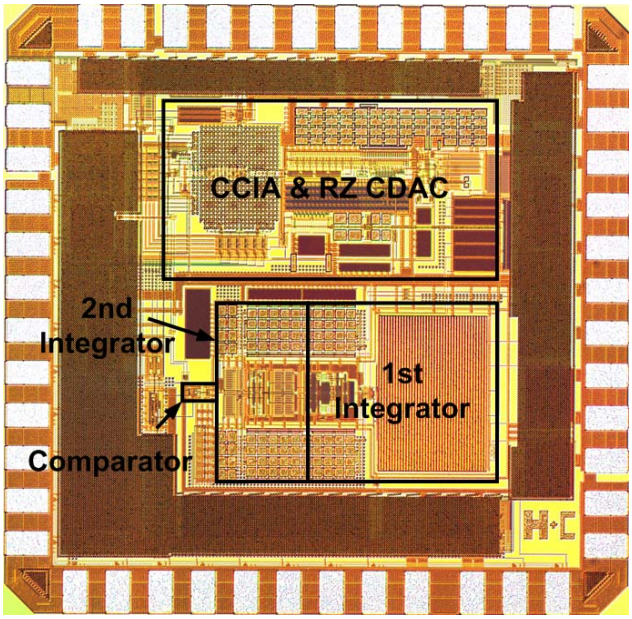

Figure 5.6: Die micrograph of the CC-CTΔΣM.

To verify the effectiveness of the proposed chopping scheme, the chopping transitions of the CCIA and the first integrator can be arranged to coincide with either the RZ or the DAC phases of the CDAC. As shown in Figure 5.7, when the CCIA is chopped during the DAC phase, severe quantization noise fold-back can be observed. It should be noted that in this case the modulator is also overloaded by chopper ripple. This is because the RRL now senses chopped quantization noise as well as up-modulated offset ripple and hence fails to settle properly.

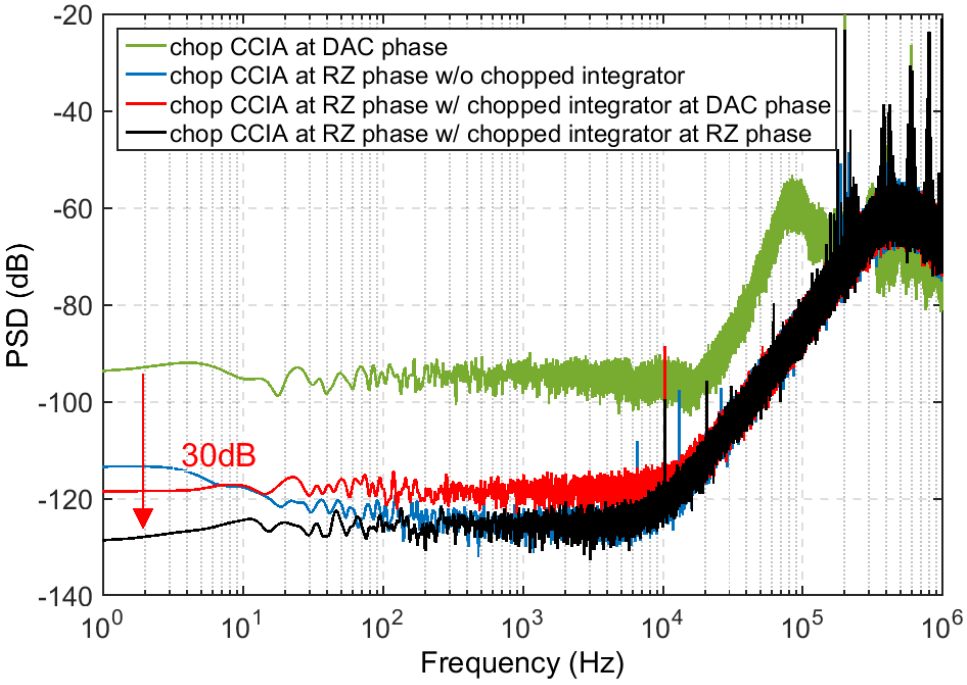

Figure 5.7: Measured bitstream PSD when the CCIA is chopped during the DAC phase (green), during the RZ phase (blue), then with the first integrator chopped during the DAC phase (red), and with the first integrator chopped during the RZ phase (black).

Chopping the CCIA during the RZ phase reduces the in-band noise floor by about 30 dB to 4.5 nV/√Hz, as shown in Figure 5.7. The corresponding 200 Hz 1/*f* noise corner can be reduced to about 0.05 Hz also by chopping the first integrator. The bitstream spectra are also shown when the first integrator is chopped during the RZ and DAC phases. It can be seen that despite the CCIA gain (50×), chopping during the RZ phase still produces significant improvements, while reducing the input-referred in-band noise by 8 dB.

To qualify the modulator as a ROIC, 10 samples were measured. As shown in Figure 5.8a, it achieves a relative gain error of 0.2% and a measured INL of 15 ppm over the full input range (Figure 5.8b). To capture the effects of finite input impedance, a voltage source with a 2 kΩ impedance (the impedance of the targeted Wheatstone bridge sensor) was used for the INL measurements. As in [2], the

multipath input impedance boosting scheme boosts the input impedance of the modulator by a factor of 5 to about 1.2 MΩ.

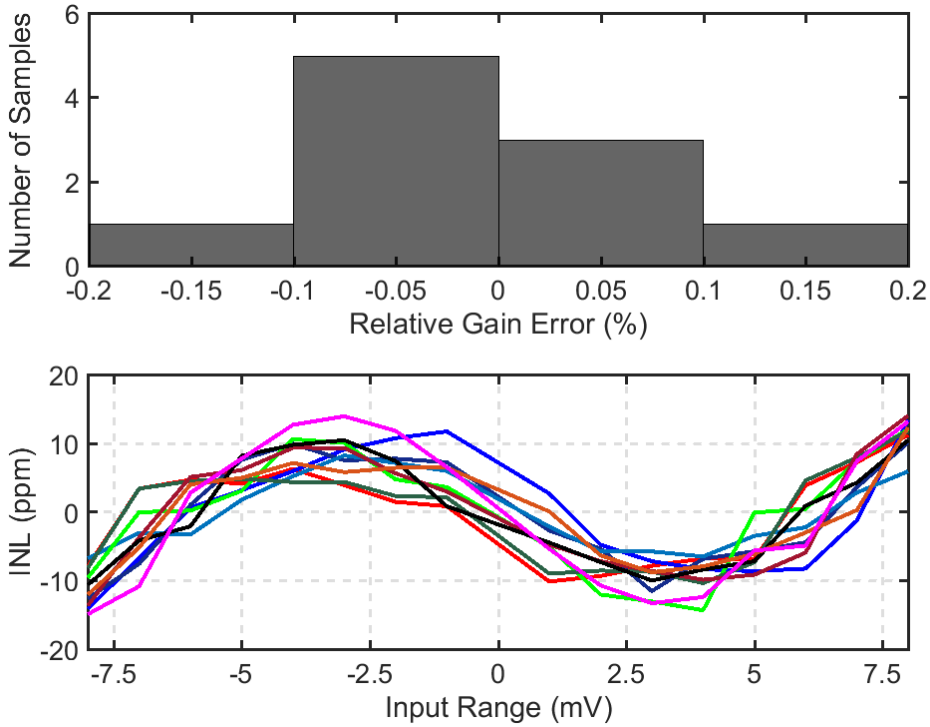

Figure 5.8: Measured relative gain accuracy of 10 samples (a), and measured INL of 10 samples (b).

Table 5.1. State-of-the-Art ROICs

	[1]	[2]	[7]	[10]	This work
Architecture	Gm-C CTΔΣM	CCIA+ CTΔΣM	CC-CTΔΣM	CC-CTΔΣM	CC-CTΔΣM
Year	2012	2017	2017	2017	2017
Input Stage	PMOS	PMOS	PMOS	PMOS	PMOS
Technology	0.7 μm	0.18 μm	40 nm	0.18 μm	0.18 μm
Supply Voltage (V)	5	1.8	1.2	1.8	1.8
Current (mA)	0.24	1.2	0.0175	0.070	1.2
±Input Range (mV)	40	10+120(DC)	50	40	8+120(DC)
CM Input Range (V)	0–2.5	0–3.3	0–1.2	0–1.8	0–3.3
INL (ppm)	15	28	79[1]	84[1]	15
Offset (μV)	1	7	300	50	< 74
Offset Drift (nV/°C)	--	12.5	--	--	12.3
Input Noise Density (nV/√Hz)	20	3.7	140	98	4.5
NEF	12	5.0	22.6	31.9	6.1

1. Estimated from THD.

In Table 5.1, the performance of the CC-CTΔΣM is summarized and compared with that of other state-of-the-art ROICs. Compared to other ADCs designed for ROIC, it achieves the best INL and noise efficiency factor (NEF). Compared to [2], which employs a separate CCIA as a pre-amplifier, its offset is relatively high, mainly due to the interaction between the mismatch of the differential CDAC capacitors (about 0.36%) and the 1.8 V reference voltage. However, it is negligible compared to the millivolt-level offset of typical Wheatstone bridge sensors. It is also quite stable, with an offset drift of < 12.5 nV/°C, and so can be well tolerated in many applications.

5.4 Conclusions

In this chapter, measurement results show that quantization noise fold-back caused by chopping a CTΔΣM can be greatly suppressed by chopping during the return-to-zero phases of an RZ DAC. The proof-of-concept modulator employs a novel architecture in which a CCIA is used as the summing node of a CTΔΣM, thus enabling the use of a simple 1-bit RZ CDAC to achieve both energy-efficiency (NEF = 6.1) and high linearity (INL of 15 ppm).

5.5 Bibliography

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A Temperature-Compensated Pressure Sensing System

As discussed in chapter 1, bridge-type piezoresistive pressure sensors are sensitive to ambient temperature variations [1]. Therefore, in precision applications, the power dissipation of the ROICs, which is typically located close to the sensor, is quite limited [2,3]. However, state-of-the-art ROICs for pressure sensors [4-8] are not sufficiently energy efficient, resulting in an excessive power or noise budget. For instance, the ROIC reported in [7], which consists of an instrumentation amplifier and a 15-bit ADC, dissipates 5.7 mW and achieves a noise floor of 39 nV/√Hz. When combined with the AC4010, the ROIC dissipates about 46% of the total system power and contributes about 82% of its noise power.

To improve system accuracy and stability, the entire pressure sensing system can be calibrated over temperature. This involves measuring the output of the system at a number of well-defined temperatures. The sensor's drift can then be corrected if the ambient temperature is known, e.g., with the help of an additional temperature sensor, as shown in Figure 6.1. However, the calibration accuracy will be limited by

This chapter is derived from a journal publication of the authors: H. Jiang, S. Nihtianov and K. A. A. Makinwa, "An Energy-Efficient 3.7 nV√Hz Bridge Readout IC With a Stable Bridge Offset Compensation Scheme," in IEEE Journal of Solid-State Circuits, vol. 54, no. 3, pp. 856-864, March 2019.

the temperature sensor's inaccuracy and the imperfect thermal coupling between the pressure sensor and temperature sensor, since they will usually be implemented as separate devices [7-9]. In [8], the pressure sensing system achieves a typical residual offset of 0.5 %FS (full-scale) with a drift of 71.4 ppm/°C after the calibration using an on-chip temperature sensor.

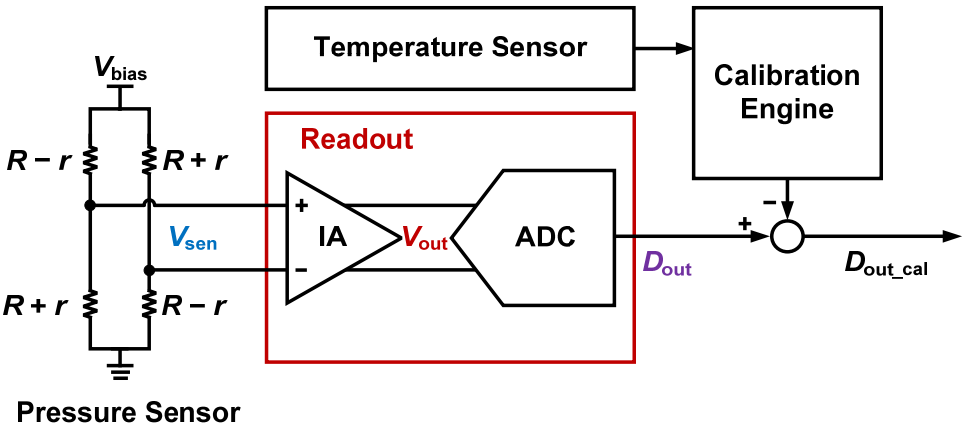

Figure 6.1: Pressure sensing systems.

This chapter presents a pressure sensing system, built with a differential pressure sensor (AC4010 [1]), the ROIC (Chapter 4), and a calibration engine. In this system, the ROIC dissipates 2.85 mW and achieves a noise floor of 3.7 nV/√Hz, which corresponds to about 30% of the total system power and about 6% of its noise power. This is significantly better than [7]. To reduce the sensor's offset drift, a temperature calibration scheme based on an external reference resistor is used. After a 2-point calibration, this scheme reduces bridge offset to 3 µV over 50 °C, which corresponds to 0.067% FS with a drift of 13.4 ppm/°C.

The rest of the chapter is organized as follows. Section 6.2 introduces the measurement setup and presents the system's measured transfer characteristic and resolution. The temperature calibration and the associated measured results are presented in Section 6.3. Section 6.4 discusses the performance of the pressure sensing system and compares it with the state-of-the-art. The chapter ends with conclusions.

6.1 Pressure Resolution Measurement

As shown in Figure 6.2, the water-level difference in a U-tube manometer can be precisely controlled by a linear stage to create a well-defined differential pressure [5]. Moving the right leg of the U-tube manometer relative to the left one by ±10 mm with a 2.5 mm step, resulting in a total differential pressure change of ±100 Pa in steps of 25 Pa.

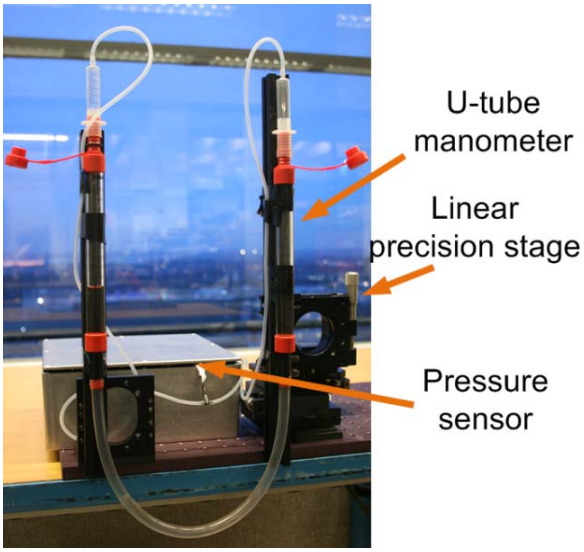

Figure 6.2: Differential pressure measurement setup.

To obtain sufficient sensitivity, the bridge sensor (AC4010) is biased by a 5 V voltage. Under these conditions, it output changes by ± 4.5 mV in response to a ±100 Pa differential pressure change. It has a resistance of 3.7 kΩ, and therefore dissipates 6.76 mW. The integrated noise of the sensor over a 1 kHz bandwidth is about 0.462 μVrms, limiting the pressure resolution to about 10 mPa. On the other hand, the ROIC, described in chapter 4, is powered by a 1.8 V supply, consuming about 2.9 mW and contributing an input referred noise about 0.117 μVrms integrated with 1 kHz bandwidth. This means that, in the system, the ROIC dissipates about 30% of the total power and contributes about 6% of overall noise power.

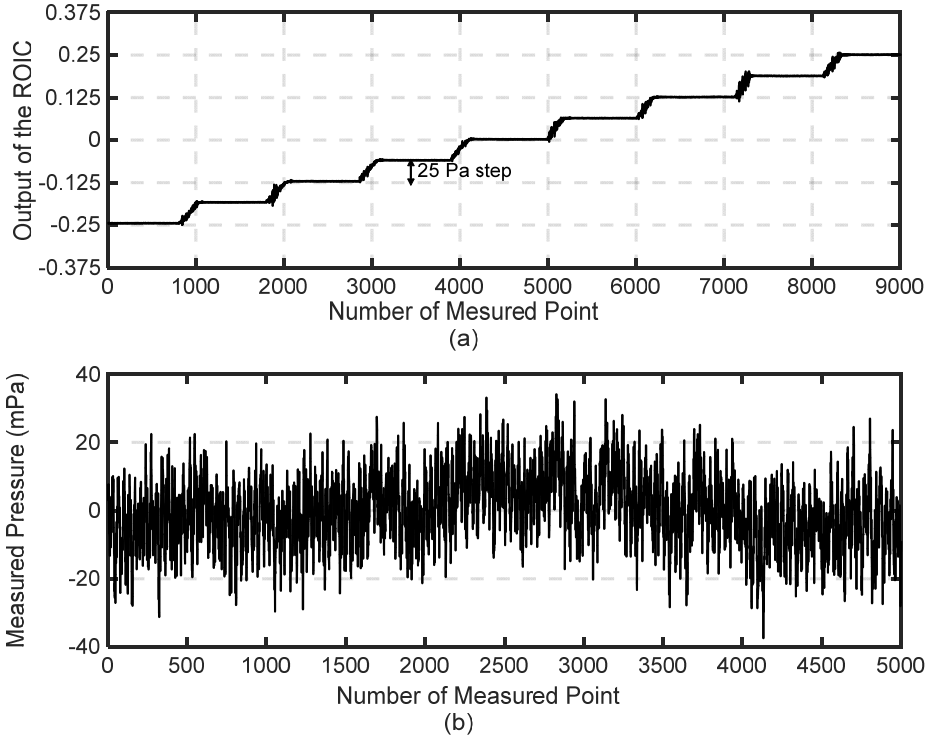

Figure 6.3: Measurement results of the sensing system: (a) decimated output of the ROIC with swept pressure input (the residual offset has been subtracted) and (b) with zero pressure input (shorted, the residual offset has been subtracted).

The real-time response of the sensing system is shown in Figure 6.3a. The pressure sensing system has a pressure sensitivity of 0.0025 (1/Pa). To evaluate the system's resolution while avoiding mechanical interference from the environment, the differential pressure inputs of the sensor were mechanically connected. The pressure resolution, obtained from the standard deviation of 5000 samples (decimated by $sinc^3$ filter with a length of 1000), is found to be 10.1 mPa with a 0.5 ms conversion time for each decimated sample (Figure 6.3b).

6.2 Temperature Calibration

Like other resistive type sensors, piezoresistive pressure sensors exhibit significant temperature dependency. The bridge resistance R_b of the pressure sensor can be approximated by a linear function of temperature T

$$R_b = R_{b0} \times (1 + TCR \times (T - T_0)), \tag{6.1}$$

where TCR is the temperature coefficient of resistance of the pressure sensor, and R_{b0} is its nominal value at temperature T_0. In [1], the typical TCR is 2800 ppm/°C and R_{b0} is 3.7kΩ. By combining a full Wheatstone bridge configuration with ratiometric readout [10], the temperature dependency of the system can be greatly reduced. However, for precision applications, the residual temperature errors are often too large and so calibration is required. For example, the AC4010, biased at 5 V, has a worst-case offset drift of 125 μV/°C, leading to a pressure readout error of 2.8 Pa/°C which is more than 2 orders of magnitude larger than the targeted resolution (10 mPa).

One generally used method to correct for a sensor's temperature dependency, is to measure the temperature of the sensor and then use a correction curve, or look-up table, which is usually provided by the sensor manufacturer. This then requires the use of an additional temperature sensor, or operation at a fixed temperature in a thermally stabilized environment, both of which increase system complexity and cost.

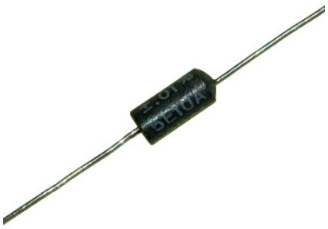

Figure 6.4: Photos illustrating (a) wirewound resistor (courtesy of [13]).

An alternative approach is to use the bridge itself as a temperature sensor, considering that its *TCR* itself is relatively high [1]. This can be done by monitoring the current through the bridge, e.g. by measuring the voltage drop across a low *TCR* shunt resistor inserted in series with the bridge. Wire-wound resistors (Figure 6.4) are well-suited for this purpose, since they can achieve low tolerance (±0.01%), excellent stability (±50 ppm/year) and low *TCR* (5 ppm/°C) by using a low *TCR* alloy and tight control of the fabrication process [12,13].

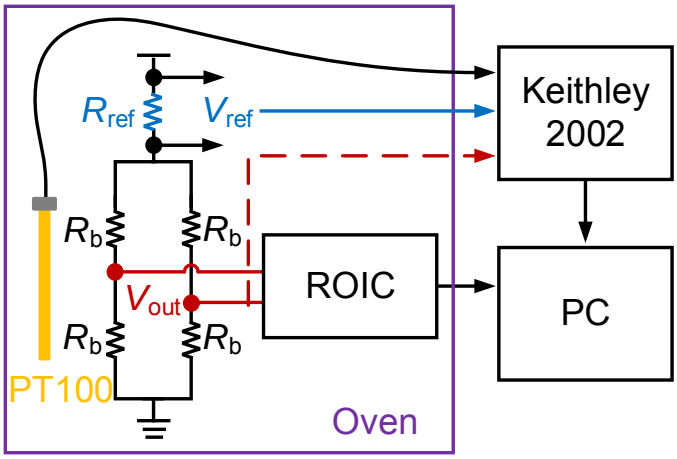

Figure 6.5: Bridge sensor with a reference resistor for temperature calibration.

Both temperature calibration methods are evaluated and compared in the same measurement. As shown in Figure 6.5, to calibrate the bridge resistance over temperature, both the bridge sensor and the ROIC were placed in an oven-stabilized aluminum block next to a PT100 thermometer. To achieve high sensitivity to pressure, the bridge sensor and the shunt resistor, R_{ref} (100 Ω and ±3 ppm/°C) are powered from a 5 V supply. The voltage across the shunt resistor was read out by Keithley 2002 [14].

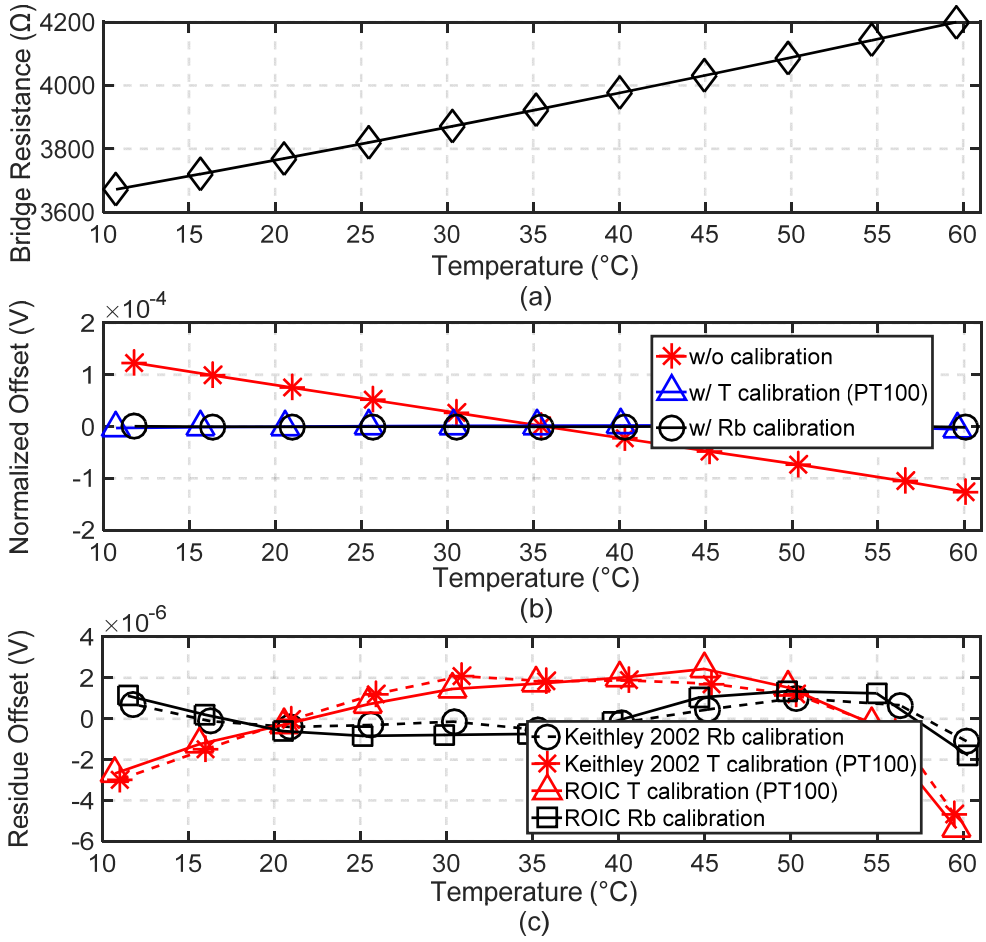

Figure 6.6: Measured (a) bridge resistance over temperature, bridge offset drift b) before and after calibration, and c) the residual offset drift.

The effectiveness of the resulting calibration was tested by first measuring the bridge sensor's offset drift and bridge resistance over temperature, this results in a *TCR* of 2682 ppm/°C (Figure 6.6a). When an external temperature sensor (PT100) is combined with a 2-point calibration, the sensor's offset decreases from 244 µV over a 50 °C range to 7 µV (or 0.156%FS). When the sensor's resistance is used as a sensor, the residual offset decreases by a further 2×, to only 3 µV (or 0.067%FS) as shown in (Figure 6.6b). In latter case, the corresponding drift is about 13.4 ppm/°C. The output of the bridge was also directly measured with a Keithley 2002 benchtop voltmeter (Figure 6.5). As shown in Figure 6.6c, the residual errors obtained by the

ROIC (solid curves) are in good agreement with those obtained by the Keithley 2002 (dashed curves), further demonstrating the precision of the ROIC.

6.3 Comparison

Table 6.1 summarizes the performance of the pressure sensing system and compares it with the state-of-the-art. In [4], a duty-cycled method to digitize a 6 kΩ bridge sensor with ultra-low power consumption is presented, which is promising for IoT devices where the power budget is greatly constrained. However, precision applications require not only minimal power consumption but also high resolution. The proposed sensing system achieves 10.1 mPa (1σ) resolution, mainly limited by the pressure sensor's thermal noise and 1/*f* noise, with a 0.5 ms conversion time.

Table 6.1 State of the Art Pressure Sensing System.

Reference No.	[4]	[5]	[6]	[7]	[8]	This work
Year	2018	2017	2015	2015	2018	2019
Sensor supply (V)	3.6	5	3.6[3]	5	5	5
P_{System} (mW)	0.0025	16.3[2]	19.3[4]	12.5	20	9.6[2]
Conversion time (ms)	4	0.5	0.5	1	1	0.5
Pressure range (Pa)	106658	±110	±100	±1000	±100	±100
Pressure resolution (mPa)	146654	12.7[4]	14.8	21.6[4]	3.1[5]	10.1
P_{ROIC}/P_{System}	80%	59%	82%	46%	66%[1]	30%
N_{ROIC}/N_{System}	99%[1]	38%	17%	82%[1]	--	6%
Offset drift (ppm/°C)	--	--	--	214	71.4	13.4

1. Estimated based on the references.
2. Power of the calibration is not considered.
3. Power consumption of the calibration block is not included.
4. AC4010 is considered here.
5. The sensor used in [8] has about 4× higher sensitivity than the sensor in this work [1,7].

After a 2-point temperature calibration, the residual offset of the system is around 0.067%FS from 10 °C to 60 °C, resulting in a drift of 13.4 ppm/°C. Although the calibrated temperature range is smaller than [7] and [8], it is sufficient for use in precision applications such as wafer steppers [2]. The power dissipation of the calibration block has not been considered in this work. However, in most cases, it can be located far away from the sensor and the ROIC, and so there are no significant constraints on its power dissipation.

6.4 Conclusions

The ROIC described in Chapter 4 has been combined with a piezoresistive differential pressure sensor to realize a complete pressure sensing system. The ROIC dissipates 2.85 mW and achieves a noise floor of 3.7 nV/√Hz, which corresponds to about 30% of the system's power consumption and about 6% of its input-referred noise power. After a 2-point temperature calibration with an external reference resistor, the residual offset drift is about 13.4 ppm/°C, 5× better than [8].

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Conclusions

This final chapter presents a benchmark for ROICs regarding their energy-efficiency, summarizes the main findings, and discusses the original contributions of this thesis. It also discusses how some of the techniques developed for ROICs can also be applied to other applications and provides an outlook on future work.

7.1 Benchmark with the State-of-the-Art ROICs

The performance of the two ROICs presented in this thesis is compared to the state-of-the-art ROICs published over the last decade [1-18]. The main architectures are IA only [1-6], IA+ADC [7-12], and direct bridge-to-digital conversion [13-18]. Figure 7.1 plots the NEF, defined by Eq. 1.3, as a function of the input-referred noise PSD, as reported in the references. This figure shows that the ROICs presented in this thesis (Chapter 4 [19] and Chapter 5 [20]) achieve state-of-the-art performance in terms of energy efficiency. This confirms the effectiveness of the techniques proposed in this thesis.

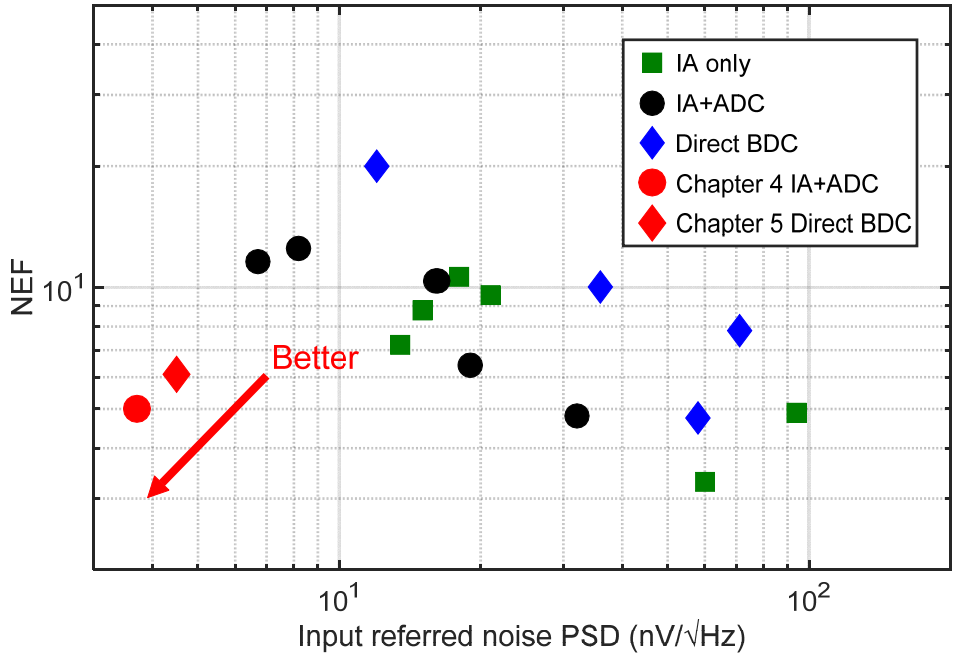

Figure 7.1: Survey of the energy efficiency of the bridge ROIC and benchmark of the readouts presented in this thesis.

Apart from achieving high energy efficiency, the capacitively coupled input stages of the proposed ROICs naturally block CM input voltages, allowing them to handle CM levels much larger than their supply. This means that the Wheatstone bridge sensor and the ROIC can be powered from different voltage supplies, allowing the ROIC's supply voltage to be optimized for energy efficiency.

7.2 Main Findings

- A CCIA can be highly energy-efficient, however, digitizing its output may degrade its energy efficiency (Chapters 2 and 4).
- CCIA output spikes cause nonlinearity and drift (Chapter 4).
- Quantization noise fold-back, due to chopping, can be analyzed in the time domain and can be significantly reduced by chopping at the correct moment (Chapters 3 and 5).
- Measuring the temperature dependent resistance of a piezoresistive bridge-type sensor is a better way to compensate for its temperature drift compared to the use of an external temperature sensor (Chapter 6).

7.3 Original Contributions

- A known drawback of CCIAs is that they output spikes at twice the chopping frequency $2f_{chop}$. These spikes can be avoided by synchronously sampling the CCIA output with a DTΔΣM. However, this limits the sampling frequency fs to $2f_{chop}$(=400kHz), thus limiting modulator resolution (for a given topology). On the other hand, synchronously over-sampling the CCIA output, while possible, would require more output current, and hence, lead to worse energy efficiency. To overcome these drawbacks, a gated CTΔΣM has been designed, whose input is gated to avoid CCIA spikes while still sampling at f_s = 2 MHz. With a 3.7 nV/√Hz input-referred noise power spectral density and a power efficiency factor of 44.1, this ROIC is about 5× more efficient than the state-of-the-art (Chapter 4).
- The offset and 1/*f* noise of a CTΔΣM usually results in relatively lower energy efficiency. In principle, chopping can overcome this limitation. However, a chopped CTΔΣM causes fold-back of quantization noise to the signal band. Solutions based on a frequency-domain analysis have been proposed in the literature, e.g. using $f_{chop}=f_s$, using a multi-bit digital-to-analog converter (DAC), and using a finite impulse response (FIR) DAC [21]. However, choosing $f_{chop}=f_s$ leads to a high chopping frequency () and thus to high residual offset and current noise. On the other hand, multi-bit DAC or FIR DAC solutions increase design complexity. In this thesis, a

solution based on a time-domain analysis is proposed. The idea is that aliasing can be avoided by synchronizing the chopping with the zero-levels of a return-to-zero DAC. Since such DACs are often used in CTΔΣMs for their superior robustness to inter-symbol-interference, the proposed solutions greatly simplify the design of the chopped CTΔΣM (Chapter 3 in [22]).

- Open-loop integrators, such as Gm-C integrators or the combination of a Gm stage and a current-controlled oscillator [9,14,16,17,23], are typically more energy-efficient than closed-loop RC integrators. However, they have a much smaller linear range, typically only a few tens of millivolts and so are not compatible with the large output swing of a 1-bit DAC. To reduce this, multi-bit DACs and extra filtering can be used in the feedback path of the modulator [13,14,16-18]. Moreover, the linearity of an open-loop Gm stage can be improved with source-degeneration, although this comes at the expense of increased noise, i.e. reduced energy efficiency. Alternatively, the virtual ground of an energy-efficient CCIA can be used as the continuous-time summing node of a CTΔΣM. Due to the local feedback provided by the CCIA, the voltage swing at the virtual ground will be quite small, and so it is compatible with the use of a 1-bit DAC. The gain of the CCIA will suppress the noise contributions of the modulator's succeeding stages, and so the modulator's noise will still be dominated by a single stage. The requirements on the CCIA gain accuracy and linearity are quite relaxed since they are within the modulator's overall feedback loop. A capacitively-coupled CTΔΣM has been designed, in which a CCIA is embedded inside the modulator loop. Compared to other capacitively-coupled ADCs designed for bridge readout, our design achieves the best INL and NEF (Chapter 5).

7.4 Future Work

The ROICs and the techniques proposed in this work can be further improved or extended by means of future work at the system and circuit level. Some possible topics are suggested:

- Although the residual offset after the ROIC bridge offset compensation is stable, it is in mV-range, which is limited by the minimum capacitance value that could be realized in the chosen technology. One way of achieving less

residual offset is to add an LSB CDAC that injects a small amount of charge into the virtual ground of the CCIA during a conversion. The exact amount of charge can be determined by nulling the bridge sensor's output during a charge-balancing calibration phase.

- A CTΔΣM based on a single-bit DAC is sensitive to clock jitter. A multi-bit DAC [16] or FIR DAC [21] can be used to relax the jitter requirement, while also providing extra resolution.
- The CC-ROICs can be used in many other sensing applications with voltage output, such as temperature sensing, bio Bioelectrical impedance sensing, current sensing. For example, in high side current sensing, the CC-ROIC can be used to obtain similar beyond-the-rails capability as [24], while achieving higher energy-efficiency or smaller area due to its CT nature. By taking advantage of the fact that the shunt resistance is quite small (tens of mΩ), input impedance boosting will not be required, thus simplifying the design.
- The CCIA could be easily configured as a Capacitance-to-Voltage Converter (CVC) by replacing its C_{in} with a capacitive sensor. Such a CVC could be used for microphone readout [25]. When a reconfigurable readout for both a Wheatstone bridge sensor and a capacitive sensor is required, the CC-ROIC architecture might be a promising way to achieve high precision and high energy-efficiency.

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Summary

This Ph.D. dissertation describes the design and realization of energy efficient readout integrated circuits (ROICs), that have an input referred noise density < 5 nV/√Hz and a linearity of < 30 ppm, as required by Wheatstone bridge sensors used in precision mechatronic systems. Novel techniques were developed, at both the system-level and circuit-level, to improve the ROIC's energy-efficiency, while preserving its stability and precision. Two prototypes are presented, each with best-in-class energy efficiency, to demonstrate the effectiveness of the proposed techniques.

Chapter 1

Chapter 1 gives an introduction to this thesis and provides motivation for this work. The basics of Wheatstone bridge sensors and their ROICs are explained. Wheatstone bridge sensors, which convert resistance (or impedance) variations into differential output voltages (or currents), are widely used due to their simplicity, stability, and accuracy. However, the design of ROICs, typically consisting of an instrumentation amplifier (IA) and an analog-to-digital converter (ADC), can be quite challenging. This is especially true in battery-powered sensing systems, and when self-heating

must be kept to a minimum, e.g. in precision mechatronic systems. Due to its gain, the IA of a ROIC usually determines its noise performance, and thus its energy efficiency. When the research described in this thesis started, however, state-of-the-art capacitively-coupled IAs (CCIAs) where 3× more energy-efficient than state-of-the-art ROICs, indicating an opportunity to improve the efficiency of the latter.

Chapter 2

Chapter 2 presents a review of energy-efficient ROICs, and discusses the architectural and circuit-level innovations that have advanced the state of the art. Apart from achieving good energy-efficiency, ROICs must achieve low input-referred offset, noise and drift, high gain accuracy, stability, linearity, as well as high immunity to power-supply and common-mode variations. Various ROIC architectures are discussed, beginning with conventional designs, in which an IA is used to drive an ADC, and moving on to more recent work, that attempt to increase energy efficiency and reduce complexity by eliminating the IA. The performances of these topologies, and in particular their energy-efficiency, are compared and summarized.

Chapter 3

In CMOS technology, IAs suffer from 1/*f* noise at low frequencies, which are usually also within the signal band of Wheatstone bridge sensors. This, in turn, degrades their energy efficiency. In addition, their offset and drift also degrade readout stability. To reduce in-band 1/*f* noise, offset, and offset drift of the IAs, chopping is often applied. However, several secondary effects of chopping need to be considered in precision applications.

Continuous-time delta-sigma modulators (CTΔΣMs) are well suited for use in bridge readout circuits, due to their greater energy efficiency and inherent anti-aliasing behavior compared to their discrete-time counterparts. To obtain low noise at low frequency, chopping is also required in CTΔΣMs. Although chopping has been successfully implemented in IAs, it is known to cause undesirable artifacts when used in CTΔΣMs, namely fold-back of quantization noise to the signal band.

In Chapter 3, the problems, associated with chopping, are analyzed. And two solutions to the fold-back of quantization noise are proposed. One based on a

return-to-zero (RZ) digital-to-analog converter (DAC), and the other based on a switched-capacitor (SC) DAC. Since such DACs are often used in CTΔΣMs for their superior robustness to inter-signal-interference (ISI), the proposed solutions can be integrated into any CTΔΣM without introducing significant overhead.

Chapter 4

Chapter 4 describes the first prototype, which consists of a CCIA that drives a CTΔΣM. By exploiting the CCIA's ability to block dc common-mode voltages, the bridge's bias voltage may exceed the ROIC's supply voltage, allowing these voltages to be independently optimized. Since the bridge output voltage is typically much smaller than the bridge offset voltage, a DAC is used to compensate the offset before amplification and increase the CCIA's dynamic range. Bridge loading is reduced by using a dual-path positive feedback scheme to boost the CCIA's input impedance. Furthermore, the CCIA's output is gated to avoid digitizing its output spikes, which would otherwise limit the ROIC's linearity and stability. The ROIC achieves an input-referred noise density of 3.7 nV/√Hz, a noise efficiency factor (NEF) of 5, and a power efficiency factor (PEF) of 44, both of which are state of the art.

Chapter 5

In Chapter 5, the second prototype, which extends and implements the technique explained in Chapter 3, is presented. To achieve a wide common-mode input range, the modulator's summing node is implemented as an embedded CCIA which can be readily combined with a highly linear 1-bit capacitive RZ DAC. Measurements show that the proposed chopping scheme does not suffer from quantization noise fold-back and also allows a flexible choice of chopping frequency. When chopped at one-tenth of the sampling frequency, the modulator achieves 15 ppm INL, 4.5 nV/√Hz input-referred noise and a state-of-the-art NEF of 6.1.

Chapter 6

Chapter 6 presents a pressure sensing system built with a differential pressure sensor (AC4010), the ROIC (Chapter 4), and a calibration engine. In this system, the ROIC dissipates 2.85 mW and achieves a noise floor of 3.7 nV/√Hz, which corresponds to about 30% of the total system power and about 6% of its noise power. This is significantly better than the prior art. To reduce the sensor’s offset drift over temperature, a temperature calibration scheme based on an external reference

resistor is used. After a 2-point calibration, this scheme reduces bridge offset to 3 μV over 50 °C, which corresponds to 0.067% FS with a drift of 13.4 ppm/°C.

Chapter 7

This final chapter presents a way of benchmarking ROICs in terms of their energy-efficiency. Both the proposed ROICs achieve state-of-the-art energy efficiency, thus demonstrating the effectiveness of the techniques proposed in this thesis. Apart from this, the capacitively coupled input stages of the proposed ROICs block common mode (CM) input voltages, allowing them to handle CM levels much larger than their supply. This allows the bridge sensor and the ROIC to be powered from different voltage supplies, and allows the ROIC's supply voltage to be further optimized.

The chapter also contains a summary of the main findings and the original contributions of this thesis. It also discusses how some of the techniques developed for ROIC circuits can be applied to other applications and provides an outlook on future work.

Samenvatting

Deze Ph.D. dissertatie beschrijft het ontwerp en de realisatie van energie-efficiënte geïntegreerde uitleescircuits (ROICs), die een ingangs-gerefereerde ruisdichtheid hebben van < 5 nV/√Hz en een lineariteit van < 30 ppm, zoals benodigd in Wheatstone brugsensoren die gebruikt worden in precisie mechatronische systemen. Nieuwe technieken zijn onderzocht op zowel systeem- als circuitniveau, om de energie-efficiëntie van de ROIC te verbeteren en tegelijkertijd de stabiliteit en precisie te behouden. Twee prototypes worden gepresenteerd, beide met een energie-efficiëntie die onder de beste in zijn klasse valt, om zo de effectiviteit van de voorgestelde technieken te demonstreren.

Hoofdstuk 1

Hoofdstuk 1 geeft de introductie van dit proefschrift en geeft de motivatie voor dit werk. De basis van de Wheatstone brugsensor en de bijbehorende ROICs worden uitgelegd. Wheatstone brugsensoren zetten de variatie in weerstand (of impedantie) om in een differentiële spanning (of stroom) en worden wijd gebruikt vanwege hun eenvoud, stabiliteit en accuraatheid. Het ontwerp van ROICs, vaak bestaande uit een instrumentatieversterker (IA) en een analoog-digitaalomzetter (ADC), wordt echter steeds uitdagender. Dit wordt voortgedreven door de recente snelle toename van het aantal batterijgevoede meetsystemen en de voortdurende noodzaak om zelf-verwarmingsfouten in precisie mechatronische system te reduceren. In een ROIC bepaald de IA normaalgesproken de ruisprestatie en daarmee de energie-efficiëntie,

door de hoge versterking. Echter de state-of-the-art IA, een capacitief-gekoppelde IA (CCIA), is 3× energie-efficiënter dan de state-of-the-art ROIC. Dit benadrukt de behoefte aan verder verbeteringen in de energie-efficiëntie van ROICs. Het overbruggen van het overgebleven gat met de prior art, blijft echter nog steeds een uitdaging.

Hoofdstuk 2

Een overzicht van energie-efficiënte ROICs wordt in Hoofdstuk 2 gegeven, met het doel de innovaties op architectuur- en circuitniveau uit te leggen die de state of the art hebben voortgedreven. Naast het bereiken van een goede energie-efficiëntie, moeten ROICS ook een lage ingangs-gerefereerde offset, ruis en drift, hoge versterkingsaccuraatheid, stabiliteit, linearieit als mede een hoge immuniteit tegen voedingsspanning- en common-mode-variaties hebben. Verschillende ROIC architecturen worden besproken, beginnend met de conventionele ontwerpen, waarin een IA een ADC aanstuurt. Vervolgens worden de meer recente werken besproken, die proberen de energie-efficiëntie te verhogen en de complexiteit te verminderen door de IA te elimineren. De prestaties van deze topologieën, met name op het gebied van hun energie-efficiëntie, worden vergeleken en samengevat.

Hoofdstuk 3

IAs geïmplementeerd in CMOS technologieën hebben bij lage frequenties last van 1/*f* ruis, die normaal gesproken binnen de signaalbandbreedte van brugsensoren ligt. Dit zorgt voor een degradatie van de energie-efficiëntie van ROICs. Daarnaast degraderen de offset en drift ook de uitlees-stabiliteit. Om de inbandige 1/*f* ruis en offset drift van de IAs te verminderen wordt chopping vaak toegepast. Bij precisietoepassingen moet men daarbij echter enkele tweede-orde effecten van chopping in acht nemen. In Hoofdstuk 3 worden deze tweede-orde effecten, zoals gereduceerde bandbreedte, uitgangs- en ingangsimpedantie besproken.

Daarnaast zijn continue-tijd delta-sigma modulatoren (CTΔΣMs) aantrekkelijker voor bruguitleescircuits door hun hogere energie-efficiëntie en inherente anti-terugvouwvervormingsgedrag in vergelijking met hun discrete-tijd tegenhangers. Om lage ruis bij lage frequenties te bereiken, is chopping ook noodzakelijk in CTΔΣMs. Alhoewel chopping succesvol wordt toegepast in IAs, veroorzaakt het ongewenst gedrag als het wordt toegepast in CTΔΣMs, in de vorm van

kwantisatieruis die terugvouwt naar de signaalband. In dit hoofdstuk wordt dit probleem geanalyseerd en worden twee oplossingen voorgesteld, gebaseerd op een naar-nul-terugkerende (RZ) digitaal-analoogomzetter (DAC) en een geschakelde-capaciteit (SC) DAC. Aangezien deze DACs vaak worden gebruikt in CTΔΣMs, vanwege hun superieure robuustheid tegen interferentie, kunnen de voorgestelde oplossingen in iedere CTΔΣM worden toegepast zonder aanzienlijke overhead.

Hoofdstuk 4

Hoofdstuk 4 beschrijft het eerste prototype, die bestaat uit een CCIA die een CTΔΣM aanstuurt. Door gebruikt te maken van de CCIA's DC common-mode blokkerende karakter, kan de biasspanning van de brug boven de voedingspanning van de ROIC liggen, waardoor deze spanningen apart geoptimaliseerd kunnen worden. Aangezien de uitgangsspanning van de brug typische veel kleiner is dan de brug offsetspanning, wordt een DAC gebruikt om de offset te compenseren voor de versterking, om zo het dynamisch bereik van de CCIA te vergroten. De belasting van de brug wordt verminderd door tweepads positieve feedback toe te passen om de CCIA's ingangsimpedantie te verhogen. Daarnaast wordt de uitgang van de CCIA selectief doorgelaten om te voorkomen dat uitgangsspikes gedigitaliseerd worden, die anders de ROIC's lineariteit en stabiliteit zouden limiteren. De ROIC bereikt een ingangs-gerefereerde ruisdichtheid van 3.7 nV/√Hz, een ruisefficiëntiefactor (NEF) van 5 en een vermogensefficiëntiefactor (PEF) van 44, die beide state of the art zijn.

Hoofdstuk 5

In Hoodstuk 5 wordt het tweede prototype gepresenteerd, die de techniek uitgelegd in Hoofdstuk 3 implementeert en verder uitbreid. Om een groot common-mode ingangsbereik te verkrijgen, is het optelpunt van de modulator geïmplementeerd as een ingebedde CCIA, die makkelijk gecombineerd kan worden met een hoog lineaire 1-bit capacitieve RZ DAC. Metingen laten zien dat de voorgestelde manier van choppen geen last heeft van terugvouwende kwantisatieruis en ook een flexibele keuze van de choppingfrequentie toestaat. Als de modulator gechopped wordt op een tiende van de bemonsteringsfrequentie, bereikt het een INL van 15 ppm, een ingangs-gerefereerde ruis van 4.5 nV/√Hz en een state-of-the-art NEF van 6.1.

Hoofdstuk 6

Hoofdstuk 6 presenteert een drukmeetsysteem gemaakt met een differentiële druksensor (AC4010), de ROIC (Hoofdstuk 4) en een kalibratiemethode. In dit systeem verbruikt de ROIC slecht 2.85 mW en bereikt het een ruisvloer van 3.7 nV/√Hz, wat overeenkomt met 30% van het totale systeemvermogen en 6% van het totale ruisvermogen. Dit is significant beter dan eerdere druk meetsystemen. Om de offsetdrift van de sensors over temperatuur te verminderen, wordt een temperatuurkalibratiemethode gebruikt gebaseerd op een externe referentieweerstand. Na een 2-punts kalibratie, wordt de brugoffset gereduceerd tot 3 µV over 50 °C, wat overeenkomt met een drift van 0.067% FS of 13.4 ppm/°C.

Hoofdstuk 7

Het laatste hoofdstuk presenteert een energie-efficiëntie benchmark voor ROICs. Beide ROICs bereiken een state-of-the-art energie-efficiëntie en demonsteren daarmee de effectiviteit van de technieken die in dit proefschrift worden voorgesteld. Naast het behalen van een hoge energie-efficiëntie, blokkeren de capacitief-gekoppelde ingangstrappen van de voorgestelde ROICs common-mode (CM) ingangs-spanningen, wat CM niveaus toelaat die veel hoger dan de voeding liggen. Dit zorgt er voor dat de brugsensor en de ROIC door verschillende spanningen gevoed kunnen worden, waardoor de ROIC's voedingsspanning geoptimaliseerd kan worden voor energie-efficiëntie.

De belangrijkste bevindingen en originele bijdrage van dit proefschrift worden samengevat in dit hoofdstuk. Daarnaast wordt uitgelegd hoe de ontwikkelde technieken voor ROIC circuits ook gebruikt kunnen worden in andere toepassing en wordt een vooruitzicht op toekomstig werk gegeven.

List of Publications

Journal Papers

[1] **H. Jiang**, S. Nihtianov, and K. A. A. Makinwa, " An energy-efficient 3.7nV/√Hz bridge-readout IC with a stable bridge offset compensation scheme," in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 3, pp. 187-195, Mar. 2019.

[2] **H. Jiang**, C. Ligouras, S. Nihtianov, and K. A. A. Makinwa, "A 4.5 nV/√Hz Capacitively-Coupled Continuous-Time Sigma-Delta Modulator with an Energy-Efficient Chopping Scheme," in *IEEE Solid State Circuits Letters*, vol. PP, no. 99, pp. 1-1, 2018.

[3] **H. Jiang**, J. G. Vogel and S. Nihtianov, "A Power-Efficient Readout for Wheatstone-Bridge Sensors with COTS Components," in *IEEE Sensors Journal*, vol. 17, no. 21, pp. 6986-6994, Nov.1, 1 2017.

[4] **H. Jiang**, Z. Chang, and M. Pertijs, "A 30 ppm <80 nJ Ring-Down-Based Readout Circuit for Resonant Sensors," in *IEEE Journal of Solid-State Circuits*, vol. 51, no. 1, pp. 187-195, Jan. 2016.

[5] S. Hussaini, **H. Jiang**, P. Walsh, D. Macsweeney, K. A. A. Makinwa, "A 15nW per Sensor InterferenceImmune Readout IC for Capacitive Touch Sensors," in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 7, pp. 1874-1882, July 2019.

Conference Papers

[1] **H. Jiang** and K. A. A. Makinwa, "An Energy-Efficient Readout Method for Piezoresistive Differential Pressure Sensors," in *2018 IEEE Custom Integrated Circuits Conference (**CICC**)*, San Diego, CA, 2018.

[2] **H. Jiang**, K. A. A. Makinwa, and S. Nihtianov, "An Energy-Efficient Readout Method for Piezoresistive Differential Pressure Sensors," in *the 43rd Annual Conference of the IEEE Industrial Electronics Society (**IECON**)*, Beijing, China, 2017.

[3] **H. Jiang**, B. Gönen, K. A. A. Makinwa, and S. Nihitanov, "Chopping in Continuous-Time Sigma-Delta Modulators," in *IEEE International Symposium of Circuits and Systems 2017 (**ISCAS**)*, Baltimore, MD, 2017.

[4] **H. Jiang**, K. A. A. Makinwa and S. Nihtianov, "An energy-efficient 3.7nV/√Hz bridge-readout IC with a stable bridge offset compensation scheme," in *2017 IEEE International Solid-State Circuits Conference (**ISSCC**)*, San Francisco, CA, pp. 172-173, 2017.

[5] **Hui Jiang**, Samira Amani, Johan G. Vogel, Saleh Heidary Shalmany, and Stoyan Nihtianov, "A 117dB In-band CMRR 98.5dB SNR CDC for Sub-nm Displacement Sensing with an Electrically Floating Target," in *2018 Symposium on **VLSI** Circuits*, HL, 2018.

[6] **H. Jiang**, Z. Chang, and M. Pertijs, "A 30ppm <80nJ ring-down-based readout circuit for resonant sensors," in *2017 IEEE International Solid-State Circuits Conference (**ISSCC**)*, San Francisco, CA, pp. 482-484, 2015.

[7] S. Hussaini, **H. Jiang**, P. Walsh, D. Macsweeney, K. A. A. Makinwa, "A 15nW Per Button NoiseImmune Readout IC for Capacitive Touch Sensor," in *2018 IEEE European Solid-State Circuits Conference (**ESSCIRC**)*, Dresden, Germany, 2018.

[8] S. Pan, **H. Jiang**, and K. A. A. Makinwa, "A CMOS temperature sensor with a 49fJ·K2 resolution FoM," in *2018 Symposium on **VLSI** Circuits*, Kyoto, Japan, pp. C82-C83, 2017.

[9] R. K. Kumar, **H. Jiang**, and K. A. A. Makinwa, "An Energy-Efficient BJT-Based Temperature-to- Digital Converter with ±0.13°C (3σ) Inaccuracy from -40 to 125°C" will be presented in *2019 IEEE Asian Solid-State Circuits Conference **(ASSCC)***.

Patents

[1] P. Walsh, D. Macsweeney, S. Hussaini, **H. Jiang**, K. A. A. Makinwa, "Nano-power capacitance-to-digital converter," US Patent App. US 15/938,976, 2019.

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Hui Jiang

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Hui Jiang was born in Jiamusi, China. He received the B.S. degree in mechanical and automation engineering from Dalian Jiaotong University, Dalian, in 2010 and the M.E. degree in integrated circuit engineering from Tsinghua University, Beijing, in 2013. From 2013-2018, he pursued his Ph.D. at EI Lab of TUDelft. His doctoral work involved the design of energy-efficient readout ICs for piezo-based sensors and capacitive displacement sensors and had resulted in several patents and publications in *JSSC*, *ISSCC*, *VLSI*, *ESSCIRC*, and *ASSCC*.

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In his spare time, he likes playing lego bricks and reading articles about history of Earth and Azeroth.

Persistence!

坚持不懈!