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Restructuring Medium Voltage Distribution Grids

Parallel AC-DC Reconfigurable Links

RESTRUCTURING MEDIUM VOLTAGE DISTRIBUTION GRIDS

PARALLEL AC-DC RECONFIGURABLE LINKS

Dissertation

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Keywords: capacity enhancement, dc links, distribution network, efficiency, expansion, flexible, medium voltage, mmc, (n-1) contingency, parallel, reconfiguration, reinforcement, redundancy

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Dedicated with love to my Papa.

CONTENTS

SUMMARY

Energy transition will inevitably lead to greater electrification. For example, it is anticipated that electrical energy demand will rise by at least 2-3 times by 2050 with increasing share of electric vehicles and heat pumps. This will translate to significant increase in power demand on the existing medium voltage distribution grid, resulting in structural challenges on such predominantly radial ac networks. Dispersed and variable renewable energy resources further introduce power mismatches with local regions of excess generation and consumption. Under such a scenario, Distribution Network Operators (DNOs) must explore solutions to restructure the grid infrastructure with the goal of capacity reinforcement, improved controllability and efficient power redirection.

In this thesis, dc based technologies are proposed to realize the grid transition from purely ac to hybrid ac-dc networks to address the anticipated challenges posed by energy transition. Refurbishing the existing ac links to operate under dc conditions is shown to enhance the power transfer capacity by approximately 50 % within the studied constraints at higher energy efficiency. Reconfigurability between such parallel operating ac and dc links can further increase the achievable capacity gains during (n-1) contingencies, which relates to the capacity maintained with a single component failure in the system. Further, dc interlinks are introduced to weakly mesh the radial ac distribution networks for efficiently redirecting the power to minimize local demand mismatches, prevent branch overloads and increase availability of the grid.

The relevant component engineering aspects such as converter design as well as cable insulation performance under ac and dc conditions are developed to support the underlying assumptions. Control challenges such as mitigation of common mode current specific to parallel ac-dc link systems are explored. The concept of optimal active power steering capability of the dc link while supporting the full reactive power demand are developed mathematically and demonstrated using an experimental set-up of the proposed system.

In future, therefore, it is suggested that dc technologies will play a important role in restructuring the medium voltage ac distribution grids for achieving higher flexibility, controllability and inter-connectivity with enhanced capacity and efficiency. The proposed concepts of this thesis can be extended to integrate renewable energy resources directly to the embedded dc links, making the system multi-terminal and thus transition towards a universal dc grid.

SAMENVATTING

De energietransitie zal onvermijdelijk leiden tot grotere elektrificatie. Er wordt bijvoorbeeld verwacht dat de vraag naar elektrische energie tegen 2050 minstens 2-3 keer zal stijgen door een toenemend aandeel van elektrische voertuigen en warmtepompen. Dit zal zich vertalen in een aanzienlijke toename van de stroomvraag op het bestaande middenspanning distributienet, wat resulteert in structurele uitdagingen op dergelijke overwegend radiale wisselstroomnetwerken. Verspreide en variabele hernieuwbare energiebronnen introduceren verder vermogensverschillen met lokale regio's van overproductie en consumptie. In een dergelijk scenario moeten distributienetbeheerders oplossingen onderzoeken om de netwerkinfrastructuur te herstructureren met als doel capaciteitsversterking, verbeterde beheersbaarheid en efficiënte stroomomleiding.

In dit proefschrift worden dc-gebaseerde technologieën voorgesteld om de netovergang van puur ac naar hybride ac-dc-netwerken te realiseren om de verwachte uitdagingen van energietransitie aan te pakken. Het opknappen van de bestaande wisselstroomkoppelingen zodat deze onder DC-omstandigheden kunnen werken, blijkt de vermogens capaciteit met ongeveer 50% te verbeteren binnen de bestudeerde beperkingen bij hogere energie-efficiëntie. De configureerbaarheid tussen dergelijke parallel werkende ac- en dc-verbindingen kan de bereikbare capaciteitswinst tijdens (n-1) onvoorziene gebeurtenissen, die verband houdt met de capaciteit die wordt gehandhaafd met een storing in een enkel onderdeel in het systeem, verder vergroten. Verder worden dc-interlinks geïntroduceerd om de radiale ac-distributienetwerken zwak te mazen voor een efficiënte omleiding van het vermogen om disbalans in de lokale vraag te minimaliseren, overbelasting van filialen te voorkomen en de beschikbaarheid van het netwerk te vergroten.

De relevante aspecten van componenttechniek, zoals het ontwerp van de omvormer en de prestaties van de kabelisolatie onder AC- en DC-omstandigheden, zijn ontwikkeld om de onderliggende aannames te ondersteunen. Besturingsuitdagingen zoals het verminderen van de common-mode stroom die specifiek is voor parallelle ac-dc-verbindingssystemen worden onderzocht. Het concept van optimale actieve vermogens sturing van de dc-link, terwijl het de volledige vraag naar reactief vermogen ondersteunt, is wiskundig ontwikkeld en aangetoond met behulp van een experimentele opstelling van het voorgestelde systeem.

Daarom wordt in de toekomst gesuggereerd dat DC-technologieën een belangrijke rol zullen spelen bij de herstructurering van de middenspanning-wisselstroomdistributienetten voor het bereiken van hogere flexibiliteit, bestuurbaarheid en interconnectiviteit met verbeterde capaciteit en efficiëntie. De voorgestelde concepten van dit proefschrift kunnen worden uitgebreid om hernieuwbare energiebronnen rechtstreeks te integreren in de ingebedde gelijkstroomverbindingen, waardoor het systeem multi-terminal wordt en dus overgaat in een universeel gelijkstroomnet.

ABBREVIATIONS

AC	Alternating Current
BTB	Back To Back
BW	Band-Width
C0	Benchmark system with only ac conductors.
Cn	Refurbished system configuration.
CCC	Circulating Current Controller
CEF	Capacity Enhancement Factor
CPL	Constant Power Load
DC	Direct Current
DG	Distributed Generation
DN	Distribution Network
DNOs	Distribution Network Operators
DVC	Direct Voltage Control
EV	Electric Vehicle
HVDC	High Voltage DC
MMC	Modular Multilevel Converter
MVDC	Medium Voltage DC
MVAC	Medium Voltage AC
NC	Normally Open
NO	Normal Closed
NPC	Neutral Point Clamped
OCC	Output Current Controller
PCC	Point of Common Coupling
PD	Partial Discharges
pf	power factor
PLL	Phase Locked Loop
PR	Proportional-Resonator
RSS	Receiving end Sub-Station
RS	Reconfigurable Switch
SS1, SS2	Sub-Station 1 and 2
SSS	Sending end Sub-Station
SM	Sub-Modules
VSC	Voltage Source Converter
XLPE	Crosslinked Polyethylene
ZSC	Zero Sequence Current
ZSCC	Zero Sequence Current Controller

NOMENCLATURE

A_{con}	Link conductor area.
C_{cab}	Total cable capacitance in F
C_{sm}	Submodule capacitance of the MMC.
E_{loss}	Total annual energy loss of the parallel ac-dc system.
i_0	Zero sequence current component in the ac link.
$I_{\text{ac,rated}}$	Rated ac conductor current.
i_{c}	Internally circulating current of MMC.
$i_{\text{c,a}}$	Internally circulating current of MMC in phase leg a.
$i_{\text{Cn,ac}}$	Single ac conductor current for configuration Cn.
$i_{\text{Cn,dc}}$	Single dc conductor current for configuration Cn.
$I_{\text{dc,rated}}$	Rated dc conductor current.
$i_{\text{l,a}}$	Lower arm current of MMC in phase a.
$\overrightarrow{I_{\text{R}}}$	Receiving end ac current phasor.
$\overrightarrow{I_{\text{S}}}$	Sending end ac current phasor.
$i_{\text{s},\alpha\beta}$	Actual output ac current.
$i^*_{\text{s},\alpha\beta}$	Reference output ac current.
$i_{\text{u,a}}$	Upper arm current of MMC in phase a.
$i_{\text{ua,3h}}$	Third harmonic component in $i_{\text{u,a}}$.
$I_{\text{s,dc}}$	Sending end dc current.
k_{cf}	Correction factor for iteratively estimating y_{opt}.
k_{e}	DC voltage enhancement factor.
$k_{\text{i,ccc}}$	Integral gain of CCC.
$k_{\text{i,occ}}$	Integral gain of OCC.
$k_{\text{p,ccc}}$	Proportional gain of CCC.
$k_{\text{p,occ}}$	Proportional gain of OCC.
k_{tp}	Correction factor for thermal proximity effect.
L_{arm}	Arm inductance of the MMC.
L_{cab}	Total cable inductance in H
l, L_{link}	Distance between sending and receiving substation in km.
$L_{\text{C2,max}}$	Maximum L_{link} at which configuration C2 is the most efficient.
$L_{\text{C2,min}}$	Minimum L_{link} at which configuration C2 is the most efficient.
$L_{\text{cr,C0Cn}}$	Link length above which configuration Cn is more efficient than C0.
$L_{\text{10,C0-C2}}$	Minimum L_{link} for which the payback of C2 compared to C0 is lower or equal to 10 years.
$L_{\text{10,C1-C2}}$	Maximum L_{link} for which the payback of C2 compared to C1 is lower or equal to 10 years.
N	Number of submodules in each MMC arm.
$N_{\text{ac,Cn}}$	Number of ac conductors for configuration Cn.
$N_{\text{dc,Cn}}$	Number of dc conductors for configuration Cn.
n_{l}	Insertion indice for lower arm of MMC.

N_{ori}	Total number of link conductors.
N_{red}	Number of redundant conductors.
n_{u}	Insertion indice for upper arm of MMC.
n_{ua}	Insertion indice for upper arm of MMC in phase a.
$n_{\text{ua,3h}}$	Third harmonic component in n_{ua}.
$P_{\text{cond,Cn}}$	Link conductor power loss for configuration Cn.
$P_{\text{conv,Cn}}$	Converter power loss for configuration Cn.
$P_{\text{L,cond}}$	Total link conductor losses in the parallel ac-dc system.
$P_{\text{L,conv}}$	Total converter losses in the parallel ac-dc system.
$P_{\text{L,sys}}$	Total parallel ac-dc system losses.
$P_{\text{loss,Cn}}$	Total power loss for configuration Cn.
$P_{\text{loss,ac}}$	Dielectric Power loss under ac (Chapter 2).
$P_{\text{loss,dc}}$	Dielectric Power loss under dc (Chapter 2).
P_{R}, $P_{\text{r,ac}}$	Receiving end real power.
$P_{\text{r,mp}}$	Receiving end real power for monopolar dc link with ground return.
$P_{\text{r,bp}}$	Receiving end real power for bipolar dc link.
$r_{\text{Cn,ac}}$	Single ac conductor resistance in Ω/km for Cn.
$r_{\text{Cn,dc}}$	Single dc conductor resistance in Ω/km for Cn.
R_{cab}	Total cable resistance in Ω
$R_{\text{ac,90}}$	AC conductor resistance at 90 °C.
$R_{\text{dc,90}}$	DC conductor resistance at 90 °C.
S_{base}	Base power for per unit representation.
$S_{\text{conv,RSS}}$	Apparent power of the receiving end converter.
$S_{\text{conv,SSS}}$	Apparent power of the sending end converter.
$S_{\text{max,ac}}$	Maximum power capacity of ac link.
$S_{\text{max,dc}}$	Maximum power capacity of dc link.
S_{link}	Power capacity of a single link in the system.
S_{RSS}	Apparent power demand at receiving substation.
$T_{\text{Cn,ac}}$	Single ac conductor temperature for Cn.
$T_{\text{Cn,dc}}$	Single dc conductor temperature for Cn.
$V_{\text{ac,rated}}$	AC voltage rating of the cable.
$V^{\Sigma}_{\text{cu,a}}$	Sum capacitor voltages of upper phase a arm of the MMC.
V_{dc}	Voltage of the dc link.
$V_{\text{LL,rms}}$	Line to line r.m.s. substation ac bus voltage.
$v_{\text{l,0}}$	Zero sequence lower arm voltage of MMC.
V_{ph}	AC phase voltage.
$\overrightarrow{V_{\text{R}}}$	Receiving end ac voltage phasor.
$\overrightarrow{V_{\text{S}}}$	Sending end ac voltage phasor.
$v^{*}_{\text{s},\alpha\beta}$	Reference output voltage of OCC.
$V_{\text{s,dc}}$	Sending end dc voltage.
v_{u}	Inserted upper arm voltage of MMC.
$v_{\text{u,0}}$	Zero sequence upper arm voltage of MMC.
v_{ua}	Inserted upper arm voltage of MMC in phase a.
$v^{\Sigma}_{\text{ua,3h}}$	Third harmonic component of $V^{\Sigma}_{\text{cu,a}}$.
w	Grid frequency in rad/s.

y	Ratio of active dc power flow to total active power demand at system receiving end.
y_{act}	Actual operating y of the parallel ac-dc system.
y_{con}	Approximation of y for minimizing $P_{\text{L,cond}}$.
$y_{\text{min}}, y_{\text{max}}$	Minimum and maximum y, respectively.
y_{opt}	Optimal y for minimum $P_{\text{L,sys}}$.
Y	Admittance.
Z	Impedance of the cable.
Z_{L}	Load Impedance.
α_{vff}	Bandwidth of voltage feedforward.
$\alpha_{\text{P,occ}}$	Bandwidth of OCC.
$\alpha_{\text{R,occ}}$	Bandwidth of Resonant Integrator for OCC.
$\alpha_{\text{i,ccc}}$	Bandwidth of Resonator for CCC.
ΔE_{loss}	Energy saving potential with optimal power flow.
$\Delta P_{\text{L,sys}}$	Change in system losses with varing operating condition.
Δy	Deviation of y_{act} from y_{opt}
η_{RSS}	Efficiency of the receiving substation converter.
η_{SSS}	Efficiency of the sending substation converter.
$\theta, \theta_{\text{R}}$	Phase angle at receiving end for power factor $\cos\theta$.
θ_{S}	Phase angle at sending end of distribution link.
ρ_{ins}	Resistivity of the cable insulation.

1

INTRODUCTION

This chapter is based on:
A. Shekhar, L. Ramírez-Elizondo, X. Feng, E. Kontos & P. Bauer "Reconfigurable DC Links for Restructuring Existing Medium Voltage AC Distribution Grids," *Electric Power Components and Systems,* 45:16, 1739-1746, 2017.

The aim of this thesis is to design a framework for efficient integration of dc links to achieve a capacity enhanced hybrid ac-dc medium voltage distribution grid. In this context, this chapter highlights the motivations for the proposed technology and discusses the state of the art. The main assumption is set for introducing dc distribution technologies in predominantly ac networks. Research questions are formulated based on the assumption and key challenges in addressing these questions are highlighted. Finally, the specific objectives and thesis outline is provided.

1.1. THE CHALLENGE OF INCREASING POWER DEMAND

Fuelled by the thrust for green energy resources, increase in new energy consumers like electric vehicles (EV), all electric houses and heat pumps has changed the localized energy consumption patterns and increased the expected power demand from grid infrastructure [1, 2]. Charging modern electric cars simultaneously during a specific time of the day may induce temporary and localized power deficits [3, 4]. For example, due to dependence on gas pipes for heating in residential areas in The Netherlands, the present power demand on distribution networks (DN) is relatively low. With emerging concepts of electric houses and heat pumps, the power demand is expected to increase significantly [5, 6]. Distribution network operators (DNOs) face the challenge of meeting the increasing power demand due to mismatch between variable distributed generation (DG) (example: wind, solar) and energy intensive loads (example: EVs), as illustrated in Figure 1.1.

In [7], the ac transmission and distribution network capacity augmentation is achieved by (a) Adding multi-circuit lines with addition of new links (b) Re-conductoring to higher

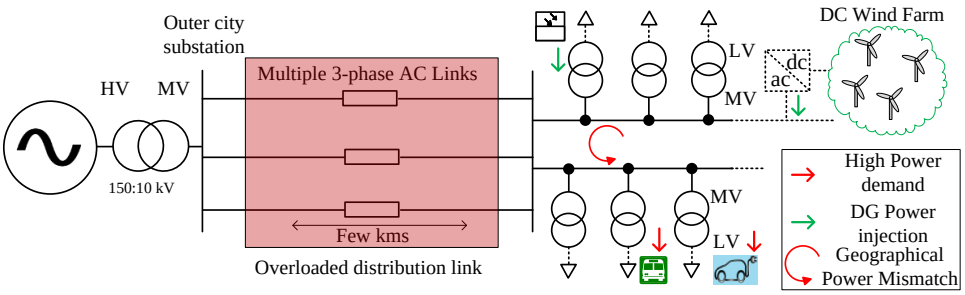

Figure 1.1: Reconfigurable DC links for bulk power transmission into the city collection center.

cross-sectional area (c) Series compensation (d) Reactive power support at receiving end. In [8], the optimal conductor is selected for feeder reinforcement by minimizing the operating losses in trade-off with investment cost. Thus, the straightforward option available to address the challenge of grid capacity deficit is to reinforce the ac infrastructure. However, this approach will not only result in high incurred costs, but also involve a massive digging and installation operation which is not always practically feasible. With expensive digging, particularly in old heritage cities of countries such as Netherlands, socio-economically viable solutions to address localized power deficits are of urgent need. This thesis proposes dc based capacity enhancement solutions that are generically applicable in distribution grids facing similar challenges.

1.2. STATE OF THE ART

In [9], optimal operation of DG is coordinated with upgradation of distribution lines and high/medium voltage transformers with an objective to minimize the investment, operational loss and reliability cost. A dynamic improvement of inter-area power transfer capability is suggested in [10] for under-utilized HVDC grid infrastructure under low wind conditions. Here, under-utilized refers to an operating condition with low power transfer requirements as compared to the installed infrastructure capacity. Reference [11] maximizes the hosting capacity of distribution network by optimizing the chargeable region of EVs given the power quality constraints and uncertainty in power demand. The concept of reliability enhancement of DN with EVs as active components in vehicle to grid applications is extended in [12]. Use of energy storage for peak shaving to avoid installing under-utilized medium voltage grid infrastructure for network reinforcement is explored in [13]. Such avenues of strategic DN reinforcement combined with smart operation must take into account the ownership of grid assets. For example, it is discussed in [14] that DNOs may be prohibited from owning generation units due to regulations aiming to separate the business interests associated with concerned entity. The coordinated planning of DG, EV and storage placement and sizing for efficient DN reinforcement can be difficult with decentralized ownership. The concept of prosumers based on clustered micro-generators could be used, specially with autonomous transaction with bitcoins/smart meters. This thesis addresses the ownership challenge to grid capacity reinforcement with an alternative solution.

Power supply reliability is a challenge for DNOs, particularly with emerging grid assets and forcasted exponential rise in demand [15]. The necessity of maintaining the minimum supply capacity even if a single component in the system fails (referred to as (n-1) contingency), is therefore, the bedrock of DN planning. For example, the importance of network reconfiguration and component rating of DN in relation to daily load curves is highlighted in [16]. The link infrastructure responsible for bulk power transfer to down-line radial DN is typically over-designed with multiple three-phase ac circuits [17]. In this context, it is proposed to refurbish the existing ac underground cable to operate under dc conditions to achieve enhancement in power transfer capacity [18]. Furthermore, most of the transmission losses in the distribution grid occur in these first few kilometres of cables, and hence employing dc links for efficiency enhancement at these locations would be beneficial.

1.3. PREMISE

This thesis is based on the premise that dc links can increase the power delivery capacity of distribution networks. The concept is applied to restructure the existing medium voltage ac grids by integrating reconfigurable dc links as shown in Figure 1.2.

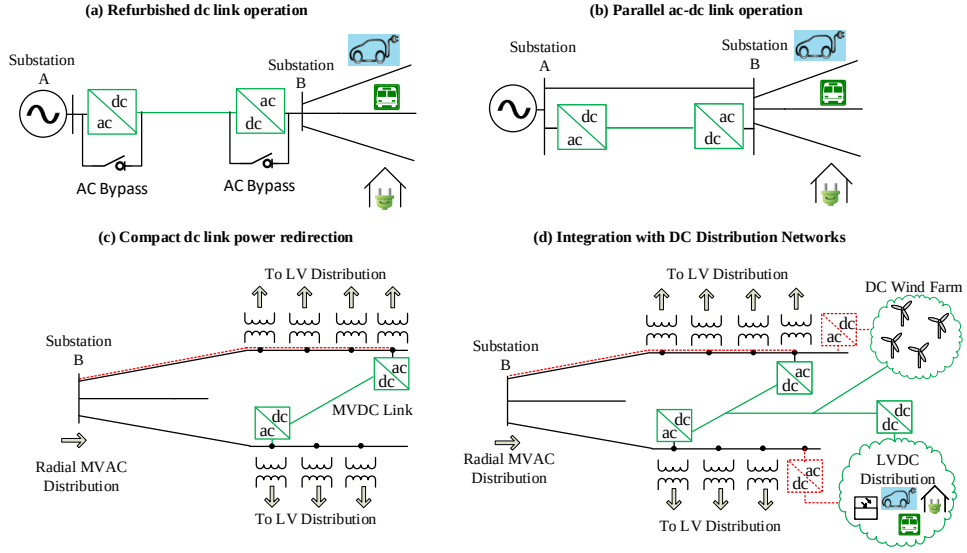

Figure 1.2: Restructuring medium voltage distribution grids with reconfigurable dc links.

The figure illustrates four different dc-based restructuring scenarios to reinforce the existing ac distribution networks. The principles developed in this thesis are applicable to these scenarios as elaborated in the subsequent sub-sections.

1.3.1. REFURBISHING AC LINKS TO DC OPERATION

Figure 1.2 (a) shows the distribution link which brings the bulk power (few MWs) into the city collecting center (Substation B) from the central substation A at medium voltage

(10-66 kV). Traditionally, this short distance link consists of few kilometers of multiple three-phase ac underground cables with adequate capacity during (n-1) contingencies. It is anticipated that the radial distribution network down-line of Substation B will see an exponential rise in power demand with accelerated transport electrification, growing interest in electric vehicles and increasing shift towards electric heat-pumps instead of gas-based heating solutions. As a consequence, the DNOs may need to enhance the capacity at this critical location. This thesis suggests that a refurbishment of the ac infrastructure to dc operation can achieve 50-60 % capacity enhancement for the same link conductors within specific assumptions. For example, with a medium voltage 10 kV underground cable link, the dc to ac voltage enhancement ratio of $\sqrt{2}$ is assumed based on the empirical evidence provided in Appendix A. Different factors such as voltage rating associated with the conductor insulation performance, current rating, power factor correction, voltage regulation and system topologies are evaluated to make the quantification supporting the concept premise. Reconfigurability can be introduced between ac and dc link conductor operation to achieve further capacity improvement during (n-1) contingencies.

1.3.2. PARALLEL AC-DC RECONFIGURABLE LINKS

Figure 1.2 (b) shows a Back-To-Back Voltage Sourced Converter (BTB-VSC) based dc link operating in parallel with ac link between the two medium voltage substations A and B. This thesis defines the boundaries for which such parallel ac-dc operation is more efficient and economically viable as compared to completely ac or dc system with similar capacity. The theory is important because the reconfigurable architecture proposed in Figure 1.2 (a) can be configured with different number of ac and dc links during normal operation even with the same system capacity during (n-1) contingencies. The preferred choice of configuration depends on trade-offs between efficiency, incurred costs, reliability and operational complexity.

1.3.3. MESHING RADIAL GRIDS WITH DC INTERLINKS

Figure 1.2 (c) shows how point-to-point dc interlinks can be used to restructure the existing radial medium voltage ac grid for compact and efficient active power redirection between regions of excess generation to local pockets of high power demand. The network capacity improves because the overloads are prevented by realizing a meshed grid architecture with controlled power flow. The BTB-VSC dc interlink based 'asynchronous meshing' ensures that both radiality of the ac network as well as point-to-point dc link operation can be achieved. Both these criteria are relevant for power flow control and protection related challenges.

1.3.4. INTEGRATING RENEWABLE RESOURCES

Figure 1.2 (d) is an extension of concepts explored in Figure 1.2 (a)-(c), where in a multi-terminal dc network is embedded within the radial ac distribution grid to act as a flexible backbone. It is possible that future wind farms, microgrids and fast electric vehicle charging stations employing inner dc distribution grid can be directly integrated to this dc framework. Power electronics can also be used for ancillary services for making the grid This thesis envisions that in future, universal dc grids can evolve from the existing

ac infrastructure by step-wise implementation of concepts presented in the subsequent chapters. This aspect, however, is not the focus of this thesis, and only the concepts discussed in Section 1.3.1-1.3.3 are developed in detail.

1.4. RESEARCH CONTRIBUTIONS AND CHALLENGES

The main contributions of this thesis are towards addressing the following research questions and challenges:

1. How much capacity enhancement can be achieved by refurbishing existing ac link infrastructure to operate under dc conditions?

   Key Challenges:

   - The achievable dc capacity gain is influenced by various factors that must be quantified as compared to ac in relation to varying system parameters. For example, the impact of factors such as voltage rating and regulation, capacitive currents, dielectric losses, skin effect, thermal proximity, reactive power demand and the system topology, can vary with grid voltage, link length, conductor type and cross-sectional area.
   - Determining a fair assumption on dc voltage enhancement is not so straightforward.The magnitude by which the imposed dc voltage can be increased while ascertaining comparable insulation performance as under ac operating voltages can significantly influence the achievable capacity gains. In this context, the partial discharge behaviour can be a possible insulation lifetime performance indicator.
   - There is a decrease in power delivery capacity that can be maintained during single component failure in the system (referred to as (n-1) contingency). Contingency analysis related to maximum capacity of the proposed architecture during different fault conditions must be considered.

2. What are the advantages of developing a flexible architecture with reference to ac-dc distribution link reconfigurability?

   Key Challenges:

   - System aspects such as number of link conductors, whether they are overhead lines, single cored or three cored underground cables, rating, link topology and number of substation converters can influence the viability of the proposed technology.
   - The trade-offs associated with infrastructure and operational complexity should be identified and weighed against the capacity, efficiency, availability and economic benefits of the reconfigurable architecture.

3. What is the design criteria for ac/dc converters used in grid connected medium voltage high power applications?

Key Challenges:

- Half-bridge based multilevel converters can improve converter efficiency with superior harmonic performance but the selection of number of levels is a trade-off between conduction and switching losses for a fixed medium voltage dc link.
- The trade-offs associated with the five degrees of freedom: switch blocking voltage, submodule capacitance, modulation technique, arm inductance and reliability factors can influence design choices in terms of size, cost, reliability, efficiency and harmonic performance of the converter.
- The design choice must ensure acceptable capacitor voltage balancing and high frequency ripple in the internal circulating currents.

4. In which configuration should the distribution link architecture be operated during healthy system conditions?

Key Challenges:

- The operating losses vary based on several dimensions such as the receiving end active and reactive power demand, power sharing between ac and dc links in the system, grid voltage, dc link voltage, converter efficiency, link length and conductor area. Therefore, the system configuration with optimal efficiency must be determined by accounting for the sensitivity to all these aspects simultaneously.
- The economic viability is governed by differences in link conductor and converter installation costs for maintaining the required capacity with different configurations in trade-off with associated efficiency gains. The break-even boundaries for parallel ac-dc operation as compared to completely ac or completely dc solutions must be determined based on the related payback time involved.

5. By how much can the substation converter be derated while maintaining the required system capacity during different (n-1) contingencies?

Key Challenges:

- The dc link voltage, active power sharing between the ac and dc link, reactive power support by the receiving end converter and full load rating of substation converters are tightly tied in the dimensioning problem formulation.
- Reducing the substation converter rating can reduce the operating efficiency during healthy condition and increases the operational complexity for maintaining the required capacity during different (n-1) contingencies.
- The economic viability of converter downsizing is influenced by demand profile at receiving end, grid voltage, link length and conductor area. The payback time due to the system operation at sub-optimal efficiency as a consequence must be computed.

6. What are the control challenges involved in the dynamic operation of parallel ac-dc distribution links?

   Key Challenges:

   - Zero sequence currents (ZSC) circulate between the 3-line ac link and the back to back converter based dc link in the absence of isolating transformer. Depending on the converter parameters and link length, the magnitude of these currents can result in additional losses in the system. The output current controller of the link converter should be designed to mitigate the ZSC.
   - If modular multilevel converters are used, the implementation of output current 3^{rd} harmonic ZSC controller results in 4^{th} harmonic ripple in internally circulating currents in the MMC phase arms. Therefore, an additional resonator tuned to mitigate this fourth harmonic ripple is needed.
   - The sending end converter must control the dc link voltage at its rated value while the converter at the receiving end of the dc link must be responsible for active power steering between the ac and dc links in the system while supporting the full reactive power demand at the substation.
   - The optimal efficiency that the parallel ac-dc link system can operate varies with the receiving end power demand, and must be dynamically estimated specifically to system parameters such as grid voltage, dc link voltage, load dependent converter efficiency, link length and conductor area.

7. Where can the dc interlink be optimally positioned in the radial distribution grids and what is its proper sizing for effective active power redirection?

   Key Challenges:

   - For a n-bus radial distribution network, there are n x n possible combinations for the placement of a point-to-point dc interlink. Depending on the node from where it draws and the receiving end where it injects active power, the system distribution losses can be influenced.
   - Depending on the capacity of the dc link, the distribution losses, reverse power flows, power redirection needs with distributed generation and high power loads can vary.

1.5. SPECIFIC OBJECTIVES

The main objectives addressed in this thesis are as follows:

- Determine the achievable capacity enhancement when existing ac link conductors are refurbished to operate under dc conditions.
- Analyse the potential of post-fault reconfigurable architecture to improve system capacity during different (n-1) contingencies.

- Define operational boundaries in which refurbished parallel ac-dc reconfigurable link system is economically viable as compared to completely ac or dc system.
- Obtain the proper dimensioning of the reconfigurable dc link by exploring various cost, efficiency and operational complexity trade-offs using case-studies and generalize the insight by performing sensitivity analysis on various system parameters.
- Show the dynamic operation of BTB-VSC based dc link in parallel with ac link and mitigate the arising zero-sequence currents in the system.
- Develop a control algorithm that can steer the active power between ac and dc links to optimize the operating efficiency while simultaneously supporting the reactive power needed using receiving end substation converter.
- Explore the optimal location and sizing of a point-to-point dc interlink in a 33-bus radial distribution network for active power redirection in presence of distributed generation and high power load such as EV charging station.

1.6. THESIS OUTLINE

Figure 1.3 shows the research flow that will be followed in this thesis.

In Chapter 2, it will be discussed that 50-60 % capacity enhancement can be achieved by refurbishing existing ac links for dc operation. The supporting empirical evidence on cable insulation performance under different ac and dc conditions is offered in Appendix A. The application of dc-based capacity enhancement is explored using an actual ac distribution link system as an example to develop different refurbished dc architectures. The importance of reconfigurable ac-dc architecture in maintaining capacity during (n-1) contingencies is highlighted.

Chapter 3 proves that capacity enhancement with refurbished parallel ac-dc reconfigurable link is economically viable as compared to conventional solution of network reinforcement by installing additional ac link conductors. The chapter explores the preferred configuration in which the developed reconfigurable architecture should be operated during healthy system conditions. It is discussed that the configuration with BTB-VSC based dc link in parallel with ac link can be relatively more efficient within the defined operating boundaries of power demand, grid voltage, link length and area as compared to completely ac or dc operation. The converter efficiency curves used for the calculations are derived from an optimised design of a half-bridge based modular multilevel converter (MMC) for medium voltage high power applications. The design steps are detailed in Appendix B.

Chapter 4 shows the dynamic operation of the BTB-VSC based medium voltage dc link in parallel with the ac link. A control strategy is developed to mitigate the zero-sequence currents that exist in the parallel ac-dc link system and validated through both simulations and experiments. A control algorithm is developed to show that active power can be steered using the dc link to ensure that the system operates at its optimal efficiency point while fully supporting the reactive power demand at the receiving end.

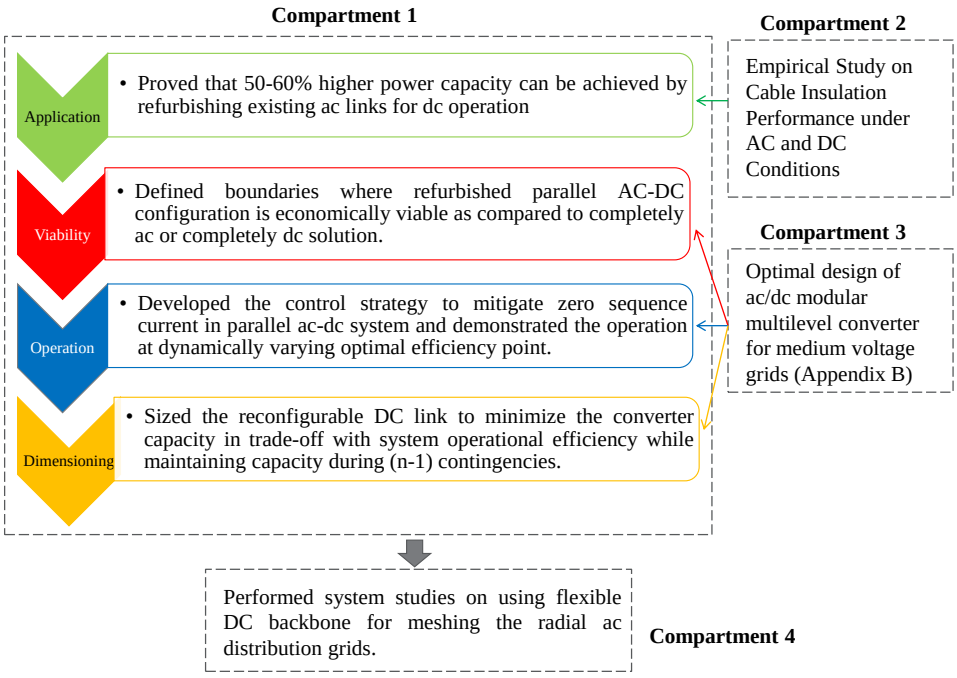

Figure 1.3: Research structure for the thesis outline.

In Chapter 5, the dc link is dimensioned in terms of converter sizing, number of converters per substation and dc link voltage to maintain the required capacity during (n-1) contingencies. Contingency analysis for available capacity is performed for single conductor to ground, three conductor to ground and converter faults. The chapter explores different post-fault reconfiguration strategies to minimize required converter rating for the same system capacity. The trade-off of this converter downsizing potential with optimal efficiency operation during healthy system condition is highlighted. The dimensioning method is explained using two case-studies by adapting data from an actual medium voltage substation. The economic viability of the sizing trade-offs is generalized by performing sensitivity analysis on grid voltage, link length and conductor area.

In Chapter 6, the concept of weakly meshing the existing radial ac distribution grids by installing an optimally sized and placed point-to-point dc interlink is developed. The main application considered is the dc based active power redirection from regions of excess generation to local pockets of excess consumption in a test 33-bus network. The theory includes cases with distributed generation and high power loads at different locations in the distribution grid, thus creating a geographical power mismatch.

The main conclusions of this thesis are summarized in Chapter 7. The possibilities of future research work such as dynamic dc link voltage operation, online reconfiguration and network restructuring for realizing universal dc distribution grids are discussed.

The main contribution of this thesis is to justify that the use of dc power redirection in medium voltage ac distribution networks will have economic advantage in terms of efficiency and capacity enhancement of the system, particularly if a parallel ac-dc reconfigurable link architecture is developed.

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2

REFURBISHING EXISTING AC LINKS FOR DC OPERATION

This chapter is based on:
Aditya Shekhar, Epameinondas Kontos, Laura Ramírez-Elizondo, Armando Rodrigo-Mor, Pavol Bauer, "Grid capacity and efficiency enhancement by operating medium voltage AC cables as DC links with modular multilevel converters," *International Journal of Electrical Power & Energy Systems,* Volume 93, 2017, Pages 479-493.

The chapter presents the concept of refurbishing existing ac distribution links between two medium voltage substations to operate under dc conditions. The capacity enhancement factor is quantified based on factors such as voltage rating and regulation, capacitive currents, dielectric losses, skin effect, thermal proximity, reactive power demand and the system topology specific to 10 kV ac grid for varying link lengths and conductor area. The concepts are applicable for other medium voltage levels as well, within the indicated assumptions. Contingency analysis is performed on an actual grid section to develop a reconfigurable architecture capable of maintaining the enhanced capacity during different system component faults. Insight is provided on operational reliability, efficiency and cost trade-offs if such a reconfigurable ac-dc link architecture is used to improve the system capacity.

2.1. DC CAPACITY ENHANCEMENT CLAIMS

While the delivered power can be enhanced with refurbished dc operation, different claims on the factor by which it is increased exist in the literature. For instance, an early work illustrates that an increase of 3.5 times is feasible [1] for overhead lines. The assumption here is that a single HVDC pole voltage could be raised to twice the line to line rms ac voltage. Furthermore, a closer scrutiny shows that the capacity gains were achieved by changing the tower head, insulator assemblies and configuration. This capacity gain factor may not be achievable with underground cables due to insulation con-

straints. Figure A.1 in Appendix A shows the cable geometry describing different layers and explains in detail the difference in cable insulation behaviour under ac and dc operating voltage with experimental results.

The study [2] proposes a combined ac-dc operation of the same conductor without exceeding the peak of the phase voltage V_{ph}. Here, a dc component of $V_{\text{ph}}/\sqrt{2}$ was superimposed on the ac of $V_{\text{ph}}/2$. The reason a complete changeover to dc operation was not considered was to avoid a dc circuit breaker. But for point to point connections, the ac breaker could be on the ac side of the link, and therefore, this operationally and infra-structurally complex composite ac-dc operation can be avoided. A capacity gain of 75-85 % was reported as the power angle varied from 30° to 80°. This idea was proposed for extremely high voltage long distance overhead lines, wherein, the capacity gains were due to dynamic stability constraint that did not allow for the loading of purely ac transmission to its thermal limit. This may not be a critical constraint at medium voltage short distance underground cables that we are considering.

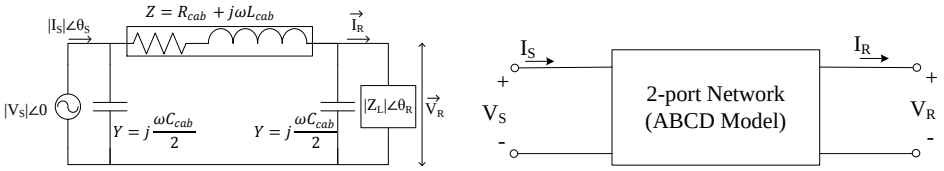
The study in [3, 4] looks into converting high voltage ac overhead lines and describes a capacity increase of 150 % (factor of 2.5) by choosing a voltage enhancement factor with assumptions on expected insulation performance under ac and dc voltages. The purpose of the study was to offer approximate numbers for specific cases, representing order of magnitude of power increase and loss reduction [3]. Simplifying assumptions such as 5 % voltage drop and 5 % current enhancement were helpful to gather sense of the potential of this concept with some test cases. However, trends pertaining to varying conductor area and receiving end load power factor were not explored. For instance, the voltage drop is more prominent for lower conductor cross-sections and varies with load power factor, while the current enhancement is greater for higher area of cross sections. Furthermore, capacitive currents and dielectric losses also play a role in cables, unlike overhead lines.

Therefore, need was felt to derive a mathematically meticulous, generalized understanding of capacity enhancement adapted for refurbishing underground cable infrastructure. The mathematical framework is derived in this chapter to help take into account the exact contributions of all influencing factors. Trends associated with varying parameters will help DNOs to decide whether it is beneficial to refurbish the system from ac to dc operation.

2.2. POWER DELIVERY BY MVAC DISTRIBUTION LINK

For varying cable parameters based on the conductor area of cross-section and length, varying load power factor and the known rated reference sending end voltage phasor, power transferred to the receiving end of the cable link must be computed. In this problem, the unknown variables are the phase angle of the sending end current and the magnitude of the load impedance that would impose the rated cable current magnitude at the sending end of the link. The equivalent circuit for underground MVAC cable link for power transmission described as a π-network is shown in Figure 2.1.

The reference phasor is the sending end voltage with magnitude corresponding to the cable operating voltage rating. The cable current rating is to be imposed as the sending end current magnitude with unknown angle θ_S depending on the cable parameters and the load impedance. The cable parameters Z and Y can be computed in terms of



(a) (b)

Figure 2.1: Equivalent circuit for underground MVAC distribution cable link (a) pi-model (b) ABCD 2-Port Network.

the resistance (R_{cab}), inductance (L_{cab}) and capacitance (C_{cab}) based on the varying link length and conductor cross-section area.

In order to determine the receiving end real power $P_{\text{R}} = \text{real}\{\vec{V_{\text{R}}}.\vec{I_{\text{R}}}^*\}$ for load power factor $\cos\theta_{\text{R}}$ varying from 0 to 1, the unknown sending end current angle θ_{S} and the load impedance magnitude $|Z_{\text{L}}|$ must be computed for varying cable lengths and conductor cross-sectional areas, such that, the rated cable current is drawn from the sending end. The π-network of Figure 2.1. can be represented as a 2-port network with ABCD parameters [5] given by (2.1)-(2.4).

$$A = |A|\angle\alpha = 1 + \frac{YZ}{2} \tag{2.1}$$

$$B = |B|\angle\beta = Z \tag{2.2}$$

$$C = |C|\angle\gamma = Y\left(1 + \frac{YZ}{4}\right) \tag{2.3}$$

$$D = |D|\angle\delta = A \tag{2.4}$$

The receiving end voltage $\vec{V_{\text{R}}}$ and current $\vec{I_{\text{R}}}$ of this 2-port network are expressed in terms of the sending end parameters [6] by,

$$\begin{bmatrix} \vec{V_{\text{R}}} \\ \vec{I_{\text{R}}} \end{bmatrix} = \begin{bmatrix} D & -B \\ -C & A \end{bmatrix} \begin{bmatrix} \vec{V_{\text{S}}} \\ \vec{I_{\text{S}}} \end{bmatrix}$$

The subsequent section deals with solving for the unknowns $|Z_{\text{L}}|$ and θ_{S} based on the above equations.

COMPUTATION OF LOAD IMPEDANCE MAGNITUDE

The objective is to determine the load impedance magnitude $|Z_{\text{L}}|$ for varying cable length, conductor cross-sectional area and load power factor such that rated cable current $|I_{\text{S}}|$ is drawn from the sending end. The receiving end current can be expressed as,

$$\vec{I_{\text{R}}} = \frac{\vec{V_{\text{R}}}}{|Z_{\text{L}}|\angle\theta_{\text{R}}} \tag{2.5}$$

Solving for $\overrightarrow{I_S}$, we obtain,

$$\overrightarrow{I_S} = \left(\frac{D + C.(|Z_L|\angle\theta_R)}{B + A.(|Z_L|\angle\theta_R)}\right)\overrightarrow{V_S} \tag{2.6}$$

Separating and equating the real and imaginary parts of (2.6),

$$\begin{aligned}&|V_S|(|D|\cos\delta + |C||Z_L|\cos(\gamma+\theta_R) = \\ &|I_S|\cos\theta_S(|B|\cos\beta + |A||Z_L|\cos(\alpha+\theta_R) - I_S|\sin\theta_S(|B|\sin\beta + |A||Z_L|\sin(\alpha+\theta_R)\end{aligned} \tag{2.7}$$

$$\begin{aligned}&|V_S|(|D|\sin\delta + |C||Z_L|\sin(\gamma+\theta_R) = \\ &|I_S|\cos\theta_S(|B|\sin\beta + |A||Z_L|\sin(\alpha+\theta_R) + I_S|\sin\theta_S(|B|\cos\beta + |A||Z_L|\cos(\alpha+\theta_R)\end{aligned} \tag{2.8}$$

Rearranging both (2.7) and (2.8) to express $|Z_L|$ in terms of θ_S,

$$|Z_L| = \frac{|V_S||D|\cos\delta - |I_S||B|\cos(\beta+\theta_S)}{|I_S||A|\cos(\theta_S+\theta_R+\alpha) - |V_S||C|\cos(\theta_R+\gamma)} \tag{2.9}$$

$$|Z_L| = \frac{|V_S||D|\sin\delta - |I_S||B|\sin(\beta+\theta_S)}{|I_S||A|\sin(\theta_S+\theta_R+\alpha) - |V_S||C|\sin(\theta_R+\gamma)} \tag{2.10}$$

We have two equations for two unknowns ($|Z_L|$ and θ_S). Equating (2.9) and (2.10) and simplifying, θ_S is given by (2.11).

$$x\sin\theta_S + y\cos\theta_S = \lambda \tag{2.11}$$

Herein, x, y and λ are known from the line parameters varying based on the cable length, conductor cross-section area and the load power factor, given by the expressions,

$$x = |A||D|\cos(\alpha+\theta_R-\delta) - |B||C|\cos(\beta-\theta_R-\gamma) \tag{2.12}$$

$$y = |A||D|\sin(\alpha+\theta_R-\delta) - |B||C|\sin(\beta-\theta_R-\gamma) \tag{2.13}$$

$$\lambda = \frac{|V_S|^2|C||D|\sin(\gamma+\theta_R-\delta)}{|V_S||I_S|} + \frac{|I_S|^2|A||B|\sin(\alpha+\theta_R-\beta)}{|V_S||I_S|} \tag{2.14}$$

Thereby, the solution of (2.11) for θ_S is given by (2.15),

$$\theta_S = \sin^{-1}\left(\frac{\lambda}{\sqrt{x^2+y^2}}\right) - \tan^{-1}\left(\frac{y}{x}\right) \tag{2.15}$$

Therefore, the magnitude of load impedance $|Z_L|$ for imposing the rated cable current at the sending end of the MV distribution line can be computed by substituting the value of θ_S found from (2.15) in (2.9) and/or (2.10).

RECEIVING END POWER

Figure 2.2 depicts the receiving end real power in p.u. for varying cable lengths and conductor cross-sectional area for unity load power factor. By depicting in p.u., the increase in power due to increasing current rating is cancelled out.

The reduction in power is due to reduced voltage regulation and greater capacitive currents in the π-network. The

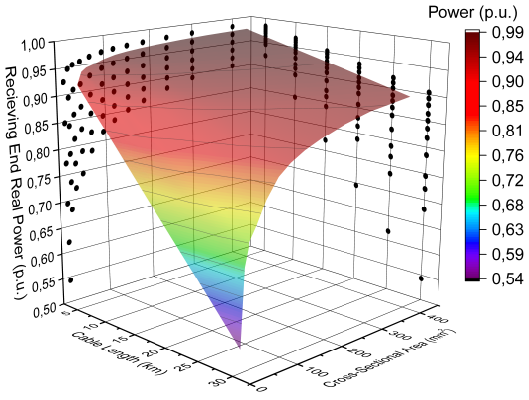


Figure 2.2: Variation in receiving end transmitted real power with cable length and conductor cross-sectional area at unity load power factor.

- The X-Z projection of power profile shows a linear decrease in the transmitted power with increasing cable length. This is because the resistance and inductance of the cable increase, leading to reduced voltage at receiving end. Also, the capacitive currents increase, leading to lower receiving end current.
- The Y-Z projection shows a non linear decrease in the transmitted power with decreasing cable conductor cross-sectional area. This variation is more significant for smaller cross-sectional areas.

  This is because as the area increases, the cable resistance and inductor decrease, leading to better voltage regulation, and hence higher p.u. transmitted power. However, the greater capacitance leads to reduction in the receiving end current, thereby reducing the power. The profile of the transmitted power with variation in conductor area is , hence, a result of these two opposing factors.
- The p.u. real power profile is shown for unity load power factor. The reduction in real power is more or less linear with decreasing load power factor for any cable length and area.

The computed receiving end transmitted ac power presented in this subsection takes into account the capacity drop of the underground link due to voltage regulation, capacitive currents and load power factor under rated operating conditions at the sending end.

2.3. QUANTIFICATION OF DC CAPACITY ENHANCEMENT

The parameters associated with 3-core medium voltage Crosslinked Polyethylene (XLPE) underground cables with copper conductor of different cross-sectional areas for varying link length is provided in [7]. The schematic of the refurbishment is shown in Figure 2.3.

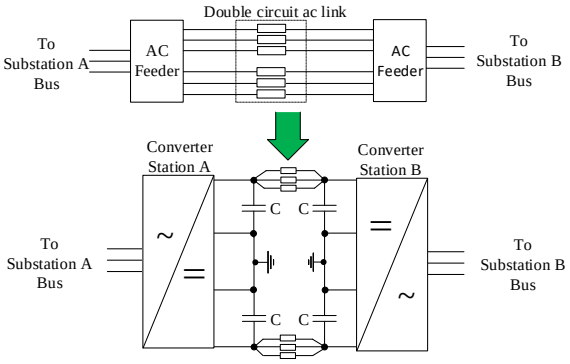


Figure 2.3: An example of ac to refurbished dc link system topology.

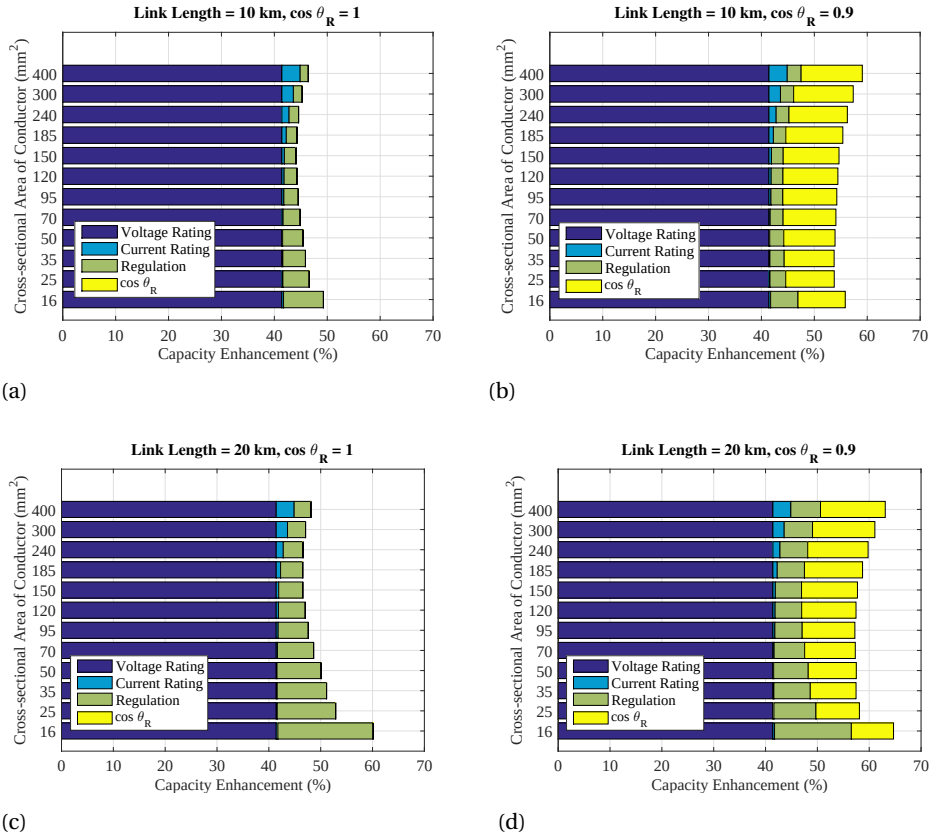


Figure 2.4: Capacity enhancement by refurbishing 3 phase double circuit ac cable link to 3x bipolar dc link.

Based on the factors presented in subsequent sections, Figure 2.4 summarizes the quantification of capacity enhancement when six conductors of a three phase double circuit is refurbished to operate under dc conditions. Results are shown for 10 km and 20 km links for power factors 0.9 and 1 with varying conductor cross-sectional areas.

A realistic capacity enhancement of 50-60 % can be achieved by refurbishing medium voltage ac underground cable to operate under dc conditions with the bulk of enhancement coming from voltage rating increase (41 %), followed by load power factor (10 %), current rating enhancement and voltage regulation (5-10 %). A brief discussion on the various contributing factors is offered in subsequent subsections.

2.3.1. CURRENT RATING

DIELECTRIC LOSS REDUCTION

Heating due to dielectric losses becomes important when the cable is operating near its thermal limit, thereby limiting the current rating of the cable [8]. With aging, these losses can increase and further deteriorate the insulation lifetime. Under dc operating conditions, the leakage losses through the insulation resistance are still present. However, the dipole losses due to ac electric fields are absent. The dielectric losses under ac and ohmic losses in the insulation under dc conditions are given by (2.16) and (2.17), respectively.

$$P_{\text{loss,ac}} = V_{\text{ac,rated}}^2 (C_{\text{ph}}\omega)\, tan(\delta) \tag{2.16}$$

$$P_{\text{loss,dc}} = \frac{\sqrt{2}V_{\text{ac,rated}}^2 (2\pi r)}{\rho_{\text{ins}}} \tag{2.17}$$

Herein, the ac dielectric loss dissipation factor ($tan(\delta)$) for XLPE medium voltage cable is taken as 10^{-4} [9–11]. Under dc conditions, the dielectric losses are without the dipole losses and only include those due to the leakage current through the insulation with resistivity (ρ_{ins}) taken as $10^{15}\,\Omega$m [12, 13]. The rated cable voltage under dc operating condition is considered to be $\sqrt{2}V_{\text{ac,rated}}$.

For the 12 cables of different area of cross-section considered in [7], the losses under dc conditions is only 0.0003-0.0005 % of the ac dielectric losses. However, considering that the ac dielectric losses are less than 0.01 % of the ac conduction losses, their contribution in capacity and efficiency enhancement under dc operating conditions is marginal.

ABSENCE OF SKIN & MAGNETIC PROXIMITY EFFECT

Skin and proximity effect in ac transmission leads to a higher cable resistance, thereby increasing the thermal losses in the cable. The current rating of the cable is limited by the thermal losses per unit length of the cable that can be effectively dissipated to maintain the operating temperature at 90°C. Therefore, for dissipating the same cable losses for maintaining the operating temperature at 90°C, greater rated conductor current ($I_{\text{dc,rated}}$) can be drawn at sending end of the system as described by (2.18).

$$I_{\text{dc,rated}} = \sqrt{\frac{I_{\text{ac,rated}}^2 R_{\text{ac,90}}}{R_{\text{dc,90}}}} \tag{2.18}$$

Where, $R_{ac,90}$ and $R_{dc,90}$ are the cable resistance per unit length at 90°C operating temperature under 50 Hz ac and dc conditions. The achievable capacity enhancement (0-4 %) increases with increasing stranded copper conductor cross-sectional area, as depicted in Figure 2.4.

THERMAL PROXIMITY

Enhancement in dc current carrying capacity of a cable due to its thermal proximity to other current carrying conductors is relevant specific to the system topology. For example, three conductors of ac system topology can be refurbished to operate with two-conductor symmetric monopolar/bipolar dc link. In such a case, the third conductor is either redundant or serves as metallic ground path. At full load rated cable current operation, conductive losses per unit length of the entire link are greater in ac case ($3 \times I^2_{rated,ac} R_{ac,90}$) as compared to dc ($2 \times I^2_{rated,dc} R_{dc,90}$). The three core cable current rating increase due to one redundant line in dc conditions can be estimated by incorporating a thermal proximity correction factor k_{tp} as given in (2.19).

$$I_{dc,rated} = k_{tp} \sqrt{\frac{I^2_{ac,rated} R_{ac,90}}{R_{dc,90}}} \tag{2.19}$$

k_{tp} is in the range of 1-1.5 depending on the ambient temperature and thermal properties of the conductor surrounding. Assuming uniform temperature around the cable and considering all three cores as single unit, the maximum value of k_{tp} can be derived to be 1.5 by equating $3 \times I^2_{rated,ac} R_{ac,90} = 2 \times I^2_{rated,dc} R_{dc,90}$. Practically, however, the achievable value of k_{tp} is lower than 1.5. Since the thermal proximity effect is case-specific and dependent on environment conditions of the installed links, its impact on dc capacity enhancement is not considered in the general results presented in this chapter and k_{tp} is taken to be equal to 1. Nevertheless, it should be noted that if dc refurbishment leads to greater number of redundant conductors, higher system capacity is achievable under specific circumstances.

CAPACITIVE CURRENTS

The influence of leakage capacitive currents is more significant for higher voltage levels and longer link lengths. For the considered application in this thesis, ≈ 0.5 % or lower capacity enhancement is possible for short links at medium voltage level. A detailed analysis on this is presented in [14].

2.3.2. VOLTAGE RATING

VOLTAGE REGULATION

In ac conditions, the frequency dependent voltage drop across the cable inductance and resistance results in the reduction of the receiving end voltage of the transmission line. This variation is called voltage regulation [5], which depends on the cable length, conductor cross-sectional area and also the load power factor. Under dc conditions, the inductive voltage drop is absent under steady state and the resistive drop is lower, thereby resulting in better voltage regulation. About 2-5 % capacity enhancement can be achieved by operating under dc conditions (observe Figure 2.4). Practically, if a higher

voltage drop is expected then voltage regulators are employed to improve the ac link system capacity, thus incurring additional cost and losses.

INSULATION PERFORMANCE

The most significant capacity enhancement (41 %) is associated with a higher operating dc voltage rating of the cable. The basis for this assumption is associated with the expectation of superior underground cable insulation performance under dc voltage as compared to ac. In this thesis, the dc voltage enhancement factor is considered as $\sqrt{2}$ times the r.m.s ac voltage rating of the cable. It is important to support this assumption with some empirical evidence correlating insulation lifetime performance under ac and dc condition. This research requirement is explored in Appendix A for EPR cables to suggest that this assumption is conservative, and in fact even higher dc voltage enhancement is possible to minimize insulation requirements. This observation is consistent with the experience from on-site implementation of the concept for XLPE cables [15].

2.3.3. LINK TOPOLOGIES

The existing ac system topology and the final dc system topology can influence the achieved enhancement in capacity. In fact, in some scenarios, this can even lead to reduced capacity in the final system despite operational benefits of dc system. The dc system can either be a monopolar link with ground return or a bipolar link (asymmetric monopolar if the mid point is grounded and no metallic return is used). The receiving end power for a single monopolar dc link with ground return $P_{\text{r,mp}}$ and a single bipolar link $P_{\text{r,bp}}$ is given by (2.20) and (2.21) respectively.

$$P_{\text{r,mp}} = I_{\text{s,dc}}^2 \left(\frac{V_{\text{s,dc}}}{I_{\text{s,dc}}} - (l \times R_{\text{dc,90}} + R_{\text{gnd}}) \right) \tag{2.20}$$

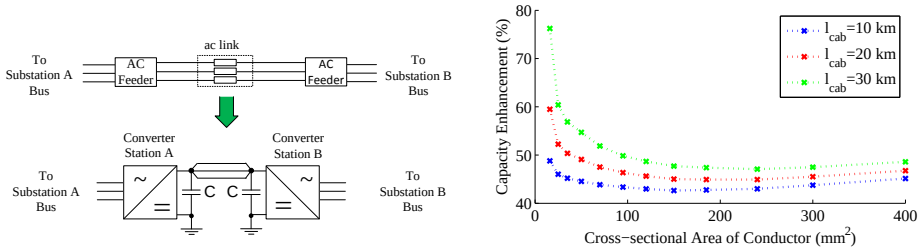
$$P_{\text{r,bp}} = I_{\text{s,dc}}^2 \left(\frac{2V_{\text{s,dc}}}{I_{\text{s,dc}}} - (2l \times R_{\text{dc,90}}) \right) \tag{2.21}$$

Where, $I_{\text{s,dc}}$ and $V_{\text{s,dc}}$ are the sending end current and voltages respectively, equal to the rated values for the cable of length l in km under dc operating conditions. $R_{\text{dc,90}}$ is the dc cable resistance in Ω/km at operating temperature of 90 °C and R_{gnd} is the ground resistance assumed to be designed at 0.5 Ω.

3-PHASE SINGLE CIRCUIT AC TO MONOPOLAR DC LINK WITH GROUND RETURN

Figure 2.5a. depicts the refurbishment of a single circuit three core underground cable connecting 3 phase ac substations at either side to operate as a monopolar dc link with ground return. It must be ascertained that ground return is permissible in the area of installation as it can lead to corrosion and damage to underground metallic structures.

The system can be designed for modularity and greater reliability by having 3 links with two converters for each link at sending and receiving end. However, as shown in this figure, the three cores can also be connected to form a single link between two converters with three times the power capacity. This choice is a trade-off to achieve higher efficiency and lower cost instead of greater modularity. The percentage capacity enhancement



(a) (b)

Figure 2.5: Transmitted power capacity enhancement with conductor cross-sectional area for different cable lengths at unity load power factor for 3-phase single circuit ac to monopolar dc link with ground return.

$CE_{\text{mp,3l}}$ is given by (2.22).

$$CE_{\text{mp,3l}} = \left(\frac{3P_{\text{r,mp}} - 3P_{\text{r,ac}}}{3P_{\text{r,ac}}} \right) \times 100 \tag{2.22}$$

Figure 2.5b depicts the total power transfer capacity enhancement for different cable conductor cross-sectional areas and link lengths for unity load power factor. Most of the enhancement (about 40 %) comes from higher dc voltage rating of $\sqrt{2}$ times $V_{\text{ac,rms}}$. Better voltage regulation is another influencing factor, particularly for lower area of cross-sections and longer link lengths. Capacity enhancement due to skin and proximity effect and dielectric losses is discernible for higher conductor areas.

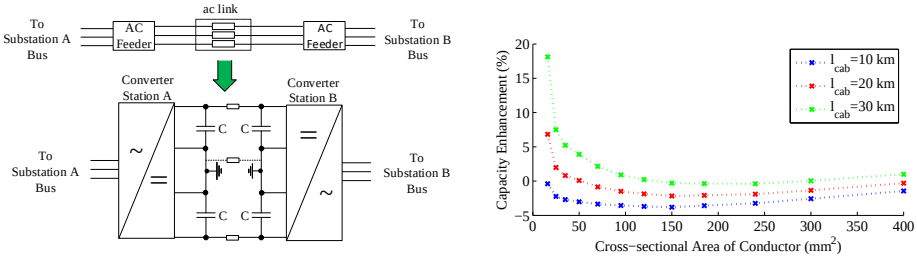
3-PHASE SINGLE CIRCUIT AC TO 1X BIPOLAR/SYMMETRIC MONOPOLAR DC LINK.

The bipolar/symetric monopolar dc link system is depicted in Figure 2.6a. Out of the three cores of the ac cable, two are used for full power transfer in a bipolar dc topology with grounded mid point. The third line shown in dash is redundant or supports ground return which carries negligible current under balanced conditions. Also it can be used during faults, where the system topology can be swapped to monopolar operation with 50 % of the bipolar loading [16]. Note that Figure 2.6a shows the possible conductor utilization, however the converter station can be different in case functionalities associated with bipolar and symmetric monopolar operation are to be realized in this system [4].

The percentage capacity enhancement $CE_{\text{bp,3l}}$ is given by (2.23).

$$CE_{\text{bp,3l}} = \left(\frac{P_{\text{r,bp}} - 3P_{\text{r,ac}}}{3P_{\text{r,ac}}} \right) \times 100 \tag{2.23}$$

Figure 2.6b shows the capacity enhancement results for different conductor cross-sectional area and cable length for unity load power factor. The power transferred to receiving end by the dc system is lower than its ac counterpart in some circuit configurations despite higher rated operating voltage, current and voltage regulation. This is because one conductor is not used for power transfer during bipolar and symmetric monopolar operation.



(a) (b)

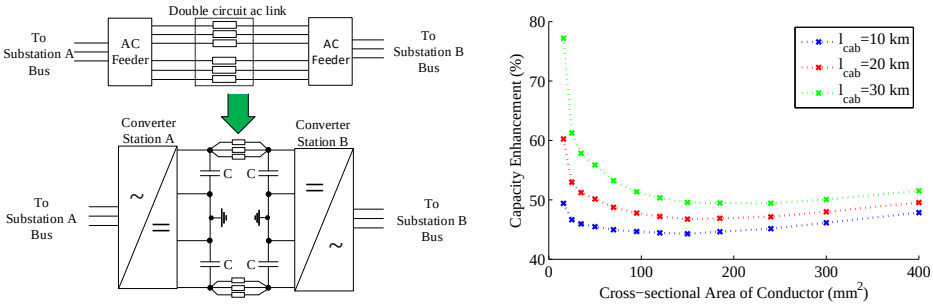
Figure 2.6: Transmitted power capacity enhancement with conductor cross-sectional area for different cable lengths at unity load power factor for 3-phase single circuit ac to 1x bipolar dc links.

In this specific case, additional capacity gains over the ones depicted in Figure 2.6b can be achieve due to the influence of thermal proximity which is described in Section 2.3.1.

3-PHASE DOUBLE CIRCUIT AC TO 3X BIPOLAR DC LINKS.

Figure 2.7a shows the refurbishment of 3 phase double circuit ac cable to 3x bipolar dc links. The three cores of each cable are interconnected to form a bipolar link between four voltage source converters. Each converter is rated for half of the full load capacity of the power delivered to the ac side. The ground return carries negligible current under balanced operation. During faults, the system can operate as monopolar link with ground return at 50 % of the rated capacity. However, this is not possible in many cases because corrosion due to ground current is not permissible.

Another possibility is to create three separate dc links with their own converter systems. The number of switches will triple but their current rating can be reduced. Since the cost and efficiency is more intimately tied with voltage rating and number of switches, this is a trade-off for the added modularity achieved in case a dc link fails.



(a) (b)

Figure 2.7: Transmitted power capacity enhancement with conductor cross-sectional area for different cable lengths at unity load power factor for 3-phase double circuit ac to 3x bipolar dc links.

The percentage capacity enhancement $CE_{\text{bp,6l}}$ is given by (2.24). In Figure 2.7b, the capacity enhancement quantification is offered for varying link length and conductor cross-sectional areas at unity load power factor.

$$CE_{\text{bp,6l}} = \left(\frac{3P_{\text{r,bp}} - 6P_{\text{r,ac}}}{6P_{\text{r,ac}}} \right) \times 100 \tag{2.24}$$

The trends in the percentage capacity enhancement presented in this section for all three system refurbishments can be explained as follows:

- With increasing cable length, the voltage drop in ac system increases due to increasing resistance and inductance. The decrease in receiving end real ac power $P_{\text{r,ac}}$ is greater than the decrease in receiving end dc power $P_{\text{r,dc}}$ at steady state. Therefore, the percentage capacity enhancement increases.
- With increasing conductor cross-sectional area the capacity enhancement is influenced in two ways:
  - The cable resistance and inductance decrease, leading to a better voltage regulation and higher receiving end real ac power. Figure 2.2. shows that this impact is more prominent for lower areas, leading to higher capacity enhancement.
  - Impact of skin effect leads to higher capacity enhancement, which is more prominent for greater conductor area.

  The opposing influence of these two factors leads to the profile of percentage capacity enhancement with respect to the cross-sectional area of the cable conductor.

2.3.4. POWER FACTOR CORRECTION

Previous section describes the capacity enhancement considering that the receiving end ac load is operating at unity power factor. Substations employ power factor correction with passive capacitors in order to improve the power quality in ac distribution networks. These are cheap and robust devices requiring little maintenance. However, changing reactive power demand of the grid can only be met by stepped switching of relevant capacitor banks. Therefore, the average load power factor of the receiving end substation can be typically between 0.9 to 1.

With power electronic converters at both ends of the dc link, this reactive power demand can be met rapidly and smoothly and the cable only transmits the real power demand of the receiving end ac grid. Figure 2.8 shows the additional percentage capacity enhancement factor (CEF) considering 0.9 load power factor.

10-20 % additional capacity enhancement can be achieved in real power delivery to the receiving end of the distribution grid at 0.9 power factor. For case (b), the power factor dependent enhancement is also lower due to redundant line operation. It can be observed that the additional capacity enhancement is the same for Figure 2.8(a) and (c) and two-thirds for Figure 2.8(b), which follows logical description of the related topologies.

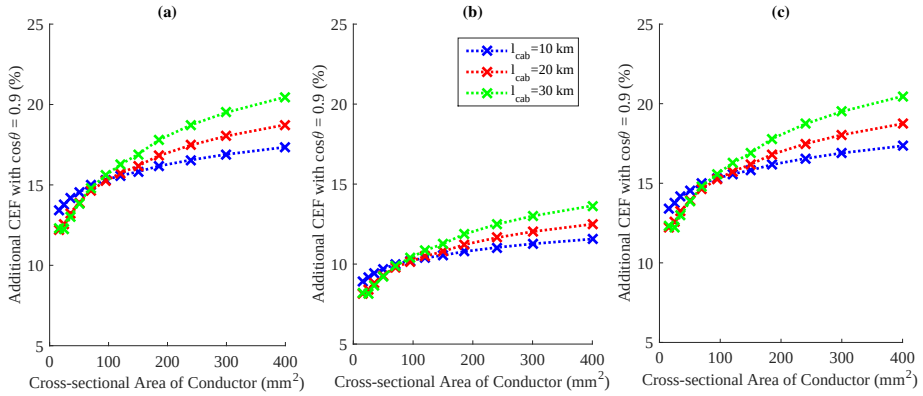


Figure 2.8: Additional capacity enhancement for different conductor cross-sectional area for different cable lengths at 0.9 load power factor for (a) 3-phase single circuit ac to monopolar dc link with ground return (b) 3-phase single circuit ac to bipolar dc link (c) 3-phase double circuit ac to bipolar dc link.

Part of the capacity enhancement is due to the direct dependence of the delivered real power on the load power factor. However, a non-linear enhancement can be observed with the link length and the conductor cross-sectional area due to the variation in voltage regulation with the load power factor. This is clearly noticeable in the quantified breakup of the various contributing factors in capacity enhancement for different cable cross-sectional areas is presented in Figure 2.4, where it can be observed that with lower power factor, the voltage regulation improves for lower cross-sectional area and worsens for higher areas for the same link length.

2.4. (N-1) CONTINGENCY CONSIDERATION

The defined capacity of the link system is the power it is able to transfer during (n-1) contingency. This is the situation when one of the components in the system fails, leading to reduction in the capacity as compared to normal operation. A simple way of understanding this problem is to revisit the system illustrated in Figure 2.3. In case a fault occurs in one of the link conductors or the dc link converter, the refurbished system no longer has higher capacity as compared to the original ac system during comparable (n-1) contingency. Therefore, the developed architecture must take faults into account and there must be enough flexibility for post-fault feeder reconfiguration to maintain required capacity when one of the components in the system fails.

2.4.1. SYSTEM DESCRIPTION

EXISTING LAYOUT

The line diagram for the studied section of a typical dutch distribution network is shown in Figure 2.9. The system consists of 3x three phase medium voltage ac underground cable power transfer links (x1, x2 and x3) between two 10 kV substations (SS1 and SS2).

Each transfer link x1, x2 and x3 consists of a 3 phase, crosslinked polyethylene (XLPE) 3x1x630 A aluminium cored cable A, B and C respectively. Conductors corresponding to

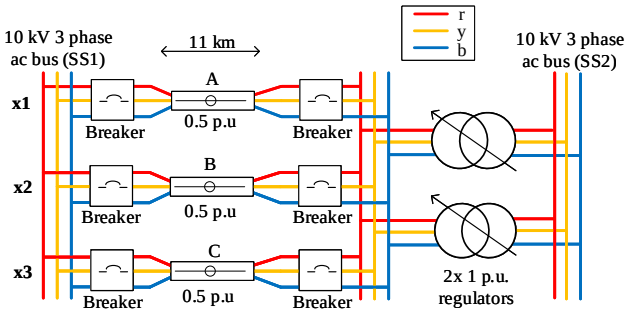


Figure 2.9: Original medium voltage ac distribution link between two 10 kV substations (Sample layout of a dutch distribution network provided by Alliander).

each phase red (r), yellow (y) and blue (b) are colour coded accordingly. This will be helpful when the proposed system refurbishment is explained in subsequent sections.

Since the link length is about 11 km, 2x 1 p.u. voltage regulators are employed at SS2 ac bus. Links x1, x2 and x3 with 0.5 p.u. power transfer MVA capacity each, bring the bulk power to SS2 at the city center. The maximum transfer MVA capacity between SS1 and SS2 is, therefore, 1.5 p.u. during normal operation.

Considering that this is a critical link catering to the energy needs of the entire locality, a certain demand level should be reliably ensured with (n-1) contingency. From Figure 2.9, it can be inferred that removal of any one system component due to fault would ensure a MVA power transfer capacity of 1 p.u. For example, if 3-cored 3-phase cable A of link x1 fails, links x2 and x3 can deliver a total of 1 p.u. power from healthy 3 phase cables B and C. Similarly, if one voltage regulator fails, the other can operate at 1 p.u.

OPERATIONAL DEMAND PROFILE

Figure 2.10. shows the measured maximum and minimum total MVA power demand of SS2 for each day of the year 2015 (Day 1 is the 1st of January). The load profile is obtained from a typical medium voltage substation supplying power to an urban area in The Netherlands (data provided by: Alliander).

Seasonal variation can be observed with lower MVA demand during summer as compared to winter months. Minimum demand, however, does not show similar seasonal variation. It can be observed that the maximum MVA demand limit of 1 p.u. during (n-1) contingency is breached several times between day 270 and 365 (winter months from Oct-Dec). This situation is unacceptable from reliable power delivery point of view. Therefore, the utility operators were forced to increase the capacity of this system. The projected near future requirement pegged the minimum MVA capacity of 1.5 p.u. during (n-1) contingency.

While Section 2.3 discusses the possibility of capacity enhancement, the actual implementation of this concept for system level refurbishment is not so straightforward. Even though a capacity enhancement of at least 50 % is possible during normal opera-

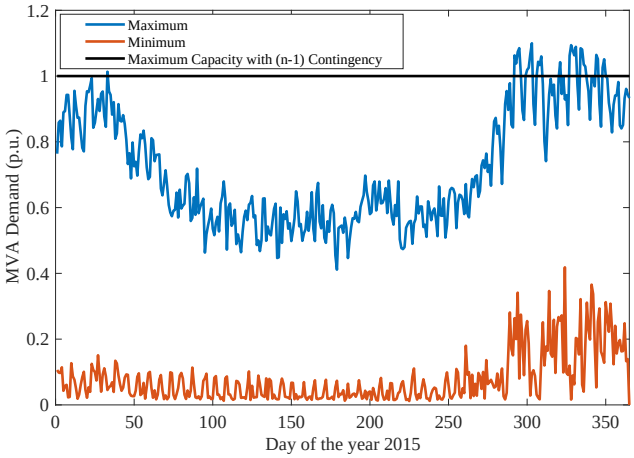


Figure 2.10: Maximum and minimum daily MVA Demand from the critical medium voltage link in the year 2015 (data provided by Alliander).

tion when all contributing factors are considered, the guaranteed uninterrupted power demand that can be met during (n-1) contingency is relevant.

2.4.2. PROPOSED ARCHITECTURES

TOPOLOGY 1

The most straightforward refurbishment strategy is depicted in Figure 2.11. The three conductor cores of cables A and B are refurbished to form symmetric monopolar dc links (x1, x2 and x3). Modular multilevel converters (MMC) of 0.5 p.u. capacity are used at both sides of each dc link in order to have higher efficiency and lower harmonics. The breakers on the ac side of the links may need to be redesigned to handle higher short circuit currents. Cable C operates as ac link x4, while the role of the voltage regulator can be carried out by one of the parallel dc link MMC connected to the SS2 ac bus in order to enable power flow through x4.

From the theory offered in Section 2.3, it can be quantified that each link (x1 - x4) would have a MVA capacity of 0.5 p.u., giving a system MVA power delivery capacity of 2 p.u. under normal conditions as compared to 1.5 p.u. for original system. During single line to ground faults in one of the links, or during converter failure, 1.5 p.u. MVA power delivery capacity is achievable with the remaining three healthy links. This is a 50 % capacity enhancement during (n - 1) contingency as compared to the original system.

However, considering that 3 cored ac cables were refurbished, during certain contingencies 3 conductors need to be removed from the system. For example, during maintenance activity on conductors of cable associated with link x1, link x3 might need to be detached as it shares a conductor core of cable 'A'. A way around this would be to schedule the maintenance activities during off-peak hours. However, this may not be an acceptable solution for DNOs. Further, in case of 3-conductor fault in any of the cables, the situation of 2 inactive dc links cannot be avoided. In such cases, the MVA capacity

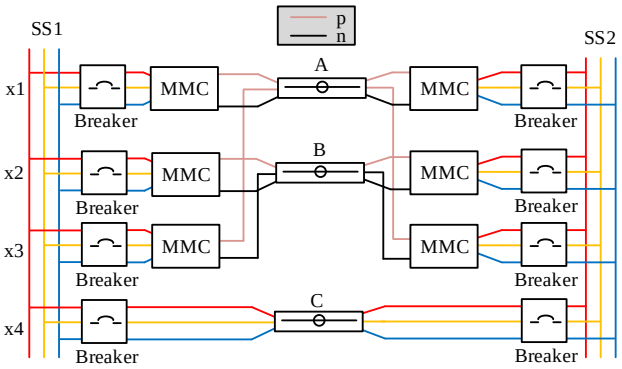


Figure 2.11: Schematic for proposed topology 1.

during (n - 1) contingency is 1 p.u., same as the original system, thus offering no improvement.

TOPOLOGY 2

In order to avoid the situation leading to no capacity enhancement during (n-1) contingencies, a new topology is proposed as shown in Figure 2.12. The system is similar to proposed topology 1, with cable C also refurbished to operate under dc. Each link (x1-x4) has a MVA transfer capacity of 0.5 p.u. during normal conditions.

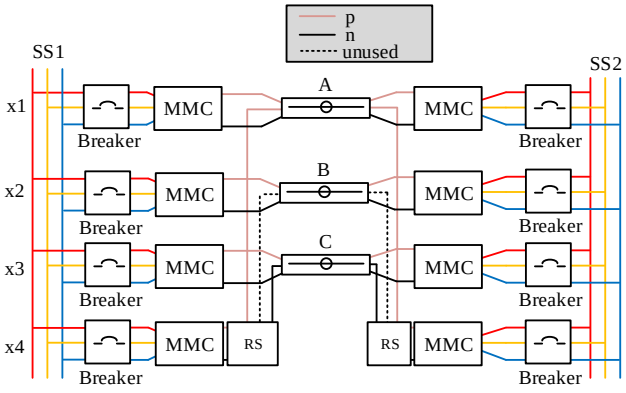


Figure 2.12: Schematic for proposed topology 2.

Out of the 9 original conductors, one is unused and is connected to reconfigurable switch block RS. The schematic of RS is shown in Figure 2.13.

For proposed topology 2, when all three conductors of cable A are out of order, the ac side breaker disconnects links x1 and x4. The RS switch reconfigures the connection such that the unused conductor from cable B becomes the positive pole for link x4. The

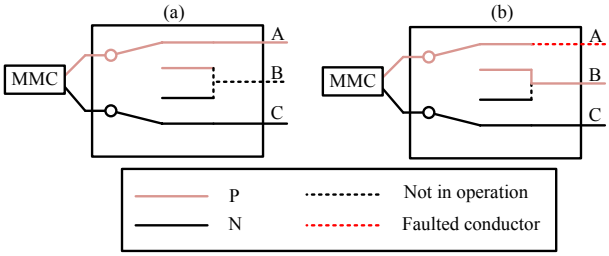


Figure 2.13: Structure of an offline reconfigurable switch (RS) (a) Internal connection during normal operation (b) Reconfigured connection during fault in cable A.

system capacity during (n-1) contingency is enhanced by 50 %, to 1.5 p.u. The proposed reconfiguration is carried out offline so that the contacts of the RS switch do not have to make or break the dc fault current. For online reconfiguration, either a dc breaker or a solid state switch would be needed, adding to the cost and losses of the system. This is because the reconfigurable switch will have to break the dc fault current.

TOPOLOGY 3

Extending the concept of topology 2, the offline reconfigurable switch can be used in each of the dc link (x1-x4), while sharing the same unused conductor from cable 'B' as shown in Figure 2.14. The advantage of this topology is that during single conductor to ground faults, the MVA capacity of the system is 2 p.u. (a 100 % increase over the original system capacity during n-1 contingency). Since single conductor to ground are the most common type of faults, this solution could be attractive, particularly in the offline case where cost of the proposed reconfigurable switch is relatively lower if it is not required to break currents.

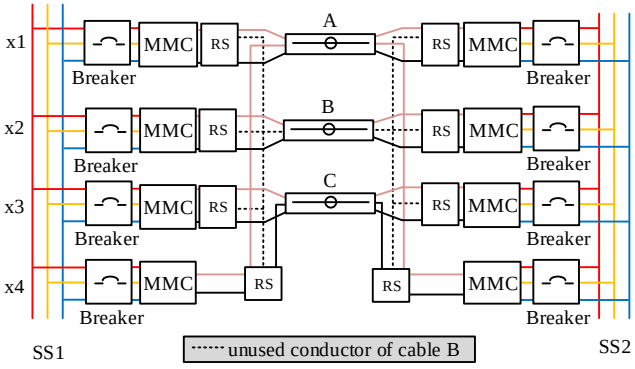


Figure 2.14: Schematic for proposed topology 3.

TOPOLOGY 4

During converter fault at any of the links, the capacity of topology 3 would be 1.5 p.u. (a 50 % enhancement). Further capacity enhancement is achievable if ac bypass to the link converters is implemented as shown in Figure 2.15.

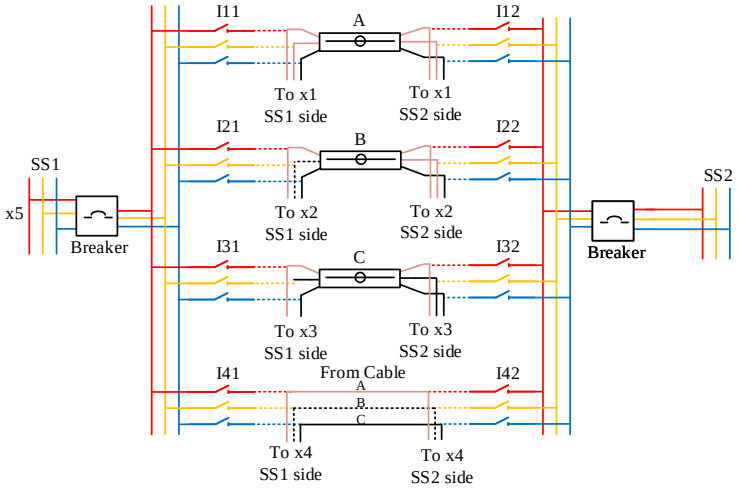


Figure 2.15: Schematic for dc to ac hardware reconfiguration (Topology 4).

In this scheme, the dc path for links x1 - x4 are similar to topology 3. All three cables (A, B and C) are connected to the ac bus of the substations SS1 and SS2, forming a redundant three phase ac path x5, shared by links x1-x4. Two extra normally open ac breakers are needed at the sending and receiving end of the system. Additionally, three phase normally open isolators (offline connectors) are needed at both sides of each dc link (I12-I41) and (I12-I42) respectively.

In case of a converter fault in link x1 the following sequential reconfiguration steps are to be followed:

1. Fault cleared through ac side breakers of link x1.
2. AC side breaker of x4 is opened.
3. Reconfigurable switch connects conductor of cable B as positive pole of link x4 instead of cable A conductor.
4. Isolators I11 and I22 are closed while x5 is still inactive.
5. AC breakers for x4 and x5 are closed.

After this system hardware reconfiguration, the links x2, x3 and x4 of the reconfigured system operate under dc, while x5 works as a three phase ac link using the conductors of cable A. In this way, the system MVA capacity during converter faults is improved to 2 p.u. (a 100 % increase over the original system) by using this strategy. One of the remaining

healthy converters connected to SS2 can be assigned the role to regulate the voltage at ac bus to ensure power transfer through ac link x5. Once the faulty converter is replaced by a healthy one, the system can revert back to topology 3 sequentially.

Note that this dc to ac reconfiguration would not be possible without the RS block in each of the refurbished dc link (x1-x4). Further, it is reiterated that offline reconfiguration strategy is considered keeping in mind the cost and efficiency trade-off with allowable downtime in the system. The summary of system capacity for different (n-1) contingencies is shown in Figure 2.16 for each proposed topology. Topology 1 offers 50 % capacity

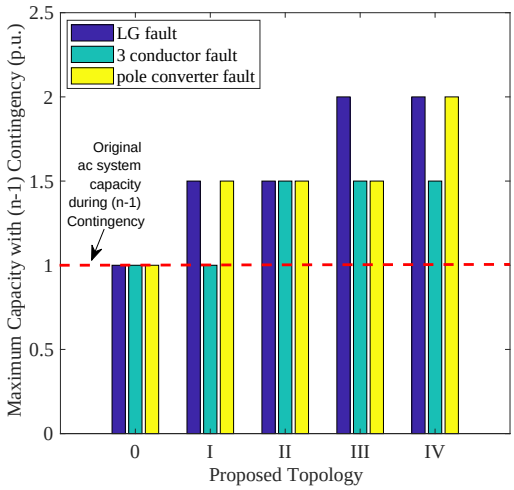


Figure 2.16: Summary of maximum capacity with (n-1) contingency. Here LG is single line to ground fault.

enhancement, but is unfavourable if 3-cored cables are refurbished. Using strategies such as reconfigurable switch in topology 2 and 3 and dc to ac hardware reconfiguration for faulty converter bypass in topology 4, as much as 100 % capacity gains can be achieved over the original system.

'Topology 0' refers to the refurbishment strategy shown in Figure 2.3. Even though the capacity enhancement with refurbished dc operation was quantified to be 1.5 times the original ac link system during pre-fault conditions, the system fails to maintain this capacity during (n-1) contingencies. Therefore, the object of this section was to show that reconfigurability within the proposed system architecture can be critical in maintaining the achievable post-fault power transfer capacity. The reconfiguration strategies are explored more in detail in Section 2.6.

2.5. LINK CONDUCTOR TRADE-OFFS

The Sending end Sub-Station (SSS) and Receiving end Sub-Station (RSS) may be connected using overhead lines or underground cables with three cored or single cored conductors. Furthermore, multiple link conductors maybe available for power transfer. This section discusses the corresponding influence of link conductors on the choices

and trade-offs pertaining to the system operation.

2.5.1. OVERHEAD AND UNDERGROUND CONDUCTORS

In case of overhead lines, economics of compact power transmission plays a role in choosing dc distribution links [17]. For underground cables, avoiding digging and installation of new insulated conductors could be an important consideration. The dc voltage enhancement factor is more liberally chosen in case of overhead lines leading to 2-3 times increase in capacity, even though some modifications in the towers and supporting structure maybe necessary [1]. A comparison on the solutions for capacity enhancement with overhead lines is illustrated in [18]. Even though it has been conservatively considered that the dc capacity enhancement factor is at 1.5 in this thesis, primarily based on the empirical evidence of cable insulation performance under ac and dc conditions, other studies consider higher capacity gains for underground cables [19]. The reasoning behind this anticipation is, possibly, lower partial discharges under dc operation as compared to ac for the same cable insulation [20]. It is important to note that it is difficult to estimate the accurate dc voltage enhancement factor ensuring safe operation without detrimental effect to insulation lifetime. Therefore, it is discouraged to implement an one step increase in operating dc voltage and a gradual increase in system capacity is recommended [15].

The role of space charges becomes important in case of dc operation of cables [21–25]. It is known that space charge accumulation can result in local electric field enhancement and even inversion within the insulation. Based on qualitative understanding, the detrimental effect on insulation lifetime in case of frequent and sudden polarity reversal may encourage minimization of dc to ac reconfiguration during (n-1) contingencies. However, many aspects need further investigation, such as: (i) magnitude of accumulated space charges at medium voltage levels (translated to imposed electric fields on the insulation) [26]. These are possibly low at medium voltage levels and therefore, less significant. (ii) time and temperature dependence of space charges when dc voltage is imposed or removed [27] (iii) insulation performance under the expected space charge accumulation at different locations in cable insulation system over its entire operational lifetime (iv) understanding of impact on insulation with dc to ac reconfiguration based on a) reconfiguration frequency b) timelag after each such reconfiguration. On one hand it is difficult to measure the accumulated space charges during on-site operation; On the other, it is even harder to quantify their precise effects on the insulation lifetime. Such performance indicators are further complicated when different insulation systems (example: XLPE, EPR) are compared [28]. Keeping these considerations in mind, incrementally gathering operational knowhow as recommended in [15] is particularly important.

2.5.2. 3-CORED OR 1-CORED CABLES

3-cored cables are vulnerable to 3-conductor to ground faults. Since the refurbished dc system uses two conductors per link, four conductors of two dc links could go out of service if 3-core fault occurs in the system [29]. Not only this, even a single conductor to ground fault could result in the removal of all three cores during maintenance activity. With single core cables, only the dc link corresponding to the faulty conductor fails. Correspondingly, it is easier to maintain the (n-1) contingency capacity of the system with

1-core cables as compared to 3-cored cables.

2.5.3. NUMBER OF CONDUCTORS

The number of conductors in the original ac system (N_{ori}) available for refurbishment is an important consideration for the network upgradation goals. The ac and dc feeder reconfiguration blocks consists of isolating switches that connect the link conductors to the ac and dc substation buses respectively. These switches can either be normally open or normally closed, resulting in different number of operational ac conductors (N_{ac}) and dc conductors (N_{dc}). Consequently, the position of feeder switches physically govern the ratio of ac and dc power flow capacity between the two substations. Based on a certain N_{ori}, the number of conductors operating under ac (N_{ac}), dc (N_{dc}) and redundant (N_{red}) condition can have different combinations. Each consideration results in its own opportunity and associated challenges. Let the maximum achievable (n-1) criterion driven capacity enhancement factor be CEF_3 for system with 3-cored and CEF_1 for system with single-cored conductor. A summary of possibilities resulting with different N_{ori} is listed in Table 2.1.

Table 2.1: Impact of number of conductors of original system on the maximum achievable capacity enhancement

N_{ori}	N_{ac}	N_{dc}	N_{red}	CEF_3	CEF_1
3	0	2	1	0	50 %
6	0	6	0	0	50 %
6	3	2	1	0	50 %
9	0	8	1	50 %	100 %
9	3	6	0	0/50 %	50/100 %
9	6	2	1	0/50 %	50/100 %

If the original ac distribution system with $N_{ori} = 3$ conductors is refurbished to operate as dc link with $N_{dc} = 2$ and one redundant conductor, no capacity enhancement is possible during (n-1) contingency if the link conductors are 3-cored. This is because all three conductors must be removed even during single line to ground fault. One the other hand, with single-cored cables, a 50 % capacity enhancement is possible (i.e. a factor of 1.5) because the redundant conductor can be reconfigured to replace the faulty one. Similar concept can be used to deduce the CEF_3 and CEF_1 for $N_{ori} = 6$ and $N_{ori} = 9$. In order to maintain the system capacity, ac to dc or dc to ac conductor reconfigurations may also be necessary, as discussed in the subsequent section.

2.6. OPERATIONAL TRADE-OFFS

In this section, the example of $N_{ori} = 9$ is used to describe the various choices available. Similar principles can be applied when the SSS and RSS are connected using different number of link conductors. The available choices result in N_{ac} as a multiple of 3 (due to 3-phase ac) and N_{dc} as an even number (2 conductors per dc link) with the sum $N_{ac} + N_{dc} \leq N_{ori}$. For example, for $N_{ori} = 9$, four combinations are possible: (i) $N_{ac} = 9$, $N_{dc} = 0$

(Case A), (ii) $N_{ac} = 6$, $N_{dc} = 2$ (Case B) (iii) $N_{ac} = 3$, $N_{dc} = 6$ (Case C) and (iv) $N_{ac} = 0$, $N_{dc} = 8$ (Case D).

The system architecture and feeder switch connections for SSS in case of Case C is shown in Figure 2.17. The same system can be connected for other configuration cases by changing the state of switches shown in ac and dc reconfiguration feeders.

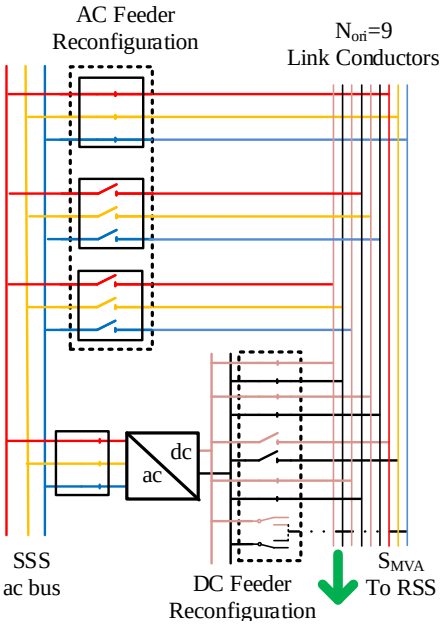


Figure 2.17: SSS connected for Case C.

2.6.1. RECONFIGURATION STRATEGIES

Figure 2.18 shows the conductor status and system capacity with different configurations during normal operation as well as a single conductor to ground fault. Conductors operating under ac conditions are depicted in blue, dc conditions in green and faulty/removed conductors in red. Those that are healthy but redundant are depicted in white.

For any system configuration, every 2x dc conductors (green) have 0.5 p.u power transfer capacity, equivalent to 3x ac conductors (blue) corresponding to a dc enhancement factor of 1.5.

Case A depicts the original system, wherein, 9x ac conductors (blue) have a total capacity of 1.5 pu under normal operating conditions. With a single conductor to ground fault, one ac link with 3x conductors (red) is isolated from the system. This leads to a (n-1) contingency capacity of 1 p.u. with remaining 6x healthy ac conductors (blue) for both 3-cored and 1-cored cables. In the subsequent discussions, Case A will be considered as the baseline system.

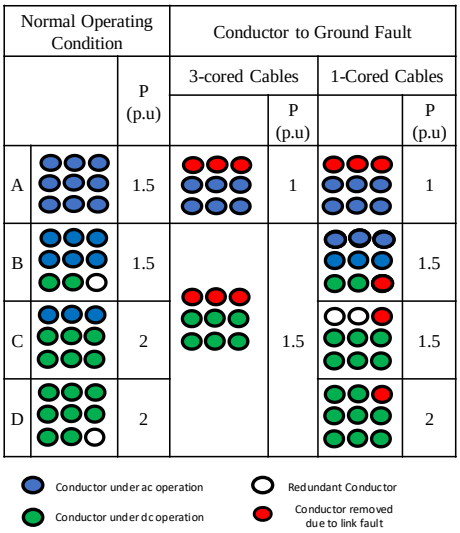


Figure 2.18: Configurations of $N_{ori} = 9$ link conductors during normal and single conductor to ground faults with ac (blue), dc (green), redundant (white) and faulty (red) conductor states.

In Case B, 6x ac conductors (blue) and 2x dc conductors (green) operate with a total 1.5 p.u. capacity under normal operating conditions. There is one redundant conductor (white) in the system during normal operation. During single conductor to ground fault, the system retains its enhanced power transfer capacity of 1.5 p.u as compared to baseline Case A using reconfigurations described as followed:

3-CORED CABLE IN CASE B

If the fault occurs in one of the ac conductors, 3x conductors of the corresponding ac link are removed (red). 3x ac to dc conductor reconfigurations and 1x redundant to dc reconfigurations are required to achieve the maximum capacity of 1.5 p.u. If the fault occurs in one of the dc conductors, 6x ac to dc reconfigurations are needed. Therefore, with both ac and dc faults, the reconfigured system operates with 6x dc conductors (green), thus requiring a minimum converter rating of 1.5 p.u per substation.

1-CORED CABLE IN CASE B

The faulty conductor has to be isolated from the system and replaced by the healthy redundant conductor during either of ac or dc single conductor to ground fault. The system requires neither ac to dc nor dc to ac reconfiguration. A minimum converter rating of 0.5 p.u is required for the system.

Case C shows the conductor configuration when the same system is operated with 3x ac conductors and 6x dc conductors with a maximum capacity of 2 p.u during normal operation. During single conductor to ground fault, the system maintains an enhanced power transfer capacity of 1.5 p.u as compared to baseline Case A using reconfigurations described as followed:

3-CORED CABLE IN CASE C

In either of ac or dc conductor fault, the system must be reconfigured to operate with 6x dc conductors. If the fault is in the ac link, all three conductors must be isolated. If the fault is in one of the dc link conductors, 3x cores of the faulty cable must be removed and 3x ac conductors should be reconfigured for dc operation. The substation converter should be rated to deliver at least 1.5 p.u.

1-CORE CABLE IN CASE C

If a minimum converter rating of 1.5 p.u is available per substation, it is possible to isolate the entire link associated with either ac or dc faulty conductor. As an example, in case the fault is in one of the ac link conductors, the system is reconfigured to operate with 2x redundant (white), 1x removed (red) and 6x dc (green) conductors as shown in the Figure 2.18. Similarly, it is possible to operate the system with 1x redundant, 1x removed, 4x dc and 3x ac conductors in case the fault is in one of the dc link conductors. This is not shown in the system, but can easily be deduced. On the other hand, with a reduced converter rating of 1 p.u per substation, the system can still maintain 1.5 p.u capacity during the fault with a trade-off with a higher number of reconfigurable switching actions.

Case D shows the situation where eight conductors are used to form 4x dc links with a total capacity of 2 p.u during normal operation. There is one redundant conductor in the system.

3-CORED CABLE IN CASE D

During conductor to ground faults, 3-cores of the faulty cable must be removed. The redundant conductor must be connected to the system to form a total of 6x healthy dc conductors with a capacity of 1.5 p.u. Therefore, the minimum converter rating is 1.5 p.u.

1-CORE CABLE IN CASE D

When a conductor to ground fault occurs, the faulty conductor can be replaced with the redundant conductor to maintain the 2 p.u capacity with equivalent converter rating available per substation as shown in Figure 2.18. With a lower converter rating of 1.5 p.u, the system can be reconfigured to operate with 2x redundant, 1x removed and 6x dc conductors. This is not shown in the figure but can easily be deduced.

Two important conclusions emerge from the above discussion: i) Under normal operating conditions, different combinations of ac, dc and redundant conductors can deliver the required power demand at RSS. This will be explored more in Section 2.6.2. (ii) For each configuration, there is a trade-off between substation converter rating and number of reconfiguration switch actions. This will be explored more in Section 2.7.1.

2.6.2. PARALLEL AC-DC OPERATION

The goal of this section is to highlight the possible trade-offs in choosing between Cases A-D during normal operation assuming that 1.5 p.u capacity can be ensured during (n-1) contingencies. It is possible to achieve this capacity in baseline Case A only by installing three additional conductors, increasing the total number of available link conductors to

$N_{ori}+3=12$. For cases B, C and D, the capacity of 1.5 p.u can be maintained with $N_{ori}=9$ using various reconfiguration techniques mentioned in Section 2.6.1. The question arises: which is the best system configuration among the various cases under normal operation?

On one hand, different N_{ac}, N_{dc} and N_{red} influences the conduction losses in the link conductors because (i) The conductor utilization is different, with 12 operational conductors under Case A, 9 in Case C and 8 in Case B and D. (ii) dc link conductor losses are lower than ac mainly due to higher dc operating voltage imposed on the cable. On the other hand, the converter losses vary for each configuration due to different ratio of dc and ac power flow in the system to deliver the required demand at RSS. Consequently, the system efficiency varies with link length, ac-dc power share and the power factor at RSS as shall be explored in this thesis. Chapter 3 suggests that parallel ac-dc operation such as Case C may offer some efficiency benefits as compared to fully ac or dc operation within the defined boundary of operation.

The added investment on the requirement of substation converters in Cases B, C and D must be compared against that of laying additional cables for capacity enhancement in Case A. Considering the efficiency enhancement, the payback time must be considered. Further, the possibility of power derating of the converter as a trade-off for greater number of reconfigurable switching actions is an important consideration which is explored in Section 2.7.1.

Finally, the consequences of the necessary reconfiguration strategies during (n-1) contingencies on the system reliability and availability must be considered. For example, increasing the number of reconfigurations may increase the operational complexity and impact the reconfiguration time. Furthermore, dc to ac reconfigurations may cause undesirable stresses on the cable due to space charges as mentioned in 2.5.1.

2.7. LINK CONVERTER TRADE-OFFS

2.7.1. POWER RATING

The substation converters must be rated according to the maximum demand that they are expected to deliver during normal operation as well as (n-1) contingencies. This value can differ based on the operational mode selected such as parallel ac-dc operation and the reconfiguration strategy employed when a fault occurs. The advantage of de-rating is reduced investment for the same capacity enhancement. Converter derating is possible when the system employs 1-cored cables may result in increase in number of reconfigurations to maintain the required capacity post-fault as described in Section 2.6.1. Table 2.2 summarizes an example of variation in reconfigurable switching operation with converter rating for ac and dc faults with different configuration cases (B, C and D).

In this analysis, whenever a conductor is reconfigured from either ac to dc or dc to ac operation, two offline switching actions are necessary. On the other hand, removing the faulty conductor or connecting the redundant conductor requires a single switching operation. The number of feeder switches needed per substation is twice the number of link conductors.

As explained in Section 2.6.1, if a ac conductor to ground fault occurs for Case C with

Table 2.2: Number of reconfiguration switching operations for maintaining 1.5 p.u capacity during single conductor to ground (CG) fault for 1-core cable based system with different configuration cases for varying substation converter ratings.

Configuration	Fault	Substation Converter Rating		
		0.5 p.u.	1 p.u.	1.5 p.u.
Case B	ac CG	2	2	2
	dc CG	2	2	2
Case C	ac CG	-	4	3
	dc CG	-	2	2
Case D	ac CG	-	-	-
	dc CG	-	-	2

1.5 p.u converter per substation, three ac conductors have to be removed from the system to maintain the system capacity when the operation resumes, leading to a total of three offline switching actions. On the other hand, if the converter is derated to 1 p.u, one faulty ac and one healthy dc conductor must be removed, while one healthy dc conductor must to be reconfigured to operate under ac condition. As a result, four offline switching actions are required to maintain the capacity when the operation resumes. Further derating the converter rating to 0.5 p.u is not possible for Case C, as this particular configuration cannot maintain 1.5 p.u system capacity during normal operating with the corresponding converter. Hence, the number of reconfigurations is highlighted in Table 2.2 with (-) for this unacceptable operating condition. Similarly, the number of reconfigurations can be calculated for other cases and faults.

2.7.2. SUBSTATION CONVERTER ARCHITECTURE

Once the rating of the converter is decided, it is necessary to chose whether modularity is required at substation converter level. A single, fully rated ac/dc converter between the ac and dc buses in the substation shown in Figure 2.17 can meet the power needs during normal conditions as well as link conductor faults. The system can maintain enhanced power delivery capacity if this converter fails, however, all the dc conductors must be reconfigured for ac operation. In such a case, all switches in the dc feeder reconfiguration block of Figure 2.17 are opened and those in ac feeder reconfiguration block are closed.

With selection of multiple converters between the substation ac and common dc bus, the dc to ac link conductor reconfiguration requirements can be minimized or even eliminated in case of converter faults. However, the investment cost as well as space requirements in the substation may increase.

Another possibility is to have a dedicated converter for every dc link operating in the system. With such an architecture, as described in [29], each converter must have an individual ac bypass switches if reconfigurability to ac is required. The advantage of this method is that each dc link can individually be protected using dedicated ac side circuit breaker.

2.7.3. NUMBER OF LEVELS

The link converters are expected to operate at a medium dc link voltage above 10 kV at a power rating of 10-50 MVA. In this range voltage sourced converters (VSC) with more than two levels are appropriate. Topologies such as neutral point clamped (NPC-VSC) have acceptable performance upto three to five levels [30]. Further, with superior harmonic performance and higher efficiency due to reduced switching, modular multilevel converters (MMC) can be an interesting solution [31, 32]. Most importantly, the possibility of modular operation with ability to bypass one or more faulty submodules without rendering the entire converter inoperative is particularly advantageous. The optimal design of the required medium voltage dc link MMC considering number of levels, switch rating, redundancy, efficiency, submodule capacitance and the investment costs is, therefore, esplored in detail in Appendix B.

2.7.4. OPERATIONAL OPPORTUNITIES

The optimal value of ac-dc link load share for maximizing system efficiency is dependent on operating conditions and can be actively controlled using the dc link converters. Therefore, a dynamic power steering in Case B and C depending on RSS demand and power factor can be beneficial. A competing objective of active power steering in the parallel ac-dc link system could be to decrease the thermal cycling at the junction of the dc link converter switches to improve the reliability of power electronic components [33, 34]. However, increasing or decreasing the ac link power share in order to minimize the dc link converter thermal cycling can move the system away from the optimal efficiency point.

With dc operation, the system efficiency and capacity can further be enhanced by dynamically enhancing the dc cable voltage as suggested in [7]. In order to achieve this without increasing the MMC submodule component voltage rating, an interesting solution is proposed in [35]. In this method, the average arm energy is controlled while enhancing the dc link voltage taking advantage of the sum capacitor voltage ripple.

2.8. CONCLUSIONS

The main conclusion of this chapter is that 50-60 % capacity enhancement can be achieved if existing ac links are refurbished to operate under dc conditions under specified assumptions. Using an example of a 10 kV medium voltage grid with underground XLPE cable links between two substations, the variation in the achievable capacity enhancement was shown with different topologies, link length, conductor area and reactive power demand. Contribution of various factors such as dc voltage rating, voltage regulation, skin effect, dielectric losses, power factor, thermal proximity and capacitive currents was quantified. It was found that the main capacity enhancement comes from voltage rating increase (41 %), followed by load power factor (10 %) and voltage regulation (5-10 %).

Contingency analysis was performed to suggest that a reconfigurable ac-dc architecture was necessary to maintain the enhanced capacity during different system component faults. The corresponding improvement in infrastructure utilization can even double the achievable capacity enhancement due to this reconfigurability. The various availability, efficiency and cost trade-offs were discussed in consideration to link conductors,

substation converters and operational aspects. The insight shows that the system can be operated in different configurations while maintaining the same capacity during (n-1) contingency. The subsequent chapter will discuss the techno-economic benefits of this opportunity.

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3

HYBRID AC-DC DISTRIBUTION

This chapter is based on:
Aditya Shekhar, Laura Ramírez-Elizondo, Thiago Batista Soeiro and Pavol Bauer, "Boundaries of Operation for Refurbished Parallel AC-DC Reconfigurable Links in Distribution Grids," *IEEE Transactions on Power Delivery,* 2019.

The previous chapter highlighted that the total capacity of underground ac cables can be improved by at least 1.5 times if they are refurbished to operate under dc conditions under specified assumptions. The field implementation of renovated dc operation for capacity upgradation of XLPE cable line showed four years of uninterrupted operation with economic and reliability benefits as compared to the ac solution [1]. The study anticipated significant increase in achievable capacity gains and recommended a gradual rise in the operating dc link voltage with growing experience about the system. Similar or higher enhancement is possible if the system involves overhead lines [2, 3].

Superior efficiency of the employed ac/dc power electronic devices ensured that some efficiency gains over the original system are also achievable. Due to modularity, scalability, better harmonic performance and higher efficiency, half bridge ac/dc modular multilevel converters (MMC) [4–6] were chosen for the proposed high power medium voltage dc link operation. The optimal design of half bridge MMC for medium voltage high power applications is discussed in Appendix B and the results are used to develop the theory presented in this Chapter.

The contingency analysis of such a refurbished dc system indicated that during fault conditions, some level of architecture reconfigurability is necessary to maintain the enhanced capacity [7]. In [8], it was highlighted that during healthy conditions, the same system can be operated under different physical configurations while maintaining the same capacity during (n-1) contingencies. It was further highlighted that the selection of the best possible configuration requires the quantification of trade-offs related to cost, efficiency and reliability. In this chapter, it is shown that a reconfigurable distribution system architecture with refurbished parallel operating ac-dc links can offer some advantages over either completely ac or completely dc operation.

Among the earliest accounts of parallel operation of ac and dc lines for high voltage power transmission is found in [9]. In this work, greater flexibility of dc transmission as well as rapid control were considered advantageous for the composite system operation. Considering the effective conductor utilization with dc operation, in addition to the stability benefits, simultaneous operation of ac and dc in the same link is proposed in [10]. Some challenges of parallel ac-dc system were explored in [11]. Over the years, the power system apparatus, corresponding device capabilities as well as grid requirements have significantly changed [12]. Consequently, the application of parallel ac-dc power delivery concept has broadened. Recognizing the advantage of using dc alongside ac distribution, authors in [13] proposed a unified load flow model applicable to hybrid radial networks with distributed resources. The optimal operation of hybrid ac-dc power distribution is explored in [14, 15]. An interesting recent research aims at interconnecting Crete island to the Greek mainland using parallel ac-dc links [16, 17]. The project explored the ability of these interconnectors for ensuring the continuity of supply, while minimizing the use of local generation in maintaining the capacity during (n-1) contingency. The operating boundaries wherein a parallel ac-dc link is advantageous as compared to a purely ac or a purely dc system of equivalent capacity is less explored in the literature.

The focus of this chapter is to prove that reconfigurable parallel ac-dc links can be an efficient and economically preferred option, particularly for delivering high power (few tens of MVA) at medium voltage levels (one to few tens of kV) for short distances (0-50 km). The specific contributions are as followed:

- Developing a generalized approach describing the possible system configurations and their capacity constraints.
- Establishing the equations describing the system losses under different configurations.
- Defining the efficiency boundaries for a case-study with varying link lengths, power demand and power factor.
- Performing the sensitivity analysis to describe the variation in the defined boundaries with grid voltage, link conductor area and average efficiency of station converter.
- Presenting an economic analysis of the payback of added investment associated with different configurations.

3.1. SYSTEM DESCRIPTION

3.1.1. SCHEMATIC DIAGRAM

Let us consider that the Sending end Sub-Station (SSS) and the Receiving end Sub-Station (RSS) of an overloaded benchmark ac link system are interconnected using a specified number of conductors (equal to N_{ori}). In order to enhance the capacity during (n-1) contingencies, this system is refurbished to form a reconfigurable parallel ac-dc link as shown in Figure 3.1.

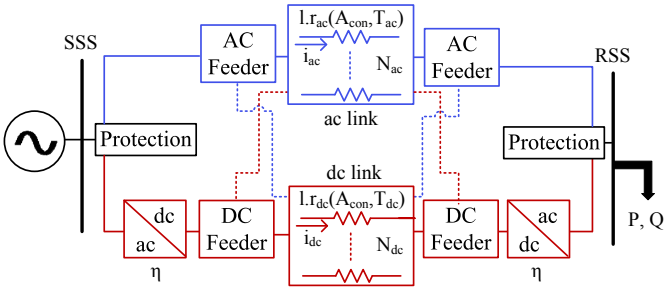


Figure 3.1: Refurbished parallel ac-dc reconfigurable links in distribution grids.

The power flow between SSS and RSS is directed by the reconfiguration of switch blocks marked 'DC Feeder' and 'AC Feeder' that select the number of l km link conductors operating in dc (N_{dc}) and ac mode (N_{ac}) respectively. Depending on the combination of normally open (NO) and normally closed (NC) switches in these feeders, different system configurations are possible (see Section 3.1.2). The reconfigurability is necessary if the required power delivery capacity is to be maintained during faults. However, it is important to select the best possible configuration during normal conditions to ensure the most efficient and economically viable system operation. The corresponding cross-sectional area (A_{con}) and operating temperature (T_{ac}, T_{dc}) dependent per kilometer conductor resistances are r_{ac} and r_{dc}. In this study, A_{con} of both ac and dc link are considered equal because the system is developed using the refurbishment strategy for a completely ac link system described in [7, 8]. However, the presented equations can be generically applied for any magnitude. Note that for the same A_{con}, r_{ac} is slightly higher than r_{dc} as it includes the skin and proximity effects associated with the link conductors at the fundamental frequency. The single conductor currents i_{ac} and i_{dc} depend on the respective ac and dc operating power. η is the operating power dependent efficiency of the substation ac/dc converters at both ends of the dc link.

The link conductors can be either overhead lines or underground cables. Further, the cables can be single-cored or three-cored. The protection block at the ac side of each substation can be designed such that each ac or dc link acts as a point to point connection between SSS and RSS that can be isolated from ac side individually during faults. Alternatively, a common ac circuit breaker can be employed or dc breakers can also be explored [18]. Similarly, design choices are available for the ac/dc converter blocks used for the dc link operation. A detailed discussion on different architectures, various choices available and the associated trade-offs in terms of reliability, efficiency and cost is presented in [7, 8]. In this Chapter, the results are shown with assumptions corresponding to single-cored underground cables with multiple MMCs per substation.

3.1.2. CONFIGURATION STRATEGIES

The pre-refurbished system originally operates as multiple 3-phase ac links, therefore, N_{ori} is a multiple of three, which is most commonly 6 or 9 to meet the necessary redundancy requirements. Depending on the state of the NO and NC switches in the feeders, different combinations of number of conductors operating in ac (N_{ac}) and dc (N_{dc}) are

possible. N_{ac} is always a multiple of three for three phase ac implementation, while N_{dc} is even for a symmetric monopolar dc link implementation [19]. With the goal of maximizing the link conductor utilization U_{cond}, the refurbished ac-dc system can operate in $\left(\frac{N_{ori}}{3}\right)$ possible configurations. In general, for any configuration 'Cn', the number of conductors operating in ac mode ($N_{ac,Cn}$) is given by (3.1).

$$N_{ac,Cn} = (n-1)\cdot\left(\frac{N_{ori}}{3}\right) \tag{3.1}$$

Where, n can take integer values between 1 to $\frac{N_{ori}}{3}$. Correspondingly, the number of conductors operating in dc mode ($N_{dc,Cn}$) is given by (3.2).

$$N_{dc,Cn} = \begin{cases} N_{ori} - N_{ac,Cn}, & \text{if } N_{ori} - N_{ac,Cn} \text{ is even} \\ N_{ori} - N_{ac,Cn} - 1, & \text{otherwise} \end{cases} \tag{3.2}$$

The number of redundant conductors (N_{red}) during normal operation for any configuration is given by (3.3),

$$N_{red} = N_{ori} - (N_{ac,Cn} + N_{dc,Cn}) \tag{3.3}$$

Additionally, the benchmark configuration referred to as 'C0' refers to the conventional solution where additional conductors are installed by the DNOs for capacity enhancement in the ac link system. Based on the results presented in [20], C0 needs approximately 1.5 times more conductor area than the configuration with complete dc operation for equivalent capacity during (n-1) contingencies. Therefore, the total number of conductors $N_{ac,C0}$ is given by (3.4).

$$N_{ac,C0} = 1.5\cdot N_{dc,Cn}, \text{when, } N_{ac,Cn} = 0 \tag{3.4}$$

An example of possible configurations and corresponding number of conductors for $N_{ori} = 9$ is shown in Table 3.1.

Table 3.1: Number of ac, dc & redundant conductors under operation for different configuration strategies with $N_{ori} = 9$.

	C0	C1	C2	C3
N_{ac}	12	0	3	6
N_{dc}	0	8	6	2
N_{red}	0	1	0	1

For a given N_{ori}, there are $\left(\frac{N_{ori}}{3}+1\right)$ possible architectures with the same power delivery capacity during (n-1) contingencies. The connection diagrams for these architectures corresponding to $N_{ori} = 9$ is shown in Figure 3.2.

It can be seen in Figure 3.2(a) that an additional three phase ac link is installed for the benchmark configuration C0. On the other hand, configurations C1-C3 in Figure 3.2 (b)-(d) respectively have installation costs related to the highlighted converter blocks. Each

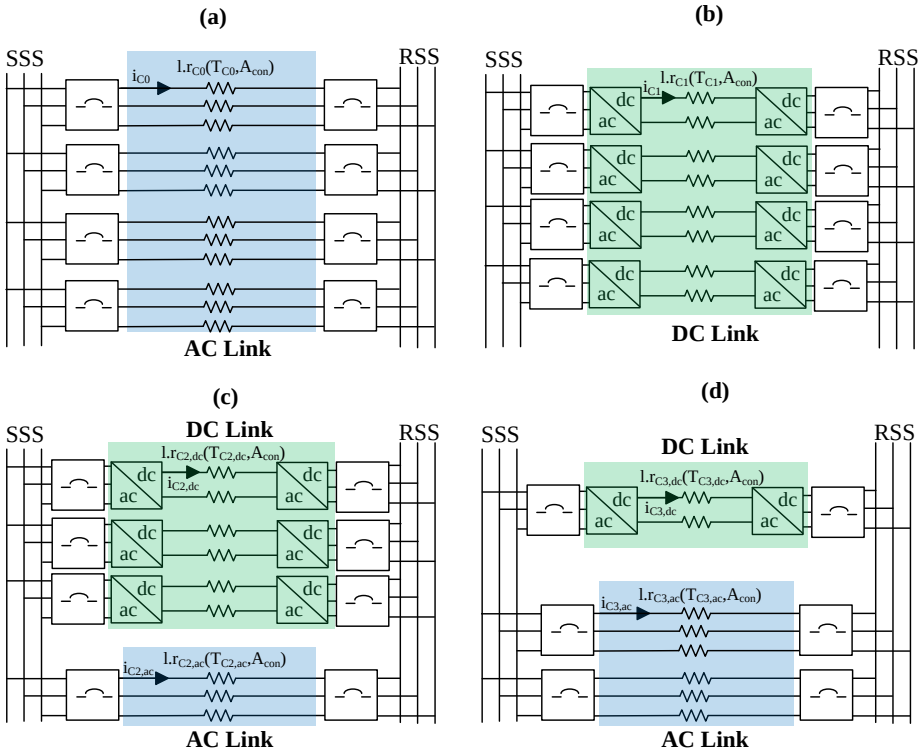


Figure 3.2: System architectures for different configuration with $N_{ori} = 9$ for configuration (a) C0 ($N_{ac} = 12, N_{dc} = 0$) (b) C1 ($N_{ac} = 0, N_{dc} = 8$) (c) C2 ($N_{ac} = 3, N_{dc} = 6$) (d) C3 ($N_{ac} = 6, N_{dc} = 2$).

configuration has a different efficiency and economic consideration, depending on the link length 'l'; per km conductor resistance 'r_{Cn}' corresponding to cross-sectional area A_{con} and temperature T_{Cn}; conductor current i_{Cn} corresponding to the power demand, dc to ac voltage and power ratio; power factor (pf); and the converter efficiency η. Subsequent sections will describe both efficiency and economic viability boundaries based on the sensitivity of the system to the above mentioned parameters and offer insight on how to select the best possible configuration.

3.1.3. POWER DELIVERY CAPACITY CONSTRAINTS

For a given configuration C_n, there are $\frac{N_{ac,Cn}}{3}$ three phase ac links and $\frac{N_{dc,Cn}}{2}$ dc links. The associated maximum power transfer capacities during normal operation, $S_{max,ac}$ and $S_{max,dc}$, are given by (3.5) and (3.6) respectively.

$$S_{max,ac} = \frac{N_{ac,Cn}}{3} \cdot S_{link} \tag{3.5}$$

$$S_{max,dc} = \frac{N_{dc,Cn}}{2} \cdot S_{link} \tag{3.6}$$

where, S_{link} is the capacity of an individual link in the system, which can be assumed approximately equal for a three conductor ac link and a two conductor dc link [20]. This simplification is based on the assumption that the dc voltage imposed on any link conductor is $\sqrt{2}$ times the ac grid phase voltage [21]. For a given substation three phase line to line rms voltage ($V_{\text{LL,rms}}$), the dc link voltage V_{d} is related by enhancement factor k_{e} according to (5.1).

$$V_{\text{d}} = \frac{2k_{\text{e}}V_{\text{LL,rms}}}{\sqrt{3}} \tag{3.7}$$

k_{e} can be conservatively chosen as $\sqrt{2}$ for ac and dc cables of similar technology and cross-section according to the discussion in [21]. The operating limits of the dc link converter can also have some influence on the chosen k_{e}. For overhead lines, this factor can be considerably higher [2, 3]. The dc link converters can be used to steer the active power (P_{dclink}) by controlling the power sharing ratio (y) for a given RSS apparent power demand (S_{RSS}) at power factor pf=cosθ as described by (3.8).

$$y = \frac{P_{\text{dclink}}}{S_{\text{RSS}}\cos\theta} \tag{3.8}$$

Assuming that the dc link converter supports the full load reactive power demand at RSS, the ac link sees unity power factor (upf) at its RSS side and thus the maximum active power capacity of the ac link ($P_{\text{max,ac}}$) is given by (3.9).

$$P_{\text{max,ac}} = \sqrt{3}\left(\frac{N_{\text{ac}}}{3}\right)V_{\text{LL,rms}}I_{\text{cond,rated}} \tag{3.9}$$

The maximum active power capacity of the dc link ($P_{\text{max,dc}}$) is given by by (3.10).

$$P_{\text{max,dc}} = \left(\frac{N_{\text{dc}}k_{\text{e}}k_{\text{cr}}}{N_{\text{ac}}}\right)P_{\text{max,ac}} \tag{3.10}$$

k_{cr} is the converter de-rating factor which is equal to unity when the dc link converter is sized according to the rated dc link conductor capacity while supporting the full load reactive power demand at RSS. The minimum power share (y_{min}) and maximum power share (y_{max}) for a given S_{RSS} at pf=cosθ is described by (3.11) and (3.12) respectively.

$$y_{\text{min}} = \begin{cases} 0, & \text{if } S_{\text{RSS}}\cos\theta \le P_{\text{max,ac}} \\ \frac{S_{\text{RSS}}\cos\theta - P_{\text{max,ac}}}{S_{\text{RSS}}\cos\theta}, & \text{otherwise} \end{cases} \tag{3.11}$$

$$y_{\text{max}} = \begin{cases} 1, & \text{if } S_{\text{RSS}}\cos\theta \le P_{\text{max,dc}} \\ \frac{P_{\text{max,dc}}}{S_{\text{RSS}}\cos\theta}, & \text{otherwise} \end{cases} \tag{3.12}$$

3.1.4. CONDUCTOR TEMPERATURE AND RESISTANCE

A range of ac and dc conductor currents, temperatures and resistances are possible for meeting the same apparent power demand, which influence the system level efficiency

of each configuration. For a particular conductor current I_{cond}, the operating temperature $T_{\text{cond,k}}$ and conductor resistance $R_{\text{cond,k}}$ at kth iteration is computed based on (3.13) and (3.14) respectively.

$$T_{\text{cond,k}} = T_{\text{amb}} + \left(\frac{I_{\text{cond}}^2 R_{\text{cond,k-1}}}{I_{\text{rated}}^2 R_{90^\circ\text{C}}} \right) (90 - T_{\text{amb}}) \tag{3.13}$$

$$R_{\text{cond,k}} = R_{90^\circ\text{C}} \left(\frac{1 + \alpha (T_{\text{cond,k}} - T_{\text{amb}})}{1 + \alpha (90 - T_{\text{amb}})} \right) \tag{3.14}$$

Herein, T_{amb} is the ambient temperature, $R_{90^\circ\text{C}}$ is the resistance of the conductor in Ω/km at 90°C and α is the temperature coefficient. $R_{\text{Tcond,0}}$ is the initial conductor resistance assumed equal to $R_{90\text{C}}$. The iterative process terminates once the difference in the estimated resistance between two iterations becomes less than $1e^{-6}$.

3.1.5. CONVERTER LOSSES

A detailed design methodology for grid connected modular multilevel converter for high power medium voltage applications is presented in Appendix B. The theory presented in [22, 23] indicates that with increasing operating power and voltage, higher number of cascaded cells are favourable for optimal efficiency and performance at a given dc link voltage. Based on these concepts it was shown that a half bridge medium voltage grid connected MMC with 3.3 kV Insulated Gate Bipolar Transistor (IGBT) switch based nine submodule cells is a reasonable design choice with high efficiency for this application [24]. The efficiency computations were performed based on the steady state analytical loss model described in [25] including switching, conduction and inductor losses and will not be repeated here in the interest of brevity. The percentage load dependent efficiency curve for a 10 MVA MMC operating at 313 Hz submodule switching frequency is shown in Figure 3.3.

This efficiency curve is adapted based on the considered full load capacity of the substation converters. Assuming that the reactive power demand at RSS is fully met by the substation converter, the RSS side converter demand $S_{\text{conv,RSS}}$ is given by (3.15).

$$S_{\text{conv,RSS}} = S_{\text{RSS}} \sqrt{y^2 \cos^2\theta + \sin^2\theta} \tag{3.15}$$

At the SSS side, the converter supplies the dc link power and its demand $S_{\text{conv,SSS}}$ is given by (3.16).

$$S_{\text{conv,SSS}} = y S_{\text{RSS}} \cos\theta \tag{3.16}$$

Based on the converter demands described by (3.15) and (3.16) and the associated efficiency η described by Figure 3.3, the total converter losses of the system can be calculated. It can be observed in Figure 3.3 that the efficiency curve of the MMC is nearly flat for a wide range of percentage loading, and thus, assuming a constant efficiency can be a reasonable simplification. This is further important if several partially rated converters are employed per substation with optimal load sharing. Nevertheless, a sensitivity analysis of the described boundaries with varying efficiency will be explored.

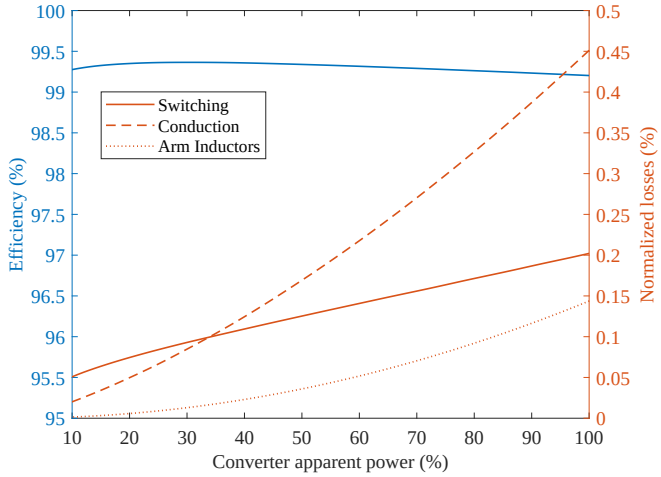


Figure 3.3: Losses and Efficiency curve for DC Link modular multilevel converter with respect to loading.

3.1.6. SYSTEM LOSSES FOR DIFFERENT CONFIGURATIONS

For any N_{ori}, the system loss equations can take three possible structure corresponding to 1) complete ac configuration (C0) 2) complete dc configuration (C1) 3) parallel ac-dc configurations (Cn with $n \neq (0,1)$).

CONFIGURATION C0 (FIGURE 3.2(A))

The current per conductor (i_{C0}) is given by (3.17),

$$i_{\text{C0}} = \frac{S_{\text{RSS}}}{\left(\frac{N_{\text{ac,C0}}}{3}\right)\sqrt{3}V_{\text{LL,rms}}} = \frac{\sqrt{3}S_{\text{RSS}}}{(N_{\text{ori}}+3)V_{\text{LL,rms}}} \tag{3.17}$$

where, $V_{\text{LL,rms}}$ is the line to line r.m.s. SSS bus voltage. The total link conductor loss $P_{\text{loss,C0}}$ is given by (3.18),

$$P_{\text{loss,C0}} = N_{\text{ac,C0}} I_{\text{C0}}^2 R_{\text{C0}} = \frac{3S_{\text{RSS}}^2 l r_{\text{C0}}(T_{\text{C0}}, A_{\text{con}})}{(N_{\text{ori}}+3)V_{\text{LL,rms}}^2} \tag{3.18}$$

where, $r_{\text{C0}}(T_{\text{C0}}, A_{\text{con}})$ is the ohmic ac resistance per kilometer depending on the operating conductor temperature T_{C0} and A_{con}.

CONFIGURATION C1 (FIGURE 3.2(B))

During normal operating conditions, the per conductor dc current i_{C1} that flows through each of the $\left(\frac{n_{dc,C1}}{2}\right)$ dc links as given by (3.19).

$$i_{C1} = \frac{S_{RSS}\cos\theta}{\left(\frac{N_{dc,C1}}{2}\right)V_{dc}} = \sqrt{\frac{3}{2}}\left(\frac{S_{RSS}\cos\theta}{V_{LL,rms}N_{dc,C1}}\right) \tag{3.19}$$

where,

$$V_{dc} = \frac{2\sqrt{2}V_{LL,rms}}{\sqrt{3}} \tag{3.20}$$

V_{dc} is the rated operating voltage of the dc link and $\cos\theta$ is the power factor of the load connected at the RSS. The total dc link conductor power loss $P_{cond,C1}$ is given by (3.21).

$$P_{cond,C1} = \frac{3S_{RSS}^2\cos^2\theta\, l\, r_{C1}(T_{C1}, A_{con})}{2N_{dc,C1}V_{LL,rms}^2} \tag{3.21}$$

where, $r_{C1}(T_{C1}, A_{con})$ is the dc conductor resistance in ohm per km depending on operating temperature T_{C1} and conductor area of cross-section. Based on Section 3.1.5, the derived converter loss $P_{conv,C1}$ is given by (3.22).

$$P_{conv,C1} = S_{RSS}[(1-\eta_{SSS})\cos\theta + (1-\eta_{RSS})] \tag{3.22}$$

η_{SSS} and η_{RSS} is the efficiency of the SSS and RSS side converter stations. For C1, the value of y for computing the equations (3.15) and (3.16) is equal to 1. From (3.21) and (3.22), the total system losses $P_{loss,C1}$ are estimated using (3.23),

$$P_{loss,C1} = P_{cond,C1} + P_{conv,C1} \tag{3.23}$$

PARALLEL AC-DC CONFIGURATIONS CN WITH N $\neq$ (0, 1) (FIGURE 3.2(C,D))

There are $\left(\frac{N_{ori}}{3} - 1\right)$ possible parallel ac-dc configurations with structurally similar loss equations. The corresponding dc and ac conductor currents, $i_{Cn,dc}$ and $i_{Cn,ac}$, are given by (3.24) and (3.25), respectively.

$$i_{Cn,dc} = \frac{yS_{RSS}\cos\theta}{\left(\frac{N_{dc,Cn}}{2}\right)V_{dc}} = \sqrt{\frac{3}{2}}\frac{yS_{RSS}\cos\theta}{V_{LL,rms}N_{dc,Cn}} \tag{3.24}$$

$$i_{Cn,ac} = \frac{\sqrt{3}(1-y)S_{RSS}\cos\theta}{\left(N_{ac,Cn}\right)V_{LL,rms}} \tag{3.25}$$

The power loss in the cable conductors is given by (3.26),

$$P_{cond,Cn} = N_{ac,Cn}i_{Cn,ac}^2 l\, r_{Cn,ac}(T_{Cn,ac}, A_{con}) + N_{dc,Cn}i_{Cn,dc}^2 l\, r_{Cn,dc}(T_{Cn,dc}, A_{con}) \tag{3.26}$$

Substituting the value of conductor currents from (3.24) and (3.25) and simplifying,

$$P_{cond,Cn} = 3l\left(\frac{(1-y)^2 r_{Cn,ac}(T_{Cn,ac}, A_{con})}{N_{ac,Cn}} + \frac{y^2 r_{Cn,dc}(T_{Cn,dc}, A_{con})}{2\cdot N_{dc,Cn}}\right)\left(\frac{S_{RSS}\cos\theta}{V_{LL,rms}}\right)^2 \tag{3.27}$$

Here, $r_{\mathrm{Cn,ac}}(T_{\mathrm{Cn,ac}}, A_{\mathrm{con}})$ and $r_{\mathrm{Cn,dc}}(T_{\mathrm{Cn,dc}}, A_{\mathrm{con}})$ are the per km operating ac and dc resistances respectively, corresponding to temperatures $T_{\mathrm{Cn,ac}}$ and $T_{\mathrm{Cn,dc}}$, imposed by the operating currents $i_{\mathrm{Cn,ac}}$ and $i_{\mathrm{Cn,dc}}$ computed iteratively based on (3.13) and (3.14).

The converter losses $P_{\mathrm{conv,Cn}}$ are described by (3.28)

$$P_{\mathrm{conv,Cn}} = S_{\mathrm{RSS}}\left[(1-\eta_{\mathrm{SSS}})\,y\cos\theta + (1-\eta_{\mathrm{RSS}})\sqrt{y^2\cos^2\theta+\sin^2\theta}\right] \tag{3.28}$$

These are lower than that for C1 (see (3.22)) because the operating value of y governing the converter demands is lower than 1 and can be set between the range described by (3.11) and (3.12). The total system loss $P_{\mathrm{loss,Cn}}$ in parallel ac-dc configuration can be estimated from conduction and converter losses similar to (3.23).

3.1.7. CROSSOVER LENGTHS

Crossover length ($l = L_{\mathrm{cr}}$) can be defined as the link length for which losses of any two configurations is equal. Theoretically, the configurations with N_{ori} link conductors can have $\frac{(\frac{N_{\mathrm{ori}}}{3})(\frac{N_{\mathrm{ori}}}{3}+1)}{2}$ crossover points, with the constraint $L_{\mathrm{cr}} > 0$. The relevant crossover points are those that describe the lowest system losses as a function of link length. The L_{cr} for any two given configurations can be derived by equating the relevant system loss equations derived in Section 3.1.6. By equating (3.23) and (3.18) and simplifying, the crossover ($l = L_{\mathrm{cr,C0C1}}$) between C0 and C1 can be found from (3.29).

$$L_{\mathrm{cr,C0C1}} = \frac{P_{\mathrm{conv,C1}}}{3\left(\frac{r_{\mathrm{C0}}}{N_{\mathrm{ori}}+3} - \frac{\cos^2\theta\, r_{\mathrm{C1}}}{2N_{\mathrm{dc,C1}}}\right)}\left(\frac{V_{\mathrm{LL,rms}}}{S_{\mathrm{RSS}}}\right)^2 \tag{3.29}$$

Similarly, the crossover of parallel ac-dc link (Cn with n≠(0,1)) with C0 ($l = L_{\mathrm{cr,C0Cn}}$) and C1 ($l = L_{\mathrm{cr,C1Cn}}$) can be found using (3.30) and (3.31) respectively.

$$L_{\mathrm{cr,C0Cn}} = \frac{P_{\mathrm{conv,Cn}}\left(\frac{V_{\mathrm{LL,rms}}}{S_{\mathrm{RSS}}}\right)^2}{3\left(\frac{r_{\mathrm{C0}}}{N_{\mathrm{ori}}+3} - \cos^2\theta\left(\frac{(1-y)^2 r_{\mathrm{C2,ac}}}{N_{\mathrm{ac,Cn}}} + \frac{y^2 r_{\mathrm{C2,dc}}}{2N_{\mathrm{dc,Cn}}}\right)\right)} \tag{3.30}$$

$$L_{\mathrm{cr,C1Cn}} = \frac{(P_{\mathrm{conv,C1}} - P_{\mathrm{conv,Cn}})\left(\frac{V_{\mathrm{LL,rms}}}{S_{\mathrm{RSS}}}\right)^2}{3\cos^2\theta\left(\frac{(1-y)^2 r_{\mathrm{C2,ac}}}{N_{\mathrm{ac,Cn}}} + \frac{y^2 r_{\mathrm{C2,dc}}}{2N_{\mathrm{dc,Cn}}} - \frac{r_{\mathrm{C1}}}{2N_{\mathrm{dc,C1}}}\right)} \tag{3.31}$$

3.1.8. ECONOMIC ANALYSIS

Even though each configuration can maintain the same power delivery capacity during (n-1) contingencies, the installation costs incurred in their realization is different. For C0, link length dependent cost $f_{\mathrm{c,C0}}(L)$ is incurred in procuring, digging and installation of an additional 3-phase cable link. Based on feedback from experts associated with the DNOs (see Acknowledgements), a ballpark value of this can be assumed between 100-200 €/m in The Netherlands. However, these figures are only indicative and location-specific.

On the other hand, the refurbished dc based configuration costs ($f_{c,Cn}$ for n≠0,1) include converter costs (assumed 50 €/kVA based on [26]) $f_{c,conv}(S_{rated,RSS}, S_{rated,SSS})$, where $S_{rated,RSS}$ and $S_{rated,SSS}$ are the substation converter rating at RSS and SSS sides, given by (3.15) and (3.16) respectively at full load. From the equations, it can be inferred that since the value of y is lower than 1 for parallel ac-dc configurations (Cn where n≠(0,1)), the corresponding costs are lower as compared to C1. Furthermore, each converter station space requirements can be assumed at 50000 €. It can be inferred that the costs for refurbished dc configurations is independent of link length.

These cost functions are used to compute the payback due to the savings associated with the losses of one configuration as compared to other. The energy savings are translated to €s using a unit cost of 0.1 €/kWh [20]. These aspects shall be explored in Section 3.4.

3.2. EFFICIENCY BOUNDARIES

In this section the efficiency boundaries are derived for different configurations (C0-C3) using a case-study with $N_{ori} = 9$. The presented results correspond to the system parameters described in Table 3.2.

Table 3.2: System Parameters

$V_{LL,rms}$	10 kV
Type of conductor	Aluminum
A_{con}	400 mm^2
Rated conductor current	450 A
Average converter efficiency	99.34 %
Capacity during (n-1) contingencies	3 p.u.
Base Power	7.8 MVA

The base power corresponds to S_{link} and will change for the sensitivity analysis in Section 3.3 showing the variation in the defined boundaries in accordance with the associated parameters.

3.2.1. SYSTEM LOSSES AND CROSSOVER POINTS

Based on the power loss equations derived in the previous section, the link length dependent system losses are shown in Figure 3.4 for different strategies C0-C3 delivering S_{RSS} = 3 p.u at pf=0.9. The depicted losses are normalized with respect to S_{RSS}. The dc active power share y is considered 0.75 for C2 and 0.33 for C3.

It can be observed that when a parallel ac-dc configuration such as C2/C3 is used, these losses are lower than C1 as a part of S_{RSS} is delivered using the ac link. The system losses are highest for C0 after crossover points $L_{cr,C0C1}$ and $L_{cr,C0C2}$ as compared to C1 and C2 respectively, which can be described by (3.29) and (3.30). This is because the ac conductor losses are higher than that for dc, mainly due to lower link voltage, and these dominate the system losses over the fixed converter losses as the link length in-

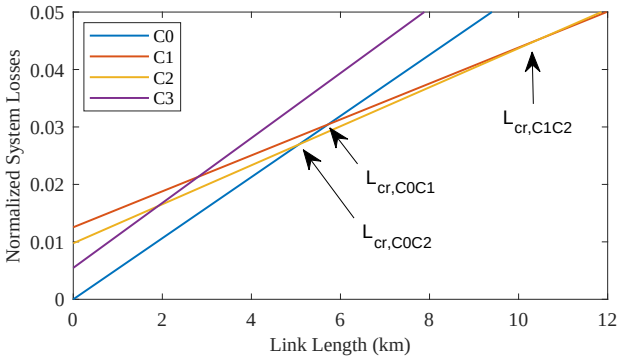


Figure 3.4: Link length dependent normalized system power losses for different operational mode strategies.

creases beyond the crossover points. Similarly, C2 becomes less efficient as compared to C1 after crossover point $L_{\text{cr,C1C2}}$ as described by (3.31). Configuration C3 is not the most efficient at any link length in this example, and thus its role will not be further explored in describing the efficiency boundaries. However, this configuration can offer some operational advantages along with the possibility to reduce converter costs as discussed in [8].

Equations (3.29)-(3.31) suggest that even if the system parameters are fixed according to Table 3.2, the crossover points can vary depending on the operating conditions such as S_{RSS}, pf and y. Therefore, a proper knowledge of these dependencies are necessary to define the efficiency boundaries based on the expected operating conditions of the system over its lifetime.

3.2.2. VARIATION IN CROSSOVER LENGTHS WITH OPERATING CONDITIONS

In Figure 3.5, the variation in the crossover lengths is shown as y varies between the range y_{min} to y_{max} for configuration C2. The main observation is that in any considered scenario, preference for a parallel ac-dc link configuration has a optimal value with respect to the set value of operating y. Furthermore, the crossover length decreases with increasing S_{RSS}, consistent with (3.30) and (3.31).

Specifically, Figure 3.5a indicates a minimum $L_{\text{cr,C0C2}} = L_{\text{C2,min}}$ at $y = \approx 0.75$. If the operating point is shifted by $\pm\Delta y$, the incurred losses in C2 are higher, mainly because the corresponding $P_{\text{cond,C2}}$ increases due to the uneven distribution of conductor currents in the ac and dc links. The influence of converter losses also play a role to determine the exact optimal point. Similar principle can be applied to explain the maximum $L_{\text{cr,C1C2}} = L_{\text{C2,max}}$ in Figure 3.5b. As observed, the optimal point varies with the S_{RSS}, pf as well as link length and the minimum and maximum attainable values $L_{\text{C2,min}}$ and $L_{\text{C2,max}}$ for the given S_{RSS} and pf can be determined from Figure 3.5a and Figure 3.5b respectively.

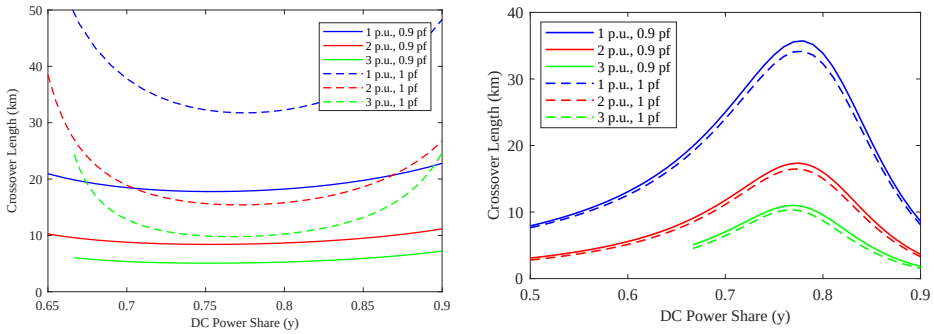


Figure 3.5: Variation of crossover lengths with y for different S_{RSS} and pf (a) $L_{\text{cr,C0C2}}$ (b) $L_{\text{cr,C1C2}}$.

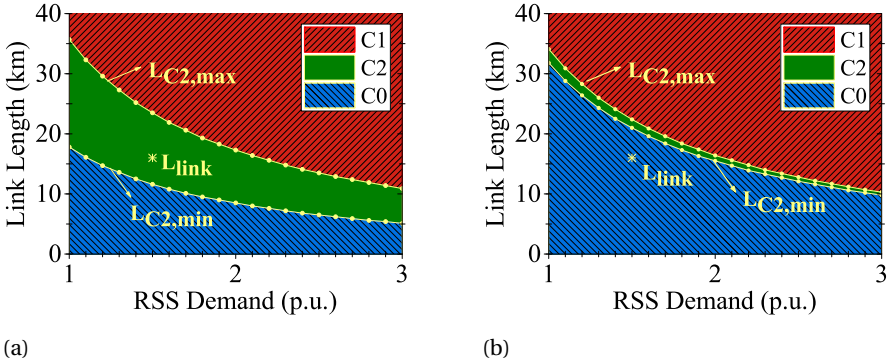


Figure 3.6: Optimal efficiency configuration corresponding to link length and RSS power demand at (a) pf=0.9 (b) pf=1.

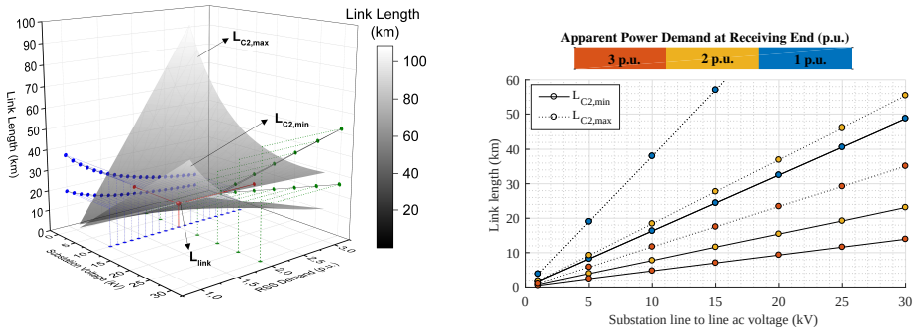
3.2.3. EFFICIENCY BOUNDARIES

For a system described by the parameters in Table 3.2, the appropriate choice of the configuration (C_{apt}) varies with the given link length $l = L_{\text{link}}$ and the operating conditions. For the studied case, only two relevant crossovers define C_{apt} as per (3.32).

$$C_{\text{apt}} = \begin{cases} C0, & \text{if } (L_{\text{link}} < L_{\text{C2,min}}) \\ C1, & \text{if } (L_{\text{link}} > L_{\text{C2,max}}) \\ C2, & \text{if } (L_{\text{link}} \geq L_{\text{C2,min}}) \wedge (L_{\text{link}} \leq L_{\text{C2,max}}) \end{cases} \tag{3.32}$$

The maximum efficiency boundaries for selecting the operational configuration specific to the normalized RSS demand $S_{\text{RSS}}/S_{\text{link}}$, pf and link length between SSS and RSS are shown in Figure 3.6 and are computed based on (3.32).

From Figure 3.6a, it can be observed that the boundary $L_{\text{C2,min}}$ at which a shift in C_{apt} occurs from configuration with only ac links (C0, blue) to a parallel ac-dc link operation



(a) (b)

Figure 3.7: Sensitivity of C2 efficiency boundary to (a) $V_{\text{LL,rms}}$ (x-axis) with varying operating S_{RSS} (y-axis) at pf=0.9 (b) XZ projection for different apparent power demands.

(C2, green) decreases as the power demand increases. A similar trend with demand is observed in the shift from C2 (green) to pure dc operation (C1, red) at boundary $L_{\text{C2,max}}$. It can be inferred that as S_{RSS} increases, preference for dc based power delivery for a given L_{link} increases. For example, C2 is the most efficient configuration for the depicted point L_{link}(1.5,16). However, if the demand is 3 p.u, C1 is more efficient, while, C0 is more efficient if the demand is 1 p.u. Another important observation from Figure 3.6a is that the efficiency range ($\Delta L_{\text{link}} = L_{\text{C2,max}} - L_{\text{C2,min}}$) for C2 increases with decrease in S_{RSS}. Also, Figure 3.6b depicts that ΔL_{link} is relatively lower if the operating pf=1.

In conclusion, this section shows that the parallel ac-dc link based power delivery is relatively the most efficient configuration within a defined window of link lengths that expands with decreasing RSS demand and power factor.

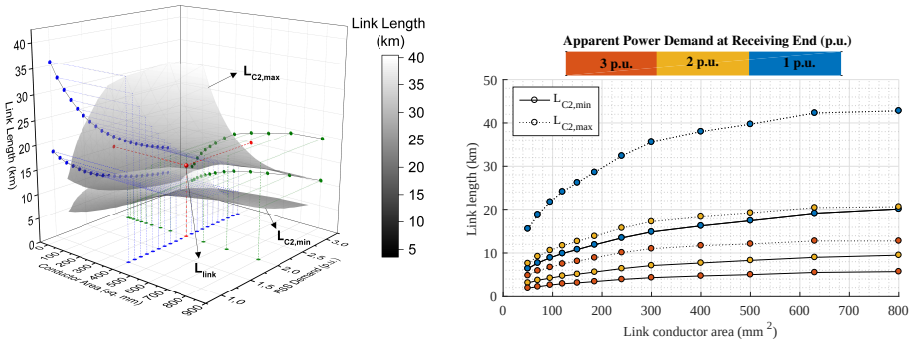
3.3. SENSITIVITY ANALYSIS

The previous section defines the efficiency boundaries of parallel ac-dc link configuration C2 for the link lengths bounded by $L_{\text{C2,min}}$ and $L_{\text{C2,max}}$ with varying operating conditions specific to a system with parameters listed in Table 3.2. This section provides the sensitivity analysis of the defined boundary with varying grid voltage, link conductor area and converter efficiency. During the sensitivity analysis corresponding to a particular variable, the values of all other parameters is the same as Table 3.2, unless otherwise specified.

3.3.1. AC SUBSTATION VOLTAGE

Figure 3.7a shows that the region bounded by the surfaces representing $L_{\text{C2,max}}$ and $L_{\text{C2,min}}$ increase with $V_{\text{LL,rms}}$ (x-axis) and S_{RSS} (y-axis). C2 is the most efficient configuration for any system with link length L_{link} operating in this region. Figure 3.7b shows the XZ-projection of Figure 3.7a for different power demands.

The projection of the two surfaces in the YZ plane at $V_{\text{LL,rms}} = 10\,\text{kV}$ corresponds to the 2D representation of the same operating condition shown in Figure 3.6a. The projec-



(a) (b)

Figure 3.8: Sensitivity of C2 efficiency boundary to (a) A_{con} (x-axis) with varying operating S_{RSS} (y-axis) at pf=0.9 (b) XZ projection for different apparent power demands.

tion of the surfaces in the XZ-plane at $S_{RSS} = 2$ p.u shows that $L_{C2,min}$ and $L_{C2,max}$ linearly increase with grid voltage. This is consistent with the direct-square relationship mathematically predicted in (3.30) and (3.31) because the base power (S_{link}) used to normalize the depicted S_{RSS} also proportionally increases with $V_{LL,rms}$. The main conclusion is that the efficiency range of C2 expands with increasing grid voltage but the bounded region occurs at higher link lengths for a given S_{RSS}.

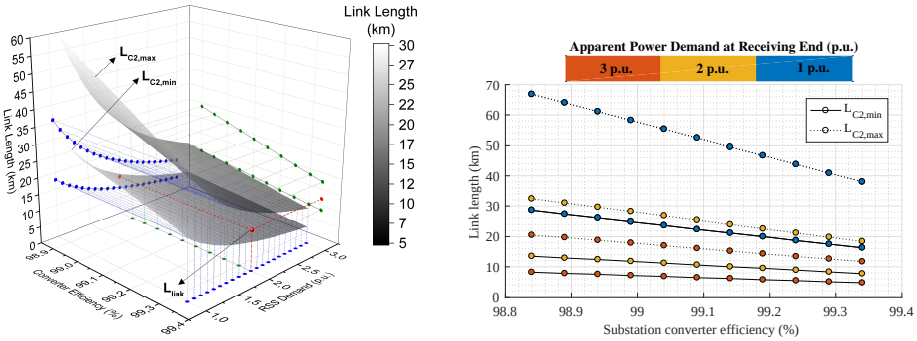
3.3.2. CONDUCTOR AREA

Figure 3.8a shows the efficiency boundary surfaces $L_{C2,min}$ and $L_{C2,max}$ with varying A_{con} (x-axis) and S_{RSS} (y axis). C2 is the most efficient configuration for any system with link length L_{link} operating within this bounded region. Figure 3.8b shows the XZ-projection of Fig. 3.8a for different power demands.

The base power S_{link} used to normalize the actual MVA demand S_{RSS} increases with cross-sectional area due to a corresponding increase in the rated current carrying capability of the conductor. The YZ-plane projection at $A_{con} = 400\,mm^2$ corresponds to the 2D representation of the same operating condition as Figure 3.6a. The XZ-plane projection shows the variation of $L_{C2,min}$ and $L_{C2,max}$ with A_{con} at S_{RSS} =2 p.u. Mathematically, the relationship is described by the corresponding variation in the ac and dc link conductor resistances in (3.30) and (3.31). The main conclusion is that the efficiency range of C2 expands with increasing A_{con}, however, the bounded region occurs at higher link lengths for a given S_{RSS}.

3.3.3. SUBSTATION CONVERTER EFFICIENCY

Thus far, results are presented by assuming a flat efficiency curve for MMC at 99.34 %. However, the substation efficiency can vary with converter design, rating as well as number of converters per substation. Furthermore, even for a given converter station design, the efficiency can dynamically vary with loading as a percentage of rating corresponding to Figure 3.3. Figure 3.9a offers a generic insight on the variation in the surfaces $L_{C2,min}$



(a) (b)

Figure 3.9: Sensitivity of C2 efficiency boundary to (a) converter station efficiency (x-axis) with varying operating S_{RSS} (y-axis) at pf=0.9 (b) XZ projection for different apparent power demands.

and $L_{C2,max}$ with varying efficiency (x-axis) corresponding to any possible demand (y-axis). Figure 3.9b shows the XZ-projection of Fig. 3.9a for different power demands.

For example, if the $S_{RSS} = 2$ p.u, the value of $L_{C2,min}$ and $L_{C2,max}$ for any possible converter efficiency can be estimated from the XZ-projection. The observed relationship is consistent with the analytical expression derived in (3.30) and (3.31). Similarly, the slice of the surface plot at 99.34 % projected onto the YZ-plane shows the variation with S_{RSS}, consistent with the result in Figure 3.6a. Therefore, C2 is the most efficient configuration if the system with link length L_{link} exists in the region bounded within the surfaces $L_{C2,min}$ and $L_{C2,max}$ for the possible operating power and converter efficiency.

3.4. ECONOMIC CONSIDERATIONS

In this section, the economic viability boundaries of the configurations for the system corresponding to the case-study in Section 3.2 will be described based on the assumptions highlighted in Section 3.1.8. The considered converter cost is 50€/kVA, while that of laying an additional 3-phase ac cable link is 100€/m; a sensitivity analysis to the economic viability considerations corresponding to these parameters will be explored. Let $L_{10,C0\text{-}C2}$ be the link length for which the payback period of additional investment of C2 over C0 ($f_{c,C2} - f_{c,C0}$) is 10 years. Also, let $L_{10,C1\text{-}C2}$ be the link length for which the payback period of additional investment of C2 over C1 ($f_{c,C2} - f_{c,C1}$) is 10 years. Then, the region enclosed by $L_{10,C0\text{-}C2}$ and $L_{10,C1\text{-}C2}$ describes the economic viability for configuration C2. This economic viability region is overlayed upon the efficiency boundaries in Figure 3.6a and depicted in Figure 3.10.

It can be observed that the plot lines $L_{C2,min}$, $L_{C2,max}$, $L_{10,C0\text{-}C2}$ and $L_{10,C1\text{-}C2}$ segregate the area plot into 5 zones. Each zone corresponds to a different efficiency and economic viability combinations of possible configurations as shown in Table 3.3.

Zone 4 is the most interesting as it indicates that even though a system with only dc links (C1) is the most efficient in this region, the parallel ac-dc configuration (C2) can be a more economically viable choice. This is because even though the system has the

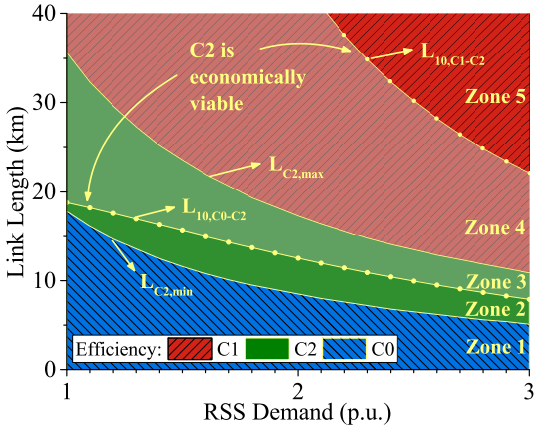


Figure 3.10: C2 economic viability boundary for a 10 year payback period with varying link lengths and RSS demand at pf=0.9.

Table 3.3: Viability Zones for Different Configurations

Zone	1	2	3	4	5
Most Efficient	C0	C2	C2	C1	C1
Economically viable	C0	C0	C2	C2	C1

same power delivery capacity during (n-1) contingencies, the required converter rating is lower for C2. The main conclusion is that configuration C2 is the ideal choice for a system with any link length in the region comprising (Zone 3) ∪ (Zone 4) within the operating conditions depicted for the parameters listed in Table 3.2. In this region, it will also be relatively more efficient than a solely ac link configuration (C0).

If the converter costs are reduced from 50€/KVA to 25€/KVA, it can be expected that the converter station costs of both configurations C1 and C2 will proportionally reduce. Consequently, the plot curves for $L_{10,C0\text{-}C2}$ and $L_{10,C1\text{-}C2}$ will shift downwards by a negative y-offset as shown in Figure 3.11. It can be observed that all zones except Zone 2 represent the same efficiency and economic viability boundaries as Table 3.3, albeit at different operating conditions and link lengths.

Zone 2a represents the region where C2 is more efficient but the payback on the additional investment as compared to C0 is greater than 10 years. In Zone 2b, C0 is the most efficient configuration but the additional investment in installing a new ac link does not recover within the considered 10 year payback time. Therefore, C2 should be the preferred solution in regions comprising (Zone 2b) ∪ (Zone 3) ∪ (Zone 4). The main conclusion is that if the converter costs reduce, the economic viability of parallel ac-dc link configuration will increase at comparatively shorter link lengths.

Figure 3.12 shows that if the considered cost of installing an additional underground 3-phase ac link is increased from 100€/m to 200€/m, the plot line corresponding to $L_{10,C0\text{-}C2}$ shifts downwards by a negative y-offset as compared to Figure 3.10. However,

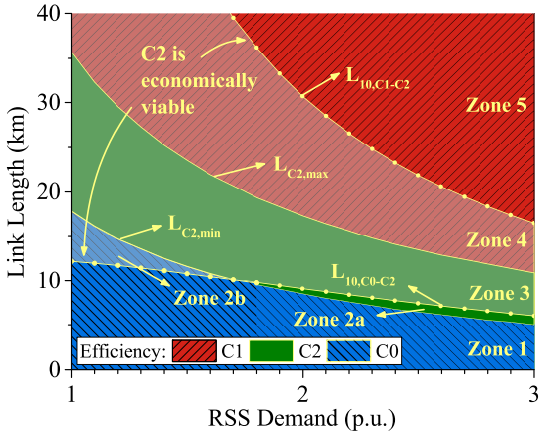


Figure 3.11: Sensitivity of C2 economic viability boundary to reduced converter price of 25 €/kVA with varying link lengths and RSS demand at pf=0.9.

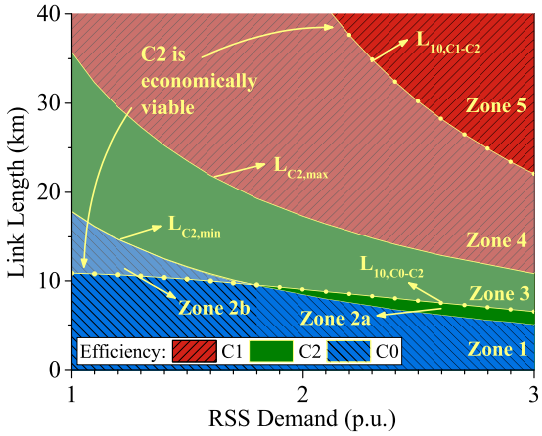


Figure 3.12: Sensitivity of C2 economic viability boundary to link conductor installation cost of 200 €/m with varying link lengths and RSS demand at pf=0.9.

the curve-line described by $L_{10,C1\text{-}C2}$ remains the same. Thus, it can be inferred that if the considered link conductor installation costs are higher, the region of economic viability of refurbished parallel ac-dc links expand, particularly to include relatively lower link lengths.

3.5. CONCLUSIONS

Different configurations, using ac to dc refurbishment concept, were compared in terms of the operating efficiency and economic viability for different power demands, power factors, dc link power share and link length, with respect to the conventional ac capacity

enhancement solution. The main premise is that the studied system configurations can maintain the same power delivery capacity during (n-1) contingency. To achieve this capacity, the configuration with only ac links have incurred costs for installing additional link conductors and that with only refurbished dc links have full load converter costs. On the other hand, refurbished parallel ac-dc link configurations can reduce the converter costs by maintaining the required capacity using reconfiguration.

The main finding is that a refurbished parallel ac-dc configuration can offer superior efficiency as compared to configurations with, solely, either ac or dc links, within a certain operating range. Based on the derived analytic equations, these efficiency boundaries were defined for a case-study. It was shown that within a window of relatively short link lengths the parallel ac-dc configuration (C2) is the most efficient, and this region expands with decreasing delivered power and power factor.

Sensitivity analysis suggests that the region in which C2 is relatively more efficient expands with increasing grid voltage, increasing link conductor area and decreasing converter efficiency. However, the link length coordinates for the surfaces by which this region is bound, consequently increases for given operating power, thus implying that the equivalent efficiency is achieved at longer link lengths.

The economic viability region of C2 does not completely overlap with its efficiency boundary and is relatively wider for the given RSS demand. The study suggests that the parallel ac-dc link configuration can be a favoured economic choice as compared to a system with only dc links for the defined zones because of lower converter costs even if the efficiency is not necessarily higher. A sensitivity analysis with decreased converter cost as well as increased link conductor installation cost can shift the economic viability window of C2 towards lower lengths for given operating power.

Therefore, the main conclusion is that refurbished parallel ac-dc reconfigurable distribution links can be an efficient and economically preferred possibility, particularly for delivering high power (few tens of MVA) at medium voltage levels (one to few tens of kV) for short distances (0-50 km).

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4

OPERATIONAL ASPECTS

This chapter is based on:
Aditya Shekhar, Thiago Batista Soeiro, Yang Wu and Pavol Bauer, "Optimal Power Flow Control in Parallel Operating AC and DC Distribution Links," *IEEE Transactions on Industrial Electronics,* Under Review, 2019.

In this chapter, the dynamic operation and control of the parallel ac-dc link between points of common coupling (PCC) will be shown to steer the active and reactive power. The studied system is illustrated in Figure 4.1. Specifically, it is shown that Zero Sequence Currents (ZSC) exist in the proposed system and control action to mitigate these currents is demonstrated with both simulations and experiments. Furthermore, it is shown that the optimal system efficiency depends on the power sharing ratio between the ac and dc links. It is mathematically proven that this ratio varies dynamically with operating conditions, based on which an algorithm is developed to steer the power with varying demand profile. This concept is verified through simulations and experiments and the potential energy savings are determined using case-study with adapted measured data from an actual medium voltage substation.

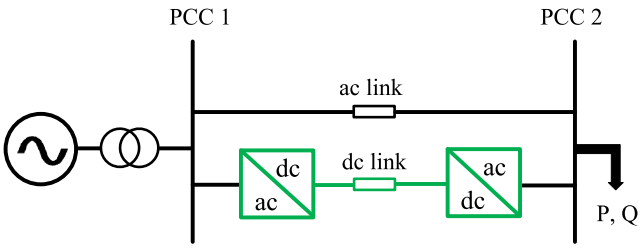


Figure 4.1: Illustration of parallel ac-dc link in a distribution network.

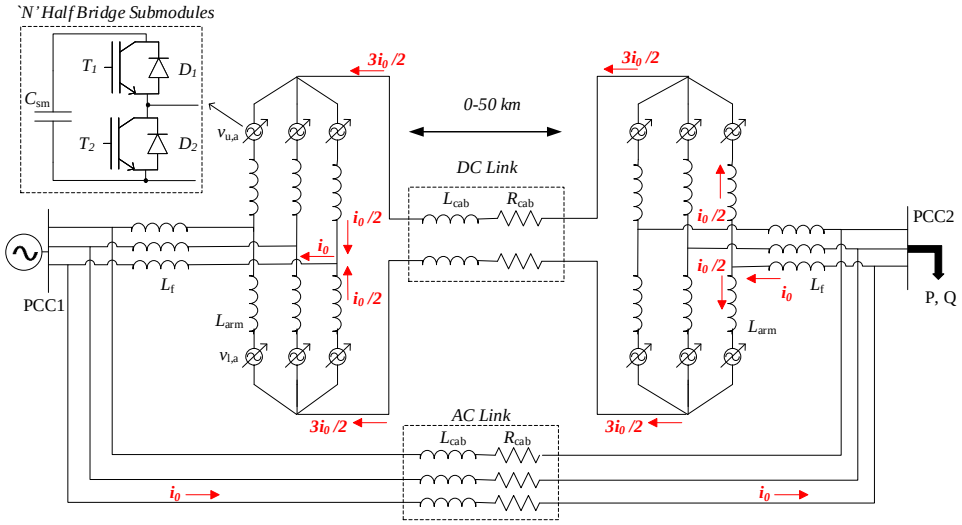


Figure 4.2: Path of zero sequence current flow in modular multilevel converter based parallel AC-DC distribution links.

4.1. CIRCULATING ZERO SEQUENCE CURRENTS (ZSC)

This section focuses on the problem on ZSC that externally circulate between the BTB-VSC based dc link and the ac link via the path provided by the dc link conductors. Although the system architecture constitutes of three wires in the ac link side, the dc-link creates a path for the zero sequence. Due to short link length, the inductance separating the converters is relatively small and consequently, the system is similar to parallel connected ac/dc converters sharing a common ac and dc side. The problem of ZSC in such systems with VSCs sharing a common ac and dc side is explored in [1–4]. This can lead to additional conduction losses, impact the operational range and in worse cases, cause failure in system components [5].

4.1.1. EQUIVALENT CIRCUIT FOR ZSC PATH

The equivalent circuit of a dc link with BTB MMCs in parallel with an ac link is shown in Figure 4.2. The MMCs are connected to the PCC1 and PCC2 via inductance L_f. Each arm of the MMC is abstracted as a inductance L_{arm} in series with a variable voltage source consisting of 'N' number of half bridge submodules. The submodule can either insert or bypass a capacitance C_{sm} using two IGBT switches T_1 and T_2 with antiparallel diodes D_1 and D_2 respectively. The conductors of both ac and dc links can be modelled as having a resistance R_{cab} and inductance L_{cab} that vary with the link length. For ac link phase current i_a, i_b and i_c, the zero sequence current component i_0 is given by (4.1).

$$i_0 = \frac{i_a + i_b + i_c}{3} \tag{4.1}$$

The path of i_0 through the parallel ac-dc link system is shown in Figure 4.2. For each phase of the ac link, i_0 splits into half for each arm of the MMC phase leg and returns via

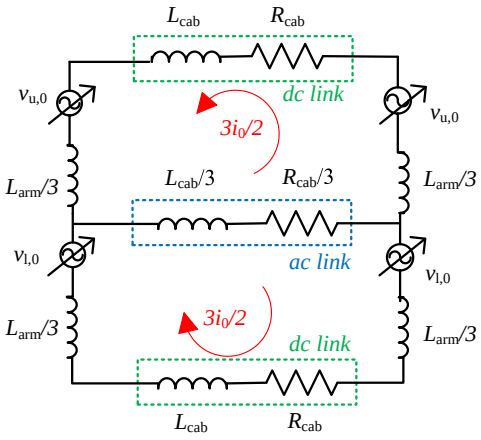


Figure 4.3: Equivalent circuit for the ZSC externally circulating between the dc link of the BTB MMC and parallel ac link.

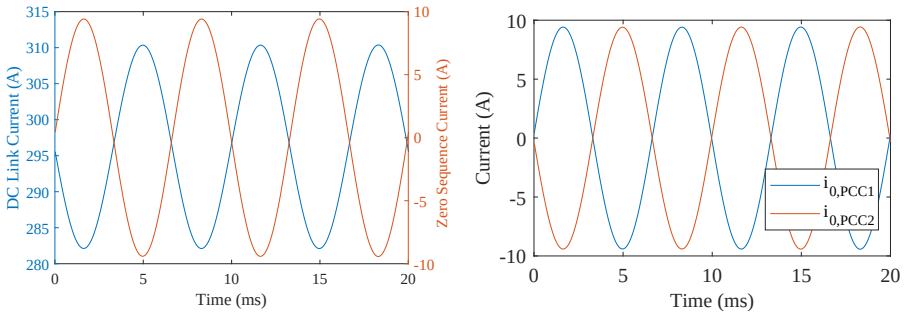
the dc link. The equivalent circuit for the zero sequence currents externally circulating between the dc link of the BTB MMC and the parallel ac link is shown in Figure 4.3.

The various system parameters used in this work are presented in Table 4.1. The ac and dc link each deliver 50 % power demand at PCC2. In order to simplify the interpretation of results, it is assumed that L_{arm} is designed such that the filter inductance L_f is zero.

Table 4.1: System parameters used for the simulation results.

Converter Capacity	10 MVA, pf=0.9
AC Grid Voltage (Line to line, rms)	10 kV
Submodule Capacitance C_{sm}	3.3-10 mF
Arm Inductance L_{arm}	2-5 mH
Total Power Demand at PCC2	10 MVA, pf=0.9
Number of Submodules (N)	9
DC Link Voltage	17 kV
Link Conductor Resistance	65 mΩ/km
Link Conductor Inductance	0.554 mH/km

The third harmonic current equal to $\frac{3i_0}{2}$ flows through each dc link conductor as shown in Figure 4.4a. The ZSC of the ac link given by (4.1) is depicted in the secondary y-axis of Figure 4.4a. The direction and magnitude of these ac and dc link ZSC are consistent with equivalent circuit depicted in Figure 4.3. The ZSC of MMC ac output currents at PCC1 and PCC2 are denoted by $i_{0,PCC1}$ and $i_{0,PCC2}$ shown in Figure 4.4b.



(a) (b)

Figure 4.4: Waveform for zero sequence circulating currents in the (a) dc and ac link (b) SSS and RSS side converters with link length of 5 km for C_{sm}=3.3 mH and L_{arm}=3 mH.

4.1.2. ZERO SEQUENCE CURRENT CONTROLLER (ZSCC)

RSS-SIDE MMC CONTROL SCHEMATIC

The controller schematic of RSS-side MMC is shown in Figure 4.5. The control structure of Output Current Controller (OCC), Circulating Current Controller (CCC) and Direct Voltage Control (DVC) is developed based on the theory presented in [6].

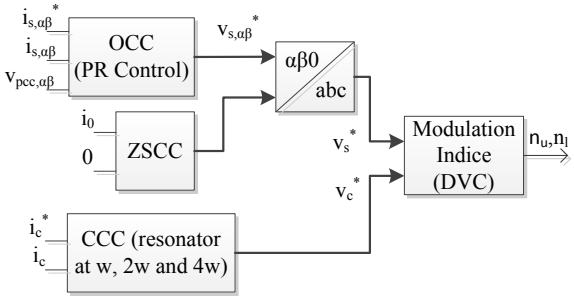


Figure 4.5: Controller block diagram for the RSS-side MMC with ZSCC.

The OCC generates the reference output voltage $v^*_{s,\alpha\beta}$ based on the error between the actual output ac current ($i_{s,\alpha\beta}$) and the reference current ($i^*_{s,\alpha\beta}$) corresponding to the required active and reactive power set-points. The bandwidth (BW) of the Proportional-Resonant (PR) OCC is $\alpha_{P,occ} = 2000$ rad/s so that the proportional gain $k_{p,occ} = \alpha_{P,occ} * L_{arm}/2$. The BW of the resonant integrator $\alpha_{R,occ} = 50$ rad/s so that the integral gain is given by $k_{i,occ} = 2\alpha_{R,occ} k_{p,occ}$. The BW of the voltage feed-forward $\alpha_{vff} = 1000$ rad/s.

The internally circulating arm current i_c (this current is different from the externally circulating ZSC in BTB MMC with shared ac and dc link) is controlled using CCC to the dc component corresponding to one-third of the dc link current (i_d) delivering the required active power share. The P-gain $k_{p,ccc} = 10$ with resonator gains $k_{i,ccc}$ corresponding to $\alpha_{i,ccc} = 200$ rad/s for frequencies w, $2w$ and $4w$, where w is the fundamental grid fre-

quency in rad/s.

Based on the generated reference voltages, the insertion indices for the upper and lower arms (n_u and n_l respectively) are calculated using Direct Voltage Control (DVC). The SSS-side MMC has identical bandwidths for OCC, CCC and DVC and is used to voltage control of the dc link. The RSS-side MMC control structure is modified by adding a ZSCC in the OCC and a 4^{th}-harmonic resonator in the CCC (i.e. at 4w) as shown in Figure 4.5. The simulated response of the system with and without these adaptations is discussed in subsequent sections.

OUTPUT CURRENT ZSCC

Figure 4.6 shows the control structure based on the theory in [5] for the ZSC suppression.

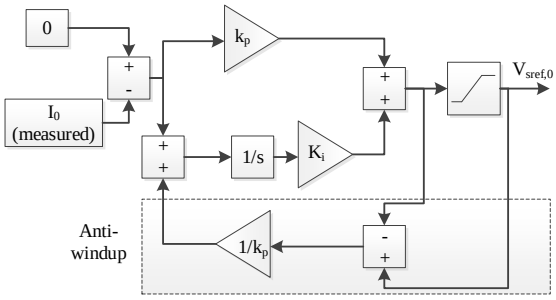


Figure 4.6: ZSCC PI-Control Structure with anti-windup.

The proportional-integral (PI) controller gains k_p and k_i are tuned based on the link length dependent inductance. The anti-windup loop is added to avoid high currents drawn by the converters due to the non-linearity introduced by the saturation block. The waveform for the dc link current and the zero sequence current in the ac link is shown in Figure 4.7, with ZSCC enabled at $t_0 = 0$. A variable time step solver is used in Simulink with a maximum of 1 ms.

It can be observed that i_0 nearly reduces to zero and the dc link current settles to nearly a constant value corresponding to the active power demand from the converter.

CIRCULATING CURRENT CONTROL WITH ZSCC

The internal circulating current of a given phase ($i_{c,a}$) is defined based on the upper ($i_{u,a}$) and lower ($i_{l,a}$) phase arm of the MMC as (4.2).

$$i_{c,a} = \frac{i_{u,a} + i_{l,a}}{2} \tag{4.2}$$

It is discussed in [6] that the dc component of $i_{c,a}$ is one third the dc link current during steady state. The parasitic component in sum-capacitor voltages translate to a 2^{nd} harmonic ripple in the internally circulating current, which is removed using a Proportional-Resonant (PR) controller sensitive to twice the fundamental frequency.

However, when the output current ZSCC was activated, a fourth harmonic ripple was observed in the $i_{c,a}$ at steady state for $t > t_0$ as shown in Figure 4.8. $i_{c,a,4h}$ circulates

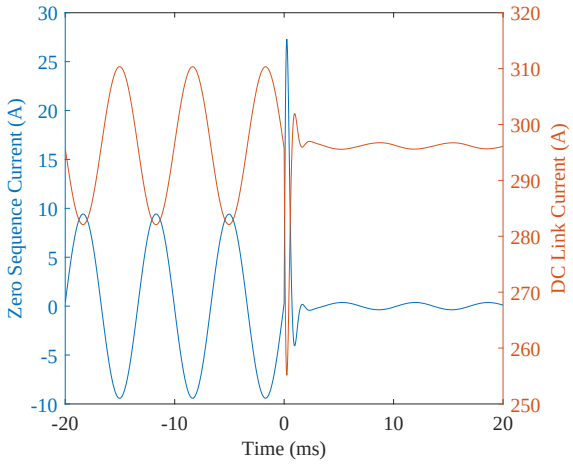


Figure 4.7: Zero Sequence and dc link current waveforms with ZSCC triggered at $t_0 = 0$.

between the arms of the MMC and does not appear in the output ac current of the dc link current, causing additional conduction losses. Therefore, a resonator tuned for four times the fundamental frequency was added to the internal circulating current control to eliminate $i_{c,a,4h}$, as can be observed in Figure 4.8.

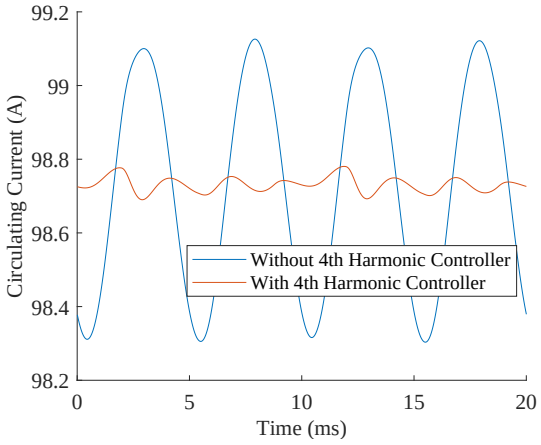


Figure 4.8: Effect of ZSCC on the internally ciculating currents in the MMC.

4.1.3. QUANTIFICATION OF ZERO SEQUENCE CURRENTS

The ZSC result in reduction of system efficiency due to conduction losses in the ac and dc link conductors. A sensitivity analysis of the ZSC problem with various parallel ac-dc system parameters must be performed at the design stage.

SENSITIVITY TO SYSTEM PARAMETERS

The system is simulated for varying link lengths for different submodule capacitance C_{sm} of 3.3 mF, 5 mF and 10 mF. The peak of the zero sequence current ($i_{ac0,peak}$) in the ac link when no ZSCC is employed is depicted in Figure 4.9.

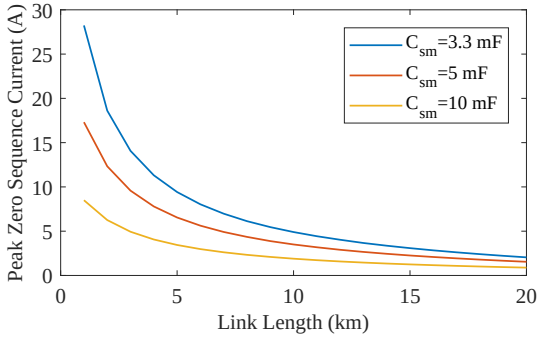


Figure 4.9: Peak zero sequence current with respect to link length for different MMC submodule capacitances with L_{arm}=3 mH.

It is evident that increasing the C_{sm} can limit the externally circulating ZSC in the parallel ac-dc link, particularly for short link lengths. On the other hand, this can increase the size and cost of the dc link MMCs as discussed in [7].

With increasing link length, the ZSC decreases due to a corresponding increase in the link conductor inductance. A similar reduction in ZSC can be expected if arm inductance is increased. However, an increase in L_{arm} would not only increase the cost, size and losses in the MMC, but also reduces the PQ-capability of the converter [8]. Therefore, mitigating the impact of ZSC using control techniques is important and shall be explored in Section 4.1.2.

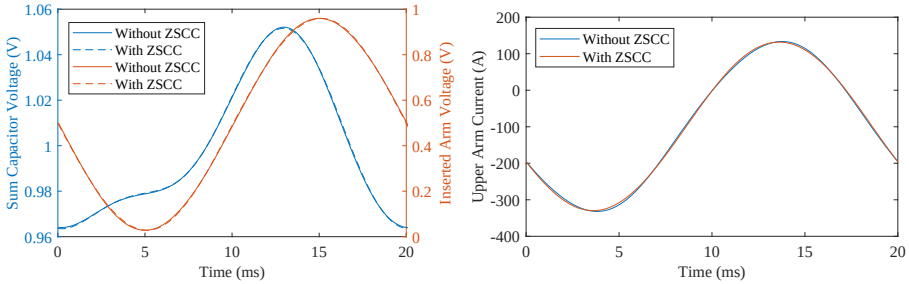
HARMONIC ANALYSIS OF SYSTEM WAVEFORMS

In order to numerically trace the path of ZSC depicted in Figure 4.3, the waveforms of arm current (i_u) and inserted arm voltage (v_u) are analysed. The relation between the sum capacitor voltages on an upper phase arm of the MMC ($V^{\Sigma}_{cu,a}$), the insertion indice (n_{ua}), the arm current (i_{ua}) and the inserted arm voltage (v_{ua}) is given by (4.3) and (4.4) as described in [6].

$$V^{\Sigma}_{cu,a} = \left(\frac{N}{C_{sm}}\right)\int n_{ua}\, i_{ua} \tag{4.3}$$

$$v_{ua} = n_{ua}\, V^{\Sigma}_{cu,a} \tag{4.4}$$

Figure 4.10 shows the MMC arm waveforms with and without ZSCC under full load condition with $N = 9$, $C_{sm} = 3.3\,\text{mF}$ and $L_{arm} = 3\,\text{mH}$ for a 5 km link. It can be observed that for these values, the impact of i_0 is not significant, and therefore, the converter losses may not change considerably. On the other hand, the i_0 with a peak of about 10 A will flow through the link conductors, leading to additional conduction losses if left unchecked.



(a) (b)

Figure 4.10: Converter arm parameter wave-forms with and without ZSCC for (a) Sum capacitor voltage and arm voltage (b) Arm Current.

It can Let t_0 represent the time instant at which the zero sequence current controller (described in Section 4.1.2) is enabled. The Fast Fourier Transform (FFT) is performed on 10 cycles of the waveforms for i_{ua}, $V^{\Sigma}_{\text{cu,a}}$ and n_{ua} at steady-state for $t < t_0$ and $t > t_0$. The third harmonic (3h) component as a percentage of fundamental (50 Hz) for different submodule capacitance and link length is given in Table B.1.

Table 4.2: Third harmonic components arm current ($i_{\text{ua,3h}}$) and sum capacitor voltage ($v^{\Sigma}_{\text{ua,3h}}$) with varying link length (l) and submodule capacitance (C_{sm}) before and after $t = t_0$.

l	C_{sm}	$i_{\text{ua,3h}}$		$v^{\Sigma}_{\text{ua,3h}}$		$n_{\text{ua,3h}}$	
km	mF	% of fundamental amplitude					
		$t < t_0$	$t > t_0$	$t < t_0$	$t > t_0$	$t < t_0$	$t > t_0$
1	3.3	5.86	0.14	2.16	0.72	0	1.07
	5	3.76	0.13	1.38	0.5	0	0.76
2	3.3	4.1	0.21	1.29	0.68	0	1.07
	5	2.72	0.14	0.86	0.47	0	0.76
5	3.3	2	0.09	0.34	0.7	0	1.07
	5	1.39	0.07	0.25	0.48	0	0.76
10	3.3	0.98	0.04	0.34	0.71	0	1.05
	5	0.71	0.03	0.21	0.48	0	0.76

The variation in $i_{\text{ua,3h}}$ is in accordance to the trend observed in Section 4.1.3 with different l and C_{sm} for $t < t_0$ and significantly reduces, close to 0 due to control action for $t > t_0$. This can be inferred from the consequent change in $n_{\text{ua,3h}}$ from 0 at $t < t_0$ to a higher value at $t > t_0$. The related influence of $i_{\text{ua,3h}}$ and $n_{\text{ua,3h}}$ can be observed in $v^{\Sigma}_{\text{ua,3h}}$. Note that even though $v^{\Sigma}_{\text{ua,3h}}$ varies with both l and C_{sm} for $t < t_0$, the dependence of l is negligible for $t > t_0$, indicating good performance of the control designed.

4.2. OPTIMAL POWER FLOW CONTROL

This section focuses on developing the concept of optimal power sharing between the ac and dc links to achieve the maximum dynamically varying operating efficiency . The analytic expression describing the dependency of this power sharing ratio on the system parameters like ac grid voltage, dc link voltage, link conductor area and length as well as operating conditions such as converter efficiency, power demand and power factor is derived. The working of the developed algorithm is validated by simulating a 10 kV, 30 MVA system with three dc links employing back to back modular multilevel converters operating in parallel with a single three phase ac link. Further, the concept is also validated experimentally. In Figure 4.11, the system diagram is shown for a parallel ac-dc link of a given length 'l' between Sending-end Substation (SSS) and Receiving-end Substation (RSS) as per the discussion in preceding chapters.

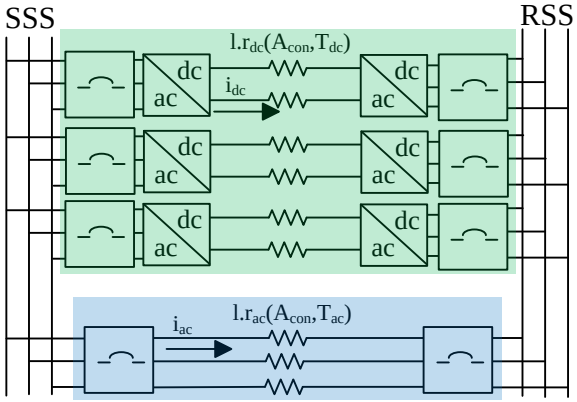


Figure 4.11: Schematic Diagram of parallel operating dc and ac links.

Table 5.1 lists the test parameters used for the presented results, unless specified otherwise. These values correspond to the refurbishment strategy of a benchmark ac distribution link system described in Chapter 2. The base power physically describes the rated capacity of a single 3-phase ac link in the system.

Table 4.3: Test Parameters

$V_{\text{LL,rms}}$	10 kV
Type of conductor	Aluminum
A_{con}	630 mm^2
Rated conductor current	590 A
N_{ac}, N_{dc}	3, 6
Capacity during (n-1) contingencies	3 p.u. at pf=0.9
Base Power	10.2 MVA

4.2.1. APPROXIMATION BASED ON LINK CAPACITIES

Although the reconfigurable dc link in parallel with the ac link can be dimensioned with considerably low converter rating to achieve the same system level capacity during (n-1) contingencies, the losses during normal operation can be minimized if the share of RSS active power demand met by the dc link (y_{opt}) is increased. This is particularly important as the average demand at RSS and the link length between SSS and RSS increases [9]. The conductor currents i_{ac} and i_{dc} are described by (4.5) and (4.6), respectively.

$$i_{\text{ac}} = \frac{(1-y)S_{\text{RSS}}\cos\theta}{\left(\frac{N_{\text{ac}}}{3}\right)\sqrt{3}V_{\text{LL,rms}}} = \frac{\sqrt{3}(1-y)S_{\text{RSS}}\cos\theta}{N_{\text{ac}}V_{\text{LL,rms}}} \tag{4.5}$$

$$i_{\text{dc}} = \frac{yS_{\text{RSS}}\cos\theta}{\left(\frac{N_{\text{dc}}}{2}\right)V_{\text{dc}}} = \frac{\sqrt{3}yS_{\text{RSS}}\cos\theta}{N_{\text{dc}}k_{\text{e}}V_{\text{LL,rms}}} \tag{4.6}$$

The total power loss in the link conductors ($P_{\text{L,cond}}$) is given by (4.7),

$$P_{\text{L,cond}} = N_{\text{ac}}i_{\text{ac}}^2 lr_{\text{ac}}(A_{\text{con}}, T_{\text{ac}}) + N_{\text{dc}}i_{\text{dc}}^2 lr_{\text{dc}}(A_{\text{con}}, T_{\text{dc}}) \tag{4.7}$$

Figure 4.12 shows the operating parameters of the ac and dc link conductors for different S_{RSS} at pf=0.9 with varying y.

The observed variations in currents and temperature, and therefore the resistances are in part due to the conductor utilization corresponding to y, N_{ac} and N_{dc}; and in part due to dc voltage enhancement factor k_{e}. The conductor utilization is maximum for the operating point $y = y_{\text{con}}$, at which the ac and dc link conductor currents are equal. This can be derived be equating (4.5) and (4.6), given by (4.8).

$$y_{\text{con}} = \frac{k_{\text{e}}N_{\text{dc}}}{N_{\text{ac}} + k_{\text{e}}N_{\text{dc}}} \tag{4.8}$$

Due to differences in operating conditions for ac and dc links, the respective conductor resistances can be different even though A_{con} is equal for both, leading to a small shift in the optimal efficiency point. The total system efficiency is also influenced by the losses in the dc link converters resulting in a dynamic shift in the optimum dc to ac active power ratio (y_{opt}), as shall be discussed in Section 4.2.2. y_{con} is a reasonable first approximation for minimizing system losses, in particular serving as a starting value for iterative loops required for estimating the y_{opt}.

4.2.2. SHIFT DUE TO CONVERTER LOSSES

Assuming that the reactive power demand at RSS is fully met by the substation converter, the RSS side converter demand $S_{\text{conv,RSS}}$ is given by (4.9).

$$S_{\text{conv,RSS}} = S_{\text{RSS}}\sqrt{y^2\cos^2\theta + \sin^2\theta} \tag{4.9}$$

Based on the loading, the corresponding efficiency, η_{RSS} can be selected. At the SSS side, the converter supplies the rated dc link power and the demand $S_{\text{conv,SSS}}$ is ideally approximated as (4.10).

$$S_{\text{conv,SSS}} = yS_{\text{RSS}}\cos\theta \tag{4.10}$$

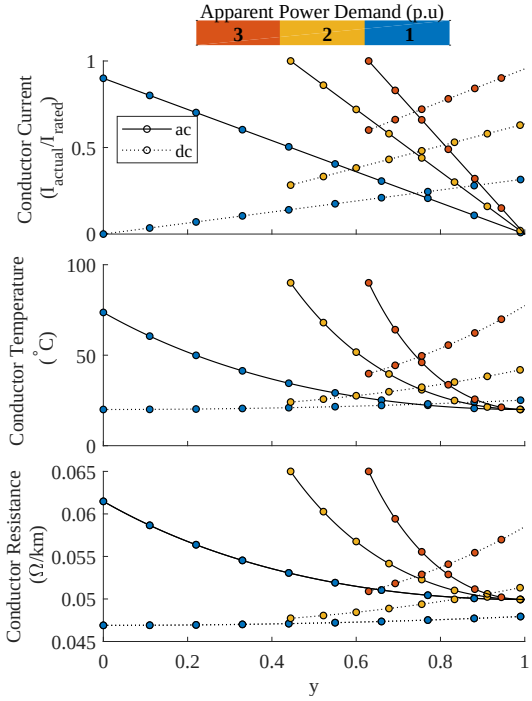


Figure 4.12: Estimated operating current, temperature and resistance for ac and dc link conductors for different RSS apparent power demand at pf=0.9 with varying y.

The efficiency of the SSS converter is η_{SSS}. The exact $S_{\text{conv,SSS}}$ is slightly higher corresponding to the RSS converter and dc link conductor losses. The total converter losses ($P_{\text{L,conv}}$) in the system is given by (4.11).

$$P_{\text{L,conv}} = (1-\eta_{\text{SSS}})S_{\text{conv,SSS}} + (1-\eta_{\text{RSS}})S_{\text{conv,RSS}} \tag{4.11}$$

The total system losses $P_{\text{L,sys}}$ is the summation of (4.7) and (4.11), given by (4.12).

$$P_{\text{L,sys}} = P_{\text{L,cond}} + P_{\text{L,conv}} \tag{4.12}$$

$P_{\text{L,sys}}$ as a percentage of S_{RSS} for different operating scemarios is shown in Figure 4.13.

It can be observed that y_{opt} increases with S_{RSS}. Furthermore, an increase in link length l increases the conductor losses but not the converter losses, thus shifting the y_{opt} in the favour of dc operation. It can be inferred that y_{opt} depends on several operating factors such as $V_{\text{ll,rms}}$, k_{e}, η, l, A_{con}, N_{ac}, N_{dc}, S_{RSS} and pf. A sensitivity analysis of the system efficiency with variation in these paramters is offered in Chapter 3.

4.2.3. ANALYTIC EXPRESSION FOR OPTIMAL POWER SHARING POINT

The analytic expression for the optimal value of y which will be derived is necessary to obtain insight on the various dependencies with variables $V_{\text{ll,rms}}$, k_{e}, η, l, A_{con}, N_{ac}, N_{dc},

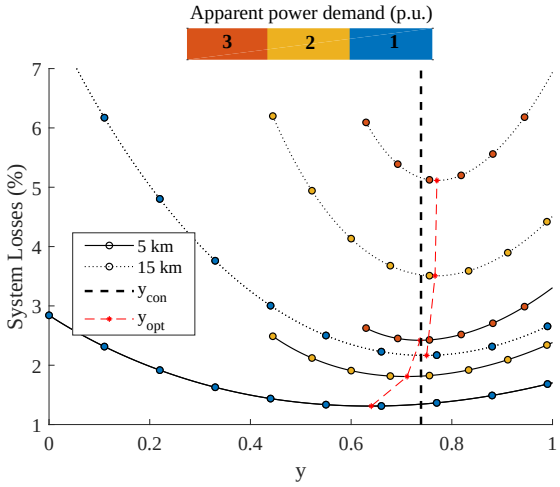


Figure 4.13: System losses as function of dc power share (y) for different apparent power demand and link length at pf=0.9. The y_{opt} (dashed red) and y_{con} (dashed black) are highlighted.

S_{RSS} and pf as suggested in Section 4.2.2. It can be applied at design stage to select the appropriate converter rating based on the efficiency trade-off highlighted in Section 5.3. By substituting (4.5) and (4.6) in (4.7) and differentiating $P_{l,\text{cond}}$ with respect to y, the expression (4.13) is obtained.

$$\frac{\partial P_{\text{L,cond}}}{\partial y} = \left(\frac{6lS_{\text{RSS}}^2\cos^2\theta}{V_{\text{ll,rms}}^2}\right) \times \left[y\left(\frac{r_{\text{ac}}(i)}{N_{\text{ac}}} + \frac{r_{\text{dc}}(i)}{k_{\text{e}}^2 \cdot N_{\text{dc}}}\right) - \left(\frac{r_{\text{ac}}(i)}{N_{\text{ac}}}\right)\right] \tag{4.13}$$

Since the resistance of the ac and dc link conductors ($r_{\text{ac}}(i)$,$r_{\text{dc}}(i)$) are function of y, they must be iteratively estimated. Similarly, substituting (4.9) and (4.10) in (4.11) and differentiating $P_{\text{L,conv}}$ with respect to y, the expression (4.14) is obtained.

$$\frac{\partial P_{\text{L,conv}}}{\partial y} = S_{\text{RSS}}\cos\theta[(1-\eta_{\text{SSS}}(i)) + (1-\eta_{\text{SSS}}(i))k_{\text{cf}}(i)] \tag{4.14}$$

$$k_{\text{cf}}(i) = \frac{y\cos\theta}{\sqrt{y^2\cos^2\theta + \sin^2\theta}} \tag{4.15}$$

The correction factor $k_{\text{cf}}(i)$ is a function of y, and thus, should be iteratively determined during the analytic estimation of y_{opt}. A good initial estimation for (4.15) is with $y = y_{\text{con}}$, where y_{con} can be found from (4.8). Similarly, $\eta_{\text{SSS}}(i)$ and $\eta_{\text{RSS}}(i)$ are iteratively determined functions of y. According to (4.12), the first derivative of total system losses $P_{\text{L,sys}}$ with respect to y can be found from (4.16).

$$\frac{\partial P_{\text{L,sys}}}{\partial y} = \frac{\partial P_{\text{L,cond}}}{\partial y} + \frac{\partial P_{\text{L,conv}}}{\partial y} \tag{4.16}$$

It can be inferred that the second derivative of $P_{\text{L,sys}}$ with respect to y, given by (4.17), is positive.

$$\frac{\partial^2 P_{\text{L,sys}}}{\partial y^2} = \left(\frac{6lS_{\text{RSS}}^2\cos^2\theta}{V_{\text{ll,rms}}^2}\right) \times \left(\frac{r_{\text{ac}}(i)}{N_{\text{ac}}} + \frac{r_{\text{dc}}(i)}{k_{\text{e}}^2 \cdot N_{\text{dc}}}\right) \tag{4.17}$$

This implies that the value of y for which (4.16) is equal to zero represents the minimum $P_{\text{L,sys}}$ for the specified operating conditions. The optimal efficiency point, y_{opt}, is therefore given by (4.18).

$$y_{\text{opt}} = \frac{1}{\left(\frac{r_{\text{ac}}(i)}{N_{\text{ac}}} + \frac{r_{\text{dc}}(i)}{k_{\text{e}}^2 \cdot N_{\text{dc}}}\right)} \left[\left(\frac{r_{\text{ac}}(i)}{N_{\text{ac}}}\right) - \left(\frac{V_{\text{LL,rms}}^2}{3lS_{\text{RSS}}\cos\theta}\right) \times \left(\frac{(1-\eta_{\text{SSS}}(i)) + (1-\eta_{\text{RSS}}(i))k_{\text{cf}}(i)}{2}\right)\right] \tag{4.18}$$

The analytically estimated y_{opt} using (4.18) with respect to S_{RSS} at pf=0.9 for link lengths of 5 km, 15 km and 30 km are shown in Figure 4.14 as compared to its exact solution. The value of y_{con} is also highlighted.

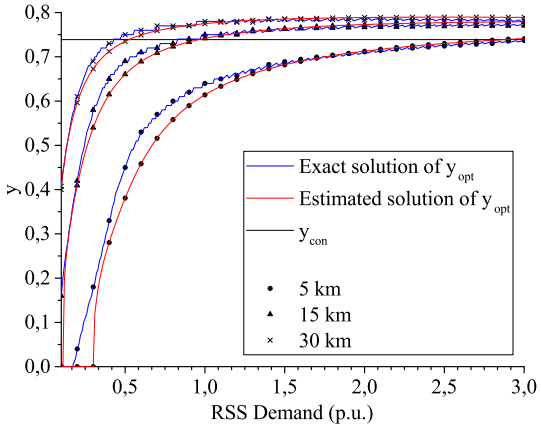


Figure 4.14: Analytically estimated y_{opt} as compared to its exact solution with varying S_{RSS} at pf=0.9 for different link lengths.

As S_{RSS} increases, y_{opt} is higher, indicating a greater preference for the dc link operation. Similarly, with increasing link lengths, the dc link must operate with higher share of power for the system to operate with minimal losses. The associated dependencies of y_{opt} shift with various system parameters, as described by (4.18).

Suppose the actual dc link active power share is $y_{\text{act}} = y_{\text{opt}} + \Delta y$, the deviation Δy from y_{opt} can occur due to a number of reasons, one of them associated with the constraint due to installed dc link converter capacity. Furthermore, if the power sharing algorithm is not dynamically employed, the parallel ac-dc link system will inevitable operate at a sub-optimal efficiency point over its operational lifetime, thus incurring avoid-

able losses. The impact of Δy on system losses ($\Delta P_{L,sys}$) is a function of operating conditions as indicated by (4.13) and (4.14), where in a higher slope implies a greater deviation in power losses from its minimum. The inferences associated with the tendencies of y_{opt} (from (4.18)) and $\Delta P_{L,sys}$ (from (4.13),(4.14)) are summarized in Table 4.4.

Table 4.4: Tendencies in y_{opt} and $\Delta P_{L,sys}$ with varying system conditions (↑ indicates increase and ↓ a decrease as the associated parameter increases).

	S_{RSS}	$V_{LL,rms}$	k_e	η	l	A_{con}
y_{opt}	↑	↓	↑	↑	↑	↓
$\Delta P_{L,sys}$	↑	↓	↓	↓	↑	↓

The inference supports the intuitive understanding that considering all other factors constant, if increase in a specified parameter implies a more efficient dc operation relative to the ac link, y_{opt} increases. Further, if this improves the efficiency of the overall system, $\Delta P_{L,sys}$ decreases. For example, an increase in η makes the dc link more efficient relative to the ac link if all other factors are assumed constant. Therefore, y_{opt} increases but $\Delta P_{L,sys}$ decreases. Considering that an increase in link length l results in a greater increase in ac link losses as compared to the dc link, y_{opt} increases. However, since the overall system losses increase, $\Delta P_{L,sys}$ increases in this case. An accurate knowledge of y_{opt} is important from power steering control point of view, as shall be explored in Section 4.2.4.

4.2.4. DEVELOPED ALGORITHM AND SIMULATED DYNAMIC PERFORMANCE

The flow diagram showing the developed algorithm for estimation of y_{opt} is shown in Figure 4.15. The method is based on the analytic equations derived in Section 4.2.

The measured values of RSS line voltage ($v_{ll,RSS}$) and current ($i_{ll,RSS}$) are used to determine the total RSS power demand (P_{RSS}, Q_{RSS}) in Step 0. In Step 1, the initial estimate ($y(0)$) at iteration i=0 is determined from (4.8). In step 2 and 3, all the indicated intermediate variables are estimated using the equations highlighted in Figure 4.15. The value of y_{opt} at i^{th} iteration is calculated in step 4 and the process is repeated until the solution converges. Optionally, if the range of operating power demand at RSS is known, Step 1 to 4 can be used to predefine a lookup table for the possible y_{opt}. Finally, the active and reactive power set points (P_{ref},Q_{ref}) for the output current controller of the RSS side converters is determined. The system shown in Figure 4.11 is simulated to verify the dynamic working of the developed algorithm. The specific parameters used for the depicted results are listed in Table 4.5.

All ac and dc link conductors are modelled as a resistance in series with a inductance. Substations at each side of the link system has three MMCs of 10 MVA capacity each, corresponding to $k_{cr} = 1$. Each SSS side MMC is responsible for the voltage control of an individual dc link, giving three dc links with dedicated back to back converters in parallel with a single three-phase ac link. The dc link voltage corresponds to a 10 kV ac grid with $k_e = 1.05 * \sqrt{2}$ to comply with the operating limits imposed by the considered arm inductance.

The developed optimal power sharing algorithm is only required at the RSS side

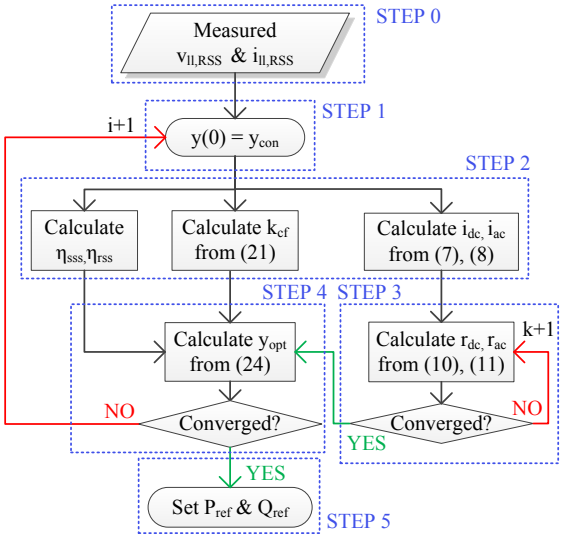


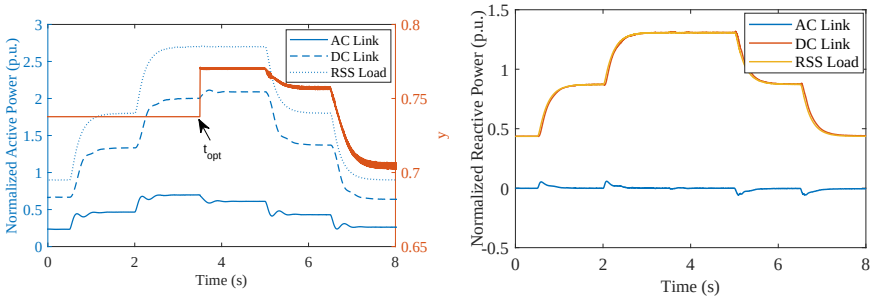
Figure 4.15: Algorithm for the estimation of y_{opt} during dynamic system operation of parallel ac-dc distribution links.

Table 4.5: Specific system parameters for the depicted simulation results.

Converters per substation	3
Per Converter Capacity	10 MVA
Submodule capacitance	3.3 mF
Arm inductance	3 mH
Arm Resistance	0.1 Ω
DC Link Capacitance	100 μF
DC link voltage	17.14 kV
Conductor Resistance	65 $m\Omega$/km
Conductor Inductance	0.55 mH/km
Link length	10 km

MMCs, each of which share one-third of the active and reactive power demand on the dc link system. All the simulated MMCs consist of a PLL, output current controller, circulating current controller and arm energy controllers as described in [10]. The insertion indices of the MMCs are computed using direct voltage control. The simulation results are shown in Figure 4.16.

For time t< t_{opt}, as the RSS load varies from 1 p.u. to 3 p.u. at pf=0.9 corresponding to the base power in Table 5.1, the total active power share of the three dc links corresponds to $y = y_{con}$. For time t> t_{opt}, the output of the y_{opt} algorithm described in Figure 4.15 is used to generate the reference powers for the current controllers of the RSS MMCs. It can



(a) (b)

Figure 4.16: Simulation results (a) Active power and y (optimal power sharing algorithm is triggered at time $t = t_{opt}$) (b) Reactive power needs are fully met by the dc link converters at the RSS side.

4

be observed in Figure 4.16a that y decreases with decreasing RSS load, consistent with the prediction in Figure 4.14. The active powers of the ac and dc links correspondingly vary. For the entire period of simulation, the total reactive power demand of the RSS is supported by the three MMCs at the RSS side of the dc link.

4.3. EXPERIMENTAL VALIDATION

4.3.1. TEST SETUP

Figure 4.17 shows the parallel ac-dc link set-up used to validate the concepts discussed in Section 4.1 and 4.2. The depicted set-up realizes the system with the equivalent circuit shown in Figure 4.11.

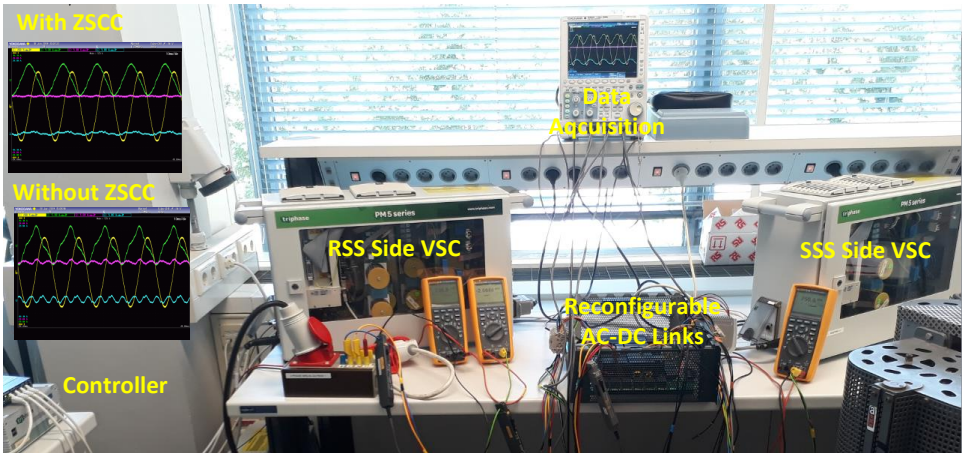


Figure 4.17: Test Setup used to validate key control concepts.

The main components consists of back-to-back two-level converters and the smart feeder prototype routing power from SSS to the RSS.

2-LEVEL VSC WITH L-C-L FILTER

A detailed description of the internal schematic, control and operation of the employed converters is described in [11]. The converter consists of three half bridge IGBT based VSC legs connected to an LCL filter on the ac side. In the current thesis, the component is used in a back-to-back dc link system connected in parallel with the ac link to steer active power from grid/3-phase ac source at SSS side to a constant power load (CPL) at RSS side. The parameters of the converter are given in Table 4.6.

Table 4.6: Parameters of the VSC used in the experimental set-up.

Parameter	Value
Rated Power	5 kVA
AC Grid Voltage	400 V (r.m.s)
Grid Side Inductance	1.5 mH
Grid Side Resistance	0.2 Ω
Filter Capacitance	20 μF
Converter Side Inductance	1.5 mH
Converter Side Resistance	0.2 Ω
DC-Side Voltage	750 V
DC Pole-to-Pole Capacitance	500 μF

SMART FEEDER FOR RECONFIGURABILITY

Figure 4.18 shows the internal connection diagram of the smart feeder prototype for parallel ac-dc reconfigurable links. This component can be used to physically select the ac and dc conductor paths between the SSS and RSS.

It can be observed that a total of 6 conductor paths exist between the 3-phase SSS bus voltages (u_a-u_c) and RSS bus voltages (v_a-v_c). Each of these paths are represented by resistances R_1-R_6. The contactors S_{ac1} and S_{ac2} can connect the paths as three phase ac links, while S_{dc1}, S_{dc2} and S_{dc3} can connect them to dc buses $dc_{sss,p}$, $dc_{sss,n}$, $dc_{rss,p}$ and $dc_{rss,n}$ as shown. S_{ac3} connects the ac terminals of the VSCs at SSS side ($vsc_{sss,a}$-$vsc_{sss,c}$) and RSS side ($vsc_{rss,a}$-$vsc_{rss,c}$). Each conductor path can be connected to either the ac or dc bus in a reconfigurable link architecture. The on-board protective logic shown in Figure 4.19 prevents simultaneous connection of the same link conductor to both ac and dc bus of the system. The logic ensures that (i) Neither S_{dc1} nor S_{dc2} can be closed if S_{ac1} is selected and vice versa (ii) Niether S_{dc2} nor S_{dc3} can be closed if S_{ac2} is closed and vice versa.

Figure 4.20 shows the schematic diagram depicting how different system components are physically connected.

The 3-phase ac source or grid at 400 V r.m.s is connected at SSS bus (u_a-u_c) while the load is connected to RSS bus (v_a-v_c). The powers P_{in} and P_{out} at SSS and RSS nodes are measured using three-phase power analyzer 1 and 2 respectively. These measurements are used to determine the system efficiency. The terminals of the rectifying VSC, responsible for dc voltage control, are connected between ac bus $vsc_{sss,a}$-$vsc_{sss,c}$ and dc

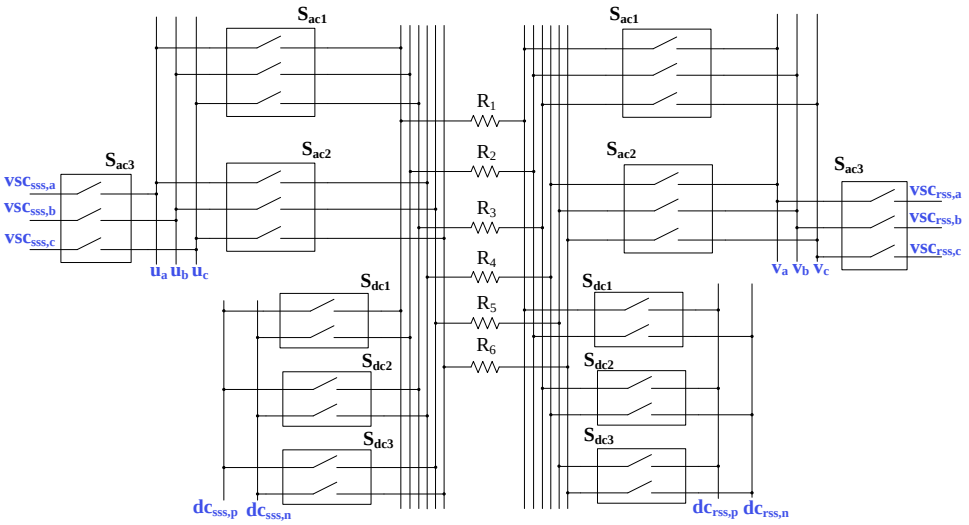


Figure 4.18: Internal connection diagram of the smart feeder prototype for parallel ac-dc reconfigurable links.

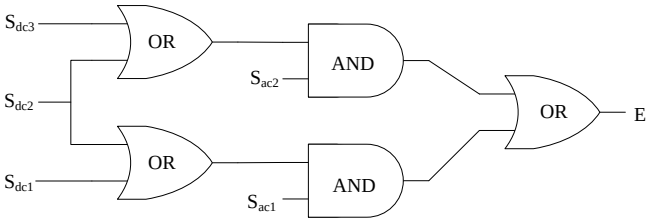


Figure 4.19: Internal logic of the smart feeder prototype.

bus $dc_{\text{sss,p}}$-$dc_{\text{sss,n}}$ at SSS side. The inverter VSC with active and rective power control is connected between ac bus $vsc_{\text{rss,a}}$-$vsc_{\text{rss,c}}$ and dc bus $dc_{\text{rss,p}}$-$dc_{\text{rss,n}}$ at RSS side.

The conductors of parallel ac and dc links are selected by sending six depicted optical signals to the smart feeder prototype. In the following experiments, the switches S_{ac1} and S_{dc3} are connected such that resistances R_1, R_2 and R_3 operate as three phase ac link while resistances R_5 and R_6 operate as positive and negative pole conductors of the dc link respectively. Each ac link conductor resistance is 6 Ω while dc link resistance is 2 Ω such that the operating condition with 3x ac conductors and 6x dc link conductors is emulated in the experiments. An oscilloscope is used to measure the ac link current (i_{ac}) and the output ac current of the VSC at the RSS side of the dc link ($i_{\text{vsc,rss}}$). Further, the line to line voltages of the RSS bus is also measured. From the oscilloscope waveforms, the actual active power share ratio y can be determined.

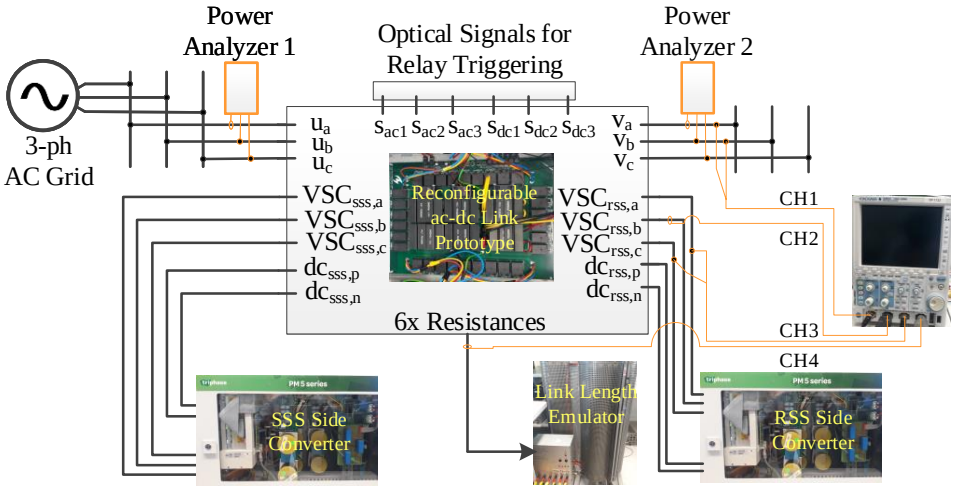


Figure 4.20: Schematic diagram of the experimental setup.

4.3.2. MITIGATION OF COMMON MODE CURRENTS

The ZSCC from Section 4.1 was implemented in the 2-level VSC controller in the experimental set-up. Figure 4.21 shows an oscilloscope measured waveform snapshot for $i_{\text{vsc,rss}}$, i_{ac} and the dc link current i_{dc} with and without the ZSCC active. In the test, the dc link is controlled to deliver the full power drawn by a 50 Ω constant resistance load at RSS bus, such that the fundamental 50 Hz component of current in the parallel ac link conductors is ideally zero.

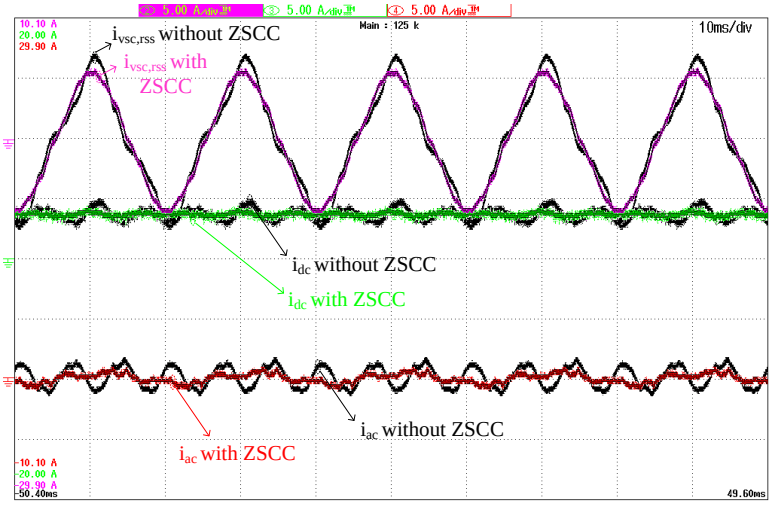


Figure 4.21: Measured waveforms of parallel ac-dc link set-up with and without ZSCC activated.

In the shown experimental results, a third harmonic current is clearly observed in i_{ac} and i_{dc} (black coloured waveforms) when the ZSCC is not active. As a consequence, the waveform of $i_{vsc,rss}$ is significantly distorted. When the ZSCC is activated, the zero sequence currents are mitigated such that measured i_{ac} is close to its ideal value of zero (red waveform), i_{dc} is a constant dc (green waveform) and $i_{vsc,rss}$ is a sinusoidal at 50 Hz (pink waveform).

4.3.3. MEASURED SYSTEM EFFICIENCY AND OPTIMAL POINT OF OPERATION

Figure 4.22 shows typical waveforms of current and voltages in the test setup with varying y.

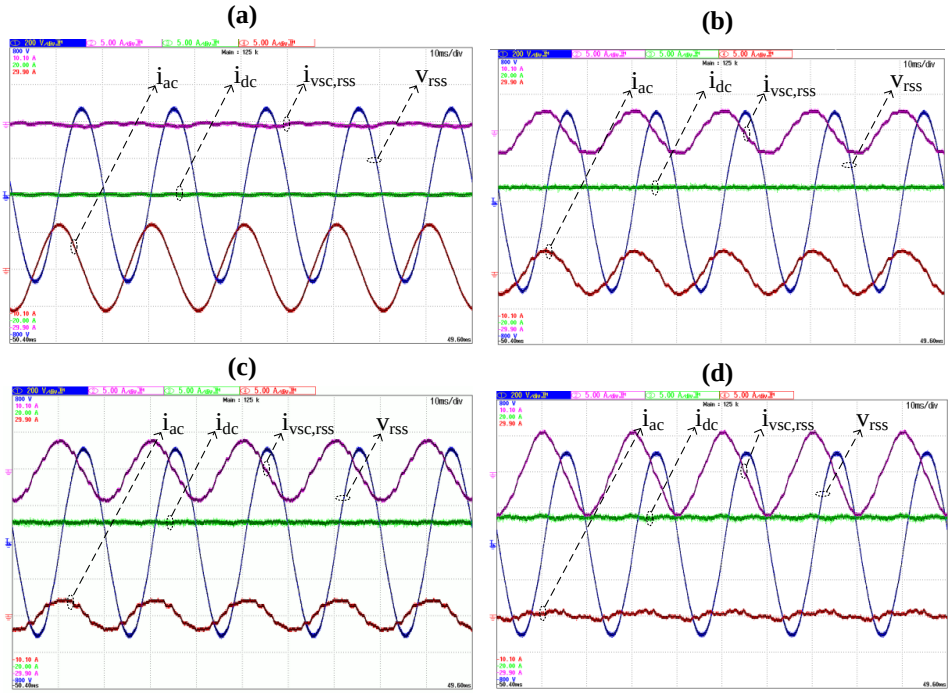


Figure 4.22: Measured waveforms of parallel ac-dc link set-up with (a) $y = 0$ (b) $y = 0.52$ (c) $y = 0.68$ (d) $y = 1$.

Therefore, it can be observed that the dc link can steer the share of active power in parallel ac-dc link system for a given load. Figure 4.23 shows the measured system efficiency as a function of y for a RSS load of 3.5 kW (blue) and 4 kW (red).

Note that as the share of dc link power increases for a given load power, the RSS side voltage increase due to lower voltage drop in the ac link resistances. To keep the power drawn constant, a CPL was used to correct for this effect with varying y. It can be seen that system efficiency reduces both for relatively high and low values of y, giving an optimal sharing point as discussed in Section 4.2. The theoretical estimate of y_{opt} and

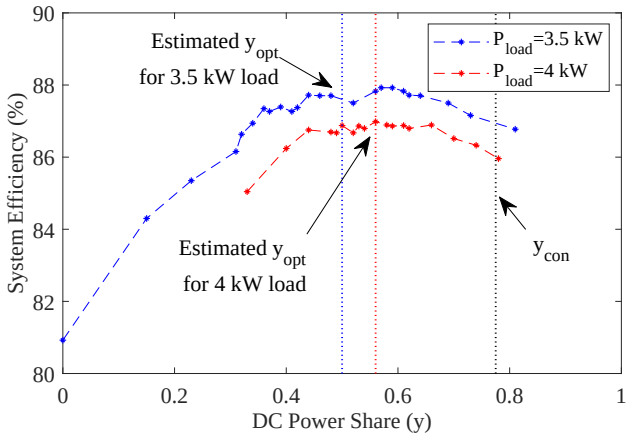


Figure 4.23: Measured system efficiency as a function of y.

y_{con} is highlighted considering measured full load converter efficiency of 94 % and line resistance of 2 Ω using (4.18) and (4.8) respectively. It can be observed that the system efficiency is lower if the power sharing is decided based on the thermal capacity of the ac and dc link conductors.

This optimal point shifts with operational conditions. For example, it can be observed from Figure 4.23 that when load power increases from 3.5 kW to 4 kW, the measured optimal efficiency power sharing ratio increases, consistent with the theory presented in Section 4.2. Thus, it can be concluded that dynamic optimal power flow control is important for efficient operation of the parallel ac-dc link system proposed in this thesis.

4.4. CASE-STUDY FOR ENERGY SAVING POTENTIAL

As highlighted previously, the system presented in Fig. 4.11 is based on the proposed dc refurbishment strategy of an existing 10 kV ac distribution link with physical parameters listed in Table 5.1. The annual data for the hourly average apparent power demand profile at the RSS of this system is shown in Fig. 4.24a. The values are shown in p.u. and the profile is adapted such that the peak demand (at 3 p.u.) corresponds to the maximum system capacity during (n-1) contingency. The corresponding exact solution of y_{opt} for a link length of 5 km is shown in Fig. 4.24b.

It can be observed that the tendency of y_{opt} to increase with demand is consistent with the theory presented in preceding sections. The total system energy loss over one year computed for constant power sharing ratio of y_{con} and optimal ratio y_{opt} is given by $E_{\text{loss},}(y_{\text{con}})$ and $E_{\text{loss},}(y_{\text{opt}})$, respectively. The annual energy saving potential (ΔE_{loss}) of implementing the optimal efficiency power sharing is thus given by (4.19).

$$\Delta E_{\text{loss}} = E_{\text{loss},}(y_{\text{con}}) - E_{\text{loss},}(y_{\text{opt}}) \tag{4.19}$$

ΔE_{loss} as a function of link length for different grid voltages (5 kV, 10 kV, 15 kV and

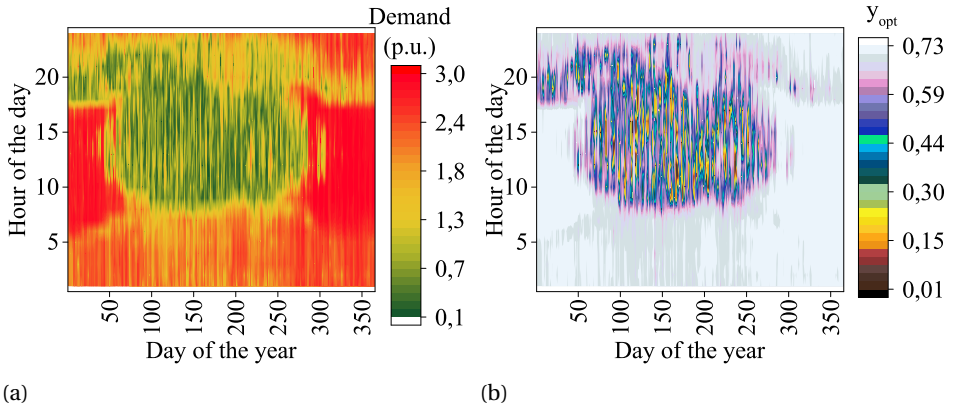


Figure 4.24: Case-study (a) Annual hourly average apparent power demand (b) Corresponding y_{opt} for a 10 kV grid voltage with link length and conductor area of 5 km and 630 mm^2 respectively.

20 kV) is given in Fig. 4.25. Note that the demand profile is the same as Fig. 4.24a in p.u. for all cases. For a given grid voltage, the base power is described by $S_{base} = \sqrt{3} v_{LL,rms} I_{cond,rated}$. While the cross-sectional area dependent rated link conductor current is kept constant at 590 A, S_{base} and therefore, the S_{RSS} in MVA varies as a function of grid voltage. Considering that y_{opt} varies as a function of $v_{LL,rms}$, l and S_{RSS}, the observed tendencies in ΔE_{loss} are correspondingly related to the simultaneous impact of these parameters.

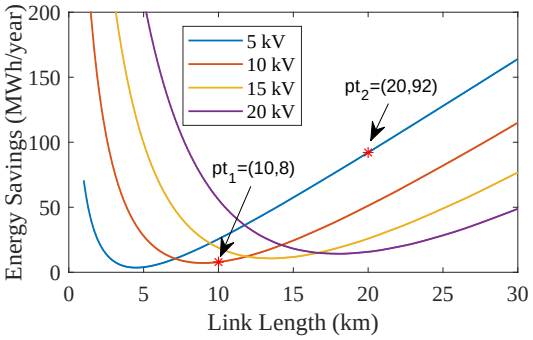


Figure 4.25: Energy Saving potential as a function of link length for different ac grid voltages.

It can be observed that for a given $v_{LL,rms}$ (and thus fixed S_{RSS} MVA demand profile), ΔE_{loss} saving potential has a minimum at a certain link length ($l_{\Delta Eloss,min}$). This tendency is an effect of variation in y_{opt} and the cumulative impact of $\Delta P_{L,sys}$ at various operating points over the year in accordance with Table 4.4. In the range $l < l_{\Delta Eloss,min}$, y_{opt} increases with link length from a magnitude relatively lower than y_{con}. This results in a net reduction in ΔE_{loss} with increasing l, even though $\Delta P_{L,sys}$ has an increasing tendency. In the range $l > l_{\Delta Eloss,min}$, y_{opt} is greater than y_{con} for relatively high RSS power demand and the slope of its variation reduces with l (refer Fig. 4.14). Therefore, ΔE_{loss} increase

due to the cumulative impact of the variation in y_{opt} relative to y_{con} and the increase in $\Delta P_{L,sys}$ due to increase in l. Finally, the energy savings increase with grid voltage for short link lengths, while decrease with increasing grid voltage for relatively longer link lengths. Furthermore, the $l_{\Delta Eloss,min}$ increases with increasing grid voltage.

ΔE_{loss} as a function of link length for different link conductor area (630 mm^2, 400 mm^2, 240 mm^2 and 185 mm^2) is given in Fig. 4.26. The grid voltage is taken constant at 10 kV and therefore, S_{base} varies as a function of $I_{cond,rated}$. It can be observed that the variation of ΔE_{loss} as a function of link conductor area is relatively less significant as compared to l and $v_{LL,rms}$.

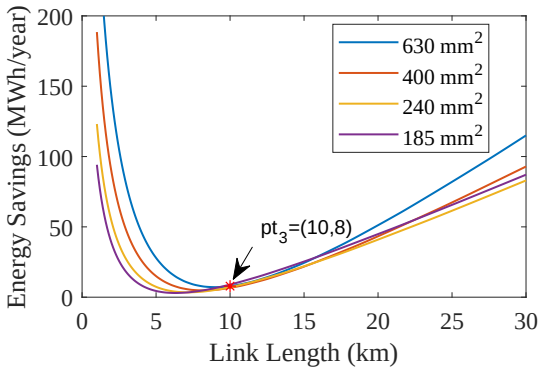


Figure 4.26: Energy Saving potential as a function of link length for different link conductor area.

4.5. CONCLUSIONS

This chapter proves that a back to back dc link can be operated in parallel with a medium voltage ac distribution link to optimally steer the active power while supporting the full reactive power at receiving end. This optimal efficiency power sharing ratio is not straightforward to calculate because the part of active power that flows through the parallel ac link does not have associated converter losses; however, it has higher link conductor thermal losses.

Both simulations and experimental results support the observation that significant efficiency gains can be achieved if the developed optimal power flow algorithm is used for dynamically varying the active power sharing ratio between parallel ac and dc links as a function of load power. This ratio and the potential energy savings are shown to vary with system parameters such as active and reactive power demand, ac grid voltage, dc link voltage, converter efficiency, link length and conductor area.

Using a case-study with load profile adapted based on measured substation data of hourly average power demand profile for one year, it is shown that annual energy saving potential in the range of 8-92 MWh can be achieved with varying link length between 10-20 km for grid voltages of 5-20 kV and conductor area of 185-630 mm^2. Since only computational cost is involved, this translates to 800-9600 euro savings per annum in operation. Therefore, the main conclusion of this chapter is that as distribution network

operators increase adopting dc technologies in their grid, optimal power flow control is relevant from the context of efficiency improvement of hybrid ac-dc power transmission systems.

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5

PROPER SYSTEM DIMENSIONING

This chapter is based on:
Aditya Shekhar, Thiago Batista Soeiro, Laura Ramírez-Elizondo and Pavol Bauer, "Offline Reconfigurability based Substation Converter Sizing for Hybrid AC-DC Distribution Links," *IEEE PES Transactions on Power Delivery,* Under Review, 2019.

In this chapter, it will be shown that with the design constraint of achieving constant system power capacity during (n-1) contingency, the competing dimensioning objectives for dc link voltage enhancement, dc active power share and substation converter rating will influence the operational complexity, operating efficiency during normal operation and installation cost. These aspects will be quantified using case-studies and sensitivity analysis to suggest optimal design values.

5.1. PARAMETERS CONSIDERED

5.1.1. DC LINK VOLTAGE RATIO (k_E)

As discussed in Chapter 3, for a three phase line to line rms voltage ($V_{LL,rms}$), the dc link voltage V_d is given by (5.1).

$$V_d = \frac{2k_e V_{LL,rms}}{\sqrt{3}} \tag{5.1}$$

where,

$$k_e = k_{opr} k_{ins} \tag{5.2}$$

The voltage enhancement factor k_e is defined by (5.2). k_{ins} depends on the dc to ac voltage ratio in consideration to the insulation performance of the link conductor infrastructure. k_{ins} is conservatively chosen as $\sqrt{2}$ for ac and dc cables of similar technology and cross-section according to the empirical study presented in Appendix A of this thesis. It is possible that k_{ins} can be more freely chosen based on the capacity and operational

requirements of the system in trade-off with higher costs related to the converter semiconductor and link insulation. Further, the minimum operating dc voltage limit of the converter depends on the reactive power requirements, fault current limiting and filter inductance, availability of grid connecting transformer tap and the modulation technique. Based on these considerations, the value of k_e must be adjusted in relation to k_{ins} by a correction factor k_{opr}, which is typically between 1 to 1.1. The minimum dc link voltage ratio $k_e \geq \sqrt{2}$ is, therefore, an important dimensioning constraint used in this thesis. The present chapter explores the influence of increasing k_e on different dimensioning aspects.

5.1.2. SHARE OF DC LINK ACTIVE POWER (y)

The dc link converters can be used to steer the active power (P_{dc}) by controlling the power sharing ratio (y) for a given RSS apparent power demand (S_{RSS}) at power factor pf=cosθ. The relevant equations describing the constraints y_{min} and y_{max} are given in Section 3.1.3. The selection of the appropriate y between y_{min} and y_{max} can influence the operating efficiency during healthy operating conditions, as shall be explored in Section 4.2.

5.1.3. SUBSTATION CONVERTER RATING (k_{CR})

k_{cr} is defined as the ratio of the rated active power of the substation converter ($P_{r,conv}$) to the total thermal power rating of the dc link conductors ($P_{r,cond,dc}$) for the given N_{dc}. It is constrained by $k_{cr} \leq 1$, signifying that if $P_{r,conv} > P_{r,cond,dc}$, no further improvement in system capacity can be achieved with increasing $P_{r,conv}$ for given configuration of N_{ac} & N_{dc}.

Maximizing k_{cr} may be of interest from maximum achievable system capacity point of view, however, it also increases the converter cost and size. Further, if k_{cr} is low, reconfiguration can be used to increase system capacity by decreasing N_{dc} and directing a higher active power flow through the ac path. This method of capacity enhancement can be advantageous during (n-1) contingency corresponding to converter faults (as explored in Section 5.2). Physically, dc to ac reconfiguration increases the utilization of the installed converter capacity (by increasing the effective k_{cr}). On the other hand, the thermally limited power capacity of the link conductors is higher for dc operating conditions as compared to ac at least by a factor of k_e. Thus the installation cost driven minimization of k_{cr} is a trade-off between the optimal converter and conductor utilization for achieving the required system capacity.

It can be inferred that the minimum converter derating for the given configuration of N_{ac} & N_{dc} is obtained at $y_{max} = y_{min}$. Therefore, by equating (3.11) and (3.12) and substituting $P_{max,dc}$ from (3.10), the minimum value of converter de-rating factor ($k_{cr,min}$) can be estimated based on (5.3), where, $P_{max,ac}$ can be computed from (3.9).

$$k_{cr,min} = \frac{S_{RSS,max}\cos\theta_R - P_{max,ac}}{\left(\frac{N_{dc}k_e}{N_{ac}}\right)P_{max,ac}} \tag{5.3}$$

Equation (5.3) is valid only for $N_{ac} > 0$ where the definition of y is relevant. The minimization of k_{cr} can decrease the operating efficiency of the system during healthy oper-

ation even if the system capacity requirement during (n-1) contingency is met, as shall be discussed in Section 5.3.

5.1.4. PROBLEM FORMULATION

The purpose is to highlight that the main challenge in the dimensioning of reconfigurable ac-dc links is the trade-off involved in selecting k_e, y and k_{cr}. Subsequent sections will show that with design constraint of achieving constant system power capacity during (n-1) contingency, the competing dimensioning objectives for k_e, y and k_{cr} will influence the operational complexity (Section 5.2), operating efficiency during normal operation (Section 4.2) and installation cost (Section 5.4). Table 5.1 lists the test parameters used for the presented results, unless specified otherwise.

Table 5.1: Test Parameters

$V_{LL,rms}$	10 kV
Type of conductor	Aluminum
A_{con}	630 mm^2
$I_{cond,rated}$	590 A
N_{ac}, N_{dc}	3, 6
Capacity during (n-1) contingencies	3 p.u. at pf=0.9
Base Power	10.2 MVA

The base power can be calculated from (3.9) at $N_{ac} = 3$ and physically describes the rated capacity of a single 3-phase ac link. Therefore, it will vary for the presented sensitivity analysis with $V_{LL,rms}$ and A_{con}. These values correspond to the refurbishment strategy of a benchmark ac distribution link system described in [1, 2]. k_e is initially assumed at minimum possible value of $\sqrt{2}$ and k_{cr} is considered at maximum possible value of 1. Consequently under normal operating conditions, it can be estimated from (3.9) and (3.10) that $P_{max,ac} = 1$ p.u and $P_{max,dc} = 2.8$ p.u respectively. The dc active power share y can be varied between 0.63 to 1 under these conditions. The rated active power of the installed substation converter is given by $P_{r,conv} = P_{r,cond,dc} = 2.8$ p.u corresponding to $k_{cr} = 1$.

5.2. RECONFIGURATION DURING (N-1) CONTINGENCIES

The maximum active power demand at RSS during (n-1) contingencies ($P_{max,RSS,n\text{-}1}$) is given by (5.4).

$$P_{max,RSS,n\text{-}1} = P_{cap,ac,n\text{-}1} + P_{cap,dc,n\text{-}1} \tag{5.4}$$

The active power capacities of the ac link ($P_{\text{cap,ac,n-1}}$) and dc link ($P_{\text{cap,dc,n-1}}$) are given by (5.5) and (5.6) respectively.

$$P_{\text{cap,ac,n-1}} = \frac{k_{\text{q}} N_{\text{ac,n-1}} V_{\text{LL,rms}} I_{\text{cond,rated}}}{\sqrt{3}} \tag{5.5}$$

$$P_{\text{cap,dc,n-1}} = \frac{k_{\text{cr,n-1}} k_{\text{e}} N_{\text{dc,n-1}} V_{\text{LL,rms}} I_{\text{cond,rated}}}{\sqrt{3}} \tag{5.6}$$

Here, $N_{\text{ac,n-1}}$ and $N_{\text{dc,n-1}}$ are the number of actively operating ac and dc link conductors respectively during a given (n-1) contingency in the system. $k_{\text{cr,n-1}}$ describes the ratio of active power that the substation converter can deliver ($P_{\text{cap,conv,n-1}}$) with respect to the dc link thermal capacity ($P_{\text{cap,dc-cond,n-1}}$) corresponding to $N_{\text{dc,n-1}}$ conductors during fault conditions. It is limited by the maximum value of 1, signifying that $P_{\text{cap,conv,n-1}} > P_{\text{cap,dc-cond,n-1}}$ cannot increase $P_{\text{cap,dc,n-1}}$. The factor k_{q} depends on the reactive power support provided by the RSS converter and is equal to 1 if the full load reactive power (Q_{rated}) is supported by the RSS converter. The total apparent power capacity of the system $S_{\text{cap,n-1}}$ is given by (5.7).

$$S_{\text{cap,n-1}} = \sqrt{P^2_{\text{max,RSS,n-1}} + Q^2_{\text{rated}}} \tag{5.7}$$

5.2.1. CAPACITY DURING SINGLE-CONDUCTOR TO GROUND FAULT (F_{1LG})

Consider a single line to ground fault in a practical distribution link system with $N_{\text{ori}} = 9$ described in Chapter 2. The remaining 8 conductors can be reconfigured within the constraint (5.8) to give different active power capacity based on (5.5) and (5.6).

$$N_{\text{ac,n-1}} + N_{\text{dc,n-1}} \leq N_{\text{ori}} - 1 \tag{5.8}$$

With F_{1LG}, the full reactive power needs at the RSS can be met by the healthy substation converter. Figure 5.1 shows the $S_{\text{cap,n-1}}$ that can be met during F_{1LG} with respect to $P_{\text{r,conv}}$ for different link configurations and k_{e}.

It can be seen that the maximum capacity is limited by k_{e} for the given $N_{\text{ac,n-1}}$ and $N_{\text{dc,n-1}}$, corresponding to the thermal limit of the link conductors associated with the specific configuration. While the achievable capacity reduces with the active power rating of the substation converter, an increase in $N_{\text{ac,n-1}}$ using system reconfiguration can achieve the required capacity for a lower converter rating. For example, 3 p.u. apparent demand at RSS with pf=0.9 can be met for F_{1LG} with 0.7 p.u, 1.7 p.u and 2.7 p.u active power converter rating for $N_{\text{ac,n-1}} = 6$, 3 and 0 respectively. Though minimization of converter rating can reduce installation cost, the required number of post-fault reconfigurations increase, therefore increasing the operational complexity of the system [2]. Furthermore, a lower converter rating can reduce the system efficiency during normal operation as shown in Section 4.2.

5.2.2. CAPACITY DURING THREE-CONDUCTOR TO GROUND FAULT (F_{3LG})

The (n-1) contingency analysis associated with achievable system capacity during link conductor faults with F_{1LG} is sufficient if the system consists of overhead lines or single cored cables. However, if the system consists of 3-cored cables, the possibility of F_{3LG}

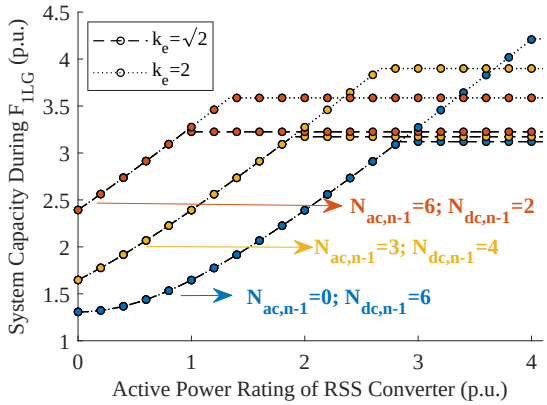


Figure 5.1: RSS apparent power demand capacity during (F_{1LG}) for different link conductor configurations with varying active power capacity of converter and k_e.

can occur. In such case only $N_{ori} - 3$ healthy conductors are available for post-fault reconfigurations. Figure 5.2 shows the $S_{cap,n-1}$ that can be met during F_{3LG} with respect to $P_{r,conv}$ for different link configurations and k_e.

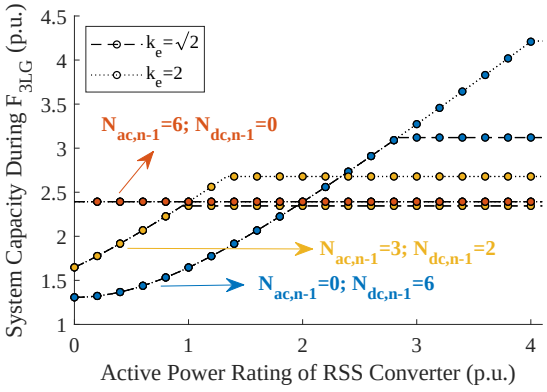


Figure 5.2: RSS apparent power demand capacity during F_{3LG} for different link conductor configurations with varying active power capacity of converter and k_e.

It can be observed that unlike with F_{1LG}, post-fault reconfigurability provides limited opportunity to derate the active power capability of the converter. This is because the the maximum achievable system capacity is significantly limited by the thermal capacity of the remaining healthy conductors. Maximizing the number of conductors operating under dc conditions is important as the dc power delivery capacity for the same conductor area is inherently higher [3].

5.2.3. CAPACITY DURING CONVERTER FAULTS (F_{CONV})

If a substation converter fault (F_{conv}) occurs, the total ac and dc link capacity reduces according to (5.5) and (5.6), respectively. Considering N_{conv} number of converters per substation for the given $P_{r,conv}$, the reduction in system capacity can be estimated using (5.9) and (5.10).

$$k_{cr,n\text{-}1} = \frac{P_{cap,conv,n\text{-}1}}{P_{cap,dc\text{-}cond,n\text{-}1}} = \frac{P_{conv,rated}\left(1 - \frac{1}{N_{conv}}\right)}{P_{cap,dc\text{-}cond,n\text{-}1}} \tag{5.9}$$

$$k_{q,n\text{-}1} = \sqrt{1 - \left(\frac{\sqrt{3}Q_{rated}}{N_{conv}N_{ac,n\text{-}1}V_{LL,rms}I_{cond,rated}}\right)^2} \tag{5.10}$$

The correction factor $k_{q,n\text{-}1}$ is relevant when the F_{conv} is on the RSS side converter, leading to a increase in reactive power flow in the ac link. Figure 5.3 shows the $S_{cap,n\text{-}1}$ that can be met during F_{conv} with respect to N_{conv} for different link configurations and k_e. The active power rating of the converter is considered constant for all configurations considered, corresponding to the maximum achievable capacity with $N_{dc,n\text{-}1} = 6$. This value is $P_{r,conv} = 2.8$ p.u. for $k_e = \sqrt{2}$ and $P_{r,conv} = 4$ p.u. for $k_e = 2$.

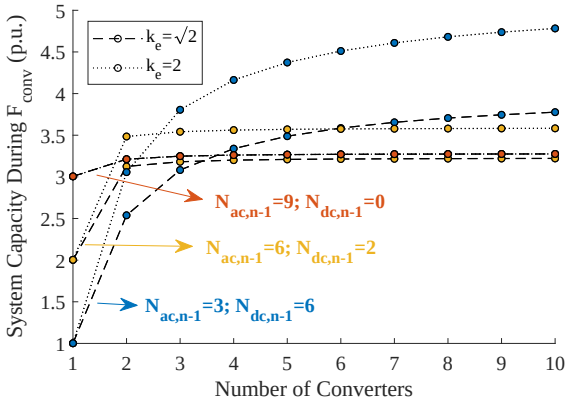


Figure 5.3: RSS apparent power demand capacity during F_{conv} for different link conductor configurations and k_e with respect to number of substation converters with maximum rated active power of the substation.

It can be observed that if $N_{conv} = 1$, no active power can be transferred by the dc link conductors. In the worse case scenario, if F_{conv} is on the RSS side, the entire reactive power flows through the ac link. Therefore, the $S_{cap,n\text{-}1}$ for a given configuration corresponds to the capacity of the $N_{ac,n\text{-}1}$ ac link conductors. With increasing N_{conv}, the active and reactive power support by the dc link during single converter fault improves. It can be observed that the required capacity of 3 p.u. at 0.9 can be met without the necessity of dc to ac reconfiguration with $N_{conv} = 3$ for $k_e = \sqrt{2}$. If the active power rating of the converter is minimized for F_{1LG} according to Figure 5.1, the $S_{cap,n\text{-}1}$ during F_{conv} for different configurations is shown in Figure 5.4 for varying number of converters.

$P_{r,conv}$ for all three configurations is considered equal to 0.7 p.u corresponding to $k_e = \sqrt{2}$. It can be observed that even if higher N_{conv} is chosen, reconfiguration towards

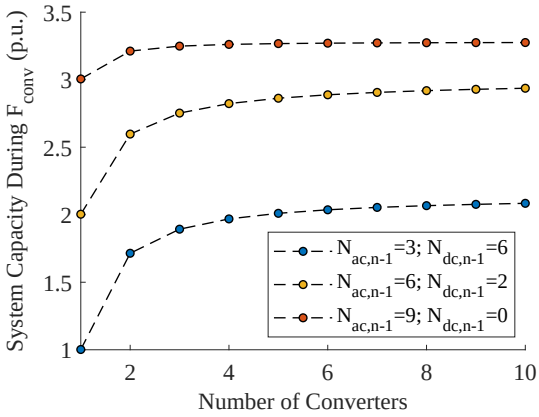


Figure 5.4: RSS apparent power demand capacity during F_{conv} for different link conductor configurations and k_e with respect to number of substation converters with minimum rated active power of the converter for $k_e = \sqrt{2}$.

a system with $N_{ac,n\text{-}1} = 9$ is necessary during any F_{conv}. This is because the converter capacity is such that it cannot fully utilize the available thermally limited capacity of the dc link conductors even with $N_{dc,n\text{-}1} = 2$ and $N_{conv} = 10$.

Therefore, the main conclusion from the contingency analysis performed in this section is that the required RSS apparent power demand capacity of 3 p.u. at pf=0.9 can be met with either with 3x converters with cumulative capacity of 2.8 p.u per substation or 1x converter with a capacity of 0.7 p.u per substation if single-cored link conductors are used. Though the latter is beneficial from installation cost point of view, greater number of reconfigurations are required in case a fault occurs in the system. The subsequent section will highlight that a reduction in converter size can reduce the system efficiency during normal operating conditions.

5.3. LOSS MINIMIZATION DURING NORMAL OPERATION

Both y_{opt} and y_{con} discussed so far are governed by the y_{max} boundary corresponding to $k_{cr} = 1$ (see (3.10),(3.12)). The required RSS and SSS converter rating can be estimated from the maximum expected apparent power demand ($S_{RSS} = S_{RSS,max}$ at rated pf $\cos\theta_R$) described by (3.15) and (3.16), respectively. While it is desirable to operate the system at its optimal efficiency point y_{opt}, selecting a lower k_{cr} can be advantageous in reducing the installation costs corresponding to the converter rating. The immediate trade-off of these competing requirements necessitates the system to operate at sub-optimal efficiency under some operating conditions as illustrated in Figure 5.5. The y_{opt} as a function of S_{RSS} at pf=0.9 with $k_{cr} = 1$ is shown for link length of 5 km and 15 km. The first approximation y_{con} is also highlighted.

The dotted black lines in Figure 5.5 correspond to the y_{max} as a function of S_{RSS} at $\cos\theta = 0.9$ for different Δk_{cr}. The highlighted values of Δk_{cr} as a percentage of $k_{cr,min}$

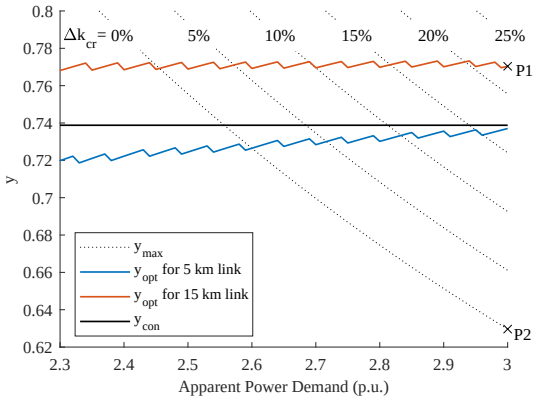


Figure 5.5: Constraint of converter rating on the operating active power ratio between ac and dc link.

5

can be used to determine the system k_{cr} using (5.11).

$$k_{cr} = k_{cr,min} + \Delta k_{cr} \tag{5.11}$$

As an example, the highlighted point 'P1' in Figure 5.5 represents the optimal efficiency operation for $S_{RSS} = 3$ p.u at $\cos\theta = 0.9$ for a 15 km link. If the substation converters are de-rated so that $k_{cr} = k_{cr,min}$ with $\Delta k_{cr} = 0$ %, the link system is forced to operate at point 'P2'. It can be seen from Figure 4.13 that by operating the system at point P2 instead of optimal efficiency point P1, additional losses of about ≈1 % are incurred. On the other hand, to avoid these losses at the specific operating point, the converter has to be overrated corresponding to 20-25 % higher Δk_{cr}. Figure 5.5 shows that with decreasing link length (see for 5 km; blue line) and increasing Δk_{cr}, operating range, for which the described trade-off is valid, shortens. It can be inferred that for a given link length and Δk_{cr}, the intersection between the demand dependent plot-lines for y_{opt} and y_{max} define the maximum apparent power demand for which the system can operate at the highest efficiency that is achievable unconstrained by the converter rating. The payback associated with the additional incurred losses, cumulative for $S_{RSS} > S_{max,opt}$ over the given RSS load profile, in relation to the investment costs for the installed converter rating governs the appropriate choice. Consequently, the selection of k_{cr} is case specific as shall be explored further in Section 5.4.

5.4. ECONOMIC VIABILITY OF CONVERTER DOWNSIZING

Section 5.2 shows that the same system capacity can be maintained using reconfigurations even though the dc link converters are significantly downsized. Section 5.3 highlights that as a consequence of such a converter downsizing, the system cannot operate at its optimal efficiency (y_{opt}) during normal operation. In this section, the economics of this trade-off will be explored with a case-study using examples of two adapted RSS demand profiles.

5.4.1. SYSTEM LOSSES AND CONVERTER DOWNSIZING

Figure 5.6 shows the effect of this trade-off on system losses with varying S_{RSS} at pf=0.9 for different link lengths (l) and Δk_{cr}. The system parameters used for the computations are listed in Table 5.1, with $N_{\text{ori}} = 9$ single-cored link conductors operating with $k_{\text{e}} = \sqrt{2}$.

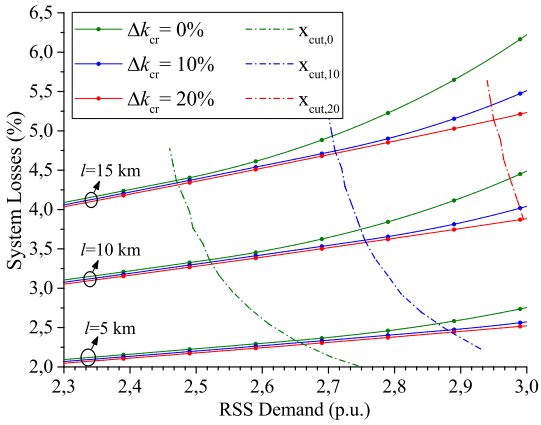


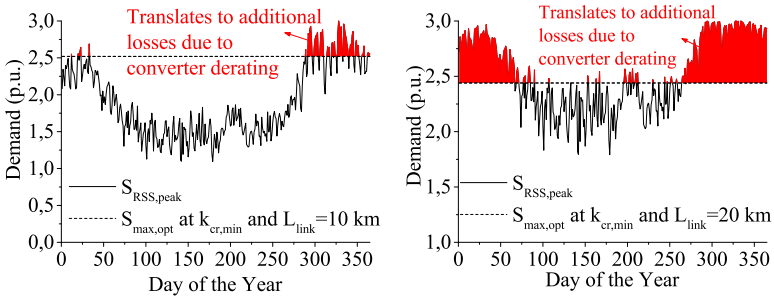
Figure 5.6: System losses with varying converter rating and RSS power demand at pf=0.9 for different link lengths.

The highlighted cutlines $x_{\text{cut,0}}$, $x_{\text{cut,10}}$ and $x_{\text{cut,20}}$ show the variation in $P_{\text{L,sys}}$ with link length dependent $S_{\text{max,opt}}$ for $\Delta k_{\text{cr}} = 0\,\%$, $10\,\%$ and $20\,\%$ respectively. Here, $S_{\text{max,opt}}$ is defined as the maximum S_{RSS} that can be met at the optimal efficiency point. It is obtained at the intersection between the link length dependent y_{opt} and the Δk_{cr} dependent y_{max} from Figure 5.5. For a given link length, it can be observed from Figure 5.6 that $P_{\text{L,sys}}$ can significantly decrease for $S_{\text{RSS}} > S_{\text{max,opt}}$ as Δk_{cr} increases from $0\,\%$ to $20\,\%$, particularly for relatively longer l. On the other hand, for power demands below $S_{\text{max,opt}}$, $P_{\text{L,sys}}$ slightly increase with Δk_{cr}.

5.4.2. CASE-STUDIES

The energy savings over the operational life of the system is a function of the RSS load profile shown in Figure 5.7 for two test cases.

The described load profiles are adapted from annual power demand data in [1] such that the maximum peak in power demand is consistent with the test system parameters listed in Table 5.1. In Case I (Figure 5.7a), the shaded area in red corresponds to the period where daily peak demand is greater than $S_{\text{max,opt}}$ at $k_{\text{cr,min}} = 0.607$ and $l = 10\,\text{km}$. Considering the RSS power demand with per hour resolution, 20.6 MWh/year savings can be achieved if the the converter rating is $10\,\%$ higher. However, this has an additional incurred cost of 0.16 M€ at 50 €/kVA as per the cost trends mentioned in [4], giving exceedingly high payback time if energy costs are assumed at 0.1 €/kWh. Therefore, it is economically viable to downsize the converter to $k_{\text{cr,min}}$ for Case I (that is, $P_{\text{r,conv}} = 1.7\,\text{p.u}$), even though it operates at sub-optimal efficiency for RSS power de-



(a) Case I. (b) Case II.

Figure 5.7: Daily peak RSS power demand and maximum optimal power limit for a parallel ac-dc link system with converter derating factor of $k_{cr} = k_{cr,min}$.

mand in the shaded red region of Fig, 5.7a. For Case II load profile shown in Figure 5.7bis modified such that the average power demand of the system is 1.71 p.u.compared to 1.16 p.u. in Case I, while the maximum peak demand is maintain constant at 3 p.u. corresponding to the system capacity during (n-1) contingencies. The highlighted red area represents RSS power demand which cannot be met at optimal efficiency for $l = 20$ km if the converter is downsized to $k_{cr,min} = 0.607$. A 10 % increase in converter size can offer energy savings of 239.4 MWh/year, with a payback of 6.6 years. Therefore in this case, the optimal converter size depends on its cost trade-off with higher power losses associated with sub-optimal system operation due to converter downsizing, even though the power delivery capacity during (n-1) contingencies can be maintained constant. Figure 5.8 shows the payback for different Δk_{cr} with varying link lengths.

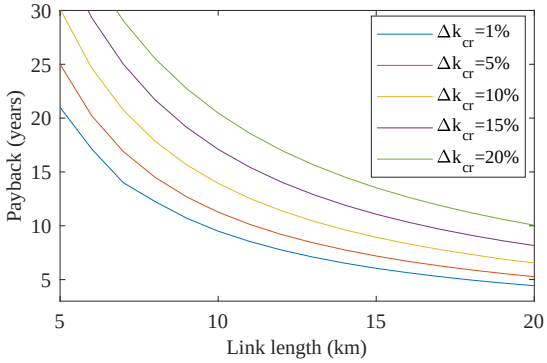
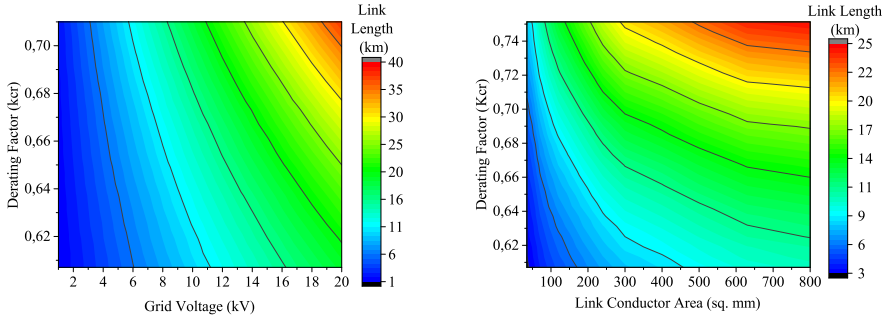


Figure 5.8: Payback due to variation in derating factor and link length for Case II.

5.4.3. SENSITIVITY ANALYSIS WITH GRID VOLTAGE AND CONDUCTOR AREA

The $v_{ll,rms}$ and A_{con} of the system is varied while keeping the p.u. values of the Case II load profile (Figure 5.7b) constant. Therefore, the base power associated with the pre-

sented results of this section varies in accordance to (3.9). The heat-map of minimum link length for which a payback of 10 year can be achieved for varying converter derating factor as a function of $v_{ll,rms}$ and A_{con} is shown in Figure 5.9a and 5.9b, respectively.



(a) Variation with grid voltage.

(b) Variation with link conductor area.

Figure 5.9: Link lengths giving 10 year payback for converter downsizing in Case II.

The contour lines show the variation of optimal converter de-rating factor with $v_{ll,rms}$ and A_{con} for given link length. It can be observed that greater converter downsizing is possible with increasing $V_{\text{LL,rms}}$, A_{con} and decreasing link length, because these parameter tendencies decrease the efficiency of dc link operation in relation to the ac link. If k_{e} is increased from $\sqrt{2}$ to adjust k_{opt} and/or to increase the capacity of the system further, the losses in the dc link conductors will decrease for the given power. It is inferred that an increase in k_{e} will limit the economic viability of converter downsizing from optimal efficiency perspective.

5.5. CONCLUSIONS

DC link dimensioning involves interrelated trade-offs between dc voltage, substation converter rating and optimal dc active power share. Post-fault reconfigurability between ac and dc link converters is shown to offer potential for converter downsizing by as much as 75 %, for example, in the range of 0.7-2.8 p.u. active power while maintaining the same power transfer capacity during different (n-1) contingencies. However, this de-rating is detrimental to system efficiency during normal operation. Furthermore, a lower converter rating will result in increased number of post-fault reconfigurations.

Using a case-study with adapted substation load profile data, the trade-off between operating efficiency and converter sizing is quantified to suggest a economically viable solution. Sensitivity analysis is performed for different grid voltage, link length and conductor area to determine the appropriate converter rating giving a 10-year payback time.

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6

MESHING RADIAL AC NETWORKS USING DC INTERLINKS

This chapter is based on:
Aditya Shekhar, Thiago Batista Soeiro, Laura Ramírez-Elizondo and Pavol Bauer, "Weakly Meshing the Radial Distribution Networks with Power Electronic Based Flexible DC Interlinks," *IEEE International Conference on DC Microgrids (ICDCM),* 2019.

Flexible dc interlinks can be used for compact and efficient active power redirection by creating a meshed structure in existing radial distribution network. It is shown that with optimal location and sizing of a back-to-back voltage sourced converter based point-to-point dc link connecting two ac buses of the test 33-bus radial distribution system, 10-15 % network loss minimization can be achieved. This possibility can be advantageous in efficiently redirecting active power flows in urban and semi -urban areas because intermittent distributed grid resources (such as photovoltaics and wind farms) and energy intensive loads (such as ultra fast charging stations for electric vehicles) are resulting in local pockets of excess generation and demand. The impact of distributed generation and high powered loads on placement of dc interlink is numerically quantified to suggest that both capacity and efficiency enhancement can be achieved in the distribution grid. It is envisioned that this method of integrating dc power transmission can be the first realistic step towards realizing a multi-terminal dc medium voltage distribution evolving out of the existing infrastructure.

The concept of installing a dc interlink for weakly meshing the radial medium voltage ac distribution network is shown in Figure 6.1. The dc interlink is a Modular Multilevel Converter (MMC) based dc link system with Back-to-Back Voltage Source Converters (B2B-VSC) interconnecting two chosen buses of a given radial medium voltage (MV) ac distribution network.

Historically, Unified Power Flow Controllers (UPFC) have been used to optimize power flows in the ac distribution grids without topology changes and generation reschedul-

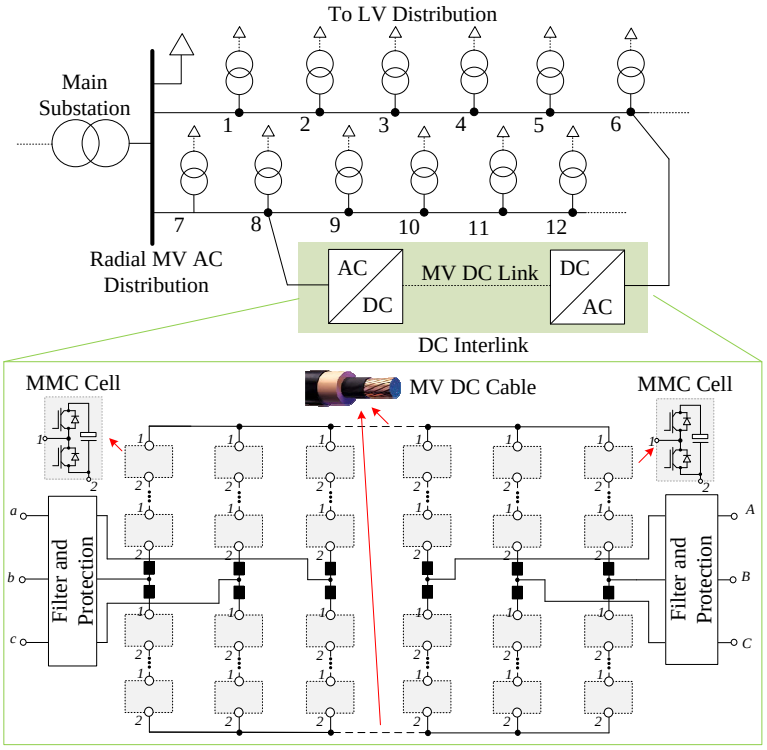


Figure 6.1: Illustration of a DC interlink for power redirection in a radial ac distribution network. Observe that the proposed point to point MVDC link forms a meshed grid.

ing [1]. While various functionalities of the UPFC such as flexible power control and voltage support in the development of power electronic based Flexible AC Transmission Systems (FACTS) have been explored [2–6], the role of delivering the actual active power from source bus to the load buses is still fulfilled by the ac line infrastructure. For example, if the losses in such a power flow controller device is neglected, the net active power exchanged with the system by the shared dc link is zero [6]. Therefore, the main difference between traditionally used UPFC and the proposed scheme in this chapter is that network power flow control is achieved using active power redirection via the dc interlinks that weakly mesh the existing radial ac grid.

There are studies that discuss the viability of high power application of dc interlink with B2B-VSC between two buses of the distribution network [7–12]. Unlike UPFC, which achieves power and voltage regulation by changing the ac line impedance, the dc interlinks can redirect the active power from one bus in the system to another as shown in Figure 6.1. Though the benefit of creating loops in the ac networks to balance power, regulate voltage and lower losses is known [9, 13, 14], doing so with a B2B-VSC based point-to-point dc link can offer a controlled asynchronous meshing solution, while addressing the protection issues known to arise in either looped ac or dc systems. At the

same time, the B2B-VSC can be used to provide grid supporting ancillary services like reactive power injection and power quality conditioning.

The focus of this chapter is to explore the possibility of increasing the capacity of a 33-bus radial distribution network by compact and efficient active power redirection using dc interlink, while reducing the distribution losses by weakly meshing it. Specifically, different considerations such as the power rating and the appropriate buses for placement of dc interlink so as to minimize the network losses is discussed in Section 6.1. The impact of installing distributed generation and high power load is described in Section 6.2 and Section 6.3 respectively. Finally, the conclusions and possible future research directions are presented in Section 6.5.

6.1. PLACEMENT OF DC INTERLINK IN A 33-BUS RADIAL DISTRIBUTION GRID

6.1.1. POINT CURRENT ABSTRACTION

In order to gain conceptual insight on the dc interlink placement problem, the point current abstraction of a lateral section in a radial distribution network is shown in Figure 6.2.

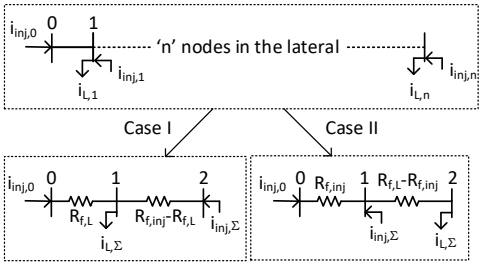


Figure 6.2: Point load and injected current abstraction for a n-node lateral in a radial distribution network.

A section of 'n' number of lateral nodes is shown to have load current ($i_{L,n}$) and injected current ($i_{inj,n}$). These currents can be a function of active and reactive loads, distributed generation sources and controlled storage elements in the network. Assuming that all branches have conductors with uniform cross-sectional area, the resistance between the n^{th} node and the source node (n = 0) represents the distance. Two possible cases of a 2-branch abstraction of this n-bus lateral is shown in Figure 6.2. The n node currents are abstracted as point current attached through a fictitious resistance with the source bus representing the resistive losses in the lateral. $R_{f,L}$ and $R_{f,inj}$ are the fictitious resistances describing the location of point load current $i_{L,\Sigma}$ and point injected current $i_{inj,\Sigma}$ from the source bus, respectively. Based on the distribution of $i_{L,n}$ and $i_{inj,n}$ at the n nodes of the lateral, the value of the fictitious resistances will vary. For example, if the current drawn from the n_{th} bus is increased, the value of $R_{f,L}$ will increase. Similarly, if instead, the injected current at the 1^{st} node of the system is increased, $R_{f,inj}$ decreases. The resistive losses $P_{loss,I}$ (Case I) and $P_{loss,II}$ (Case II) in the lateral are given by (6.1)

and (6.2) respectively.

$$P_{\text{loss,I}} = R_{\text{f,L}} \left(i_{\text{L},\Sigma} - i_{\text{inj},\Sigma}\right)^2 + \left(R_{\text{f,inj}} - R_{\text{f,L}}\right) i_{\text{inj},\Sigma}^2 \tag{6.1}$$

$$P_{\text{loss,II}} = R_{\text{f,inj}} \left(i_{\text{inj},\Sigma} - i_{\text{L},\Sigma}\right)^2 + \left(R_{\text{f,L}} - R_{\text{f,inj}}\right) i_{\text{L},\Sigma}^2 \tag{6.2}$$

It can be inferred that for a given injected source bus current $i_{\text{inj},0}$, the distribution losses can be minimized with the objective functions $\min(|R_{\text{f,L}} - R_{\text{f,inj}}|)$ and $\min(|i_{\text{inj},\Sigma} - i_{\text{L},\Sigma}|)$. This concept forms the basis for optimal placement and sizing of distributed generation sources [15–17] and storage [18–24]. However, in these cases the topology of distribution system is maintained. Some benefit of power redirection with network reconfiguration is shown in [25], but the radial structure is maintained during operation. Power redirection by weakly meshing the radial ac networks using dc interlinks can provide similar distribution loss minimization functionality. Additionally, routing active power through the dc link itself can provide enhancement in system power capacity at higher efficiency [26]. The challenge, however, is that the dc interlink influences nodes in two sections of the radial network 1) at the node where the power is drawn 2) at the node where the power is injected. The sizing and location optimization, should therefore optimize for objectives in both these sections, all the while maximizing the smallest parallel ac-dc path between the source to load in such a architecture. These aspects will be explored more in detail in the subsequent sections.

6

6.1.2. SYSTEM DESCRIPTION

In Figure 6.3, a 33-bus radial test system is depicted. At each numbered bus, the drawn active and reactive powers P_{L} and Q_{L} are specified [27]. A point to point dc link is to be placed between two selected buses of the system to redirect the active power and minimize the distribution losses. The sending end node of the dc link is 'B_s' and the receiving end is 'B_r'. For example, if the dc link is installed to transmit active power from bus 7 to 33, then B_s=7 and B_s=33.

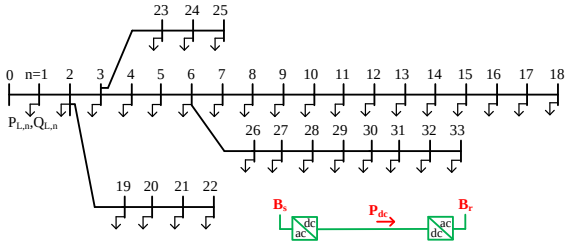


Figure 6.3: DC Link Placement in a radial 33-bus medium voltage distribution system.

Even though the back to back ac-dc converter link system is capable of bidirectional active power flow, the computations are made by considering that the dc link active power (P_{dc}) is a load drawn from the bus connected to B_s and injected at the bus connected to B_r. In this way the loop created by the installed dc link can be broken and the system can be converted to the original radial topology, similar to the power flow methodology described for weakly meshed distribution networks in [14]. In order to

simplify the power flow computation, the branch active and reactive powers (P_{br} and Q_{br} respectively) are computed from a single backward sweep step of the method described in [27].

The performance of the network can be further improved by ancillary services such as voltage regulation and reactive power injection using the grid connected MMCs employed for the dc interlink. However, only the influence of the active power redirection functionality is studied.

6.1.3. DISTRIBUTION NETWORK LOSSES

The loss in the dc link ($P_{\text{dc,loss}}$) is independently calculated from P_{dc} from (6.3).

$$P_{\text{dc,loss}} = 2\left(\left(\frac{\sqrt{3}P_{\text{dc}}}{2k_{\text{e}}V_{\text{LL,rms}}}\right)^2 r_{\text{dc}} + (1-\eta_{\text{conv}})P_{\text{dc}}\right) \tag{6.3}$$

Here, the factor k_{e} relates the dc link voltage V_{d} to the rated rms line to line ac voltage $V_{\text{LL,rms}}$ by the relation given in (6.4).

$$V_{\text{d}} = \frac{2k_{\text{e}}}{\sqrt{3}}V_{\text{LL,rms}} \tag{6.4}$$

The value of k_{e} is selected as $\sqrt{2}$ based on the considered assumptions on insulation performance requirements according to the discussion in [26, 28]. It should be noted that the installed dc link can be designed to have a higher k_{e}, which can reduce the conduction losses in the link conductors for a given power, but has higher insulation and converter costs as a trade-off. The dc link operates with back to back modular multilevel converters, each having efficiency η_{conv} as per the design considerations in [29]. This value is assumed constant at 99.33 % for delivering the considered P_{dc}. Assuming that the dc link conductors are of equal cross-section and physically routed alongside the original system conductors, their resistance r_{dc} is taken equivalent to the total resistance of the ac conductors of the branches between B_{s} and B_{r}. For example, if the dc link connects bus 7 to bus 26, the dc conductors are installed in parallel with branches between nodes 6-7 and 6-26, having resistance equivalent to the sum of ac conductor resistances of these branches. This is a simplification and in practice the installed dc interlink can be optimized for conductor type and resistance based on the power capacity and link length. The total system losses ($P_{\text{sys,loss}}$) are given by (6.5).

$$P_{\text{sys,loss}} = P_{\text{dc,loss}} + \sum_{n=1}^{33}\left(\frac{P_{\text{br,n}}^2 + Q_{\text{br,n}}^2}{V_{\text{LL,rms}}^2}\right) r_{\text{br,n}} \tag{6.5}$$

Where, $r_{\text{br,n}}$ is the resistance of the n^{th} branch in the system. It is assumed that the thermal capacity of all the branches is above the operating powers considered in this work. Further, if uniform cross-sectional area is assumed for all branch conductors, $r_{\text{br,n}}$ can be viewed to signify distance of a given bus from the source node. The voltage at all the system buses is assumed constant at its rated value of $V_{\text{LL,rms}}$ =12.66 kV. If the system losses for $P_{\text{dc}} = 0$ are $P_{\text{sys,loss,0}}$, the percentage change in losses ΔP_{loss} due to active power

redirection by dc link is given by (6.6).

$$\Delta P_{\text{loss}} = \left(\frac{P_{\text{sys,loss}} - P_{\text{sys,loss,0}}}{P_{\text{sys,loss,0}}} \right) * 100 \tag{6.6}$$

Figure 6.4 shows the variation in ΔP_{loss} with varying B_{r} for different P_{dc}. The bus from which the dc link originates is fixed at the bus $B_{\text{s}} = 0$, at which the primary energy source of the system is located. In this section, all other buses of the currently considered distribution system are load buses without any distributed generation.

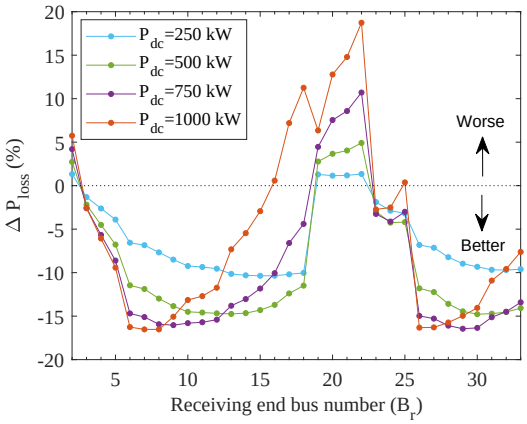


Figure 6.4: Change in distribution losses with dc interlink at varying B_{r} for different P_{dc} (B_{s} at bus 0).

It can be observed that the maximum achievable reduction in losses depends on the P_{dc}. For example, when P_{dc} is increased from 250 kW to 750 kW, energy savings increase from 10 % to over 15 %. As a trade-off, the installed capacity and therefore, the cost of the dc link converter increases. However, when P_{dc} is further increased from 750 kW to 1 MW, the maximum achievable energy savings slightly reduce, indicating that there is an optimum value of $P_{\text{dc,opt}}$.

The location of the bus at which the maximum energy savings can be achieved is influenced by two competing considerations. On one hand, the path between bus B_{s} and B_{r} has a dc link in parallel with ac link. For a given system operation, it is shown in [30] that the achievable efficiency of a parallel ac-dc link improves with increasing link length as compared to a completely ac system and receiving end load power. From this perspective, it can be inferred that B_{r} should be further away from B_{s} (in terms of length translated to the conductor resistance of the parallel path) and the dc link power should be high. On the other hand, in a radial distribution system such as the one considered, an increasing distance from the source bus also implies decreasing power delivered downline from B_{r}. This can lead to reverse branch power flows in the system if the P_{dc} is too high, as can be observed in Figure 6.5. Therefore, the optimum location ($B_{\text{r,opt}}$) varies with P_{dc}.

The observed tendency of higher energy savings with increasing P_{dc} at B_{r} located relatively closer to the source must be generically verified assuming uniformly distanced

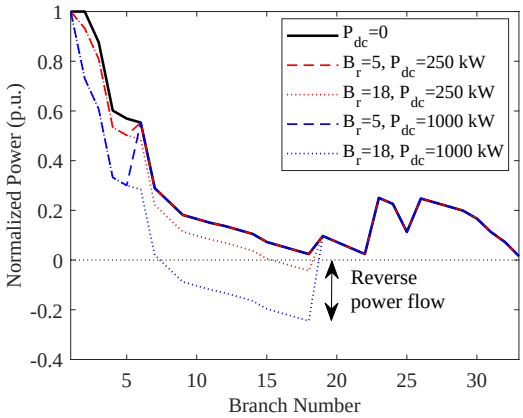
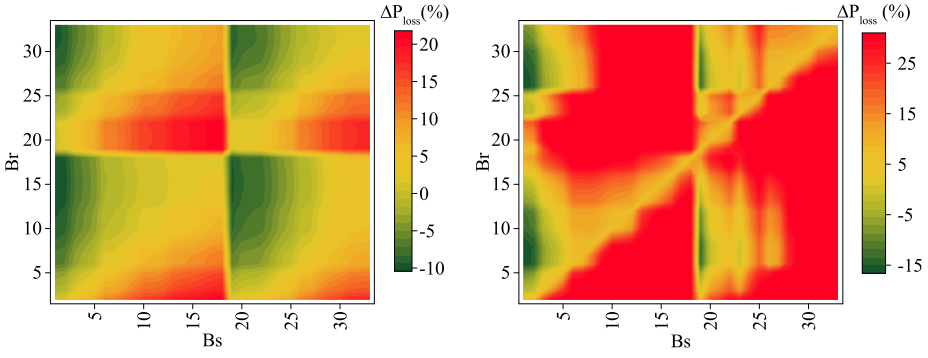


Figure 6.5: Normalized branch power flows with different B_r and P_{dc}.

buses with uniform load distribution. The economic viability of the obtained optimal design choices ($P_{dc,opt}$, $B_{r,opt}$) as a function of achievable efficiency gains will depend on the converter costs related to the dc link capacity and the link conductor installation costs related to the location of $B_{r,opt}$. These aspects are not the focus of this thesis.

Figure 6.6 shows the heatmap of ΔP_{loss} if both B_s and B_r are varied for two different dc link power capacities.



(a) (b)

Figure 6.6: Change in distribution losses with dc interlink at varying B_r and B_s for (a) P_{dc}=250 kW (b) P_{dc}=1 MW.

The green regions are those locations where the dc interlink based power redirection lead to energy savings while red regions indicate increase in losses. From Figure 6.6a and Figure 6.6b it can be inferred that though higher efficiency can be achieved with higher P_{dc}, the boundaries within which an improvement in efficiency is achievable shrinks. For example, efficiency improvements can be observed in Figure 6.6a for B_r=16 for a range of B_s between 0-4 and 19-22. However, in Figure 6.6b, a 1 MW power redirection

results in an increase in losses at these locations. With lower P_{dc}, the efficiency boundaries expand, though there is some decrease in achievable efficiency. This insight is important as the active power redirection may not be the sole objective of placing such a dc interlink. The B2B-MMCs connected at B_s and B_r can simultaneously be used to provide grid supporting ancillary services such as reactive power injection, voltage support, harmonic elimination, among others [31–36]. The optimal bus location in consideration to these objectives can compete with the need for compact and efficient active power redirection in the network. This study does not delve into the multi-objective optimization problem for dc interlink placement in radial distribution networks, however, it should be noted that greater flexibility in choosing B_s and B_r can offer some advantages in this regard.

6.2. IMPACT OF DISTRIBUTED GENERATION

In the preceding section, a single source was assumed to be located at bus 0. In such a configuration, the possible location of B_s that offers energy savings with active power redirection is typically close to this source (see Figure 6.6). It is plausible that in case of a radial grid employing Distributed Generation (DG) resources, the optimum location of B_s is close to or at lightly loaded laterals connected to these DG buses. Furthermore, the location of B_r will shift away from these regions. The impact of injecting DG power P_{dg}=1 MW at different buses (B_{dg}) on the ΔP_{loss} with varying B_s and B_r for a 250 kW dc interlink is shown in Figure 6.7.

From Figure 6.7a, it can be observed that the energy savings are significantly reduced for B_r in the range of 6-18 as compared to Figure 6.6a. For example, the maximum achievable energy savings reduce from over 10 % to about 2 % for B_r=15. Further, Figure 6.7b shows that the optimal B_s in terms of efficiency shifts to bus 20. Figure 6.7a-Figure 6.7d in contrast to Figure 6.6a suggest that a DG source installed at any bus (B_{dg}) can improve the energy savings due to active power redirection using dc interlink with proximity to B_s while worsen it for proximity to B_r.

The optimal sizing and location of DGs can, therefore, be a complementary consideration to optimal placement of dc interlinks in radial networks. Further, considering that many DG technologies (for example, wind and photovoltaics) have an intermediary dc stage, the potential for synergistic integration of DG, storage and dc interlink is an interesting research dimension to this optimization problem. The concept can be extended to look into the aspects related to highly efficient utility interfacing power electronic converters connecting low voltage dc microgrids and high powered dc loads [37–40].

6.3. IMPACT OF INSTALLING HIGH POWER LOAD

The results from Section 6.1 and Section 6.2 suggest that the preferred location for B_r is typically at buses with heavy down-line loading furthest away from the nearest cluster of energy generating units. Energy intensive loads like ultra-fast charging station of Electric Vehicles (EV) can create local pockets in the distribution grids where compact and efficient active power redirection would be critical [41–43]. Figure 6.8 shows the impact of installing such a high power load with power P_{ev}=1 MW at different buses (B_{ev}) on ΔP_{loss} for varying B_s and B_r.

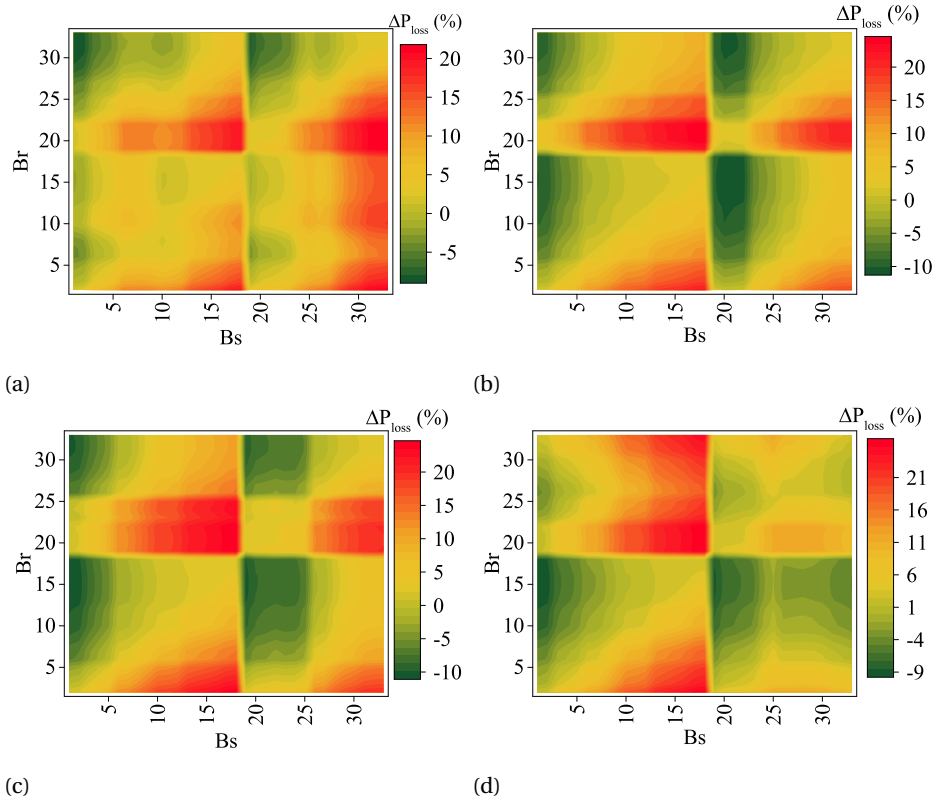


Figure 6.7: Change in distribution losses with 250 kW dc interlink at varying B_r and B_s for P_{dg}=1 MW with B_{dg} at (a) Bus 10 (b) Bus 20 (c) Bus 25 (d) Bus 33.

Figure 6.8a-Figure 6.8d in contrast to Figure 6.6a suggest that a high power load installed at any bus (B_{ev}) can improve the energy savings due to active power redirection using dc interlink with proximity to B_r while worsen it for proximity to B_s.

6.4. LOAD BALANCING AND AVAILABILITY

Conventional ac distribution grids use feeder reconfigurations for service restoration and load balancing [44–48]. For example, the role of big data to help relieve the line overloads by changing status of sectionalizing and tie switches is explored in [48]. In these studies, the radial network structure imposes an important constraint during the problem formulation. In this section, we want to argue that the greater interconnectivity achieved with proposed dc interlink installation can help achieve the goals of load balancing with higher availability without necessarily reconfiguring the system. Consider the modified 33-bus distribution network shown in Figure 6.9.

A DG source of 1 MW is installed at bus 20 and a 1 MW electric vehicle charging station is installed at bus 33. The normalized branch power flows during different operating

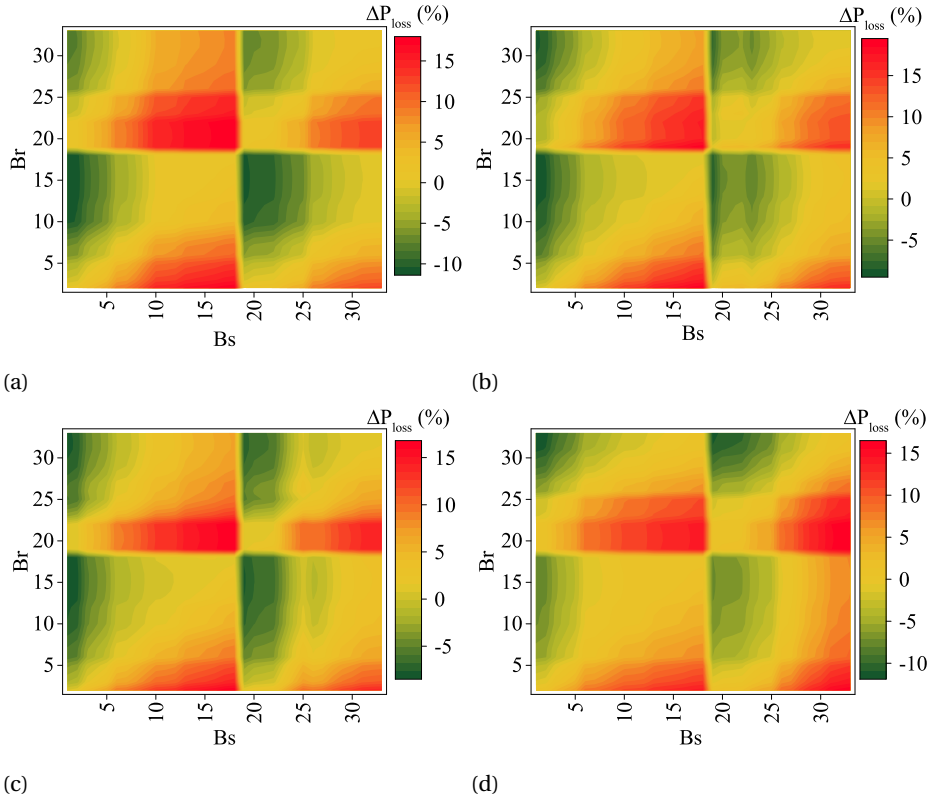


Figure 6.8: Change in distribution losses with 250 kW dc interlink at varying B_r and B_s for P_{ev}=1 MW with B_{ev} at (a) Bus 10 (b) Bus 20 (c) Bus 25 (d) Bus 33.

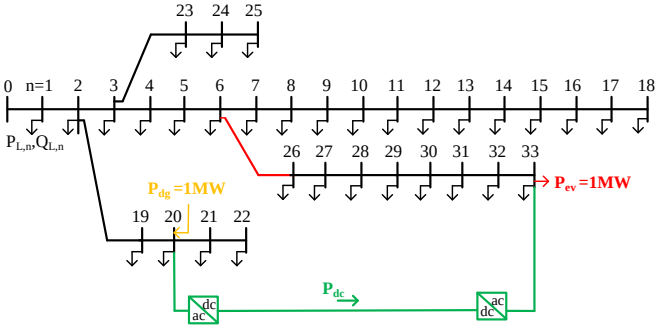


Figure 6.9: Modified 33-bus radial distribution system meshed using a dc interlink with $B_s = 20$ and $B_r = 33$.

conditions is shown in Figure 6.10. P_{dc} is 0 MW in Case I, 0.25 MW in Case II and 1 MW in Case III. The original power flow corresponds to the operation with P_{dg}, P_{ev} and P_{dc} all equal to zero.

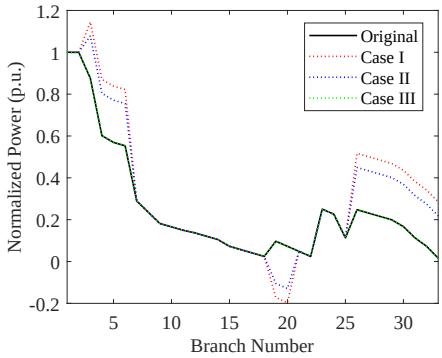


Figure 6.10: Load balancing using dc interlink to prevent overloads due to DG and EV.

It can be observed that the power flow in Case I as compared to original increases by about 50 % in branches between bus 4 to 6, while more than 100 % in branches between bus 26 to 33. Depending on the capacity of these lines, the potential overload can be avoided by increasing the P_{dc}. However, the competing interest of maximizing the system efficiency as described in Section 6.1, Section 6.2 and Section 6.3 can influence the sizing and location of the dc interlink. If varying generation/load profile is considered, the economic considerations may pose important constraint on the capacity of the installed dc link.

Consider that the branch (highlighted in red in Figure 6.9) between bus 6-26 is isolated due to a short circuit fault. For the original radial 33-bus network, a normally open tie-line is needed for service restoration to the section between buses 26-33 [44]. It can be seen that the availability of the proposed system is higher due to weak meshing achieved with the dc interlink. Therefore, since the B2B-VSC based interconnection can provide bi-directional power flow, the proper placement of B_{s} and B_{r} can aid in the service restoration goals for the distribution networks.

6.5. CONCLUSIONS AND FUTURE WORK

It is shown that a back-to-back voltage source converter based dc interlink can be used for compact and efficient active power redirection by weakly meshing the radial distribution networks. The dependence of achievable energy savings on the dc link capacity (P_{dc}) and the location of start and end points (B_{s} and B_{r} respectively) was explored. The results indicate that each has an optimal value ($P_{\text{dc,opt}}$, $B_{\text{s,opt}}$ and $B_{\text{r,opt}}$) that can have competing requirements. For example an optimization for $P_{\text{dc,opt}}$ can increase the achievable energy savings but lead to more rigid boundaries for $B_{\text{s,opt}}$ and $B_{\text{r,opt}}$. It was highlighted that if the employed back to back converters of the dc interlink are also utilized to simultaneously provide grid supporting ancillary services, the placement of dc interlink becomes a multi-objective optimization problem, wherein relaxing the boundaries for optimal active power redirection could be beneficial.

The impact of distributed generation resources and high power loads like EV installed at select buses on the dc interlink based active power redirection was studied. The

results numerically support the intuitive understanding that $B_{s,opt}$ should have proximity to regions of excess generation while $B_{r,opt}$ should have proximity to regions of excess loading while maximizing the smallest possible length of parallel ac-dc path from source to load in the network. While only fixed loading was studied in this thesis, future work can include economic advantage of installing the dc interlink depending on the varying load profile at all the buses of the distribution grid.

As future work, it is important to generalize the concept of weakly meshing the radial networks with a newly installed dc interlink. The trade-off for the achievable reduction in distribution losses with costs associated with converter capacity and link length should be explored. Even though this thesis assumes that the capacity of all the branches in the original radial system is adequate with considered penetration of DG and EV, the benefit of dc based active power redirection in preventing overloads in the system can be an important consideration. The concurrent function of dc link converters for reactive power injection, voltage support and improvement of power quality in the grid should be considered.

This chapter focused on the improvement of the distribution system efficiency with dc power redirection between local pockets of surplus generation and excess demand in the grid. The dc interlink is, therefore, assumed to be integrated using ac/dc modular multilevel converters to the optimal ac bus pertaining to these locations. However, the emerging components that cause these local pockets in the network, for example photovoltaics, wind farms and electric vehicles charging stations, may have a dc based distribution architecture before connecting to the main grid. In such cases, the concept can be extended to use the dc interlink to integrate such green energy resources along with energy storage solutions. The design of the converter topology for such applications with medium to medium and medium to low voltage dc thus becomes important and may offer additional benefits.

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7

CONCLUSIONS AND FUTURE WORK

The objective of this thesis was to restructure the existing medium voltage ac distribution grids by introducing dc technologies. This objective was met and the following conclusions can be made specific to the research questions and challenges highlighted in the introduction section of this thesis:

How much capacity enhancement can be achieved by refurbishing existing ac link infrastructure to operate under dc conditions?

The computed results prove that a capacity enhancement of at-least 50–60 % can be achieved with dc operation based on the considered assumptions for different configurations. The factors include increase in imposed dc voltage as compared to ac (41 %), better voltage regulation (2-5 %), current rating enhancement (0-3 %) and reactive power support by the converters at the receiving end of the dc link (10-15 %). Therefore, there is an interesting potential of enhancing the operating dc voltage for similar or superior insulation performance as compared to ac over the cable lifetime. In Appendix A, ac and dc insulation performance is empirically studied to show that the repetition rate of partial discharges in the prepared cable samples are much lower with dc. Based on this partial discharge behaviour as an insulation performance indicator, the dc voltage enhancement factor is conservatively assumed to be $\sqrt{2}$ times the rated r.m.s ac voltage. While it is possible to chose a higher dc voltage enhancement factor, particularly for overhead lines, it is suggested that the inception voltage should be considered as an indicator of insulation performance.

What are the advantages of developing a flexible architecture with ac-dc distribution link reconfigurability?

An important challenge identified is the reduction in power delivery capacity during failure of a single system component. It was shown that even with refurbished dc operation, it is not possible to guarantee a 50 % enhancement in power delivery capacity

over the original ac system during (n-1) contingencies. A parallel ac-dc reconfigurable link architecture is proposed to improve the infrastructure utilization during different (n-1) contingencies to suggest that a post-fault system capacity of 50-100 % is achievable. For example, ac bypass can be used during substation converter fault to improve link conductor utilization, and thus increase the power delivery capacity during such contingencies.

The various trade-offs associated with reconfigurability are discussed, such as efficiency, availability, cost, reliability and operational complexity. For example, it is highlighted that the dc link converter capacity can be downsized by approximately 66 % for achieving the same system capacity, thus reducing installation cost. However, this can increase the number of necessary reconfigurations during (n-1) contingencies, thus influencing the operational complexity. At the same time, converter downsizing can be detrimental to the operating efficiency during normal operation. The main advantages of developing a flexible architecture are therefore: enhanced system capacity during (n-1) contingencies, potential converter downsizing and relatively higher operating efficiency.

What is the design criteria for ac/dc converter used in grid connected medium voltage high power applications?

A detailed design of a half-bridge IGBT submodule based modular multilevel converter is presented in Appendix B for medium voltage high power grid connected applications. Five main degrees of freedom are identified: switch blocking voltage, submodule capacitance, modulation technique, arm inductance and reliability factors. It is numerically shown that there is an optimal number of submodules for a given dc link voltage. As an example, a 17 kV, 10 MVA dc link with back to back MMC based system integrated to a 10 kV grid is used. The comprehensive design considerations indicate that a MMC with 3 mH arm inductance and 9x half-bridge submodules of 3.3 kV IGBT switches operating with a switching frequency of 353 Hz can comply with required harmonic performance at relatively higher efficiency as compared to IGBTs of either higher (4.5 kV, 6.5 kV) or lower (1.2 kV, 1.7 kV) switch ratings. Note that higher switch rating would correspondingly result in lower number of submodules (7,5), while lower switch rating will result in higher number of submodules (17, 25) for a given dc link voltage. The optimized load dependent converter efficiency curve is derived to vary between 99.2-99 4 % for 10-100 % of the full load.

In which configuration should the distribution link architecture be operated during healthy system conditions?

It is shown that the proposed parallel ac-dc reconfigurable link architecture can be operated under different configurations during normal conditions. A sensitivity analysis is performed for different operating power demand, power factor, ac grid voltage, converter efficiency, link length and conductor area to prove that parallel ac-dc operation can be more efficient as compared to either completely ac or dc operation within defined boundaries. Based on the quantified results, it is possible to determine the boundaries

for which it is the most economically viable to refurbish the existing ac system and operate as parallel ac-dc links compared to other available solutions of equivalent capacity enhancement. For example, a payback time of 10 years is achievable for the added dc link converter cost even for short link lengths of 10-20 km for power transfer of few tens of MVA in a 10 kV grid if parallel ac-dc link is used.

By how much can the substation converter be derated while maintaining the required system capacity during different (n-1) contingencies?

For the same system capacity, it is shown that there is potential of reducing the installed substation converter size by almost 75 %. This increases the number of dc to ac reconfigurations in case a fault occurs in the link system, thus increasing the operational complexity. However, a more pertinent challenge is that of sub-optimal efficiency of the system during normal operation if the converter is downsized. For example, it is quantified for case-specific load profiles and system parameters that downsizing the converter by 5-10 % can give a 10 year payback on installation cost savings only for link lengths greater than 10-15 km. The de-rating potential becomes less economically viable with increasing ac grid voltage and link conductor area.

What are the control challenges involved in the dynamic operation of parallel ac-dc distribution links?

It is shown through simulations and experiments that it is possible to operate the back to back converter based dc link in parallel with ac link with active power steering capability. The two main converter control challenges are to (i) mitigate the common mode currents in the system (ii) steer the active power at optimal efficiency while supporting the full reactive power at receiving end. The results indicate that a path exists for the circulation of zero sequence currents between the three lines of the ac link and common dc link which is mitigated using the corresponding feedback output ac current controller. It is shown that the active power shared between the ac and dc link can be controlled depending on the operating conditions to improve the system efficiency. An algorithm is developed to determine this dynamically varying optimal efficiency point and implemented in simulation model and demonstrated using an experimental set-up for the parallel ac-dc link.

Where can the dc interlink be placed in the radial distribution grids and what is its proper sizing for effective active power redirection?

Using a test 33-bus radial ac distribution network, it is shown that weak meshing with dc interlink can reduce the geographical power mismatch by placing the sending end node closer to regions of excess generation while receiving end node closer to higher downstream power loading. It is shown that load balancing can prevent 50-100 % current overloads in the branches of the network, proportional to the dc link power capacity. For different dc power capacities between 250-1000 kW, the distribution efficiency is shown to improve as much as 15-20 % depending to the selected placement node.

Some interesting future research directions are as follows:

7.1. DYNAMIC DC LINK VOLTAGE

It is known that the use of modular multilevel converter in a back-to-back dc link system decouples the dc link voltage from the voltage ripple imposed on the submodule components such as capacitors and IGBT switches to some extent. Therefore, it is possible to dynamically increase the dc link voltage based on the operating conditions of the system without increasing the voltage seen by the submodules. Such a control strategy can dynamically improve the distribution link system efficiency and capacity under specific operating conditions.

For dynamic improvement of system efficiency, the main challenge is to determine the operating boundaries wherein this concept can be employed and realize the algorithm to achieve the specified objective. From capacity enhancement point of view however, it must be determined whether the potential gains are achievable as and when required. In this regard, the limitation of operating conditions on the ability to dynamically enhance the dc link voltage could prove to be a bottleneck.

7.2. ONLINE RECONFIGRATIONS

This thesis explores the potential of post-fault reconfigurability in maximizing the system power capacity during (n-1) contingencies. While the same system can be operated in different configurations during healthy conditions, the optimal configuration is fixed based on the highest cumulative efficiency that can be achieved based on the demand profile and operating parameters. This necessitates online reconfiguration during healthy operating conditions without power interruption.

During such healthy operating conditions, the power steering capability of the dc link converters can be used to achieve zero-current online reconfigurations to maximize the operating efficiency with varying power demand profile. Further, the concept can be applied to achieve dc link assisted zero-current bus transfers in substations. The main challenge is to investigate the potential savings achieved in trade-off with operational complexity of such a system. Further, in order to implement the online reconfiguration, it maybe necessary to over-dimension the dc link components, thus increasing installation costs. Finally, the operational/control challenges of transitioning from one configuration to another must be investigated. Nevertheless, such a functionally is possible to realize in the proposed system and has some interesting research potential.

7.3. UNIVERSAL DC GRIDS

It is evident that power redirection with embedded dc interlinks will find increasing application in medium voltage ac distribution. The solutions proposed in this thesis are synergistic steps towards future universal dc grids. While the existing ac infrastructure will be essential to determine the policy decisions in this field at present, a flexible medium voltage dc backbone can emerge within this framework as a business case for network reinforcement.

The concept can be extended with multi-terminal dc substructure that can seamlessly integrate other dc-based network structures such as wind farms, low voltage microgrids, electric vehicle charging stations and traction networks. In this context, the principles of utility-interfacing elements, power electronic converter design and control as well as system protection may be governed by the evolutionary path of dc distribution technologies alongside the medium voltage ac grid infrastructure, as suggested in Figure 1.2(a)-(d).

A

CABLE INSULATION PERFORMANCE UNDER AC AND DC CONDITIONS

This section is based on: Shekhar, A.; Feng, X.; Gattozzi, A.; Hebner, R.; Wardell, D.; Strank, S.; Rodrigo-Mor, A.; Ramírez-Elizondo, L.; Bauer, P. "Impact of DC Voltage Enhancement on Partial Discharges in Medium Voltage Cables—An Empirical Study with Defects at Semicon-Dielectric Interface " *Energies* 2017, 10, 1968.

It was shown in Chapter 2 that the capacity enhancement with refurbished dc is mainly due to the possibility of imposing higher cable operating voltage as compared to ac. It is relevant to explore a definitive proof of this assumption and its impact on cable insulation life. The object of this Appendix is to develop empirical understanding of the comparative differences between partial discharge (PD) behaviour of cable insulation under dc and ac operating conditions. While some correlations are drawn between the observed PDs and the expected insulation performance, it is important to consider that this is just one of the many interrelated factors that ultimately govern the life of the cable insulation. The discussion specifically focuses on voids at semicon-dielectric interfaces.

A.1. PARTIAL DISCHARGES

Solid insulation systems typically consist of dielectric materials of sufficiently high breakdown strengths bridging the gap between the high and low voltage electrodes. Their function is to provide mechanical support to the electrodes while withstanding electric and thermal stresses for long durations of time, sometimes on the order of tens of years as is the case with underground cable systems. Tiny voids present within the dielectric, as well as at electrode–insulation interface have much lower breakdown strengths, leading to partial discharges (PD) within these voids [1]. The detrimental effect of PDs resulting in material degradation due to modification in its chemical composition and its eventual complete breakdown has been discussed in [2]. In [3], it is mentioned that the rate of deterioration is expected to be greater for voids adjacent to the electrode, as

compared to those completely enclosed within the dielectric. Therefore, this study concentrates on voids existing at semiconducting (semicon)-dielectric interface.

Two important parameters of PD behavior governing the lifetime performance of the insulation are the repetition rate (R_r), measured in number of discharge pulses per second, and discharge magnitude (D_m), usually measured in pico-Coulomb (pC). Deterioration depends on both R_r and D_m, but in different ways. R_r increases with applied voltage and frequency of operation [4, 5]. The probable role of applied frequency, electric field and R_r in governing the deterioration limit is highlighted in [3, 4]. Defining this limit as a certain discharge magnitude below which deterioration is negligible, these papers specify that it is not a sharp limit. Discussing how the void diameter has little effect on the rate of deterioration after a certain threshold, it was shown how discharges concentrate in deep un-carbonized pits of smaller diameter within the void [3]. Nevertheless, it can be inferred that the role of R_r and D_m in governing the insulation lifetime is intrinsically related. Knowledge on the mechanism of void PD behavior and factors influencing its inception voltage, recurrence and evolution in time is necessary. A good discussion on these aspects is provided in [6–8]. Some aspects relevant in supporting our observations are discussed here.

A.1.1. INITIATION

The two necessary conditions for a PD event are: (1) voltage across the void is greater than its breakdown strength; and (2) availability of free electrons to initiate the discharge.

The first condition determines the partial discharge inception voltage (PDIV), which is defined as the voltage above which discharge occurs, and depends on the kind of gas in the void, its pressure and the void dimensions. The breakdown phenomenon in an insulation void is consistent with the Paschen curve [9]. The PDIV is usually 10–20% lower than the breakdown voltage obtained from the Pashcen's curve [10]. It follows that, under the conditions of this experiment, the PDIV is possibly independent of frequency of applied voltage, a trend we observed under specific conditions in this work. This behavior was also reported previously in [11]. However, the presence of space charges and trapped surface charges may distort the field across the defect and may result in higher observed PDIV, particularly under DC conditions.

The second necessary condition implies that there is a finite time lag t_L after reaching PDIV, but before a discharge is initiated. This time lag in availability of electrons to initiate a discharge is stochastic, resulting in a statistical over-voltage ΔV [12]. It was shown that the D_m is proportional to ΔV [7], which, in turn, affects the residual voltage across the void after the discharge has occurred.

Physical location and dimensions of the void in the insulation system are also important. For example, a flat void perpendicular to the field can have a field enhancement by the dielectric relative permittivity ϵ_r. The location may cause asymmetry in electric field, causing different discharge patterns with positive and negative polarities. However, most importantly, experimental data suggests that the material acting instantaneously as the cathode influences the discharge behavior. For example, the void can be between the inner semicon layer, which is in direct contact with the inner conductor and the insulation that surrounds it, or between the insulation and the outer semicon layer, which is in direct contact with the outer shield (Figure A.1). In the first instance, assum-

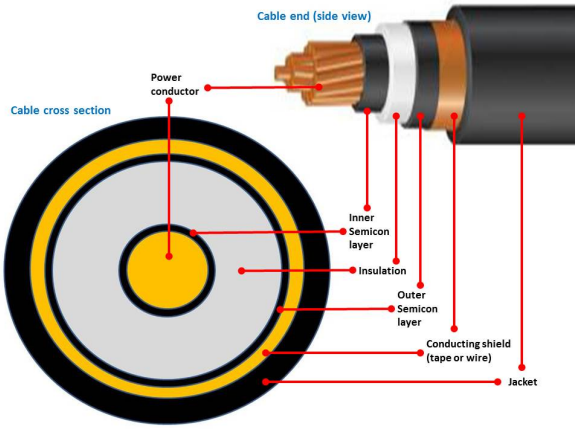


Figure A.1: Cable geometry depicting different layers.

ing that the central conductor is at a positive voltage and the outer shield is grounded, the insulator wall would act as the cathode, whereas, in the second instance, it would be the anode. This role will reverse when the central conductor is at negative polarity. Based on the availability of free electrons, it is discussed in [13] how there is a greater tendency of discharges when the insulation wall acts as the cathode. On the other hand, the discharge magnitude is greater when the semicon wall in the void is negative [10]. However, unlike the observations in [10, 13], the findings of [14] suggested that negative PDs have higher D_m as compared to positive PDs. The defects studied in the same reference were of different type at the termination of the MV High-density Cross-linked Polyethylene (XLPE) cable, but still involved the outer semicon layer and the insulation.

A.1.2. RECURRENCE

The recurrence of PD after a discharge event depends on the recovery time t_R during, which the voltage across the void builds from the residual voltage to its inception and the statistical lag time. The combined effect of these two ultimately determines the PD repetition rate and discharge magnitude. The relationships are illustrated in Equations (A.1) and (A.2):

$$R_r \propto \frac{1}{t_L + t_R}, \tag{A.1}$$

$$D_m \propto \Delta V. \tag{A.2}$$

It is discussed how t_L is inversely proportional to ΔV [15] which is independent of the applied voltage (V_a) [7, 12]. These two relationships are illustrated in Equations (A.3) and (A.4):

$$t_L \propto \frac{1}{\Delta V}, \tag{A.3}$$

$$\Delta V \propto t_L V_a. \tag{A.4}$$

Equation (A.3) tells us that the statistical nature of time lag implies a spread in ΔV and ,therefore, the observable D_m. Physically, Equation (A.3) intuits that a higher ΔV decreases the expected statistical time lag [15], implying that this distribution in D_m will favour lower discharge magnitudes if all the other variables are constant. Equation (A.4) mandates that, with increasing applied voltage, t_L must be decreasing if ΔV is to be constant [12]. This in combination with Equation (A.1) implies that R_r may increase with applied voltage. On the other hand, t_{R4} depends inversely on the charge decay rate $\frac{d\rho}{dt}$, which is a function of void dimensions (area A, diameter d), conductivity (σ) and the average electric field (E_{ave}) [16] as illustrated in Equation (A.5):

$$\frac{d\rho}{dt} = func(\frac{d\sigma E_{ave}}{A}). \tag{A.5}$$

This means that t_R will decrease with increase in d, σ and E_{ave}, while increase with corresponding increase in A. This has implications on t_R according to Equation (A.1).

A.1.3. BREAKDOWN

Erosion and chemical degradation caused by the PDs lead to a gradual deterioration of the dielectric, which, in turn, changes the behavior of the PD [11]. This is important to take into account while empirically analyzing the data. We observed in our preliminary results that fundamental frequency AC quickly altered the test artificial void. Therefore, in order to minimize the detrimental effect of PDs while studying the trends, a frequency range of 0–0.1 Hz and an applied voltage range of 0–20 kV was used.

On the other hand, the way the void evolves as well as its subsequent effect on insulation performance is important to determine insulation life. For an ageing void at the metal–insulation interface, it was observed in Ref. [17] that the PD repetition rate decreases in time, accompanied with higher D_m and increasing PDIV. The same reference shows how trace conductor material from the copper electrode migrates towards the dielectric due to PD activity and ionized air particles. In [18], it is predicted based on the conductivity change due to the migration of metallic material towards the insulation layer that space charges may appear, thus decreasing the electric field under DC conditions. It would be interesting to explore whether the test samples used in this study exhibit the aforementioned behavior and determine some empirical understanding about its trend with the considered operating conditions.

A.1.4. AC VERSES DC

It has been suggested that the PD rate in cable insulation with DC operation is lower than AC under similar conditions [8, 19]. This is because the DC time constant τ determined from the cable insulation parameters governs the PD R_r. It was discussed in Ref. [8] that, unlike the case of commercial 50–60 Hz AC, where the $\frac{dV}{dt}$ influences the repetition rate, τ is orders of magnitude higher than the theoretical value that would give equivalent PD R_r. This relationship is illustrated in Equation (A.6), derivation for which is shown in Ref. [8]:

$$\frac{dV}{dt} = \frac{V}{\tau}. \tag{A.6}$$

Our initial tests on artificially created voids embedded within insulation of Ethylene Propylene Rubber (EPR) and XLPE MV (5–30 kV) cables showed that DC voltage enhancement of at least five times could still give significantly lower PD R_r. The insulation performance over its lifetime also depends on the PDIV. Furthermore, under DC voltage, space charges are able to develop when there is conductivity gradient in the dielectric (due to thermal gradient, electrode migration or carbonization), leading to field distortion and lowering of PD activity if polarity reversal is avoided. A good theoretical discussion on space charges relevant to the conditions of our study is provided in Ref. [18]. A broader perspective on the role of space charges in bringing the insulation to failure is offered in Ref. [20]. Another reason may be that, since steady-state DC electric field is governed by the conductivity of the materials, the field strength in the void is much less than that in dielectric, which may result in less PDs under DC voltage.

A.2. THE EMPIRICAL STUDY

Measured trends at medium voltage levels (0–20 kV) and low frequency (0.01–0.1 Hz) will be analyzed in detail as compared to DC. Change in discharge activity with void evolution will be studied in order to gather understanding on the operational practices under DC that may maintain the same expected insulation performance as in the case of AC from PD point of view.

A.2.1. EXPERIMENTAL SETUP

The schematic of the test setup is shown in Figure A.2. Cable samples of 1.5 m were used and the layers at the termination at both ends were cut in a graded manner to ensure uniformly varying stress. These cable terminations were immersed in transformer oil to minimize partial discharges at these locations [21]. The C-L-3C filter, with C = 2 nF and L = 40 mH arranged in a configuration as shown in Figure A.2, has increasing attenuation greater than −6 dB above 10 kHz, thus filtering noise from the high voltage (HV) supply. The HV inductor of the filter is also completely submerged in the oil.

The high frequency current transformer (HFCT) was used to capture the small signals generated by the PD in the cable dielectric. The connection was such that a positive PD was recorded when the polarity of the inner conductor was positive. All the power equipment was reliably grounded for safe and accurate PD measurement. The data were processed by the IEC 60270 compliant [22] PD Smart system manufactured by Doble (Watertown, Massachusetts, United States of America) with a band-pass of 100–500 kHz and transferred to a computer for visualization. Unless otherwise mentioned, the threshold for PD measurement was set at 10 pC.

A high current DC power supply capable of providing up to 600 A was used to heat the cable sample. Isolators CB1 and CB2 (shown in Figure A.2) were installed to manually disconnect the high current supply during HV tests. Simultaneous operation of a high current and HV supply was avoided as this operation posed safety concerns. Furthermore, the 600 A DC source created significant radiated noise, which obfuscated the measurement from the HFCT. To hold the test sample temperature at the desired value during HV tests, the oil in the tanks at both ends could also be heated up to 80 °C using immersion heating rods. The mathematical basis and experimental validation of this

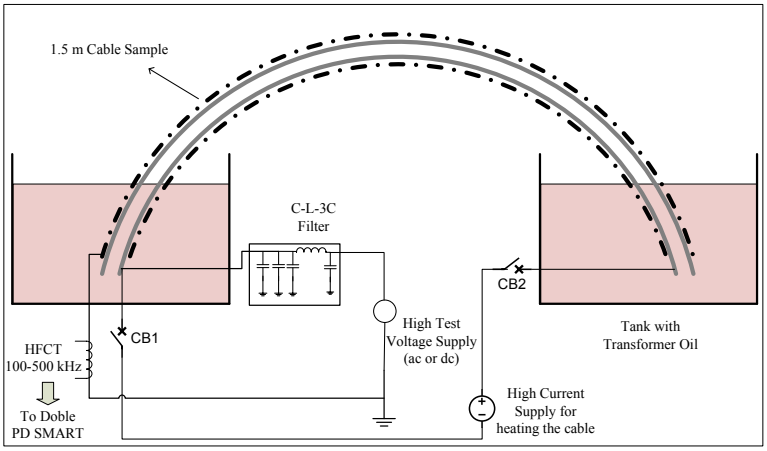


Figure A.2: Schematic of the setup for PD measurements in test cable under AC and DC voltages.

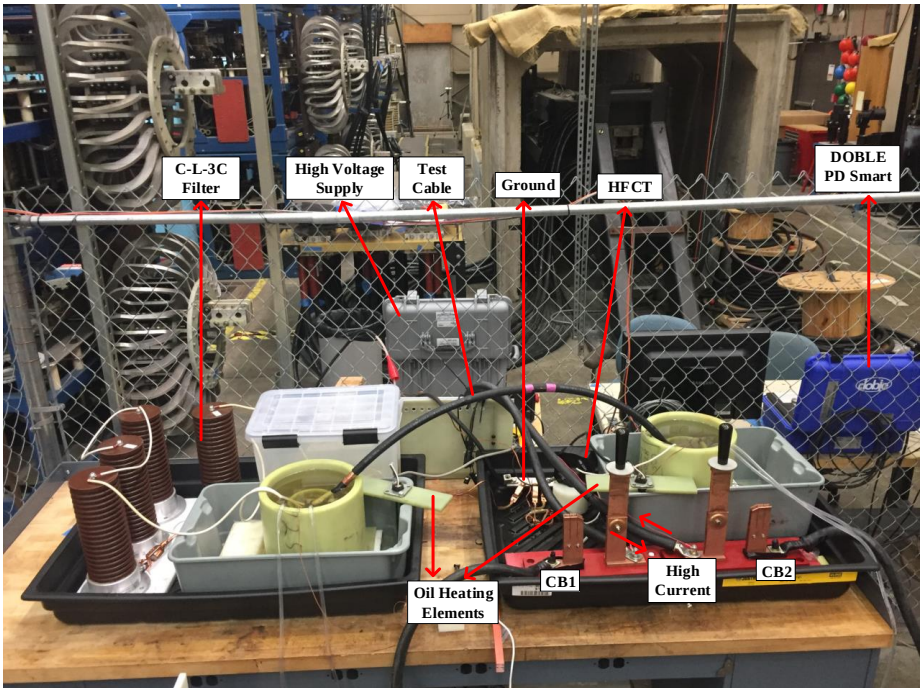


Figure A.3: Experimental set-up for PD measurements in test cables under AC and DC voltages.

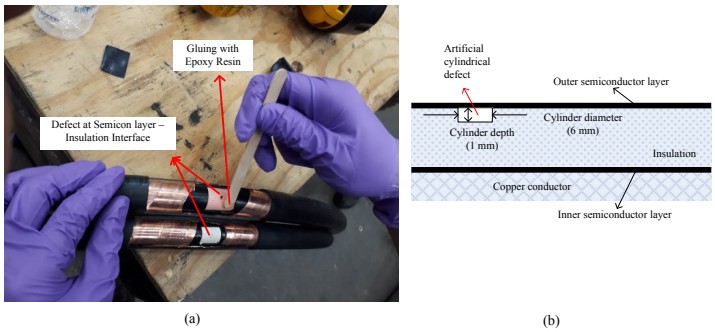


Figure A.4: Preparation of test cables with artificial defects at outer semicon layer and dielectric interface (**a**) snapshot of actual samples; (**b**) side view depicting defect location and dimensions.

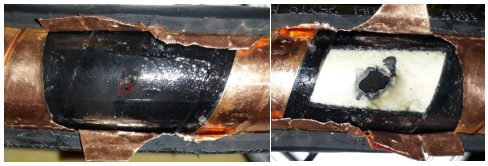
method is presented in [23]. Since the present study only reports data at room temperature, the high current set-up was used only to thermally age the cable and the oil heating apparatus was not used. The physical realization of the experimental setup at the test site is shown in Figure A.3. The setup includes an HV power supply (either AC or DC), a C-L-3C filter, test cable, HFCT, and PD measurement equipment (Doble PD Smart).

A.2.2. CABLE SAMPLES

Figure A.4 shows a snapshot of two test cables being prepared with artificial defects in the insulation at its interface with the outer semicon-layer. The location of the artificial void of 1 mm depth and 6 mm diameter in the cable at the interface of the outer semicon-layer and the insulation is shown. The dimensions of the void were chosen to achieve clear differentiation between PD activity and noise. A good discussion on the PD activity with different void dimensions is provided in Ref. [16]. Note that this insight is offered for artificial voids completely encompassed by the insulation.

The rectangular segments of the outer layer, metallic shield and the semicon layer are carefully removed one by one without damaging the outer surface of the cable insulation. Then, an artificial defect of the desired dimensions can be drilled. The bottom surface of the defect is made to be as smooth as possible. The image shows how the Epoxy resin is applied at the surface around the defects to firmly fix the semicon-layer. Finally, the metallic shield and the outer protective sheath are reattached to obtain the test cable samples. The snapshots of a test cable post breakdown is shown in Figure A.5.

In Figure A.5a, the post breakdown semicon layer segment above the artificial defect is shown. A pinhole developed in this damaged layer is highlighted. After reopening the semicon layer, Figure A.5b shows the carbonized insulation layer. These images provide physical evidence of significant discharge activity at the defect location. The analysis results presented in this chapter are from a different cable sample with identical specifications, void dimensions and preparation procedure.



(a) Post-Breakdown Image (b) Void condition

Figure A.5: Snapshots of the test cable in different stages of the complete breakbown experiment: (**a**) Post-Breakdown Image; (**b**) Void Condition.

Table A.1: PD repetition rate for cable with (a) defect (Negative: $R_{\text{defect,neg}}$, Positive: $R_{\text{defect,pos}}$) (b) no defect (Negative: $R_{\text{no\_defect,neg}}$, Positive: $R_{\text{no\_defect,pos}}$) with different frequencies at 20 kV voltage.

f_a (Hz)	$R_{\text{defect,neg}}$ (s^{-1})	$R_{\text{no\_defect,neg}}$ (s^{-1})	$R_{\text{defect,pos}}$ (s^{-1})	$R_{\text{no\_defect,pos}}$ (s^{-1})
0	-	-	2	<0.005
0.01	1	<0.01	1	<0.01
0.1	11	<0.1	9	<1

A.2.3. NOISE IDENTIFICATION

A healthy undamaged cable was tested under similar conditions in the set-up and no discharge activity was measured in this configuration. This observation, together with the physical evidence of localized post-breakdown at the artificial defect, increased confidence that the measurement results offered in this study are partial discharges in the insulation layer void created at its interface with the semicon layer.

In addition, testing was performed to determine if the process of preparing the artificial void resulted in unintended excessive PD activity. For this purpose, the procedure described by Figure A.4a was followed without creating the artificial void in a separate cable sample of identical specifications. In other words, the semicon layer was removed and re-fixed similar to the test sample without drilling the void. The altered cable was then tested in the same ranges of frequencies and applied voltages. Measurement results for PD repetition rate of defect cable as compared to the one without defect is shown in Table A.1.

It can be observed that, even at the highest test voltage level of 20 kV, the total PD activity is significantly lower in the cable in which no defect is present even though the semicon layer had been previously removed and replaced. Furthermore, the values reported in Table A.1 for the altered cable were predominantly out of phase with the applied voltage, a condition that indicates that the source of the measured PD activity was located outside the cable (this point will be discussed in more detail later). In conclusion, the confidence level that the PD activity measured in the cable with a void defect does indeed result from the void itself is very high.

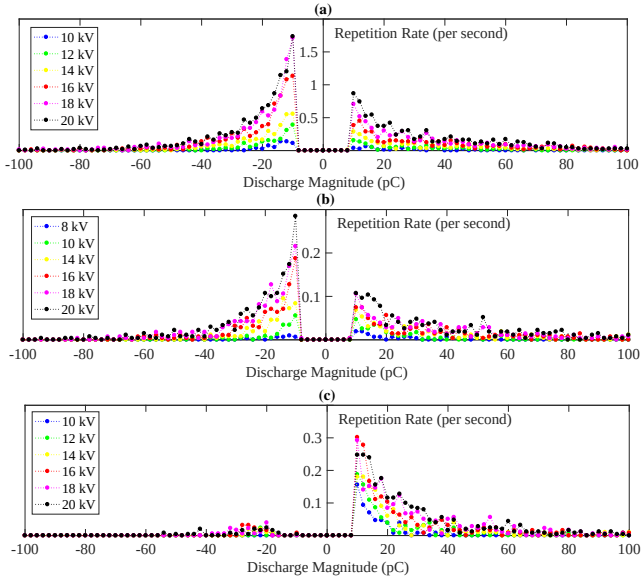


Figure A.6: Voltage dependence of PD discharge magnitude versus repetition rate for (**a**) 0.1 Hz; (**b**) 0.01 Hz; (**c**) DC.

A.3. MEASURED BEHAVIOR

A 5 kV 133 % EPR Insulation copper cable sample was prepared with an artificial void of 6 mm diameter and 1 mm depth at the interface of outer semicon layer and the insulation. The sample was tested for PDs under dc and low frequencies in the range of 0.001-0.1 Hz with voltage levels of 10-20 kV.

Figure A.6 shows the distribution of the PD R_r with respect to D_m for different voltage levels from 10 to 20 kV in steps of 2 kV. The results are shown for DC, as well as 0.01 Hz and 0.1 Hz sine wave. The voltages are stated in terms of their peak for sinusoidal voltages. The experiments are conducted at room temperature (22 °C). All measurements, done on the same day with DC tests last, are listed as 'Test Series 1' in Table A.2. The duration of test and PDIV are reported.

The following trends can be observed:

- Both negative and positive PD R_r have a specific distribution pattern with respect to the D_m, with a maximum ($R_{\max}$) at 10 pC. The distribution is asymmetrical, with negative R_r having higher values for lower D_m as compared to positive R_r. We know that the electric field across the void is asymmetrical due to the relatively large void size and the cylindrical cable geometry [16]. However, a more convincing reasoning for the asymmetry in distribution comes from considering the material in the role of cathode in each case [10, 13]. When the inner conductor is at negative polarity (resulting in measured negative PDs), the EPR insulation wall acts as the cathode, thus exhibiting a higher rate of discharges consistent with observations in [13]. During positive polarity, however, the semicon layer is the

Table A.2: Linear regression results for empirically measured variation in a total repetition rate with applied voltage for different frequencies at room temperature.

			Positive R_{tot}			**Negative R_{tot}**		
f_a (Hz)	**Time** (min)	$V_{i,obs}$ (kV)	m ($kV^{-1}s^{-1}$)	V_{inc} (kV)	R^2	m ($kV^{-1}s^{-1}$)	V_{inc} (kV)	R^2
Test Series 1 (Threshold: 10 pC)								
0	25	7	0.18	7	0.99	-	-	-
0.01	45	8	0.09	7	0.97	0.12	8	0.96
0.1	20	9	0.83	10	0.98	1.05	10	0.98
Test Series 2 (Threshold: 10 pC)								
0.01	25	10	0.06	10	0.96	0.06	10	0.95
0.03	30	12	0.19	12	0.99	0.18	12	0.98
0.05	30	12	0.33	11	0.99	0.34	12	0.996
0.07	30	12	0.44	12	0.98	0.41	11	0.98
Test Series 3 (Post-Thermal Room Temperature, Threshold: 10 pC)								
0	7	-	-	-	-	-	-	-
0.01	30	18	-	-	-	-	-	-
0.05	30	12	0.32	12	0.99	0.3	12	0.99
0.1	30	12	0.48	10	0.99	0.6	11	0.99

cathode, resulting in higher over-voltages, and, therefore, higher discharge magnitudes [10, 12].

- As the applied voltage is increased, the PD R_r increases for both positive and negative sides. Its distribution pattern with respect to discharge magnitude and the position, where $R_{\max}$, occurs does not vary significantly. The theory presented in [7, 12] supports these observations. Furthermore, the charge decay rate increases with average field across the void, and, therefore, the recovery time decreases [16].

- The value of $R_{\max}$ increases with applied voltage, but this trend is not always followed. For instance, as we go higher in voltage from 16 kV DC to 20 kV DC in Figure A.6c, $R_{\max}$ decreases. This behaviour will be further explored in the subsequent section.

- As frequency is increased from 0.01 Hz to 0.1 Hz, the R_r significantly increases. The relationship between $\frac{dV}{dt}$ and repetition rate is explained in [8]. With higher applied frequency, the lag time t_L is expected to decrease. The position at which $R_{\max}$ occurs does not change significantly. With higher frequencies, greater levels of over-voltages (on which the D_m depends) above the PDIV are achievable more quickly. However, with higher over-voltages, the statistical time lag decreases [15].

- There are only positive PDs under DC conditions, which is expected, as there is no polarity reversal. While negligible PDs can be observed in the negative side,

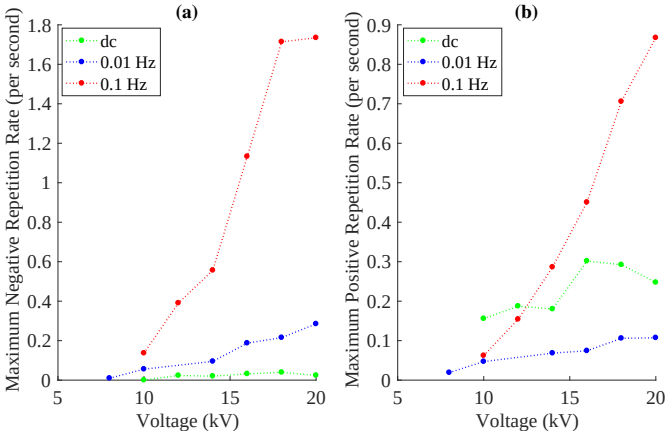


Figure A.7: Voltage dependence of maximum PD repetition rate for (**a**) negative rate; (**b**) positive rate.

for DC, these signals are considered to be caused by processes outside the cable under test, thus essentially extraneous to our experiment and equivalent to noise. The positive R_r under DC voltages is higher than the positive R_r under 0.1 Hz. However, the sum of positive and negative R_r for 0.01 Hz is greater, indicating that the total PD activity in time is slightly greater than DC.

A.3.1. DEPENDENCE ON APPLIED VOLTAGE

Figure A.7a,b describe the trend of negative and positive R_{max} with respect to applied voltage.

Results are shown for DC, 0.01 Hz and 0.1 Hz. The sinusoidal voltages are represented by their peak magnitudes. The positive R_{max} for DC is higher than that for 0.01 Hz and also for that of 0.1 Hz in the lower voltage range. The negative R_{max} is nearly double the positive for both 0.01 Hz and 0.1 Hz. A direct dependence with increasing sinusoidal voltages was observed, but this is not the case with DC, where the trend is less predictable. To derive a deeper understanding, R_{tot}, the total repetition rate cumulative over all discharge magnitudes, is shown in Figure A.8 with respect to applied voltage.

The following inferences can be drawn:

- Under similar applied voltage and frequency conditions, the positive and negative R_{tot} have comparable values. This observation from Figure A.8, in combination with Figure A.6, possibly implies that the discharges are occurring in the same void with a specific R_r distribution in D_m.

- The difference in positive and negative R_{max} in Figure A.7, in combination with the above inference, indicates that a greater number of higher D_m positive PDs are present as compared to negative PDs. For negative PDs, a higher number of lower D_m are observed. This behavior is in agreement with the observations of the role of cathode material described in [10, 13], leading to asymmetry in the PD activity during positive and negative voltage cycles.

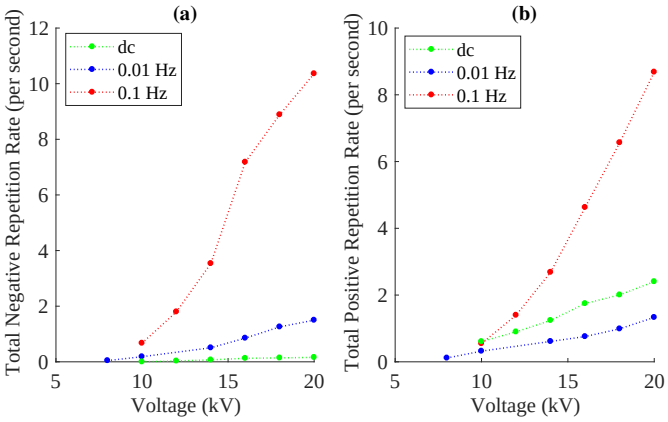


Figure A.8: Voltage dependence of total PD repetition rate for (**a**) negative rate; (**b**) positive rate.

- The total PD activity with 0.01 Hz (sum of positive and negative R_{tot}) is slightly higher than the PD activity under DC conditions.

- While the observed trend in R_{max} under DC conditions was less predictable, R_{tot} consistently increases with voltage.

- The frequency dependent increase in R_{tot} is more significant for voltages higher than the PDIV. While PD repetition rate is an important factor governing the insulation life [4], inception voltage is also relevant. The inception voltage showed weak dependence on applied frequency in the conditions tested in this study, in agreement with similar observations made in [11]. It is important to know whether inception voltage of PD activity is above the nominal operating value if the DC voltage enhancement factor, as compared to AC, is to be determined based on the insulation performance over its lifetime.

After the series of tests discussed above (Series 1), two more series of tests were conducted. These test series comprised of experiments conducted on the cable sample to investigate the gradual deterioration due to PD activity. Each series was conducted in one day. The discussion up to this point was based on 'Test Series 1'. 'Test Series 2' was conducted as a verification of the first series and to understand the frequency trend in more detail. Finally, 'Test Series 3' was conducted after thermal exposure of the sample to understand the PD behavior after void evolution. Applied voltage was varied from 0–20 kV in steps of 2 kV for each test and the rate distribution over discharge magnitudes was measured for 5 min.

In order to quantify the observed empirical trends numerically, the linear regression tool was used. It should be noted that the parameters presented herein are used solely to study the comparative trends with applied voltages and frequency specific to this study and may change with different operating conditions and void evolution. The theoretical model attempting to derive the underlying physics is discussed in [24]. To correlate the

parameters of the trend-line equation with physical quantities, Equation (A.7) was used:

$$R_{\text{tot}}(V_{a,peak}, f_a) = \underbrace{\frac{dR_{\text{tot}}(V_{a,peak}, f_a)}{dV_{a,peak}}}_{m}(V_{a,peak} - V_{inc}(f_a)), \tag{A.7}$$

where $R_{\text{tot}}(V_{a,peak}, f_a)$ is the total PD repetition rate (either positive or negative) in s^{-1} dependent on the applied voltage and frequency and $V_{a,peak}$ is the peak of the applied voltage in kV. The slope m is the variation of $R_{\text{tot}}(V_{a,peak}, f_a)$ with respect to the applied voltage with units $kV^{-1}\,s^{-1}$. The constant term $V_{inc}(f_a)$ is the estimated PDIV in kV. The slope m and constant term $V_{inc}(f_a)$ are the parameters estimated using regression analysis to fit the linear equation defined in Equation (A.7) onto the measured variation in total PD repetition rate with peak applied voltage at different frequencies. The results of the regression analysis are presented in Table A.2. The parameters were obtained from the curve fitting tool of MATLAB, including the coefficient of determination (R^2) indicating the goodness of fit. Time for which the experiment was conducted and the observed PDIV $V_{i,obs}$ are also tabulated.

The high R^2 value, greater than 0.95 and sometimes as high as 0.99, indicates acceptable confidence on the goodness of fit of the proposed linear relationship between total PD repetition rate with applied peak voltage. The slope m for DC is double that for positive R_{tot} in case of 0.01 Hz, mathematically supporting the empirical inference that the time for which HV is imposed governs the PD behavior. At this extremely low frequency, the influence of $\frac{dV}{dt}$ on PDs is not observable. Furthermore, sinusoidal polarity reversal every 50 s does not significantly affect the discharge behavior in terms of R_{tot} and its variation with peak applied voltage as compared to DC. The PDIV is also similar.

In order to gain statistical significance of the linearity of R_{tot} with applied voltages that curve fitting indicates, further experiments were conducted for PD activity at 0.03 Hz, 0.05 Hz and 0.07 Hz and different voltage levels. These are listed under 'Test Series 2' in Table A.2. The experiments suggest a strong linear relationship between R_{tot}-$V_{a,peak}$ at all measured frequencies, within the voltage range studied. These results also offered insight on the frequency dependence of PD activity, which is discussed in the subsequent section.

A.3.2. DEPENDENCE ON APPLIED FREQUENCY

Figure A.9 shows that the slope of the voltage variation in both positive and negative R_{tot} non-linearly increases as the applied frequency is increased.

This increase showcases the greater influence of $\frac{dV}{dt}$ than the PDIV on the PD activity. The nonlinearity is understandable, considering that the time for which the voltage is higher than inception, as well as the $\frac{dV}{dt}$ imposed during such voltages, are nonlinear functions of frequency. It cannot be inferred from these results, however, whether the effect of $\frac{dV}{dt}$ itself on the PD activity is nonlinear. Addressing this question is relevant from a transient behavior standpoint but is beyond the scope of this research.

Furthermore, evidence suggests that the void gradually evolves, leading to higher PDIV and lower PD repetition rates with higher discharge magnitudes. Such observations and their possible reasons were also reported in [17]. Since tests for 0.03 Hz, 0.05 Hz

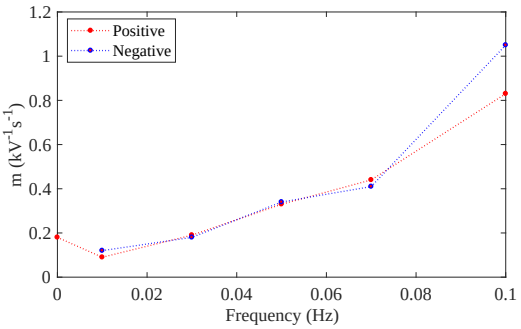


Figure A.9: Frequency dependence of the voltage variation in R_{tot}.

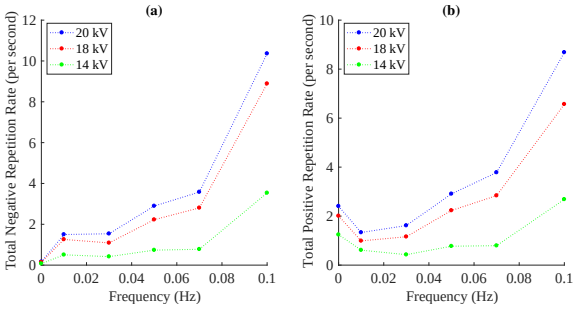


Figure A.10: Frequency dependence of total PD repetition rate for (**a**) negative rate; (**b**) positive rate.

and 0.07 Hz were conducted later, the artificial void had already been subjected to considerable aging under HV. The evidence of void evolution is revisited in the subsequent section. In Figure A.10, the results for frequency variation in R_{tot} for select applied voltages are shown.

The nonlinear dependency of PD activity on frequency is visible in this figure. The slope is similar for positive and negative PD activity. From the results, there is no clear trend indicating that one is discernibly higher than another at this voltage and frequency range.

A.3.3. TEMPERATURE AND VOID EVOLUTION

Low frequency was used to study the trends in PD activity while minimizing their deleterious effect on AC voltages. It is, however, also interesting to see how the void evolves in time. After imposing high temperature (HT) (measured 60 °C at the sheath), post-thermal, room temperature tests were conducted. These are presented as 'Test Series 3' in Table A.2. The repetition rate distribution with discharge magnitude for different voltages in 'Test Series 3' is shown for 0.1 Hz, 0.01 Hz and DC in Figure A.11.

It can be observed that the repetition rate is significantly lower as compared to those presented in Figure A.6. It was observed that the PDIV had significantly increased as compared to 'Test Series 1'. For 0.1 Hz and 0.05 Hz, the inception was observed at 12

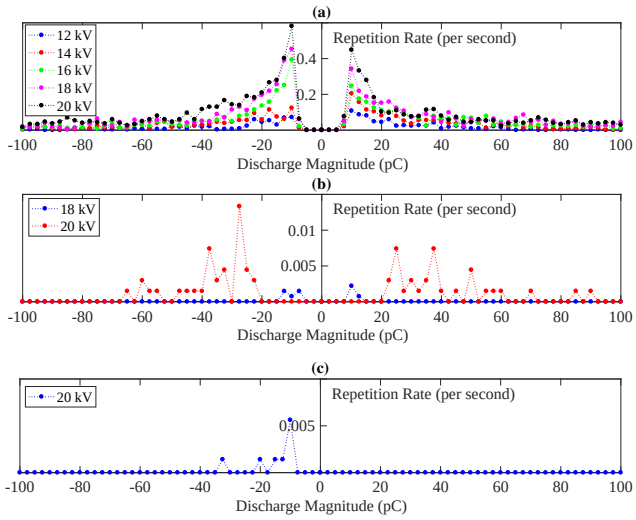


Figure A.11: PD discharge magnitude versus repetition rate for different voltages in 'Test Series 3' (**a**) 0.1 Hz; (**b**) 0.01 Hz; (**c**) DC.

kV, while, for 0.01 Hz, it was at 18 kV. For DC, no positive PD was observed even at the maximum imposed voltage of 20 kV. It is possible that the space charges and conductivity change are playing a role as predicted in [17, 18]. Observations suggest that ageing resulted in EPR conductivity larger than the unaged case in the vicinity of the void since it is much easier to induce space charge at the same voltage level. Since 20 kV is applied on a 5 kV cable (2.9 mm insulation thickness), considerable space charges can develop [25]. Specific to the voids at the semicon-dielectric interface of the cable, evolution of voids are accompanied by metal migration towards the dielectric material. This erosion changes the conductivity of the void walls, leading to change in PD behavior. For example, the copper content at the EPR surface was 0.2% [17]. The similar phenomenon could be expected with the semicon-interface.

Figure A.12 shows the distribution of PD R_r with respect to D_m for 0.1 Hz sinusoidal AC from Test Series 1 and 3 measurements.

It can be observed that the total PD rate is significantly lower with ageing. There is, however, an increase in the PDs at higher discharge magnitudes. This is consistent with the observations in [17].

A.4. CONCLUSIONS

The PD activity in the artificial void at the semicon-dielectric interface has been observed to linearly increase with applied voltage in the range 10–20 kV for 0.01–0.1 Hz frequencies as well as DC. The maximum of repetition rate distribution over the discharge magnitude occurred at 10 pC and did not shift position with varying applied voltage and frequency. The increase in repetition rate with frequency appeared nonlinear, but this

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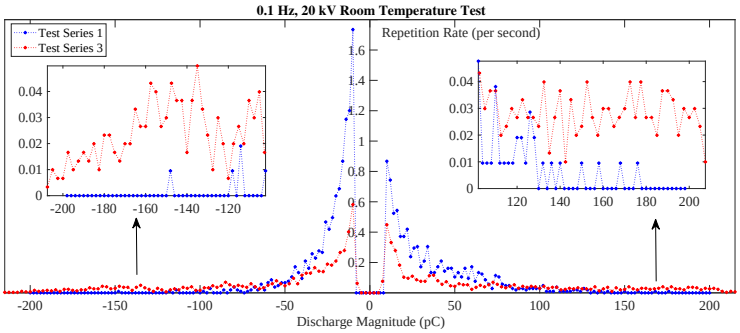

Figure A.12: Evidence of void evolution for 0.1 Hz AC sinusoidal wave at 20 kV.

could be due to the void evolution.

The density distribution of PD repetition rate was asymmetrical, with negative PDs having a higher maximum of repetition rate distribution over the discharge magnitude, but positive PDs having higher repetition rate at higher discharge magnitudes as compared to the negative PDs. Similar evidence was reported in [10, 13]. The total repetition rates, however, were found to be comparable.

In the initial tests, the total PD repetition rate at DC voltage was lower as compared to AC sinusoidal voltage. However, it was observed to be comparable to 0.01 Hz AC voltage results. The PDIV did not exhibit observable frequency dependence. Therefore, it is important to know whether the PDIV is above the nominal operating value if the DC voltage enhancement factor as compared to AC is to be determined based on the insulation performance over its lifetime.

The sample (5 kV Cu 2/0 EPR cable) showed signs of gradual deterioration over time even when subject to low frequencies. The PD activity had lower repetition rate and higher PDIV after a high temperature exposure at 60 °C, while, at the same time, higher discharge magnitudes were observed. No PD activity was seen until 20 kV with DC voltage at room temperature after the void had evolved. This could possibly indicate the change in void surface conductivity and effect of space charges predicted in [18] due to the phenomenon of semiconductor layer material migration consistent with the observations of [17].

The main observation is that the PD rate under DC voltage is significantly lower than that under 0.1 Hz and 60 Hz AC sinusoidal voltages with the same peak value. The intentional void did evolve over time, especially under the thermal exposure. The preliminary observation and test experience on medium voltage cables with intentional defects suggest that DC voltage helps to reduce cable weight/volume as compared with 50/60 Hz voltages.

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B

Design of Medium Voltage Modular Multilevel Converter

B.1. Modular Multilevel Converters

The concept of modular multilevel converters (MMC) was first introduced by Alesina in [1]. The potential of this concept was extended for a wide power range in [2]. Based on the extensive research on various aspects pertaining to MMC operation, it has particularly become the preferred topology for high voltage direct current (HVDC) applications [3].

In HVDC applications, the number of levels are adequately high corresponding to the commercial range of insulated gate bipolar transitors (IGBT) blocking voltage ratings. In such cases, minimizing the number of levels while selecting the switch with highest voltage rating and ensuring efficient performance at the expected operating power range could be more important. For example, in [4], it is shown that for HVDC applications, higher switch ratings are preferred with increasing operating power level based on cost-efficiency trade-offs. With decreasing grid voltage, lower blocking voltages may become preferable for cascaded full bridge cells [5].

Section B.2 discusses the degrees of freedom available during the design of a half bridge MMC. Their inter-dependencies are highlighted and the important trade-offs are identified. This appendix offers a non-comprehensive analysis on some less explored associations and emphasizes that a careful selection of blocking voltage class is particularly important for medium-voltage high power applications. Further research on this is relevant due to increasing focus on medium voltage dc distribution [6–9] as well as high power drive and wind turbine applications [10–14].

In Section B.3, the influence of three degrees of freedom associated with the required number of submodules (N) for a fixed dc link voltage is explored. It is shown that since N can only take discrete integer values, the appropriate capacitor voltage ripple and re-

liability factors should be carefully chosen to maximize the installed semiconductor utilization. Using installed semiconductor power as an indicator of cost, it is shown that it disproportionately increases with a unit increase in N for higher blocking voltage class.

In Section B.4, the steady state losses of the half bridge MMC are analytically determined for different IGBT blocking voltage classes. The computations discussed are specific to the case with 10 MVA power delivered at unity power factor to a 10 kV ac grid and support the intuitive understanding that as N increases, the conduction losses increase but the switching losses decrease for a fixed dc link voltage.

Section B.8 reiterates that the final choice of suitable switch rating must consider inter-dependencies between various degrees of freedom that influence the cost, efficiency, size, reliability and power quality of the converter.

B.2. DESIGN CONSIDERATIONS

Figure B.1. shows the schematic of a phase leg (M) of the three phase ac-dc medium voltage MMC.

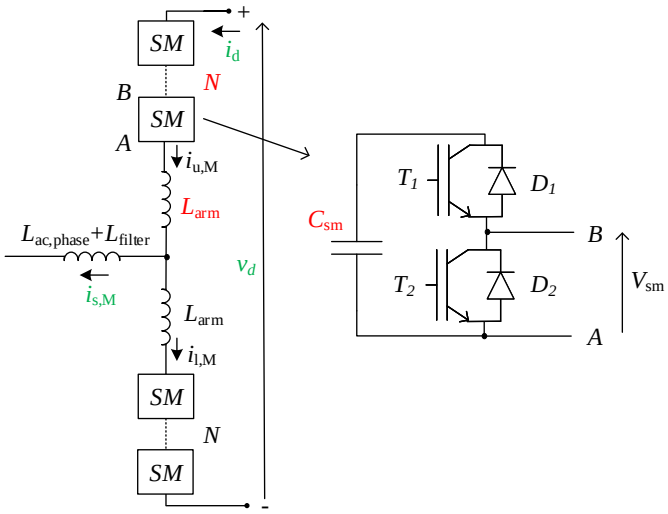


Figure B.1: Schematic of a single leg of a three phase ac-dc modular multilevel converter with half bridge submodules.

It consists of 'N' submodules (SM) and inductance L_{arm} per arm. Each SM consists of two IGBT switches (T_1,T_2) with anti-parallel diodes (D_1,D_2) and a capacitor (C_{sm}). The specifications of the converters are fixed with dc link voltage v_d and the operating active (P) and reactive (Q) powers. The upper and lower arm currents $i_{u,M}$ and $i_{l,M}$, dc link current i_d and the output current $i_{s,M}$ are shown. The available degrees of freedom and associated trade-offs during the design stage are depicted in Figure B.2.

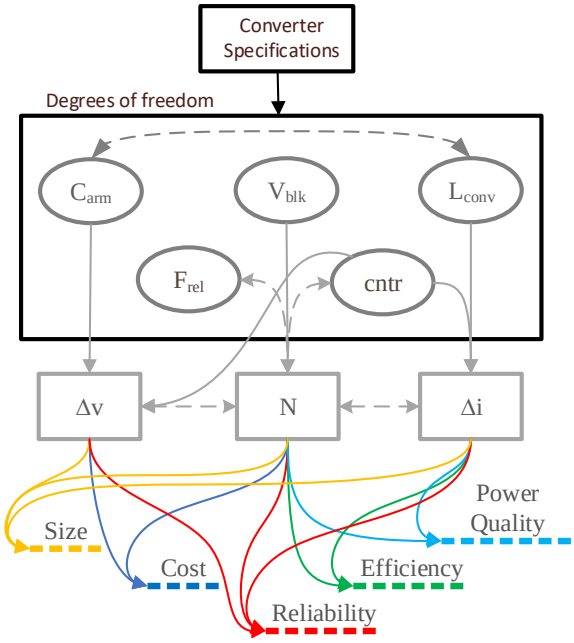


Figure B.2: Degrees of freedom and performance criteria for MMC design of given specification.

B.2.1. ARM CAPACITANCE (C_{ARM})

An interesting discussion is carried out in [15] on the capacitive energy storage requirements. It shows the influence of rated power on the requirement for C_{arm} for a given v_d and thus influences the ripple voltage ΔV. In [16], two parts of ΔV are identified: (i) The average part which is a function of C_{arm} and the converter power independent of control (ii) The local part due to the imbalance in C_{sm} which can be influenced by the blocking voltage class (V_{blk}) (refer Section B.2.2) and control methodology (refer Section B.2.5). As the selected voltge ripple factor (k_{max}) based on the acceptable ΔV increases, the required C_{arm} decreases but may increase the required N. The importance of including the capacitor ripple voltage during the selection of N is also highlighted in [17]. This relationship is explored in Section B.3 and it is shown that since N can only take integral values, the value of k_{max} should be carefully chosen to maximize the semiconductor utilization, particularly for IGBTs with higher V_{blk}.

B.2.2. RATED BLOCKING VOLTAGE (V_{BLK})

V_{blk} strongly governs N. It is discussed in [5] that for a cascaded H-bridge topology, lower switch ratings are preferred as the operating ac grid voltage decreases. This is because the efficiency of the converter is limited by switching losses for lower grid voltages, and by conduction losses for higher voltages. For HVDC application of half bridge MMC, an interesting discussion is presented in [4] about the choice between 3.3, 4.5 and 6.5 kV IGBTs based on investment cost, efficiency and transmitted power. Specifically, it was shown that as transmitted power increased, SMs based on higher blocking volt-

age may be preferred. Increasing preference for 3-level neutral point clamped voltage source converter (VSC) over a 2-level VSC with higher operating powers is also shown in [18]. Applying the combined influence of such principles for a medium voltage half bridge MMC, this analysis supports the relevance of such a design study using a single power level (10 MVA) and grid voltage (10 kV) as an example. An exhaustive investigation on the efficiency boundaries for V_{blk} with varying grid voltage and operating powers is beyond the scope of the present work.

V_{blk} can independently effect the ΔV. For example, in [16], it is shown that as N increases, the local part of ΔV decreases, but this trend is valid only upto a certain number of SMs. Nevertheless, it should be kept in mind that the capacitor voltage ripple maybe inherently lower for an MMC with higher number of SMs. Trade-offs for optimal selection of N related to other degrees of freedom are discussed in subsequent subsections.

B.2.3. RELIABILITY FACTORS (F_{REL})

The degree of freedom in reliability (F_{rel}) involves two factors. The first is the safety factor (S_{f}) that governs voltage limit for safe switching of IGBT (0.65-0.75) as well as the average voltage (0.5-0.65) with respect to reliability due to cosmic ray [4, 19]. In Section B.3, it is shown that a careful selection of S_{f} and C_{arm} can minimize the minimum required number of SMs for the specific blocking voltage class. This is necessary to maximize the utilization of installed semiconductor power. Secondly, the use of redundant SMs to improve the overall converter reliability is important [20]. In this study, it is discussed that while higher number of redundant SMs are necessary as number of components increase, integral increase in N ensures that the penalty in terms of cost and mass density is greater if IGBTs of higher V_{blk} are used, particularly for medium voltage level.

B.2.4. INDUCTANCE (L_{CONV})

The required converter inductance L_{conv} has three important components as described in (B.1),

$$L_{\text{conv}} = L_{\text{ac,phase}} + L_{\text{filter}} + \frac{L_{\text{arm}}}{2} \tag{B.1}$$

The phase inductance $L_{\text{ac,phase}}$ appears at the point of common coupling (PCC) where the MMC is connected with the ac grid. In case an isolating transformer is used, $L_{\text{ac,phase}}$ can incorporate the transformer's leakage inductance as discussed in [17]. More importantly, the magnitude of $L_{\text{ac,phase}}$ limits the rate of rise of surge currents when the ac grid feeds the dc link faults in a half bridge topology [21]. L_{arm} is designed to suppress the frequency components of circulating currents between the MMC phase arms and limit the capacitor discharge currents during dc link faults [22]. An interesting insight on resonance circuit in the half bridge MMC associates L_{arm} with C_{arm} [23]. The filter requirements influence the sizing of L_{filter} as a trade-off with effective frequency for the necessary harmonic mitigation. The association between L_{filter} and N is, therefore, necessary to account for the efficiency and size trade-off [5]. However, since the component of L_{conv} that is independent of N in half bridge MMC ([17, 22, 23]) also contributes towards the performance characteristics, an increase in N may not necessarily imply a strong variation in the final inductance required as suggested in [5].

B.2.5. CONTROL ASPECTS (*cntr*)

Switching frequency f_{sw} influences the synthesized power quality as a trade-off between the required filter inductance and the converter efficiency. For cascaded cells, the effective frequency for the same switching frequency and Δi improves as the square of N for the same filter inductance requirements [5, 24]. Furthermore, it was shown in [16] that as the switching frequency increases, the local part of ΔV decreases for the same N. Thus, the ideal choice of f_{sw} must consider the combined influence on ΔV, N and Δi while considering the efficiency-size trade-off.

Different modulation techniques can be used for the MMC operation [25]. In [26], it was shown that different switching strategies can have different efficiency under similar operating conditions. Furthermore, in [16] it was shown that these can have different impact on ΔV for the same N and f_{sw}. Therefore, the choice of the switching strategy is intimately tied to the efficiency and sizing trade-offs relevant to the optimal choice of f_{sw}, N and ΔV.

B.3. REQUIRED NUMBER OF SUBMODULES

The design trade-offs in this study are shown specifically for a 10 kV r.m.s line-to-line medium voltage ac grid ($v_{\mathrm{ll,rms}}$). Correspondingly, v_{d} is fixed at 16.33 kV based on the empirical study presented in [27] comparing the cable insulation performance under ac and dc voltages. The relationship between the MMC dc link voltage with $v_{\mathrm{ll,rms}}$ is shown in (B.2).

$$v_{\mathrm{d}} = 2.\frac{\sqrt{2}.v_{\mathrm{ll,rms}}}{m.\sqrt{3}} \tag{B.2}$$

Here, the modulation index m is considered as 1. For the MMC to function properly within its PQ limits, third harmonic injection can be used [15], giving 15 % margin in operation. The minimum number of submodules (N_{min}) is given by (B.3),

$$N_{\mathrm{min}} = ceil\left(\frac{k_{\mathrm{max}}\, v_{\mathrm{d}}}{S_{\mathrm{f}} V_{\mathrm{blk}}}\right) \tag{B.3}$$

The factor k_{max} ensures that the instantaneous value of capacitor voltage is never greater than $\frac{k_{\mathrm{max}}\, v_{\mathrm{d}}}{N}$ [15]. S_{f} is in accordance to the voltage limit for safe switching of IGBT [4]. The minimum required SM capacitance decreases with increasing k_{max} for the specified rated power but the consequent semiconductor requirement increases. Based on this trade-off, N_{min} increases with k_{max} for the specified V_{blk}. Considering the market available values of T_1 and T_2 from [28], the possible choices of blocking voltage class explored are 1.2 kV (FF450R12ME4), 1.7 kV (FF450R12ME4), 3.3 kV (FF450R33TE3), 4.5 kV (FZ800R45KL3) and 6.5 kV (FZ500R65KE3). In Figure B.3, N_{min} for different V_{blk} are shown for varying k_{max} and S_{f}.

It can be observed that with an integral increase in N_{min}, there is a range of possible k_{max} for the specified S_{f} at a given V_{blk}. The width (Δk_{max}) of this range governs the utilization of the installed semiconductor. Ideally, the S_{f} and k_{max} should be chosen such that Δk_{max} is fully utilized. While the former influences the reliability, the latter influences the size and cost of the converter; and because the Δk_{max} increases proportionally with V_{blk}, the impact of this trade-off is correspondingly more significant. For

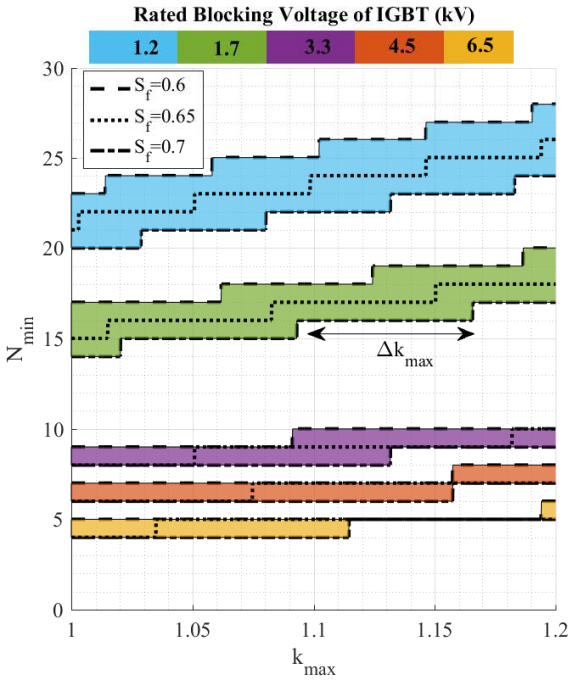


Figure B.3: Minimum required submodules (N_{min}) for different blocking voltage classes (V_{blk}) with varying capacitor voltage ripple factor (k_{max}) and safety factor (S_{f}).

example, in [5], S_{f} was varied to improve utilization. As a result the lower rated switches had 5-10 % higher S_{f} as compared to 3.3 kV. This difference can be minimized using k_{max} to give power density improvement, particularly when converters have high operating power (required capacitance being directly proportional to the converter power [15]).

The total installed semiconductor power $S_{\text{installed}}$ of the converter, given by (B.4), is used as an indicator for the costs.

$$S_{\text{installed}} = 6 * 2 * N * V_{\text{blk}} * I_{\text{r,IGBT}} \tag{B.4}$$

The factor of '6' comes from the six arms of a three phase implementation and the factor 2 is due to the number of IGBT switches per half bridge submodule. Figure B.4 shows the $S_{\text{installed}}$ corresponding to N_{min} for different V_{blk} and rated switch current $I_{\text{r,IGBT}}$ of 450 A with varying k_{max} and normalized with the base power of 10 MVA. The observation supports the intuitive understanding that a unit increment in N_{min} has a higher impact on $S_{\text{installed}}$ (thus cost & size) with higher V_{blk}.

For example in region A, $S_{\text{installed}}$ for the 1.7 kV IGBT is almost 12 % lower than that with 6.5 kV IGBT and the lowest for 1.2 kV IGBT. The difference is halved in region B while 3.3 kV switch has the lowest $S_{\text{installed}}$.

For medium voltage applications, this disproportionate increase in installed power to an unit increment in N should be considered while evaluating the various trade-offs involved in the design choices for the MMC. This is even more significant when consid-

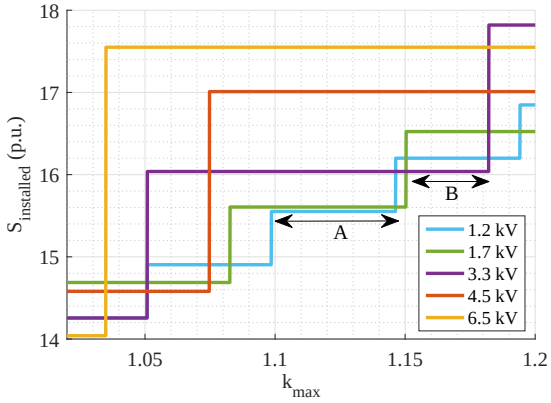


Figure B.4: Total installed semiconductor power for different IGBT blocking voltage class with varying voltage ripple factor.

ering the redundancy requirements. It is valid that with lower V_{blk}, the number of components increase and therefore, greater redundancy is require to improve the system reliability. On the other hand, from the stand point of costs and size, a unit increment in N with higher V_{blk} has greater penalty. This can be observed in Figure B.5, where the total number of SMs (N_{tot}) including 10 % redundancy requirements and the corresponding $S_{installed}$ are shown for varying k_{max}.

The $S_{installed}$ for 1.2-3.3 kV switches is 15-20 % lower than that for 6.5 kV for k_{max} in the range of 1.1-1.15. In summary, the interplay of reliability, redundancy and energy storage should be carefully compared to cost and size indicators before choosing the blocking voltage class.

B.4. CONVERTER LOSSES

This section describes the MMC conduction and switching losses for different switch ratings considered. A good basis for the steady state loss modelling of MMC is provided in [29–32].

B.4.1. CONDUCTION LOSSES

The IGBT output characteristics and the diode forward characteristics governing the conduction losses for different V_{blk} at junction temperature of 125 °C is shown in Figure B.6 and Figure B.7 respectively.

In general, it can be seen that the voltage drop across these devices increases with V_{blk} for the same conduction current. The outlier is 4.5 kV because a higher switch current rating was selected as compared to the other devices. This was because the manufacturer [28] did not offer the specific current rating for this voltage level. On the other hand, since N increases with decreasing V_{blk}, the cumulative conduction losses can be higher for lower blocking voltages. In order to compute the conduction losses, it is necessary to establish which power electronic component of the SM is conducting at any

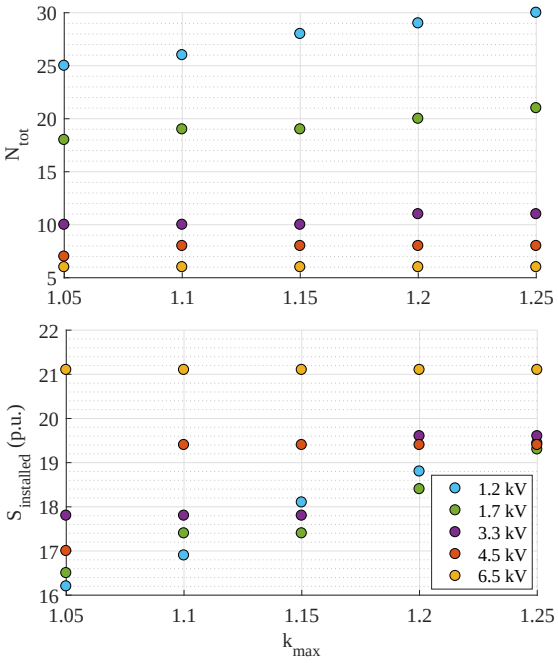


Figure B.5: Variation in (a) Total number of submodules (b) Installed semiconductor power with energy storage requirements for different submodule switch ratings including redundancy requirements with $k_{\max}$.

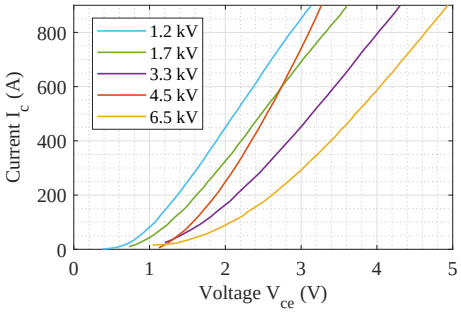


Figure B.6: IGBT output characteristics for different blocking voltages at 125 °C from the datasheets [28].

given instant of operation [29]. Figure B.8 (a) and (b) show that with positive arm current, the diode D_1 conducts when the SM is inserted, while IGBT T_2 conducts when the SM is bypassed. Similarly, Figure B.8 (c) and (d) depict that when arm current is negative, IGBT T_1 conducts in inserted while diode D_2 conducts in bypass state.

Based on the current flow in SM devices, the instantaneous total upper arm conduction losses corresponding to the active IGBTs ($P^{\Sigma}_{\text{cond,u,T}}$) and active diodes ($P^{\Sigma}_{\text{cond,u,D}}$) in

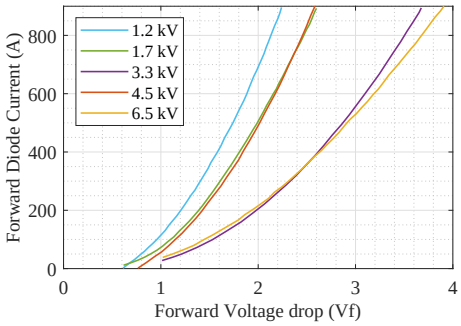


Figure B.7: Diode forward characteristics for different blocking voltages at 125 °C from the datasheets [28].

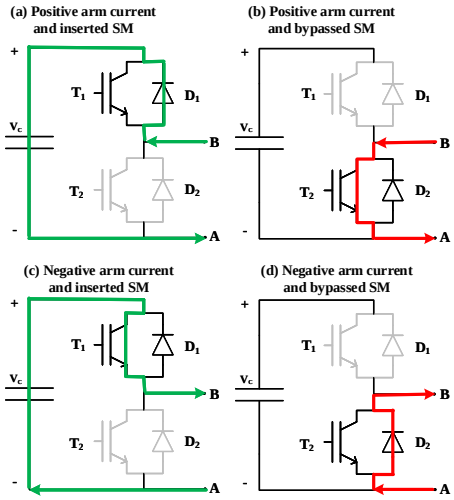


Figure B.8: Current Flow in inserted/bypassed SMs for different arm current directions.

one fundamental time period T_f are given by (B.5) and (B.6) respectively. Similar equations can be written for the lower arm conduction losses.

$$P^{\Sigma}_{\text{cond,u,T}} = \begin{cases} \frac{1}{T_f}\int_0^{T_f}(N-n_u)\cdot V_{ce}\cdot i_u\cdot dt & ;\text{if } i_u \geq 0 \\ \frac{1}{T_f}\int_0^{T_f} n_u\cdot V_{ce}\cdot i_u\cdot dt & ;\text{if } i_u < 0 \end{cases} \tag{B.5}$$

$$P^{\Sigma}_{\text{cond,u,D}} = \begin{cases} \frac{1}{T_f}\int_0^{T_f} n_u\cdot V_f\cdot i_u\cdot dt & ;\text{if } i_u \geq 0 \\ \frac{1}{T_f}\int_0^{T_f}(N-n_u)\cdot V_f\cdot i_u\cdot dt & ;\text{if } i_u < 0 \end{cases} \tag{B.6}$$

V_{ce} is the voltage drop of the IGBT and V_f is the forward voltage drop across the diode

while conducting current i_u given by (B.7) under considered operating conditions.

$$i_u = \frac{i_d}{3} + \frac{i_{s,M}}{2} \tag{B.7}$$

B

The instantaneous conduction current dependent voltage drops at 125 °C are found using interpolation of data-points in a look-up table obtained from the datasheets provided by the manufacturer [28]. The upper and lower devices in the SM will have unequal power losses, but this aspect is neglected in this analysis. n_u is the number of inserted SMs in the upper arm, computed based on the nearest level control (NLC) [33, 34]. Instantaneous insertion indices corresponding to other modulation techniques such as carrier based pulse width modulation can also be used for computation, but this is not the focus of this present study.

$$n_u = round\left(N * \left(\frac{v_u}{V_{cu}^{\Sigma}}\right)\right) \tag{B.8}$$

Here, v_u is the inserted upper arm voltage and V_{cu}^{Σ} is the total sum of voltages across all the capacitors of the upper arm. $P_{cond,u,T}^{\Sigma}$, $P_{cond,u,D}^{\Sigma}$ and the total instantaneous conduction losses in the upper arm of one phase leg of the MMC for the rated operation of 10 MVA at unity power factor with modulation index of 1 is shown in Figure B.9.

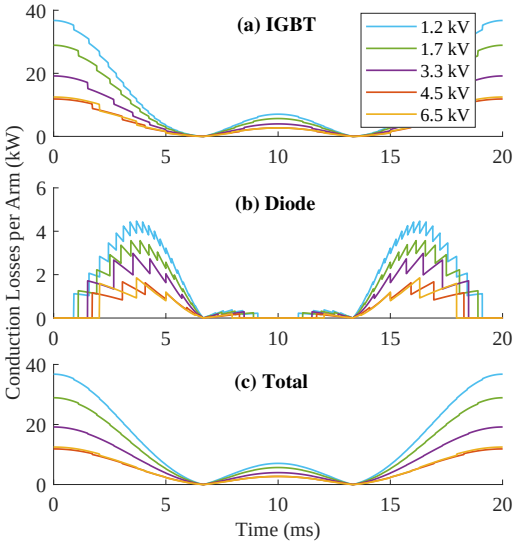


Figure B.9: Instantaneous conduction loss in a single MMC arm for one fundamental period under rated operation for different switch ratings (a) IGBT (b) Diode (c) Total.

The average conduction losses (assuming uniform losses in the top and bottom IGBT devices of the submodules) increase as the V_{blk} decreases.

B.4.2. SWITCHING LOSSES

In order to compute the switching losses, the data for switching energy loss (E) in mJ with respect to the switching currents was extracted from [28]. The diode turn-off losses, IGBT turn-on and turn-off energy for different V_{blk} is shown in Figure B.10, Figure B.11 and Figure B.12 respectively.

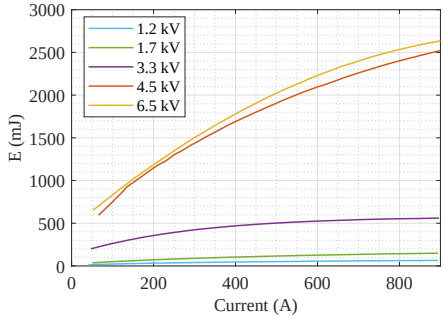


Figure B.10: Diode switching losses for different blocking voltages at 125 °C from the datasheets [28].

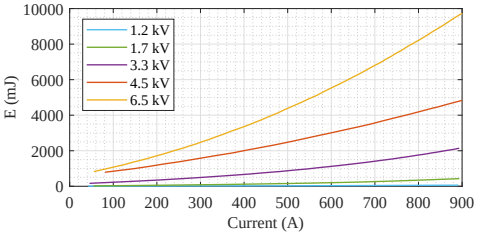


Figure B.11: IGBT turn-on energy loss for different blocking voltages at 125 °C from the datasheets [28].

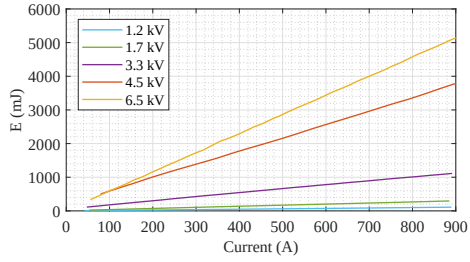


Figure B.12: IGBT turn-off energy loss for different blocking voltages at 125 °C from the datasheets [28].

As expected, it is observed that with higher voltages, the switching energy increases. Furthermore, as N increases, the switching frequency needed to maintain the same harmonic performance reduces. Therefore, the switching losses can be expected to be lower

when smaller V_{blk} is selected. To calculate the switching loss, the commutation of specific device (IGBT or Diode) based on the level transition and the direction of the arm current must be known. This is shown in Figure B.13 for a 6-level 6.5 kV IGBT operating with NLC at fundamental switching frequency.

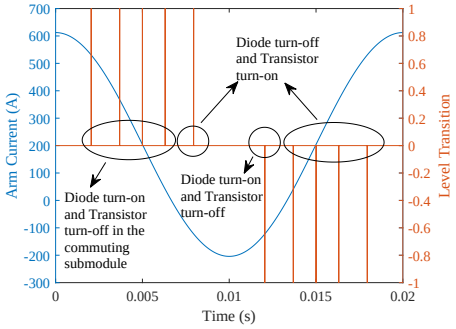


Figure B.13: Commutation of devices based on directions of level transitions and arm current for one fundamental period with 6.5 kV switch based 6-level MMC in steady state operation for NLC at fundamental switching frequency.

The level transition is +1 if a SM in upper arm inserted and -1 if a upper arm SM is bypassed. Since there are 5 SMs per arm, total number of transitions $N_{\text{transitions}} = 10$ are observed. For the associated arm current direction, the highlighted turn-on and turn-off of devices can be inferred from Figure B.8.

The average converter efficiency including both conduction and switching losses, cumulative for all 6 arms of the MMC is shown in Figure B.14 with respect to the effective frequency F_{eff}.

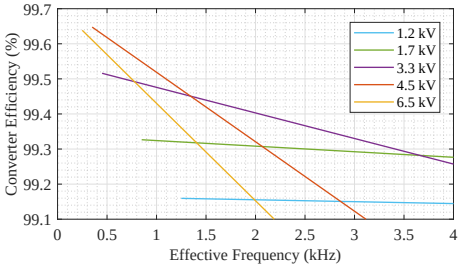


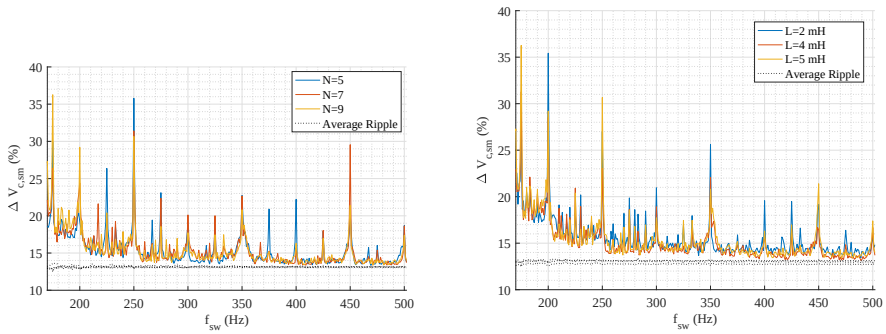
Figure B.14: Total converter efficiency considering both conduction and switching power loss for different IGBT switch voltage rating with respect to effective frequency of operation.

F_{eff} is given by the product of actual switching frequency F_{sw} and N. It can be seen that the crossover from 3.3 kV to 1.7 kV occurs at the F_{eff} of about 3.5 kHz, corresponding to a F_{sw} of 389 Hz for the former and 206 Hz for the latter. As discussed in Section B.2.5, the optimal value of the F_{eff} for the given V_{blk} is a trade-off between power

quality requirements in combination with L_{filter}, the local capacitor voltage ripple and the switching strategy employed. If the fault current limitation requires a certain minimum $L_{\text{ac,phase}}$, this condition could favour a higher V_{blk} in its F_{sw} trade-off with L_{filter}. On the other hand, a reduced N can require a higher F_{sw} to balance the individual SM capacitors, even though this relationship is shown to be less significant above $N = 12$ [16]. Furthermore, minimum switching requirements for capacitor balancing efforts for voltage ripple minimization could set a lower limit on the achievable reduction in F_{sw} with lower V_{blk}. Therefore, the efficiency crossover points depicted in Figure B.14 should be considered in relation to the performance, size and cost before choosing the optimum IGBT voltage rating. These crossover points vary with the operating voltage and power level of the MMC. Such considerations are important, but beyond the scope of this discussion.

B.5. SUBMODULE CAPACITOR VOLTAGE BALANCING

The maximum submodule (SM) capacitor voltage ripple ($\Delta V_{\text{c,sm}}$) as a percentage of average SM voltage ($\frac{v_{\text{d}}}{N}$) is shown in Figure B.15. Switch model simulations were performed using parameters listed in Table 4.1 based on the fully loaded MMC with current controllers as suggested in [35, 36] with a frequency sweep between the range of 150-500 Hz at a step of 1 Hz. PS-PWM method is used with no phase shift between the carriers corresponding to upper and lower arms of the MMC.



(a) (b)

Figure B.15: Simulated maximum voltage ripple in submodule capacitors with f_{sw} for $C_{\text{sm}}/N = 0.22$ mF and for (a) varying N with $L_{\text{arm}} = 5$ mH (b) varying L_{arm} with $N = 9$.

The observation that the local ripple due to capacitor voltage imbalance decreases with f_{sw} and that this decline is particularly significant for lower f_{sw} is consistent with the findings in [16]. However, unlike [16], a clear tendency was not observed with the variation in N (Figure B.15a), possibly because the selected simulation parameters in [16] were corresponding to extremely high power (in GW) and voltage (320 kV). Nevertheless, the same study also predicts weak to no dependence of $\Delta V_{\text{c,sm}}$ with $N > 10$. Figure B.15b shows that $\Delta V_{\text{c,sm}}$ is independent of L_{arm} as well.

The result suggests that the capacitor voltage balancing requirements set a mini-

mum limit on the required switching frequency ($f_{sw,min}$) independent of the chosen N and L_{arm} where the local ripple is negligible and the $\Delta V_{c,sm}$ converges to the operating power dependent average voltage ripple corresponding to the total arm capacitance. This aspect can be of importance while optimizing the three degrees of freedom for converter harmonic performance, but may not necessarily always be an issue because at medium voltage levels the conduction loss constraint puts an upper limit on the optimal N [5, 26]. Therefore, it is suggested as a design thumb-rule, that the first approximation of the switching frequency should be independently chosen above the minimum required $\Delta V_{c,sm}$ for the given modulation method and operating conditions before choosing the optimal N and L_{arm}. It can be observed that a $\Delta V_{c,sm}$ reasonably close to the $\Delta V_{c,avg}$ can be obtained for $f_{sw,min} > 250$ Hz. In Figure B.16, it can be seen that $f_{sw,min}$ where the actual $\Delta V_{c,sm}$ is close to the designed arm energy storage dependent average ripple is similar, about 250 Hz even with higher total arm capacitance ($C_{sm}/N = 0.37$ mF).

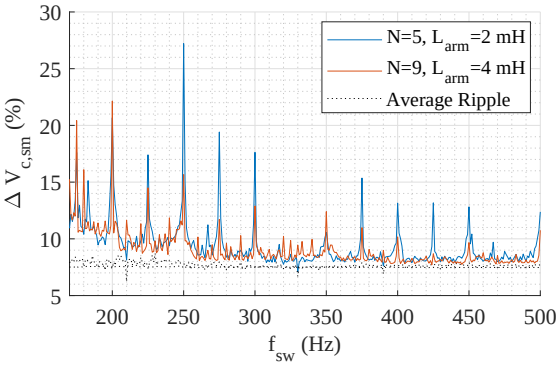


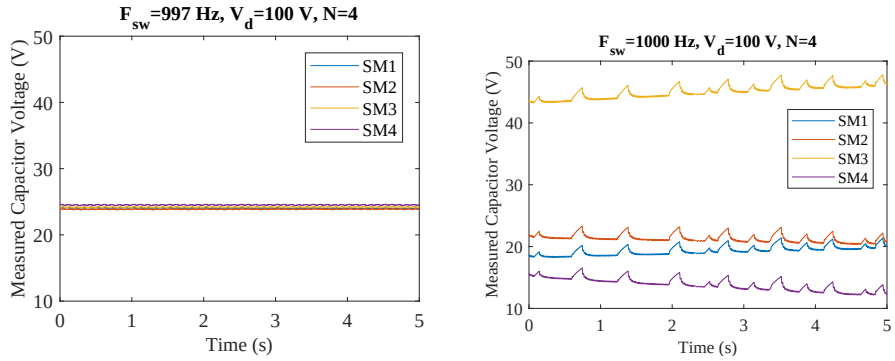
Figure B.16: Simulated maximum voltage ripple in submodule capacitors with switching frequency for $C_{sm}/N = 0.37$ mF.

Another important observation is that when f_{sw} is a multiple of 50 Hz, the capacitor balancing is much worse for PS-PWM and thus, in MMCs, the value of f_{sw} is usually selected to give a non-integer frequency ratio [36, 37]. The empirical evidence for this is shown in Figure B.17.

In this experiment, the 4-submodule MMC lab prototype with $C_{sm} = 4$ mH is run using a DC source at 100 V with a modulation index of 1 to power a resistive load of 60 Ω at the ac side. Gate signals generated using PS-PWM by the real time simulator were sent to the sub-modules using optical fibres. The individual SM capacitor voltages were observed to be balanced with non 50-multiple switching frequency of 997 Hz but not when it is 1000 Hz. With this supporting insight for [37], the design switching frequency will be chosen a prime number.

B.6. CIRCULATING CURRENT RIPPLE

An interesting discussion on circulating current ripple (ΔI_c) variation with arm inductance is provided in [38], but the impact of N is not explored. In the current work, we

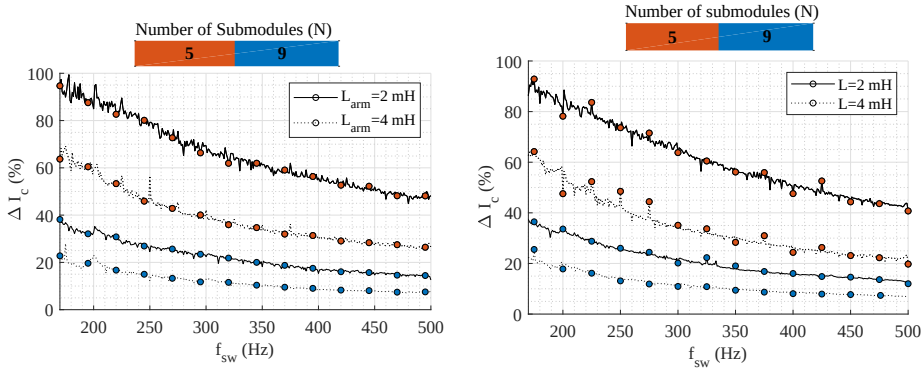


(a) (b)

Figure B.17: Experimental result showing capacitor imbalance due to slightly different switching frequency a) 997 Hz b) 1000 Hz.

want to study the combined impact of f_{sw}, N and L_{arm} on ΔI_{c}.

Figure B.18 shows the simulated frequency sweep results for ΔI_{c} as a percentage of its mean value, which decreases with increase in f_{sw}, N and L_{arm}.



(a) (b)

Figure B.18: Switching frequency, arm inductance and number of submodules trade-off for high frequency circulating current ripple with (a) $C_{\text{sm}}/N = 0.22$ mF (b) $C_{\text{sm}}/N = 0.37$ mF.

In these results, the circulating current controller is designed based on the principles in [22, 35] and the peak high frequency ripple component is computed in steady state. The main observation is that decrease in ΔI_{c} is more significant with N, as compared to f_{sw} and L_{arm} and appear independent of total arm energy. Though the circulating current controller may mitigate the resonance limits imposed, the $L_{\text{arm,min}}$ should be considered for robust design. While the impact of high frequency circulating current on efficiency of MMC may be marginal and its effect of component reliability and electromagnetic interference (EMI) is beyond the scope of this chapter, it is suggested that the

Table B.1: Maximum current distortion limits for systems rated 120 V - 69 kV (as percent of fundamental). Table for odd harmonics (even harmonics limits are 25 % of these) [39]

I_{SC}/I_L	3≤ h<11	11≤ h<17	17≤ h<23	23≤ h<35	35≤ h<50	TDD
<20	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

designed ΔI_c be below 20 % as a design thumb-rule for the considered operational conditions of the MMC.

B.7. HARMONIC PERFORMANCE

In this section, the objective is to find the minimum values of f_{sw}, N and L_{arm} in order to achieve acceptable harmonic performance.

B.7.1. ASSUMPTIONS FOR ACCEPTABLE HARMONIC PERFORMANCE

In this chapter, the current harmonic limits defined in the standard IEEE 519 (2014) are going to be followed. These are shown in Table B.1 for LV and MV applications [39]. The limits are set depending on the short-circuit ratio (SCR, the ratio of the available short-circuit current from the grid, I_{SC}, to the load current, I_L). The simulations are performed with a high SCR=100 and therefore, result in correspondingly high current harmonics at point of common coupling (PCC) due to low assumed grid inductance. However, the design procedure is chosen to comply with harmonic limits corresponding to the lowest SCR ($I_{SC}/I_L < 20$ in Table B.1), due to the fact that here the limits are the strictest. These two assumptions ensure that the design procedure follows the most stringent requirements for the output current harmonic performance. If voltage harmonic performance is used as design criteria, the worse case assumptions should be different.

The Total Demand Distortion (TDD) is defined as Eq. B.9, where I_h is the current amplitude of the h-th harmonic component (h-th integer multiple of the fundamental, f_0) [39]. $I_{1,max}$ is the maximum demand current and $H = 50$.

$$TDD = \frac{\sqrt{\sum_{h=2}^{H} I_h^2}}{I_{1,max}} \tag{B.9}$$

It can be inferred that the straightforward interpretation of (B.9) may not take into account the harmonic components that appear at frequencies that are non-integer multiple of the fundamental, referred to as 'interharmonics' in [40–42]. In the case of the MMC, interharmonic distortion might be especially important because f_{sw} is typically selected as a non-integer multiple of the fundamental (Section B.5). As a consequence, the effective switching frequency $f_{eff} = N f_{sw}$ is not necessarily an integer multiple of 50

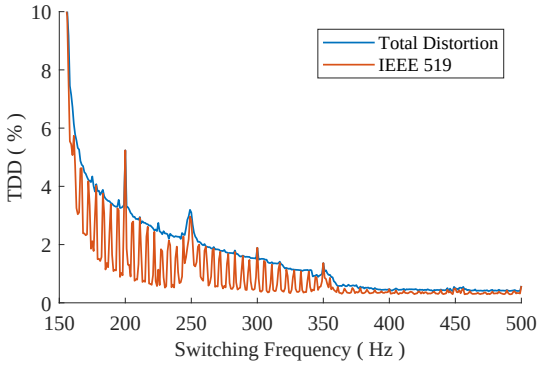


Figure B.19: Simulation results (N = 9 and L_{arm} = 3 mH). Comparison of TDD calculated without interharmonics (IEEE 519) with TDD calculated with interharmonics (all distortion).

Hz. Including interharmonics in the calculation of TDD is relevant because the associated switching harmonic sidebands will appear around the effective frequency and its multiples [43].

Figure B.19 shows the TDD calculated without interharmonics according to (B.9) as compared to the TDD calculated taking into account the interharmonics. It is observed that TDD is the same in both methods when the $f_{\text{eff}} = N f_{\text{sw}}$ is a multiple of 50 Hz, while for all other f_{eff}, the TDD is much lower if interharmonics are ignored. Thus, from here on, the TDD results presented include the interharmonic contribution.

B.7.2. DESIGN PARAMETERS INFLUENCE ON HARMONIC PERFORMANCE

Simulation results for output current TDD with varying f_{sw}, N and L_{arm} are shown in Figure B.20. It can be observed that the TDD limit of $< 5\,\%$ is met for the majority of N and L_{arm} combinations with the $f_{\text{sw,min}} = 250$ Hz set by the capacitor balancing requirement for PS-PWM (refer Section B.5).

However, the design must comply with the individual harmonic limits presented in Table B.1. As an example, the current spectrum for $N = 9$, $f_{sw} = 313$ Hz and $L_{\text{arm}} = 3$ mH is shown in Figure B.21. It can be observed that the switching harmonics appear around ($f_{\text{eff}} = 2817$ Hz) and are not compliant for the limit of 0.3 % for the orders $35 \leq h < 50$.

The current spectrum should be checked for all combinations of N, f_{sw} and L_{arm} in order to see which ones achieve compliance. Before doing this, it is useful to limit the number of possible combinations by using the relation of f_{eff} with efficiency. If the $f_{\text{eff}} = N f_{\text{sw}}$ is chosen higher than 2500 Hz, then a significant part of the switching harmonic content will fall in a frequency range that it is not restricted in the requirements (as the TDD and the individual harmonic limits are defined until the 50^{th} order i.e. 2500 Hz). Since the sidebands $f_{\text{eff}} \pm 5 f_0$ and $f_{\text{eff}} \pm 3 f_0$ typically have high magnitude, it is suggested to consider the minimum effective frequency of $f_{\text{eff,min}} = 2750$ Hz (55^{th} order).

The optimal value of N for minimizing the total converter losses as a function of f_{eff} has been discussed in preceding sections. For $f_{\text{eff}} = 2750$ Hz, it is shown that $N = 9$ presents the highest efficiency with the considered operating conditions. Thus, N =9 is

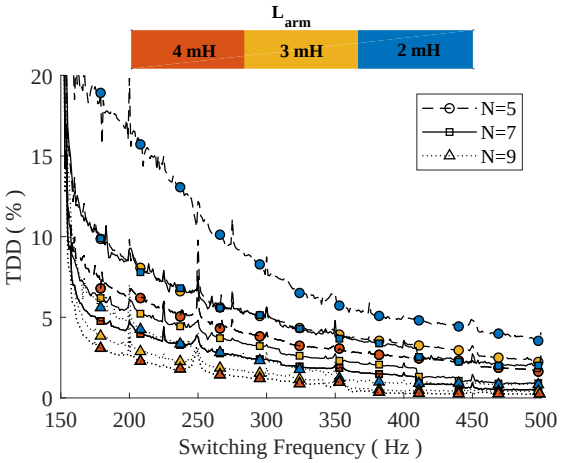


Figure B.20: Output current TDD with varying f_{sw} for different N and L_{arm}.

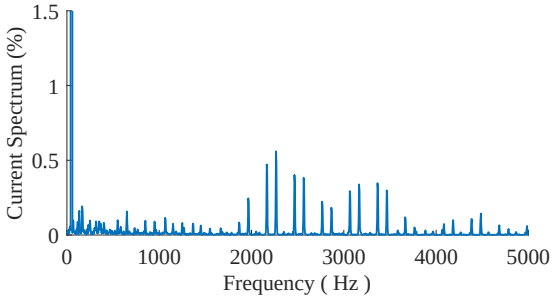


Figure B.21: Simulation results. Current spectrum (as percent from the fundamental) for $f_{sw} = 313\,\text{Hz}$, $N = 9$ and $L_{arm} = 3\,\text{mH}$.

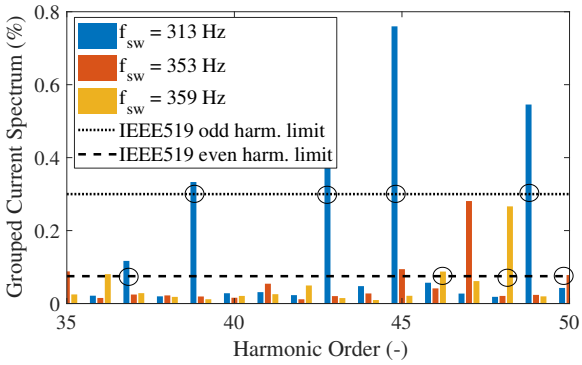


Figure B.22: Simulation results. Grouped current spectrum (as percent from the fundamental) for $N = 9$, $L_{arm} = 3$ mH and different switching frequencies.

selected and to comply with the limits, either L_{arm} or f_{sw} can be increased. $L_{arm} = 3$ mH is the minimum arm inductance required to prevent resonance with arm capacitances corresponding to $C_{sm} = 3.3$ mF. Since it is proved that the efficiency of the converter for medium voltage high power application is conduction loss limited for $N = 9$, prime numbers of $f_{sw} > 305$ Hz are considered.

Figure B.22 shows the current spectrum for $35 \leq h < 50$ for different f_{sw}. As limits in Table B.1 are defined for only integer harmonic frequencies, a grouping technique was applied, wherein the energy of the interharmonics was summed to the adjacent integer harmonic frequencies.

For harmonic orders below 35 compliance was always met. However, for $N = 9$, $L_{arm} = 3$ mH and $f_{sw} = 313$ Hz (plot in blue), the individual harmonic limits are not met (violations are marked by a circle). The switching frequency was increased until all the harmonic orders were within limits, which happened for $f_{sw} = 353$ Hz (plot in red). It was observed that the limit was violated for a higher switching frequency of 359 Hz. This is possibly due to the way that the grouping techniques work: if one interharmonic happens to lie at a frequency closer to an odd harmonic number its energy will be added to an odd harmonic number, which will be beneficial for compliance because the permissible limits are higher for odd harmonic numbers than for even numbers.

It is therefore concluded that switching frequency ($f_{sw} = 353$ Hz) achieves harmonic compliance for $N = 9$ and $L_{arm} = 3$ mH for the considered operating conditions. The final $f_{eff} = 9 * 353 = 3177$ Hz leads to an approximate semiconductor efficiency (associated with conduction and switching losses in submodules) of 99.3 % at full load. It can be inferred that this design choice maximizes the achievable efficiency while simultaneously complying with harmonic performance criteria in contrast with $N = 5$ or 7. At the same time, this design achieves reasonably low circulating current ripple ($\Delta I_c < 20$ %).

B.8. CONCLUSIONS AND FUTURE WORK

This work emphasizes that the selection of the suitable IGBT switch blocking voltage class is important for medium voltage high power applications of modular multilevel

converters. Highlighting that this choice is not straightforward, the various inter-dependencies with respect to capacitor sizing, reliability, inductance requirement, switching frequency and control strategy are identified.

It was shown that as the required switching frequency increases, the IGBTs with lower V_{blk} become more favourable from converter efficiency standpoint. In general, an increase in V_{blk} is almost always accompanied by an increase in required switching frequency in a trade-off with L_{filter} for achieving acceptable power quality. However, this dependence can be limited if N is already high enough to necessitate improvement in the harmonic performance and/or a constant inductance is required for protection needs. Therefore, as a future work, the optimal switching frequency requirement as a function of V_{blk} should be incorporated in the design stage.

Some evidence in the available literature indicates that with lower ac and dc side operating voltages, lower V_{blk} offer greater MMC efficiency. At the same time, an increase in power level favours higher V_{blk}. Mapping the effect of these two factors towards the complete design of a half bridge MMC for medium voltage, high power applications can be an interesting research effort.

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B

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List of Publications

Journal Punblications (Related to This Thesis)

4. **A. Shekhar**, L. M. Ramirez-Elizondo, T. B. Soeiro and P. Bauer, "Boundaries of Operation for Refurbished Parallel AC-DC Reconfigurable Links in Distribution Grids," in *IEEE Transactions on Power Delivery,* 2019.

3. **A. Shekhar**; X. Feng; A. Gattozzi; R. Hebner; D. Wardell; S. Strank; A. Rodrigo-Mor; L. Ramírez-Elizondo; P. Bauer, "Impact of DC Voltage Enhancement on Partial Discharges in Medium Voltage Cables—An Empirical Study with Defects at Semicon-Dielectric Interface" *Energies* 2017, 10, 1968.

2. **A. Shekhar**, E. Kontos, L. Ramírez-Elizondo, A. Rodrigo-Mor, P. Bauer, "Grid capacity and efficiency enhancement by operating medium voltage AC cables as DC links with modular multilevel converters, " *International Journal of Electrical Power & Energy Systems,* Volume 93, 2017, Pages 479-493, ISSN 0142-0615.

1. **A. Shekhar**, L. Ramírez-Elizondo, X. Feng, E. Kontos, P. Bauer, "Reconfigurable DC Links for Restructuring Existing Medium Voltage AC Distribution Grids," *Electric Power Components and Systems,* 2017, 45:16, 1739-1746.

Journal Publications (Under Review, This Thesis)

2. **A. Shekhar**, T. B. Soeiro, Y. Wu and P. Bauer, "Optimal Power Flow Control in Parallel Operating AC and DC Distribution Links ," in *Transactions on Industrial Electronics,* 2019.

1. **A. Shekhar**, T. B. Soeiro, L. M. Ramirez-Elizondo and P. Bauer, "Offline Reconfigurability based Substation Converter Sizing for Hybrid AC-DC Distribution Links," in *IEEE Transactions on Power Delivery,* 2019.

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CONFERENCE PUNBLICATIONS (RELATED TO THIS THESIS)

10. **A. Shekhar**, T. B. Soeiro, L. Ramírez-Elizondo and P. Bauer, "Zero Sequence Currents Externally Circulating between the Back to Back Modular Multilevel Converters in Parallel AC-DC Distribution Links," *IEEE 10th International Conference on Power Electronics – ECCE Asia (ICPE 2019-ECCE Asia)*, Busan, South Korea, 2019.

9. **A. Shekhar**, L. Beloqui Larumbe, Y. Wu, T. B. Soeiro and P. Bauer, "Number of Levels, Arm Inductance and Modulation Trade-offs for High Power Medium Voltage Grid-Connected Modular Multilevel Converters," *IEEE 10th International Conference on Power Electronics – ECCE Asia (ICPE 2019-ECCE Asia)*, Busan, South Korea, 2019.

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