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Output Impedance Modelling and Sensitivity Study of Grid-Feeding Inverters with Dual Current Control

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***Abstract*—In this paper, the output impedance of a three-phase inverter based on a dual current control (also called double synchronous reference frame current control) is modelled, which includes: the current loop gain, the control delay, and the Phase-Locked Loop (PLL). The impact of these parameters on the impedance is then analysed by a sensitivity study. The model is derived using transfer matrices and complex transfer functions, and it results in a compact impedance formulation that can be used in harmonic small-signal stability studies and system-wide steady-state harmonic calculations.**

***Index Terms*—inverter, dual current control, double synchronous reference frame, small-signal model, impedance**

I. Introduction

Concern about power quality has risen in recent years for all kinds of electric power systems [1], [2]. One of the undisputed reasons for this concern is the proliferation of Power Electronic Converters (PECs), which lead to increasing harmonic injections, to time-varying resonances and to unexpected grid-converter interactions at very different frequencies [1], [3]. The issue can be especially significant when the connection with the grid is weak. Several failures of power systems related to the above issues have already been reported [4]–[6]. As a consequence, modelling of PEC-based grid aiming for harmonic analysis and mitigation is obtaining more and more research effort [7]–[9].

One of the typical converter representations is the so-called impedance model, in which the PEC is modelled as a Norton or Thevenin equivalent. The idea is to use the current/voltage source to depict the harmonic emission and to use the impedance to represent both the output filter and the dynamics of the converter and of its control loops. Previous research has shown that the controllers in the PECs have a significant impact on both the current/voltage source [10] and the impedance part [11].

Of the two elements of the Norton or Thevenin equivalent of an inverter, this paper focuses on modelling the impedance part. In the literature, the majority of the impedance modelling is based on a single Synchronous Reference Frame (SRF) control structure (i.e. the typical dq-frame current control as in [9], [12], [13]), because it is frequently implemented. However, another type of control structure called double SRF or dual controller [14] is becoming widespread in several applications (e.g. in state-of-the-art offshore wind turbines [15]–[18]) due to its superior dynamic performance under unbalanced grid conditions [14]. This type of control structure has been modelled previously in the literature (e.g. [19]–[21]) although always ignoring the impact of the Phase-Locked Loop (PLL) dynamics which might have a big influence on the output impedance.

Therefore, this paper presents an impedance model for double-SRF-controlled inverters that includes the PLL dynamics. The objective of this paper is not to show the superior transient performance of the double SRF vs. the single SRF control structure, but rather, to show a model of an inverter that has the double SRF control implemented. Then, a sensitivity analysis is shown in order to find out which of the control parameters are most influential in the model and in what frequency range.

The results show that, with the double SRF, the inverter impedance presents several regions of negative-resistive behaviour that can be linked to —and modified by— the control parameters. These negative resistance regions have a different magnitude than in the single SRF case. Converters with negative damping characteristics have previously been related to high amplification factors and sometimes even to system instability [12], [13].

The paper is organized as follows: in Section II, the inverter and its double SRF control are described. In Section III, the theoretical model is presented. A sensitivity analysis on how to shape the output impedance is found in Section IV and conclusions are summarized in Section V.

II. Inverter Description

The PEC to be modelled is shown in Fig. 1. It consists of a two-level voltage-source inverter controlled by a current loop and a PLL. The converter is controlled in a grid-feeding mode; that is to say, it behaves as a current source on the

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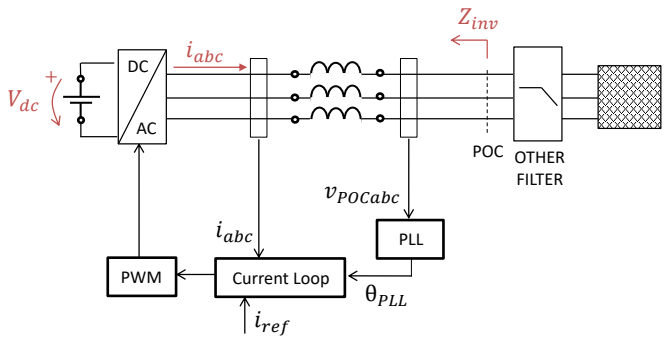


Fig. 1: Schematic of inverter with current control and PLL.

AC side. The current control receives the reference i_{ref} either from a user-defined command or from an outer control loop. As a first approximation, the DC voltage (V_{dc}) is considered constant in this study.

The converter has a filter that consists on an output inductor L with a resistance R_{L}. The objective is to calculate the impedance of the inverter Z_{inv} seen at the Point of Connection (POC) (see Fig. 1). Other filter stages can be added a posteriori to Z_{inv} with linear circuit theory.

A. Current Control Loop

In this paper, the current control considered is the dual controller or double SRF, as shown in Fig. 2. This structure controls simultaneously and separately the positive and the negative sequence currents. If the fundamental frequency of the voltage at the POC is defined as ω_1, then the aim is to control the positive sequence current in a SRF that rotates at $+\omega_1$. In such a frame, the positive sequence appears as a DC component that can be tracked with no steady-state error with the use of a PI controller. The negative sequence in this frame appears as a $2\omega_1$ component that can be easily filtered through a notch filter tuned at this frequency. In parallel, the negative sequence is controlled in a SRF rotating at $-\omega_1$ in which the positive sequence is filtered with also a notch filter.

The formula for the PI controller can be found in (1). In Section IV a base case is going to be used as a reference in order to do a sensitivity analysis. The base case is defined in order to try to mock the response of a grid-side inverter in Type IV Offshore Wind Turbines. The base case parameters can be found at the end of the paper in Tables I–III. In this base case, the values of the PI have been chosen as $K_{\text{i}} = K_{\text{p}} R_{\text{L}}/L$ in order to cancel the pole in the plant. K_{p} was selected to obtain a current control bandwidth of approximately BW_{i}=200 Hz (around 10 times lower than the switching frequency f_{sw}=2.5 kHz).

$$H_i(s) = K_p + \frac{K_i}{s} \tag{1}$$

The formula for a typical notch filter is shown in (2), where ω_{n} is the angular frequency at which the filter is tuned (in this application, $2\omega_1$) and Q_{n} and Q_{d} are two constants that need to be tuned according to how wide and deep the filtering function

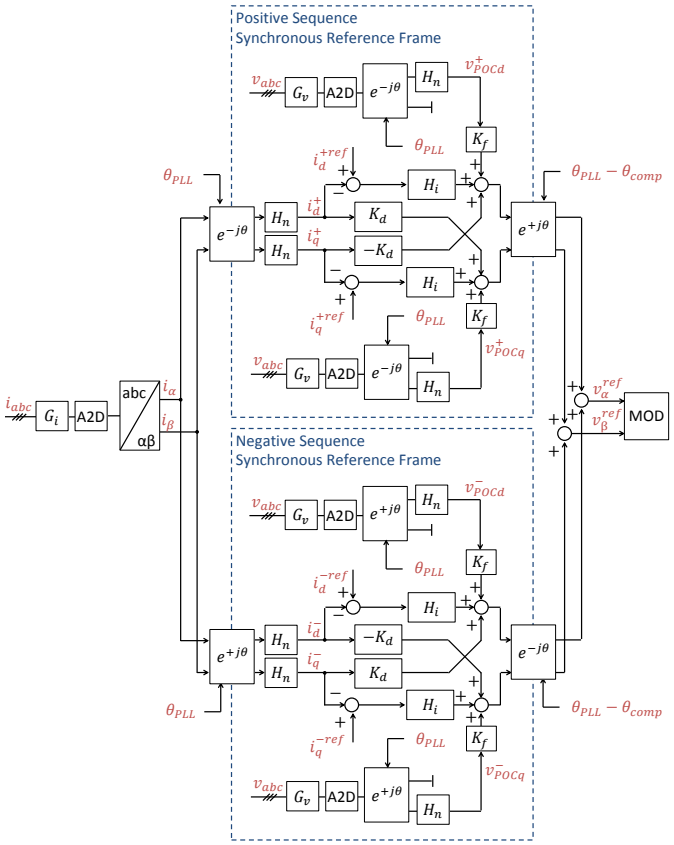


Fig. 2: Dual current control or Double Synchronous Reference Frame.

needs to be around ω_{n}. The parameters chosen for this filter are Q_{n}=10/sqrt(2) and Q_{d}=2/sqrt(2) as suggested in [16].

$$H_n(s) = \frac{s^2 + \left(\frac{\omega_n}{Q_n}\right) s + \omega_n^2}{s^2 + \left(\frac{\omega_n}{Q_d}\right) s + \omega_n^2} \tag{2}$$

The control uses a current decoupling gain K_{d} that is usually selected as $L\omega_1$. It is also possible to incorporate another loop in which the voltage is feedforwarded via a gain (or transfer function) K_{f} in an attempt to decouple the current control loop from the rest of the system. However, in the base case of this paper, it has been selected a K_{f}=0 because, as shown in [18], the feedforward loop can easily lead to an infinite gain system depending on the electrical system parameters.

B. Main Delay Contributors

Apart from the elements mentioned above, there are other elements in the control structure of the inverter that are important to consider due to their delay effect. As it will be shown in Section IV, the delay plays a very important role in shaping the output impedance.

The first delay-contributor is the filtering of the signals before sampling (anti-aliasing filter). This procedure is represented by the transfer functions $G_i(s)$ (for the current) and

$G_v(s)$ (for the voltage) as shown in Fig. 2. In this paper, the effect of the anti-aliasing filters is omitted for simplification.

The second main delay contributor is the analog-to-digital (A2D) and digital-to-analog procedures (including the modulation block, MOD in Fig. 2). In here, it is considered that asymmetric modulation is applied, which means that the currents are sampled at $2f_{\text{sw}}$ and also the PWM block samples and holds the voltage reference created by the control in order to calculate the switching pulses at this rate. This procedure creates a time-delay of $0.75/(f_{\text{sw}})$ as shown in (3).

$$G_d(s) = e^{-s0.75/f_{sw}} \tag{3}$$

In this case, note that $G_d(s)$ is not an actual block in the control loop that will be implemented digitally. $G_d(s)$ is simply a mathematical representation of the analog-to-digital and digital-to-analog procedures (including modulation), which are approximated by a pure time delay. These procedures affect both the current (i_{abc}) and voltage (v_{abc}) signals; as both are sampled at a certain rate, both are fed into the control loop, and then both are used in order to construct a v_{ref} that is fed into the modulation block. Thus, the model is done in such a way as if the signal v_{ref} would go through the block $G_d(s)$, and the output of $G_d(s)$ would be the actual voltage signal generated at the terminals of the inverter.

In the end, it is important to realize that the transfer functions $G_d(s)$, $G_i(s)$ and $G_v(s)$ create a phase shift and an amplitude variation in the signals that changes with frequency and which can be observed in their bode plots.

It is possible to compensate for $G_d(s)$, $G_i(s)$ and $G_v(s)$ at a specific frequency (typically selected as the fundamental frequency, in here: $\omega_1 = 2\pi 50$ rad/s). In order to do that, it would be necessary to evaluate the gain and phase shift of these functions at 50 Hz and compensate them.

As in this paper only $G_d(s)$ is going to be considered, the gain does not need to be compensated because $G_d(s)$ is a pure time delay. It only creates a phase shift the signals that increases with frequency. The phase shift that needs to be compensated is the one that $G_d(s)$ presents at 50 Hz:

$$\theta_{comp} = \phi\left(G_d(s)\right)_{f=50} \tag{4}$$

which, for the base case parameters, is $0.094\,\text{rad} = -5.4°$.

A simple way to incorporate this delay compensation is to subtract a constant phase θ_{comp} in the dq to $\alpha\beta$ transformation, as shown in Fig. 2. This is mathematically equivalent to adding an extra block before the modulation such as:

$$G_{comp}(s) = e^{-j\theta_{comp}} \tag{5}$$

This means that the multiplication $G_d(s)G_{comp}(s)$ has zero phase delay at 50 Hz, but not at other frequencies.

C. Phase-Locked Loop (PLL)

In a 3-phase system it is straightforward to convert the abc voltages to the $\alpha\beta$-frame, where the phase angle is directly available. However, if the voltage phase angle was estimated in this way, the inverter would be vulnerable to all kinds of perturbations in the voltage (e.g. harmonics). That is why PLL structures with a feedback loop are usually incorporated. Of course, this has many advantages in terms of disturbance rejection capabilities, but this provokes that the PLL introduces its own dynamics into the system that need to be carefully analysed. That is to say, in practice, the positive and negative SRF do not rotate exactly at $+\omega_1$ and $-\omega_1$ (respectively) due to the PLL dynamics.

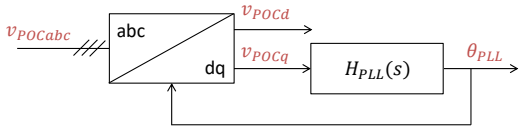


Fig. 3: Schematic of Synchronous Reference Frame PLL.

In this paper, a SRF-PLL is considered as in Fig. 3. The PLL compensator, $H_{\text{PLL}}(s)$, is a simple PI with an extra integrator as in (6). The closed-loop transfer function of the PLL is given by (7) [9], where V_1 is the amplitude of the AC output phase voltage in steady-state.

$$H_{\text{PLL}}(s) = \left(K_{\text{p-PLL}} + \frac{K_{\text{i-PLL}}}{s}\right)\frac{1}{s} \tag{6}$$

$$T_{\text{PLL}}(s) = \frac{H_{\text{PLL}}(s)}{1 + V_1 H_{\text{PLL}}(s)} \tag{7}$$

III. Output Impedance Analytical Modelling

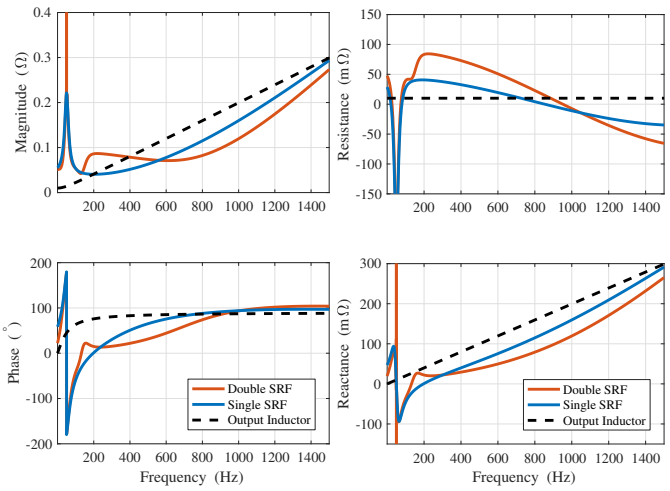
In order to model the inverter the theory of transfer matrices and complex transfer functions (i.e. transfer functions with complex coefficients) presented in [22] has been used.

The whole mathematical derivation is long and complex, and is not included in this paper due to space limitations. The detailed mathematical development will be included in a future article. The final and most important result, which is the focus of this paper, is the frequency-dependent impedance (Z_{inv}) that depends on the output inductor and the control parameters. The formula for this impedance is given in (8) (end of this paper) and its properties and how to shape it are investigated in Section IV.

IV. Sensitivity Analysis: Shaping the Output Impedance of the Inverter

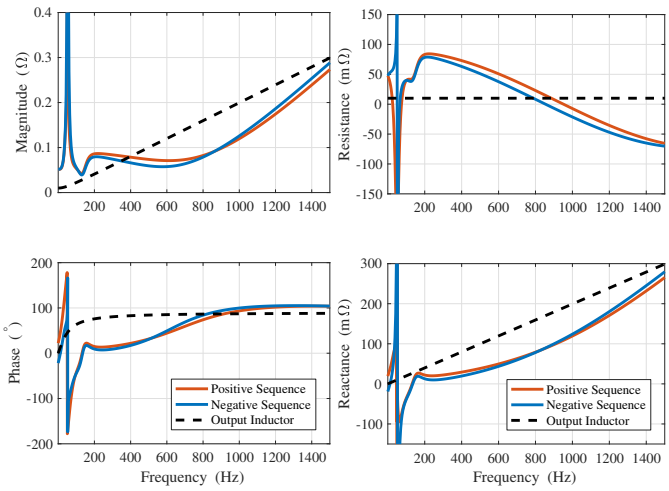
The sensitivity analysis of Z_{inv} is carried out with respect to the base case shown in Tables I–III. In the following figures, this case always appears in colour red.

Firstly, the output impedance of the inverter is compared between employing a single SRF and a double SRF (for the same parameters and design) in Fig. 4. As it can be seen, it is important to consider the exact type of control structure in order to develop an accurate small-signal model, as both control structures present very different frequency responses. In Fig. 4 (b) it is possible to see that the regions of negative resistance appear at similar frequency ranges (around 50 Hz and above 900 Hz approximately), but the resistance value



(a) (b)

Fig. 4: Output impedance comparison of single and double SRF control in the positive sequence (a) Magnitude and phase (b) Resistance and reactance.



(a) (b)

Fig. 5: Output impedance comparison of double SRF control in its positive and negative sequences (a) Magnitude and phase (b) Resistance and reactance.

is very different. An inverter with a double SRF structure is usually implemented because of its superior transient response during unbalanced conditions [14]; however, the fact that it presents a higher negative resistance (in absolute value, see Fig. 4 (b)) means that it would be more prone to instability.

Not only that, but considering or ignoring the PLL dynamics in the analysis of the dual-controller has an impact in the model. Note that, when analysing the formula for Z_{inv} (8), if the PLL dynamics are ignored (i.e. the impact of a voltage perturbation on the phase angle that outputs the PLL is neglected: $T_{\text{PLL}}(s) = 0$) then the output impedance of the inverter is a real transfer function (TF). That is to say, it is a TF that represents an element that behaves equally in the positive and negative sequences. In previous models available in the literature, in which the PLL dynamics were ignored, the same conclusion was reached [19]–[21]. However, when the PLL dynamics are included ($T_{\text{PLL}}(s) \neq 0$), this is no longer true. The impedance shown in (8) is no longer a real TF but rather a complex TF, and thus it behaves differently in both sequences. This is observed in Fig. 5.

The most noticeable difference between the behaviour of the converter in both sequences appears below 50 Hz, where the blue curve has positive resitance whereas the red curve has it negative. It is logical that the main differences between the sequences appear here, as these differences are due to the PLL dynamics, which has a bandwidth below 50 Hz.

Thus, it is concluded that taking into account the PLL dynamics when using a double SRF type of control is very relevant for studies in the low frequency range (for example, when studying Sub-Synchronous Resonances, SSR) but not so much in higher frequency ranges. For these ranges (i.e. above 100 or 150 Hz), the output impedance can be approximated as being equal in both the positive and negative sequences. This can greatly simplify the system-wide analyses in applications with a high population of PECs (like offshore wind farms).

As it can be seen in Fig. 5 (b), the impedance of the inverter has several regions of negative resistance behaviour. The model developed in this paper is an averaged model, so it neglects some of the converter dynamics that appear at frequencies higher than $f_{\text{sw}}/2$. That is why this model should be handled with care for higher frequencies than that. However, from now, in several figures the x-axis is going be higher than $f_{\text{sw}}/2$ in order to try to explain the behaviour of this negative resistance characteristic.

In the red curve in Fig. 6 (which is equal to the red curves in Fig. 4 and 5 but with a larger x-axis range) it can be seen that in the high frequency range the negative resistance has a periodic behaviour with a constant amplitude and phase (from now on, called "negative-resistance wave" for simplicity). The cause of this is the delay, as when the delay is ignored in the model, the impedance rapidly converges to such of the output inductor (although with higher resistance, see the blue curve in Fig. 6). Note that, the fact that an inverter with zero delay has no negative resistance region above approximately 100 Hz, means that the cause of the majority of the possible instabilities with inverters using a double SRF is the delay.

Further, it has been found that the period of this negative-resistance wave depends on how considerable the delay is. As the delay mainly comes from the sampling function of the current and the modulating block, and both are directly related to the switching frequency (see Section II-B), the switching frequency becomes the main parameter in determining the period of the negative-resistance behaviour (see Fig. 7 (a)). The higher the f_{sw} the smaller the delay is, and the longer the period of the wave is.

Note that, even if the period is significantly affected by

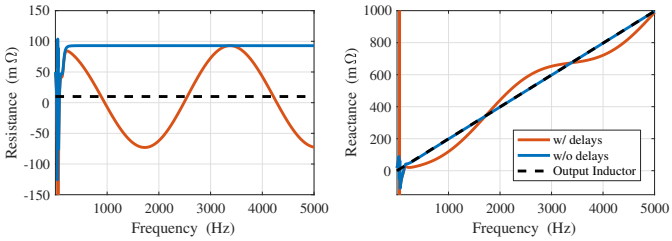
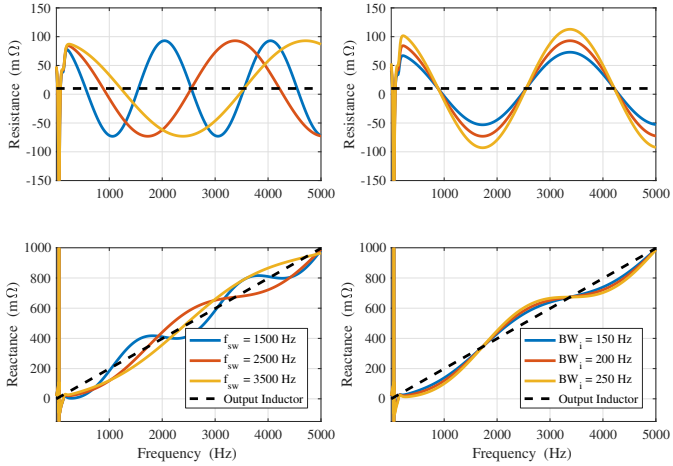


Fig. 6: Output impedance comparison of double SRF control when the delay is included or not (resistance and reactance).



(a) (b)

Fig. 7: Output impedance comparison of double SRF control with different (a) switching frequencies (i.e. delay) (b) current control bandwidth (i.e. PI constants).

f_{sw}, the amplitude of the "wave" remains constant (see Fig. 7 (a)). The amplitude depends on the current control bandwidth, as shown in Fig. 7 (b). Thus, it can be seen already that the existance of the negative-resistance wave is due to the delay, and that the amplitude and period of this wave can be controlled —and designed— independently.

Of course, there are other degrees of freedom like the frequency at which the anti-aliasing filter is tuned or whether to apply or not a compensation for the delay at 50 Hz. However, the most important degrees of freedom are the current control bandwidth and the switching frequency, as shown above.

V. Conclusions

This paper presents an impedance model for a 3-phase inverter that uses a double Synchronous Reference Frame (SRF) current control structure (i.e. dual current control). This model can be applied both in small-signal stability studies and in harmonic steady-state calculations.

In relation to the first application, the results show that considering a single or a double SRF control structure has a major impact on the severity of the stability-related negative-resistance regions. Thus, when modelling an inverter, it is crucial to consider which of these two types of control structures is implemented. That is why some previous literature has focused on developing models for both the single and double SRF structures. However, the impact of the PLL dynamics when considering the double SRF has been consistently ignored, which has produced symmetrical models that assume the same converter behaviour in the positive and negative sequence. In contrast, this paper includes the PLL dynamics in the analysis, which shows that the converter behaves differently in both sequences. Therefore, as opposed to previous practice with this control structure, this paper demonstrates that in small-signal stability studies with double SRF both sequences need to be considered separately. Fortunately, it has also been shown that the differences between the sequences can be ignored for certain frequency ranges (i.e. for $>$100 or 150 Hz), which significantly simplifies system-wide analyses.

In relation to the second use of the model, it is important to realize that, from a system perspective, the magnitude of the harmonics in the system depends both on what the harmonic sources are and on how these harmonics are amplified or reduced through the impedance network. When designing an inverter for harmonic compliance only the first issue is generally considered (i.e. the converter as a source). However, the impedance of the inverter influences the total impedance network of the system, thus having an effect also on the amplification/reduction of harmonics. Acknowledging this, what this paper offers is a closer analysis of how certain control parameters/designs may affect the converter impedance and thus the amplification or reduction of harmonics. This is very important because, for example, it is generally believed that the switching frequency should always be as high as possible to improve harmonic performance. However, this is the case only when the converter output harmonics alone, as a source, are analysed. This paper shows that the switching frequency has also a major impact on the output impedance of the converter, which affects the amplification network. Therefore, it could be the case that, in sizeable systems in which the harmonic amplification is very significant due to high values at certain frequencies (e.g. HVAC-connected offshore wind farms), increasing the switching frequency actually results in a higher harmonic content from the system perspective. Of course, this possibility has to be analysed case by case depending on the rest of the system. In order to do that, however, the first step is to know to what extent the impedance of the converter can be shaped.

As a consequence, this paper presents a sensitivity study on the output impedance. The study shows that the location of the (positive and) negative resistance frequency ranges and the magnitude of the resistance within them can be designed separately. The frequency ranges depend mainly on the modulation technique and on the switching considerations, whereas the resistance magnitude in these regions depends mostly on the current control bandwidth.

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$$
\begin{aligned}
Z_{inv} = \Big(& Ls + R_L + \left([H_i\left(s - j\omega_1\right) - jK_d] H_n\left(s - j\omega_1\right) + [H_i\left(s + j\omega_1\right) + jK_d] H_n\left(s + j\omega_1\right) \right) G_i(s) G_d(s) G_{comp}(s) \Big) \\
& \Bigg(1 + \left(H_n\left(s - j\omega_1\right) K_f\left(s - j\omega_1\right) G_v(s) + H_n\left(s + j\omega_1\right) K_f\left(s + j\omega_1\right) G_v(s) \right) G_d\left(s\right) G_{comp}(s) + \\
& \Big(- I_1 e^{j\phi_{i1}} [H_i\left(s - j\omega_1\right) - jK_d] H_n\left(s - j\omega_1\right) - I_1 e^{j\phi_{i1}} (L\omega_1 j + R_L) - V_1 + V_1 H_n\left(s - j\omega_1\right) K_f\left(s - j\omega_1\right) G_v(s) \\
& + I_1 e^{j\phi_{i1}} [H_i\left(s + j\omega_1\right) + jK_d] H_n\left(s + j\omega_1\right) - V_1 H_n\left(s + j\omega_1\right) K_f\left(s + j\omega_1\right) G_v(s) \Big) \frac{T_{PLL}\left(s - j\omega_1\right)}{2} G_d\left(s\right) G_{comp}(s) \Bigg)^{-1}
\end{aligned}
\tag{8}
$$

TABLE I: Main parameters of inverter (base case)

	Description	**Value**	**Unit**
$V_{\mathbf{dc}}$	DC Voltage	1200	V
$V_{\mathbf{POC}}$	Line-to-line AC Voltage	690	V
$P_{\mathbf{rated}}$	Rated Power	4.3	MW
L	Output Inductor	31.71 (0.1)	μH (p.u.)
$R_{\mathbf{L}}$	Resistance of Output Inductor	0.01	Ω

TABLE II: Operating point considered (base case)

	Description	**Value**	**Unit**
I_1	Output Current	5.09	kA
$\phi_{\mathbf{i1}}$	Angle difference between Current and Phase Voltage	0	°

TABLE III: Control parameters of the inverter (base case)

	Description	**Value**	**Unit**
$f_{\mathbf{sw}}$	Switching Frequency	2500	Hz
$f_{\mathbf{s}}$	Sampling Frequency	5000	Hz
$K_{\mathbf{d}}$	Current Coupling Compensation Gain	0.01	Ω
$K_{\mathbf{f}}$	Voltage Feedforward Gain	0	V/V
$K_{\mathbf{p}}$	Proportional Constant PI Current	0.04	Ω
$K_{\mathbf{i}}$	Integral Constant PI Current	12.6	Ω/s
$\mathbf{BW_i}$	Current Control Bandwidth	200	Hz
$K_{\mathbf{p\text{-}PLL}}$	Proportional Constant PI PLL	0.3	rad/s
$K_{\mathbf{i\text{-}PLL}}$	Integral Constant PI PLL	15.3	rad/s^2
$\mathbf{BW_{PLL}}$	PLL Control Bandwidth	30	Hz