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Nanofabricated tips for device-based and double-tip scanning tunneling microscopy

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NANOFABRICATED TIPS FOR DEVICE-BASED AND DOUBLE-TIP SCANNING TUNNELING MICROSCOPY

NANOFABRICATED TIPS FOR DEVICE-BASED AND DOUBLE-TIP SCANNING TUNNELING MICROSCOPY

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus Prof.dr.ir. T.H.J.J. van der Hagen,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op donderdag 20 februari 2020 om 12:30 uur

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Keywords: scanning tunneling microscopy, nanofabrication, double-tip, local gate

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INTRODUCTION

Parts of this chapter have been published in Nanotechnology **30(33)**, 335702 (2019) [1].

1

Scanning tunneling microscopy (STM) is a leading tool for probing electronic and topographic information at the atomic scale [2]. Since its inception a few decades ago, data quality has dramatically improved by focusing on mechanical stability, tip preparation and lower temperatures [3–5]. New possibilities have emerged and greatly extended the range of STM, including quasi-particle interference studies with density of states mapping [6–10], spin-polarized STM [11, 12], scanning Josephson spectroscopy [13–15] and ultra-low temperature operation [3, 16, 17].

The majority of these new techniques have been achieved by relatively subtle -yet challenging- changes in the measurement apparatus. Many rely on three main improvements made over the years e.g. increased stability, lower operating (and electron) temperatures [3–5] and improved electronics. However, the scope of physical properties that can be probed by STM has mainly improved by changes to the tip itself. For example people have introduced spin-polarized tips to conventional STM to make it sensitive to spin orientation at the atomic scale [11]. Although additions like these seems subtle from a hardware point of view, development of these techniques has taken years and it has resulted in a new branch of STM based research. The emergence of scanning Josephson spectroscopy follows along that same path; it utilizes a superconducting tip, often made by dipping it into a superconductor or picking up a flake of high-T_c superconductor, to create a superconductor-insulator-superconductor junction and spatially map the superfluid density [13–15]. These two techniques exemplify to large extent the inventiveness of the STM community to probe new branches of physics at the atomic scale without large changes to the instrument itself by innovations at the tip.

New techniques such as pump probe STM [18], electron spin resonance STM [19] and scanning noise spectroscopy [20–24] change the instrument beyond just the tip. Here the microscope is typically equipped with special cables for low attenuation throughput of high frequency signals. In the case of scanning noise spectroscopy the authors implemented a cold MHz amplifier based on a LC resonant circuit only few tens of centimeters from the STM junction to probe shot noise at the atomic scale [20, 21]. It turns out the capacitance of the coax cable from the tip to the amplifier fundamentally limits the bandwidth that can be achieved and forces the circuitry close to the tip (the low temperatures also make a critical impact).

We not only observe a shift towards adding functionality to conventional STM, we also see the additions are often moved close to the tip. Furthermore, we notice a shift that moves our view from a simple tunnel junction towards either a highly tunable Josephson junction (in case of superconducting tip and sample) or an interesting impedance as a part of a larger circuit. More challenging and perhaps longer term visions for STM have emerged very recently and they draw on a closer link to the ever growing field of quantum computing/sensing. The first example is to exploit a Majorana bound state living on the end of a one-dimensional semiconducting nanowire for the (local) detection of odd-frequency superconductivity [25]. The second is a newly proposed technique to use a superconducting charge qubit coupled to a tip to resolve tiny temperature and resistivity changes with the high spatial resolution provided by STM [26].

Here we want to add experimental prowess to visions like these and invite further ingenuity to the field. Therefore, we introduce a platform for bringing device-based functionality to STM, with the aim to utilize decades of progress in device engineering for the

field of scanning probes. We replace the conventional electrochemically etched, pointy metal wire with an integrated metal tip on a silicon chip. This new platform, which we call smart tip, allows in principle to directly add additional capabilities to a STM tip, including novel spin-sensitivity, local heating, local magnetic fields, local gating, high-frequency compatible coplanar waveguides, qubits, and double-tips. However, it is *a priori* unclear whether a nanofabricated tip will function for STM measurements, as several challenges arise: the stability needs to be below the picometer scale, stringent requirements exist on the shape and sharpness of the freestanding tip, and contamination from fabrication residues need to be absent. In the first half of this thesis, we demonstrate the feasibility of nanofabricated tips and the novel smart tip platform. We first discuss our newly developed fabrication procedure and then experimentally show the functionality of these tips in standard STM measurements.

The challenge in realizing smart tips is to make devices that are fully compatible with conventional STM, yet allow for compatibility with standard nano- and microfabrication processes. Specifically we need: (i) a clear protrusion of the tip relative to the underlying chip, (ii) precise control of the tip shape, and (iii) reliable, reproducible fabrication recipes. To meet these requirements, we developed a new fabrication method using suspended silicon nitride (SiN) tips covered with gold to create on-chip STM smart tips.

DOUBLE-TIP STM

A large part of this thesis describes our attempt to use the platform we introduced above to develop a double-tip STM that can be integrated in regular commercial STM systems. Double-tip STM, where two tips are brought into tunneling simultaneously to probe electron correlations within a few (tens of) nanometers, has been a long standing dream of scanning probe microscopy. However mostly due to the many technical challenges it has not gained much traction since its inception in the nineties of the last century. Much of the effort to the experimental realization of the double-tip STM has come from the multi-probe community that mostly focuses on studying resistance properties in mesoscopic systems on (sub)micrometer length scales by contacting the surface with two, three or, ideally, four probes. To large extent a double-tip STM with few nanometer probe separation operating in the tunneling regime is a natural goal to which their tools will evolve [27, 28].

Similar to conventional STM, multi-probe STM's are commercially available and mostly rely on four individually (piezo) driven STM and an additional scanning electron microscope (SEM) for navigation. Both do not benefit the mechanical stability that is so important to (spectroscopic imaging) STM and increase the complexity of the microscope significantly. However steady progress in stability [29] and control of the tips [30] has resulted in tip-to-tip distances down to 30 nm and the first double-tip transconductance (see Ch. 5) measurement to date [31].

In this thesis we start with a different approach that is aimed at overcoming some of the challenges double-tip STM faces. Our goal is to expand the use of our smart tip platform to create on-chip double-tip devices and directly implement them into a commercially available STM head. The most immediate challenge is the fabrication of the device and minimize the tip-to-tip distance. Given the joined nature of the tips we avoid part of the navigation problems and we thereby eliminate the use of an SEM column and

make them compatible with ultra-stable compact Pan type STM heads widely used for single tip experiments. Lastly we conclude with a discussion of the two main trade off that comes with our approach: reduced degrees of freedom and getting two fixed tips into tunneling requires tilt.

STM WITH A LOCAL GATE

Interestingly, a new opportunity appears to use the double-tip devices for STM with a local gate also known as scanning gate spectroscopy [32]. The idea is conceptually straightforward, one probe acts as a normal STM tip while the other provides locally a strong electric field to induce or deplete carriers at the surface (under the adjoined tip). We are primarily interested in the application of such a technique on quantum materials such as (doped) Mott insulators or twisted bilayer graphene (TBLG). The concept of using scanning gate spectroscopy on quantum materials is appealing for two main reasons. First it will likely yield a more straightforward experiment compared to double-tip STM since we only need one tip in tunneling range. Second, simultaneous gating of quantum materials while studying the surface using STM proves challenging in some cases.

We will explore in detail the requirements and sample choices we need to make in Ch. 6. From the outset the obvious candidates will be materials with relatively low carrier density (at the surface) as a fully metallic surface will perfectly shield the electric field impose by the gating tip. Many low carrier materials such as Mott insulators at low doping, (twisted bilayer) graphene and (2D) semiconductors will be interesting to study. The latter two can in principle incorporate a bottom gate electrode as the are fabricated on a chip that contains contacts to the flake/thin film. Yet often obtaining a clean surface for STM after fabrication is challenging and may require annealing under ultra-high vacuum (UHV) conditions. Mott insulators (at low doping levels) can also be grown on insulating crystal substrates and contacted with lithographically defined top contacts but several problems arise. In-situ cleaving generally does not work for these samples and sample transfer from the growth chamber to the STM has not (yet) lead to overwhelming amount of new high quality data on these systems, despite efforts using UHV suitcases and the development of combined molecular beam epitaxy (MBE)/STM systems. Furthermore, the fabrication of a back gate on these crystalline materials proves difficult. The (thin) films generally grown using pulsed layer deposition (PLD) or MBE require meticulous matching of film and substrate lattices, especially for extremely thin films most suited for a back gate [33]. Ionic liquid based top gates have been successful in tuning the doping level to similar degree as chemically doped samples [34], but it is not always clear whether the gating is purely electrostatic or caused by oxygen displacement [34]. Also, ionic liquid gating is not suited for STM.

In short, we see that electrostatic (back) gating of Mott insulators proves difficult in combination with STM. Perhaps the most difficult would be the doped Mott insulator $(Sr_{1-x}La_x)_2IrO_4$ that requires cleaving at low temperatures to obtain an unreconstructed, atomically flat and clean SrO terminated surface [35]. In this thesis we aim to briefly explore the possibility of local gating using our second tip with this material in mind. Beyond the difficulty of traditional gating on this material there are several other reasons that make it interesting. As a result of the insulating behavior at low chemical doping bending of the electron bands has already been observed and modeled using the dielectric character of the material [36]. From a physics point of view the iridates are

proving very insightful in the understanding of the emergence of high-T_c superconductivity in doped Mott insulators. They show remarkable resemblance to the well-studied cuprates while chemically very different, meaning that if superconductivity is found in the iridates it would be a consequence of the doped Mott state and not exclusive to copper oxide planes. To observe the potential superconductivity in $(Sr_{1-x}La_x)_2IrO_4$ it requires a higher doping level that so far has been beyond the reach of crystal growers and therefore we are interested in exploring if our tip based gate can play a role here.

THESIS OUTLINE

In this thesis we present a new kind of tip for scanning tunneling microscopy by fully incorporating a metallic tip on a silicon chip using newly developed fabrication techniques and demonstrate its performance. We then explore the potential of additional functionality to the tip with the main focus on double-tips and its applications for studying quantum materials.

In Chapter 2 we describe in detail the challenges overcome to create the novel smart tips and the final fabrication process. The tips we create in this chapter are single tip devices without any additional features and where the full chip acts as a contact pad. These are the tips that we test in Chapter 4.

Chapter 3 is dedicated to the development of a new, homebuilt low temperature scanning tunneling microscope. Although the smart tips can by implemented in (existing) commercial systems, we built a dedicated microscope that is ideally suited for the implementation and testing of the new tips.

Chapter 4 consist of a series of proof of principle experiments to confirm that many of the building blocks are in place to create a fully functioning double-tip STM. First we demonstrate the performance of the smart tip in a commercial STM and test in-situ tip preparation methods. Second we test the homebuilt STM's performance by scanning on atomically flat Au(111) and analyzing the noise at the tunnel junction. Last we approach again a Au(111) surface with the double-tip devices we develop in Chapter 5, in an attempt to get good quality data using one of the two tips. This would be a big step towards a working STM with a local gate that we explore in Chapter 6.

In Chapter 5 we take an important step towards a fully functioning double-tip STM by extending the fabrication procedures of Chapter 2 to incorporate two probes separated by only few tens of nanometers. In addition we outline the challenges to get two fixed tips into tunneling simultaneously that still stand.

In Chapter 6 we propose and explore the possibility of using the double-tip devices for STM with a local gate. Here only one tip needs to be in tunneling and the other is used to locally induce or deplete charge carriers at the surface. This yields a more straightforward experiment and seems most suited for crystals that require in-situ cleaving and have low carrier densities.

Chapter 7 provides the main conclusions of this thesis together with an outlook on the potential future application of the smart tip platform for high frequency STM in the GHz regime. As a final note we argue that upscaling the fabrication to full waver processing should be straightforward and may help to push smart tips towards the mainstream.

1

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2

FABRICATION OF SMART TIPS

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2.1. INTRODUCTION

In order to introduce our platform for bringing device-based functionality to STM, we aim to use modern nano- and microfabrication techniques presented here to replace the conventional electrochemically etched, pointy metal wire with an integrated metal tip on a silicon chip. This new platform, which we call smart tip, allows in principle to directly add additional capabilities to a STM tip, most of which we briefly mentioned in the previous chapter.

As stated before, the main challenge in realizing smart tips is to make devices that are fully compatible with conventional STM, yet allow for compatibility with standard nano- and microfabrication processes. Specifically we need: (i) a clear protrusion of the tip relative to the underlying chip, (ii) precise control of the tip shape, and (iii) reliable, reproducible fabrication recipes. To meet these requirements, we developed several fabrication methods each with their own advantages and limitations. Over the course of this chapter we learn about the challenges and, with each new fabrication method, we improve and often simplify our process to finally arrive at the devices we test in Ch. 4.

The first and perhaps most intuitive method (Sec. 2.2.1) is based on the cleaving of a silicon chip to create a pointy chip where the tip overhangs at the apex of the chip. In Sec. 2.2.2 we look at tips made out of tungsten that are brought to and over the edge of the chip by using a through wafer silicon etching process called a Bosch etch. Finally we describe a newly developed fabrication method using suspended silicon nitride (SiN) tips covered with gold to create the on-chip STM smart tips in Sec. 2.3. They prove to be both flexible and fast to make. These are the tips that we present in Sec. 2.3.6 and extensively test in Ch. 4.

2.2. TOWARDS ON-CHIP STM TIPS

We aim to create a silicon chip that carries a protruding metal tip. Not only does the tip need to be very sharp to make it capable of resolving atoms, we also want to avoid accidental touches of the chip to the sample. Therefore we like to control the shape of the chip as well; ideally we create a pointy chip with the tip overhanging the apex of the chip. There are numerous ways to create a pointy chip, several will be discussed in this chapter.

2.2.1. CLEAVED TIPS

The most elementary approach is to use the crystal structure of the silicon to our advantage. By simply cleaving the Si along a crystal axis we should be able to create a very well defined and clean break, leaving smooth sidewalls. This technique is often used to (i) break pieces too large to dice or that leave toxic residue such as iii-v materials, (ii) create sidewalls smooth enough to act as mirrors facets in diode lasers [2], (iii) create flat and clean surfaces for scanning probe microscopy when cleaved in ultra-high vacuum [3].

In fact, two examples utilizing cleaved chips to create chip based STM tips have been recently been reported. The first example is a InAs nanowire glued onto the corner of a chip. The chip used there is a square piece of cleaved GaAs [4, 5]. In the second example the authors used a cleaved glass chip coated with a metal layer. The pointy edge of the chip where the two cleave lines meet is so sharp that chip itself can even be used to

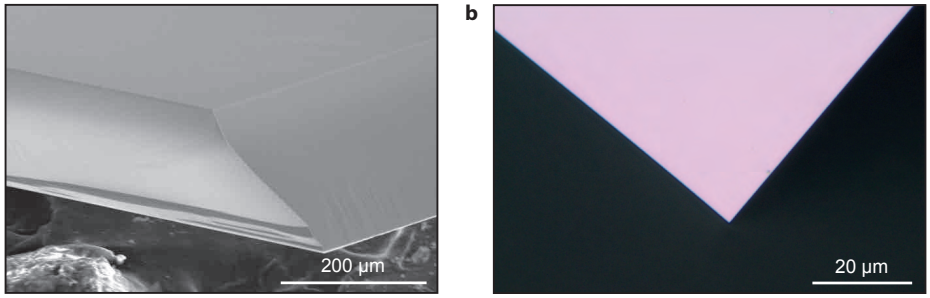

Figure 2.1: **a** SEM image of a cleaved Si(100) chip. The two cleaved planes meet in the center of the image. **b** Top view optical image of a similarly cleaved Si(100) chip.

successfully perform the STM measurements [6].

Fig. 2.1 shows two examples of a cleaved Si(100) chips where cleave lines along [110] and the orthogonal [1$\bar{1}$0] axes meet in a point. We cleave the chips by making a small scratch with a diamond cutter on the edge of the chip, holding sharp pair of metal tweezers under the scratch and pressing down with different set of soft tip tweezers on either sides of the chip, such that the cleave line travels through the material along the crystal axis and we do not get residue from the scratch on the center of the chip. From the top the cleave lines look very straight and the apex of the chip very sharp. The inclined view from in the SEM image shows that the cleavage planes can have varying slopes indicative of competing (111) and (110) planes as natural cleavage planes [7].

The chips shown in Fig. 2.1 are promising, they show that one can create a sharp apex of the chip, but whether the top or bottom of the chip has the foremost apex remains unpredictable. This can clearly been seen in Fig. 2.1a. In addition, for future fuctionalization of the tips we require full control over the tip shape and we aim to achieve that by including electron beam lithography to define our tips. The tip we define needs to be exactly aligned with the apex of the chip and protrude from there. This turns out the be the major complication of cleaving (by hand) independent of the chosen material. The alignment accuracy that needs to be ~10 μm is even challenging to achieve with a dedicated tool, where the cleave line is aligned using a sufficiently powerful microscope and precision stage [8].

In summary, although using cleaving to create the appropriate chip shape seems clean and simple, it lacks reproducibility and accuracy without a dedicated and capable tool that is not available here.

2.2.2. DEEP ETCHED SMART TIPS

INTRODUCTION TO BOSCH ETCH

Given the limitations of cleaving we proceed to explore the use of Deep Reactive Ion Etching (DRIE). DRIE is a highly anisotropic plasma etch that can create deep etches in silicon at a high etch rate and with excellent directionality [9]. The latter makes is very well suited for high aspect ratio structures and it has to ability to create very straight sidewalls. The high etch rate of typically 5 μm/min allows through wafer etches within

reasonable time. Here we use it to cut out the chip we define by a mask layer on top. The main benefits are the straight, smooth sidewalls, the ability to cut out many chips at once with great precision and (therefore) reproducibility.

The type of DRIE we perform here is also called Bosch process or Bosch etch and it usually performed without any cryogenic cooling but rather between T=-10°C and T=20°C. The Bosch etch creates the anisotropy by a alternating between plasma pulses based on two gasses. The first pulse, the longer one, chemically etches the silicon at a high rate using a plasma formed from SF_6 gas. The etcher used here is inductively coupled meaning that the plasma is formed by a coil around the main chamber that creates an oscillating magnetic field that induces an electric field to circulate the plasma. The inductively coupled plasma (ICP) power used to create the ions for the chemical etching mostly sets the number available ions. The two capacitor plates used in traditional Reactive Ion Etching (RIE), that is often used by itself to create a plasma using an oscillating electric field between the plates, are primarily used to control the momentum of the ions that is important for mechanical etching, this is set by the DC bias [10].

The second pulse deposits a passivation layer. For this shorter pulse the SF_6 gas is replaced by C_4F_8. The plasma now isotropically deposits a protective layer on both the etched silicon and the mask. The physical bombardment of the accelerated ions, the mechanical etching, is very directional and removes the passivation layer only in the bottom of the trench created before. The newly exposed silicon is then chemically etched again by the next SF_6 step. Upon repetition this creates very deep, straight etches. Balancing the etch step and the passivation step is of crucial importance to the profile of the etch and the etch rate of the mask [9].

In this section we will present fabrication schemes, each with their own advantages and disadvantages, all using DRIE to cut out the chip. The first is an initial attempt to create a metallized overhanging structure without the use of electron beam lithography to define the tip shape: the sharpness is merely determined by the thickness of the film in combination with the sharpness of the chip shape that follows the DRIE mask layer. In the second scheme, developed in parallel with the first, we do incorporate EBL to create a sharp metal tip and subsequently try to suspend it.

PLANAR TUNGSTEN TIPS

The most important part of the fabrication process at this stage is the creation of overhang. To start off simple and properly test the DRIE process we first proceed with the fabrication of a planar tip made out of tungsten covered SiN and plain tungsten respectively. Planar means the tip consists of a sheet of material that overhangs and its sharpness, as seen from top, is determined by the shape of the chip as shown in Fig. 2.2.

We start with a 200 μm thick Si(100) chip covered on both side with 194 nm high stress LPCVD SiN (Fig. 2.2a). Here we choose to deposit a tungsten film, because it is traditionally often used for STM tips and more importantly it can be etched by SF_6 gas that is also used for etching through the chip. We deposit the tungsten layer by RF sputtering at 150W in an Alliance AC450 for 90 s to obtain a film thickness of 50 nm (Fig. 2.2b). We define the shape of the chip using optical lithography for which we first spincoat a 6 μm thick layer of AZ9260 photoresist (we spin at 5500 RPM and bake at 110°C for 230 s), see Fig. 2.2c. This may seem very thick but the etch needs to be long in order to go through the full 200 μm thick chip.

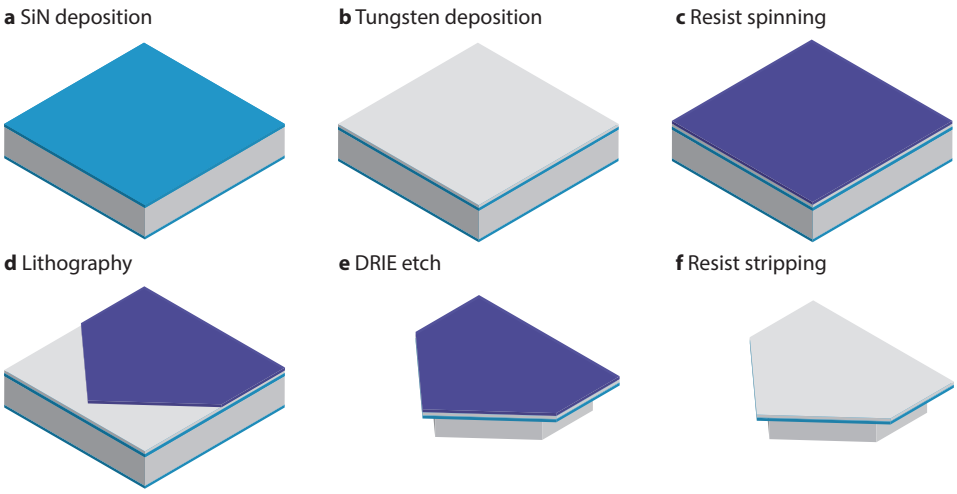

Figure 2.2: Overview of fabrication steps for the planar SiN supported W tips. Note: The bottom layer of SiN is omitted starting at (e), the layer is still there, however after the Si etch any protruding SiN at the bottom is removed by (the removal of) the adhesive oil applied before the etch.

For the exposure we use a DMO ML-2 laser writer, which uses a scanning laser with a wavelength of 375 nm instead of an UV lamp in combination with a mask. The maskless process allows us to change the design rapidly without having to order/produce a mask for every iteration. The laser beam is 1 μm wide and takes 1 μm steps with a dose of 600 mJ/cm^2. The development typically takes place is a 1:3.5 mixture of AZ400K:H2O for 3 min and is stopped by immersion in water for 60 s.

The chip we aim to cut out is now covered by photoresist and the area around it consists of exposed tungsten on top of SiN (Fig. 2.2d). Here we use the DRIE to etch through all layers in a single etch (Fig. 2.2e). The tungsten is only 50 nm thick and etched well by SF_6 plasma [11]. Etching the SiN will be less efficient, but works [11]. We start by placing the chip on a silicon carrier wafer with a drop of oil under the chip for thermal anchoring. The 4 inch carrier wafer is required to load chips into the etcher. To prevent the carrier wafer from being etched they are coated with 4.3 μm SiO_2, dramatically extending their lifetime due to the low etch rate of SiO_2. The etch itself consists of a 40-45 min sequence of alternating pulses, a 7 s SF_6 etch (flow 200 sccm, source power 2000 W, DC bias 60 W) followed by a 2 s C_4F_8 passivation step (flow 100 sccm, others the same), all at T=10°C. In addition to etching straight down through the chip, the DRIE also creates an overhang of the SiN/W planes of 1 μm with these settings (Fig. 2.2e).

The last step before we obtain the final device is resist removal (Fig. 2.2e). Submerging the chips in heated acetone at 45°C for 30 min does not seem to completely remove the resist layer, but rather leave thin sheets of residual resist on the chip. Prolonged exposure to N–Methyl–2-pyrrolidone (NMP) at 80°C for 60 min does fully remove the resist layer in the majority cases, but cleanliness remains a concern. To wash of the NMP and dry the chips when we take them out we dip them twice in IPA and blow dry them with

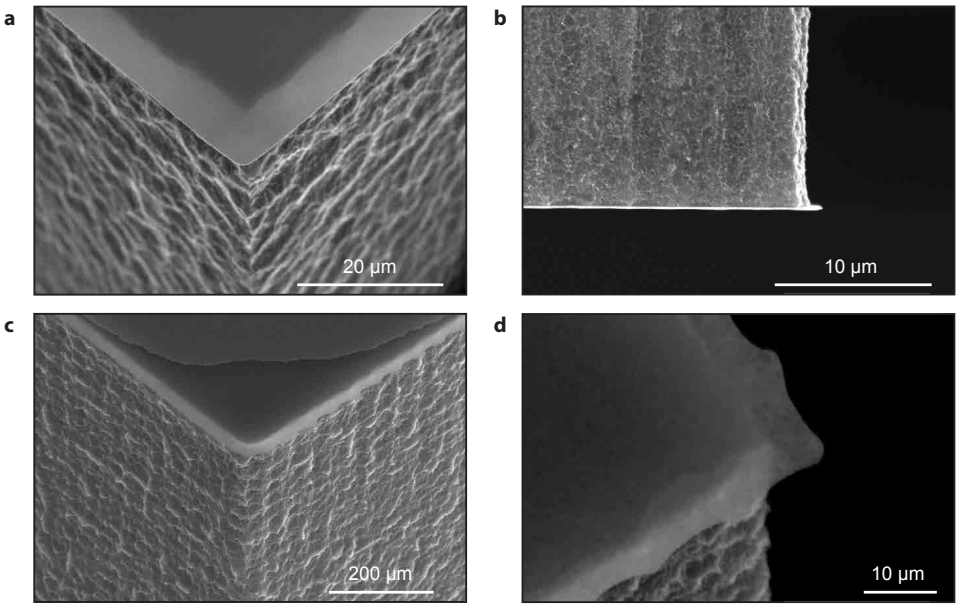

Figure 2.3: SEM images of the SiN supported W planar tips. **a** The apex of a successfully fabricated tip where the light gray parts are the overhanging SiN/W. The overhang measures 6.5 μm perpendicular to the side of the chip. **b** Side view of a suspended device to show the straight silicon sidewall and the overhang created by the Bosch process. **c** Similar to (a) but here the tungsten has retracted while the SiN seems unaffected. **d** Planar tungsten tip made by almost identical fabrication process but without the layer of SiN under the tungsten.

N_2 gas.

Fig. 2.3 shows examples of the resulting devices. In Fig. 2.3a we show the device we set out to create: clear overhang of the SiN/W plane and nicely etched Si sidewalls, further demonstrated in Fig. 2.3b. Note that the sharpness of the plane and its waving sides (Fig. 2.3d) are a result of the profile created by the lithography. However using (nearly) identical process we also obtained devices where tungsten layer seems to be removed in the last ~8 μm from the apex as shown in Fig. 2.3c. At first hand the most likely explanation is the lack of resist at the very end of the process, but the resist layer is 6 μm thick, whereas a typical Bosch etch requires ~ 4 μm. We present another interesting observation in Fig. 2.3d, where we use an almost identical fabrication process but starting with a bare Si chip without any SiN. Again the overhang is created by the Bosch etch using SF_6 gas, indicating that the SiN plane is not per se necessary to protect the tungsten and that the W can in fact survive exposure to the Bosch etch. Another hypothesis would be that the Bosch etch has difficulty etching through the SiN layer and affects the W laterally. If that is indeed what happens we could use a succession of dedicated etches: an SF_6 based W etch, an CF_3 based SiN etch and lastly the Bosch etch.

In conclusion, we have seen that planar W tips can in principle create workable devices, but come with complications: (i) even though their planar nature makes them intrinsically (somewhat) sharp, we do not have control over the tip shape at the nanoscale,

(ii) extending to device based STM will require additional steps that we show in Sec. 2.2.2 and, (iii) proper removal of the resist, attacked by the long etch, appears hard and that raises concerns about the cleanliness of the tips.

SiN SUPPORTED TUNGSTEN TIPS

In order to move towards device based STM tips that include more complicated patterns such as two tips or on-chip circuitry, we strive for the ability to lithographically define the tips. To achieve this at the such a small length scale we use electron beam lithography to define the metal tips and contact pads. The fabrication is an extension of Sec. 2.2.2, where we replace the deposition of tungsten on the full chip (Fig. 2.2b) by a contact pad and an increasingly narrow line that will become the tip as shown in Fig 2.4.

The metal tips are created by a liftoff process where we spin on a layer of ARP-6200.09 resist (baked at T=150°C for 3 min), write the structures with an electron beam (the spot size is 29 nm, beam step size 2.5 nm and the dose 320 $\mu C/cm^2$), deposit the tungsten and lift off the non-exposed parts by dissolving the resist in NMP at T=80°C for over 60 min while stirring. Next we will proceed to create the final chip shape, again following (Fig. 2.2). Only this time we need to carefully align the chip mask to the tungsten tip

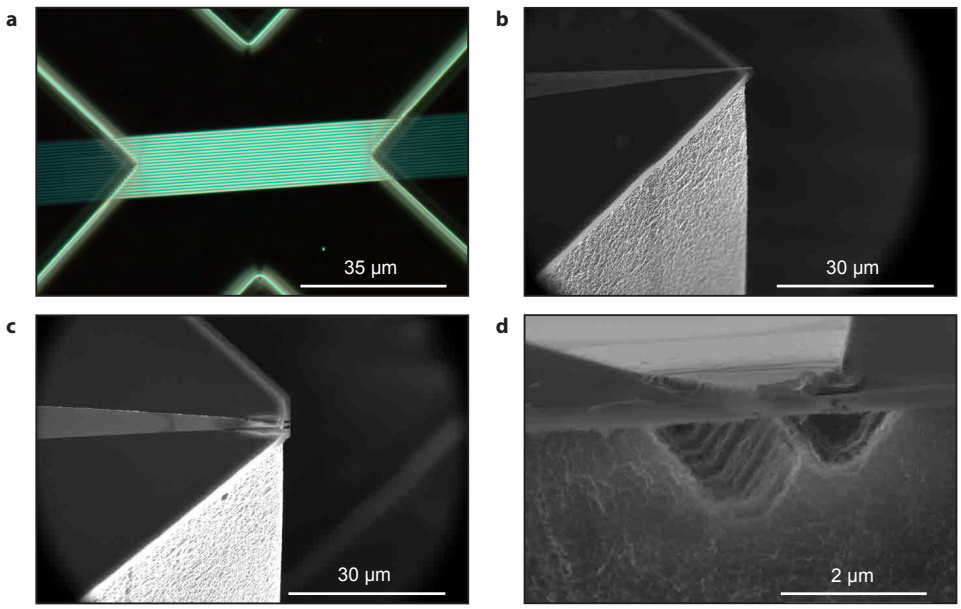

Figure 2.4: **a** Optical microscope (dark field) image of a mask alignment test on several closely packed lines etched into SiN. Although the mask is centered quite well on the lines, a slight tilt is still clearly present. **b** SEM image of a lithographically defined tungsten tip supported by a SiN sheet. The overhanging SiN sheet is almost transparent and the tungsten line is gray. Notice the alignment is off by about a micron. **c** Top view SEM image of a device similar to (a), but here the Bosch etch damaged the silicon, SiN and tungsten along the edges of the tungsten structure. (d) SEM image perpendicular to the tip shown in (c) clearly shows the damaged SiN and the etch extending into the silicon as well.

to ensure the tip is at the apex of the chip. The laser writer has the ability to align to markers using either and optical microscope (magnification of 40 x plus 4x digital zoom) or a laser microscope (magnification of approx. 200x), however it proves difficult to align with a precision smaller than 2 μm. It can also occur that the rotation is not corrected for properly like in Fig. 2.4a. Therefore the tips do not always align perfectly to the apex of the overhanging SiN sheet but slightly next to it, e.g. in Fig. 2.4a,b,c.

Fig. 2.4b shows a somewhat successful device where the tungsten tip does extend all the way to the edge of the chip, albeit the alignment is still slightly off. In case it is successful the metal tip can be the foremost point that provides the tunneling, to be sure it is we will place the tip under a small angle, but more on that in Ch. 3. If necessary a short dip in a HF solution can help to make the tungsten protrude by etching the SiN. Note that this way the overhang of can never be more that the thickness of the SiN and thinning down the SiN may create additional complications such as bending or reduced stability. In some cases the metal does not fully extend to the edge of the SiN sheet and is outside of the <200 nm range where we can retract the SiN with HF. Here again the tungsten near the edge is slightly etched.

Another complication is shown in Fig. 2.4c,d. We notice that along the sides of the tungsten line the tungsten, SiN and underlying silicon are etched. This comes as a surprise since the tungsten, a material that can be etched by the SF_6 plasma, is protected by the resist on top and the SiN on the bottom. Even if the SF_6 makes it through from the side it should barely etch SiN like we observe here due to the lack of mechanical etching. While the origin of this behavior remains mysterious we made the following observations: (i) we tested several tungsten widths and narrower lines are more affected, (ii) it may well be connected with the withdrawal of tungsten in Sec. 2.2.2 and (iii) it occurs frequently.

In conclusion, using lithographically defined tungsten tips that are supported by a SiN plane yields very mixed results and comes with challenges that seem hard (but not impossible) to overcome and of which the nature is, at this moment, not always clear. Implementing a dedicated SiN etch instead of a Bosch etch through all layers may drastically improve the yield of the process in the future. However in the next section we move to a more simple fabrication scheme where we shape the SiN and put the metal on the chips at the very last, thereby avoiding the problems that occurred here.

2.3. FABRICATION OF SiN BASED SMART TIPS

2.3.1. OVERVIEW

Reading through the previous sections it becomes apparent that the two methods described each have their limitations. While the use of cleaving is fast, clean and elegant, it is very difficult to align the sharp apex of the chip to where the tip structure is defined. In addition, to get the chip in the exact shape needed and not only following the crystal structure of the material, one would need additional dicing step to further shape the chip to easily fit in the STM (depending on the tip holder design).

In this work we aim to make these tips a platform for potential applications and therefore we want to be able to lithographically define a variety of tip shapes and bring them to and over the edge of the chip. The Bosch etch method, where we etch through

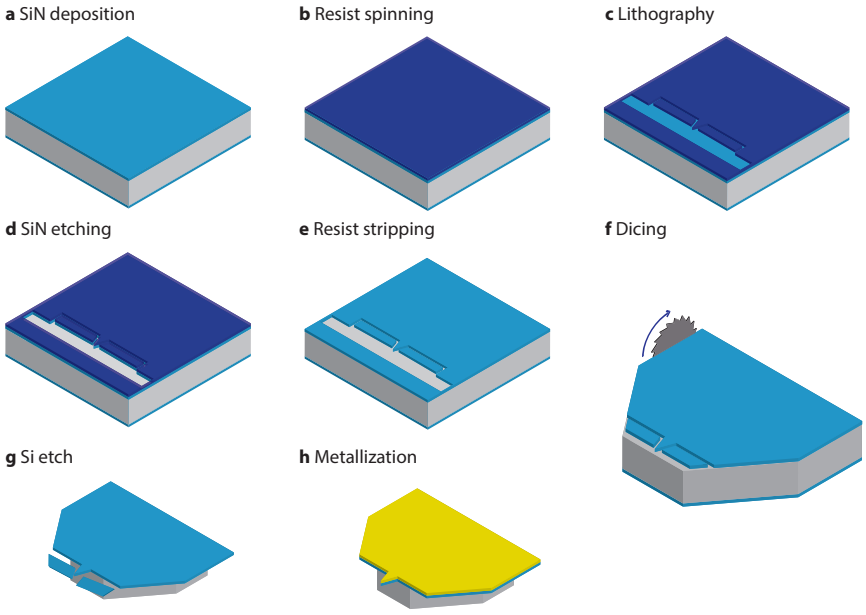

Figure 2.5: Overview of fabrication steps for STM smart tips. Note: 1) resist layer to protect the chip during dicing is not displayed for visual clarity. It is applied after (e) and removed before (g). 2) The bottom layer of SiN is omitted starting at (g), the layer is still there, however after the Si etch any protruding SiN at the bottom is removed by the adhesive oil applied during the etch.

the full wafer, can be aligned to the pre-patterned tip shape fairly well, but in the creation of the overhang the tungsten tips seem to be attacked. In this section we will present our final fabrication method to create smart tips with a single tip that utilizes SiN to greater extent.

Using SiN as a base for our suspended STM tips has a number of key advantages. First, it has a large selectivity to the Si etch we use to suspend the tip, allowing for clear protrusion. Making the tips solely out of metal without underlying SiN would also limit the choice of metal to those compatible with the etch described below. Second, it has a high mechanical stiffness, yielding robust tips that are resistant to tip treatment, as discussed later. Finally, it allows for a process where the metallic layer is added as a last step. This allows us to avoid any contamination by chemicals such as etchants and resists.

2.3.2. PATTERNING SiN TIP

Our process starts with a 500 μm thick Si(100) chip covered on both sides with a 200 nm thick layer of high stress low-pressure chemical vapor deposition (LPCVD) silicon nitride (SiN) (Fig. 2.5a). A 550nm thick layer of ARP-6200.13 resist on the top side is patterned using electron beam lithography (Raith EBPG5200, 100 kV, dose 370 $\mu C/cm^2$, spotsize

23 nm, beam step size 2.5 nm). After exposure to the electron beam, we develop the chip in Pentyl Acetate (1 min) and MIBK:IPA 1:1 (1 min) followed by an IPA rinse (1 min), see (Fig. 2.5b,c). The pattern, consisting of the tip shape and two shields, is transferred into the SiN layer using a CHF_3 etch for 5 min at 20°C (Fig. 2.5d). The shields are slabs of SiN on both sides of the tip, which we include to minimize the undercut of the Si once the overhang is created: the 50 nm lines around the shields reduce the etch rate of the Si etch significantly compared to a large exposed region without shields. We then clean the chip by two successive 1 min immersions into N-N-Dimethylformamide (DMF) followed by a boiling piranha solution at 135°C to remove all traces of resist and other organic contamination.

2.3.3. DICING

In order to bring the tip close to the edge we will proceed with dicing the chip (Fig. 2.5f). There are two main reasons to choose dicing over a Bosch etch, where we can cut out multiple chips at once: it allows us to easily vary the shape for each new iteration until we find settle on a final design and a Bosch etch requires a soft or hard mask and an additional etch step, both can be time consuming and introduces additional challenges. For the latter, in case of a soft mask, the removal of the thick and heat affected resist can yield inconsistent results as we have seen in Sec 2.2.2.

Before we dice the chip we first protect it against any residual debris from the dicing process by applying a new layer of photoresist. Out of a typical 10x10 mm^2 chip we cut out two smart tips adjacent to each other, as shown in Fig. 2.6a, to ensure the small features of the tip are in the center of the chip so ensure optimal resist conditions for the EBL. For the dicing we use a Disco dicer DAD 3220 where we stick the chip on a dedicated, 140 μm thick sticky sheet. The dicing shares a lot of the requirements we also set for the Bosch etch: (i) smooth sidewalls, such that the overhanging tip will be the

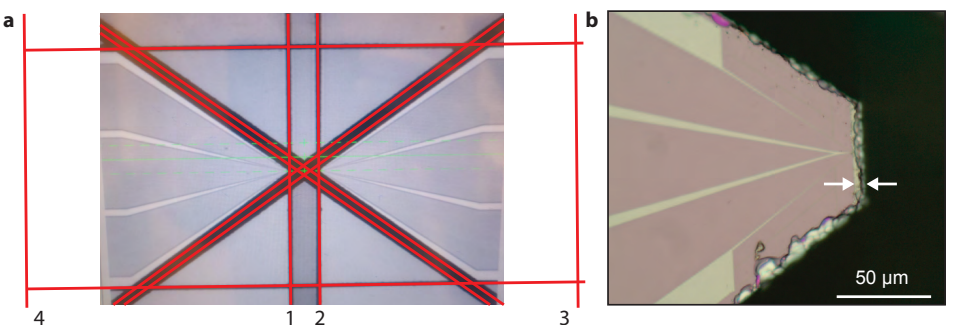

Figure 2.6: **a** Screen capture of a chip after dicing as seen through the microscope of the dicer. For illustrative purposes the image is taken on low magnification, the alignment of the blade is done at high magnification. The black areas are diced, the red lines indicate the sequence of individual cuts as indicated by the numbers. The chip is bigger than the field of view, but the final shape of the chip follows the (red) dice lines. **b** Optical microscope image of a chip after dicing. The silicon (gray) left after the dicing extends up to 6 μm beyond the SiN (pink). Note that the chips has a different lithographic pattern than described in this section, however the principle and the front shields are the same.

most protruded feature, (ii) minimal chipping of the Si and, (iii) alignment accuracy.

The first we obtain by choosing the optimal blade but we also make sure we dice at least 50 μm into the underlying tape. This prevents any roughness at the bottom of the chip. To find the optimal blade and settings we tested several different blades and speeds with which the blade moves forward and found that the ZH05-SD2000-N1-90 at 3 mm/s yields the best result in terms of chipping and sidewall smoothness. Residual roughness on the sidewall is further smoothed out by the isotropic Si etch described in the next section.

The second requirement is minimal chipping of the Si. Contrary to for example a Bosch etch, the blade can cause more roughness not only on the sidewalls, but also it can chip away small pieces of Si along the dice line near the top surface (Fig. 2.6). To align the dice consistently down to a few micron from the patterned tip, we need to minimize the amount of chipping. Our choice for the ZH05-SD2000-N1-90 blade at a feed speed of 3 mm/s makes a significant difference, but there is another trick that helps reduce the chipping: dressing the blade. By dicing through a block of very hard material (or dressing board) one can wear softer materials off the blade and thereby increase the exposure of the diamonds in the blade. This process makes the blade wear faster but reduces chipping. Typically we dress the blade before we dice each chip and perform the two critical dices (number 1 and 2 in Fig. 2.6a) first as the chipping worsens with each dice.

To align accurately to the patterned tips we need to calibrate the width of the blade accurately by a so called hairline adjustment. We perform a single dice on the outskirts of the same chip and with the settings that will be used for the actual dices and put the lines that indicate the width of the blade throughout the procedure on the width we get from the test line.

The full procedure works as follows. First we dress the blade, remove the dressing board and load our chip that sits on the sticky sheet into the dicer. We proceed to make a first cut and perform the hairline adjustment. Then, with a sequence of individually aligned dices as indicated in Fig. 2.6 we cut out the shape we need. Lines 1 and 2 are the ones close to the tips and are therefore the first after dressing. Lines 3 and 4 follow keeping the same alignment, that way we ensure that when the chip stands upright, the bottom is exactly parallel to the top where the tips protrudes. The cross lines 5-8 run through the shields typically around 20 μm away from the tip on each side. Finally we dice lines 9 and 10 parallel to each other, these set the width of the chip to 3 mm. After completing all the lines we unload the tape holding the chip and dry it, expose it to UV light to reduce the stickiness of the tape, making it easier to remove the two tips. For tips longer than 4-5 mm long one can either follow the procedure above but start with chips longer than 10 mm or write two tips next to each other and dice the chips in two parts. Now we have two (smaller) chips each housing a single device.

2.3.4. SUSPENDING SiN TIP

The residue created by the dicing process is washed away with the removal of the protective photoresist layer. After this cleaning step, we isotropically remove part of the Si substrate using a dry reactive-ion etch based on SF_6. The etch is performed by a plasma of F^- ions formed inside an ICP etcher. Reactive ion etching is often a combination of chemical reactions, the F^- ions reacting with the Si, and ion bombardment, where the

ions are accelerated by a DC bias into the sample hence removing material. However, to prevent any anisotropy in the etch we do not put a DC bias except for a short ignition pulse < 1 s, resulting in an isotropic Si etch.

For improved selectivity of the SiN over the Si the chip is cooled to −50°C. During a typical etch the thickness of the SiN reduces from 200 nm to ~120 nm. The exposed Si sidewalls are removed at a rate of around 4 μm/min until both the tip and the two shields protrude by about 10−12 μm, causing the shields (10 μm) to fall off (Fig. 2.5g, 2.7). The straight sides next to the tip can be made very small or even rounded, as shown in Fig 2.7b to avoid accidental touches when aligning to a sample, this would not have been possible using an anisotropic KOH wet etch.

In approximately 20% of devices, one or both of the released shields lands on top of the chip (Fig. 2.7c). Spraying acetone followed by IPA in the appropriate direction often suffices to remove them, depending on the placement of the shield. For these single tip devices where the complete plane will be metallized to create a single contact, the shields do not cause any problems unless they protrude beyond the tip itself. Later in Sec. 5.3.2 we will see that the irregular release can be a result of resist residue being present in the trenches and can cause significant yield problems, here the latter is not the case.

2.3.5. METALLIZATION

The final step in fabricating the STM tip involves depositing a metal on the chip through sputtering to ensure proper coverage of both the top and the side of the SiN tip (Fig. 2.5h). Here, we choose to deposit 20 nm of gold (Leica ACE200) as the tip material; it is relatively

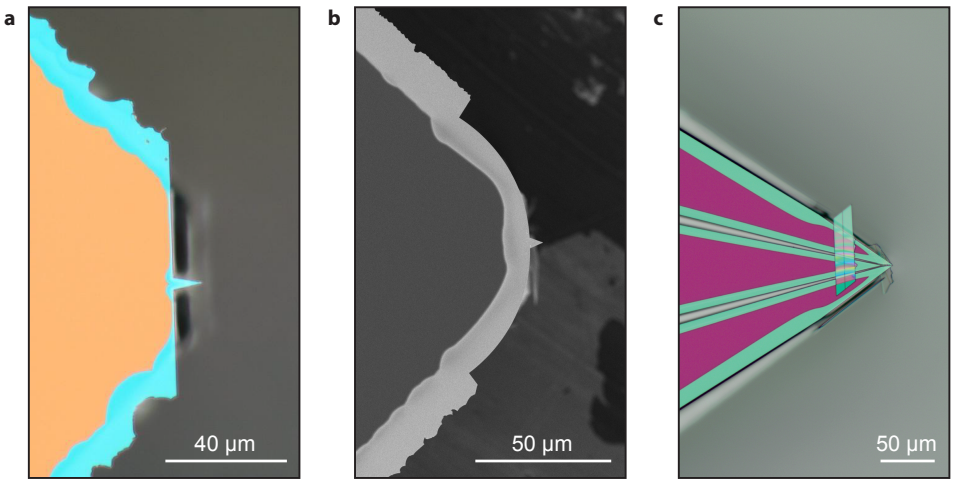

Figure 2.7: **a** Optical microscope image of a SiN tip after release off the shields where the orange part is still attached to the underlying silicon and the green parts is suspended. Notice that two shields next to the tip have reduced the overhang at the straight (right) side compared to top and bottom side. **b** SEM image of smart tip with a rounded profile around the tip. **c** Optical image of a smart tip containing multiple probes that demonstrates the improper release of the shield on top of the chip. Here the purple parts connect to the silicon and the green parts are suspended.

straightforward to use other interesting materials for the tip. The main boundary conditions for choosing materials are good adhesion to the SiN and compatible stress level in the film. In the next section we also show that we can use tungsten covered SiN tips, for these we typically sputter ~50 nm tungsten using a Alliance Concept AC450 (150 W RF power at 2×10^{-7} bar base pressure). Evaporation of the metal film is also possible and will be discussed in Sec. 5.3.1.

2.3.6. SMART TIP DEVICES

Images of a typical devices are shown in Fig. 2.8(a-c). The diameter of the apex of the tip depends on the initial thickness of the SiN, the electron beam spot size and dose, the SF_6 etch time and temperature, and the metal film thickness. However, as can be seen from Fig. 2.8(c), the tip diameter is mostly determined by the grain size of the metal film. Our tips achieve radii of a few (tens of) nanometers for the gold film, is comparable to specialized commercially available metal wire tips. The ("macroscopic") tip sharpness for the tungsten tips defined by the curvature of the foremost part of the film has a radius in the order of the film thickness of the tungsten. The tungsten film has however a fine grain structure which in practice determines the tip sharpness at the scale of the junction itself. Here, the stress in the film causes a slight upward bend in the overhanging tip. The severity of the effect depends on the geometry: the bending in a geometry like in Fig. 2.8b is below a micron. If the suspended tip does not connect to the surrounding plane very adiabatically but forms a narrow line the bending seems to increase. This could affect us once we start looking at other geometries in Ch. 4. The overall yield of the fabrication as described in this section is around 80%.

2.4. CONCLUSION

Throughout this chapter we have worked towards a smart tip fabrication method that is fast, (relatively) easy to implement and flexible such that it can act as a platform. The latter stipulates that we need control over the shape of the tip and we obtain this by incorporating electron beam lithography. Furthermore, to create the overhang of the tip with high yield we need the lithographically defined tips to be very close to the edge of the chip before we create the overhang. We discovered that, while able of making very sharp, pointy chips, cleaving chips does not suffice here because it lacks the above mentioned ability to align it accurately.

We conclude that the creation of the chip shape and (simultaneously) the overhang can be achieved using a Bosch etch through the full chip. We have shown this first with chips covered with LPCVD SiN and sputtered tungsten. Later we incorporated lithographically defined tungsten films to increase tip sharpness and to work towards adaptable designs. Although the etch itself shows great promise the optical resist based mask proved hard to remove and raises concerns about cleanliness of the tips (and chips). For the sharper tungsten tips supported by a plane of SiN we have encountered a more mysterious problem where the small structures that form the tip are somehow attacked by the etch despite being protected on top and bottom.

It may very well be that all the complication we mentioned above can be overcome with further optimizations, however, a simpler and intrinsically clean process became

apparent. By creating the tips out of lithographically defined SiN, which is almost inert to the Si etch used here and which can be thoroughly cleaned using a wide variety of chemicals such as a piranha solution, we circumvent all the obstacles we encountered.

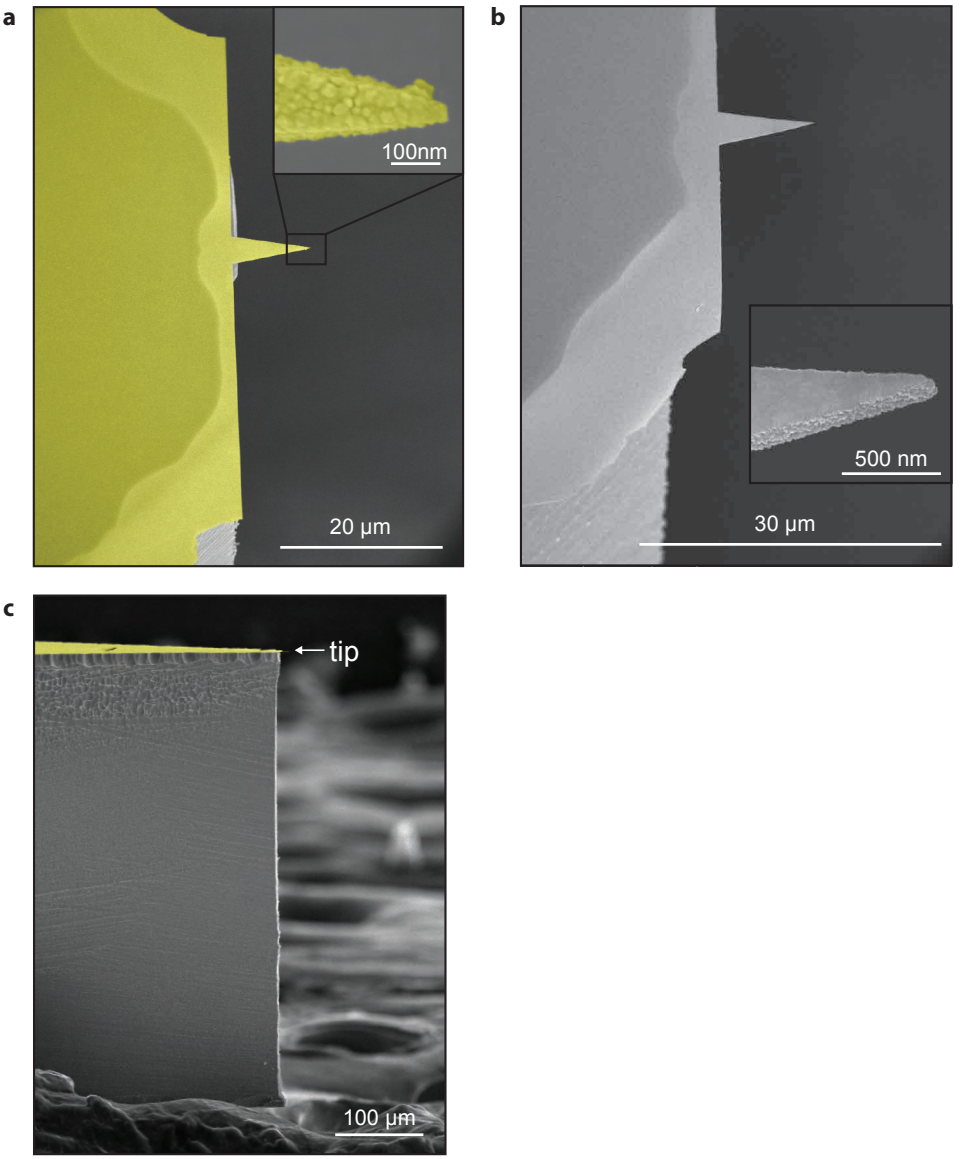

Figure 2.8: **a-c** SEM images of a smart tip from the top (a,b) and the side (c). **a** The freestanding tip made of Au (colored in yellow) covered SiN has a length of 10 μm and a tip radius of approximately 20 nm. The light yellow area is suspended, while the dark yellow parts are still attached to the underlying Si. **b** Smart tip covered by W that shows finer grain size but slightly more bending. **c** Side profile of a smart tip.

Only at the very last we metallize the tip and thereby ensure its cleanness.

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3

REALIZATION OF THE SMART TIP STM

3.1. INTRODUCTION

In this chapter we describe the design and realization of a homebuilt, stable, low temperature scanning tunneling microscope that we built specifically but not exclusively for the new smart tip platform. Specifically, because the ability to house the smart tips instead of traditional wire tips comes with additional requirements concerning the tip holder and the wiring. Not exclusively, because we aim to build a versatile and low consumption STM where we can also use traditional tips, exchange tips easily, prepare a wide variety of samples, etc., while retaining excellent performance at low operational cost. Throughout this chapter we witness how this large variety of demands guides the design of the STM. While the STM described here is (mostly) designed and constructed in-house, it is more accurate to call it a hybrid where we combine commercially available parts to a full system that meets our requirements. This way, at the core, we mostly rely on proven parts made by specialized companies and we reduce the workload.

We start out with a short overview of the full system to present an overview of the overall design, what all components look like and where they are placed with respect to each other. Afterwards we land on the individual components. We motivate our choices, describe in detail how the parts work (together) and report on their abilities. First we focus on the heart of the system, the STM head, where tip and sample meet (Sec. 3.2). Many of the system's features are determined by the STM head and it has a large effect on the subsequent design choices. A good example is the top mounted cryostat we describe in Sec. 3.3 that we use to achieve a base temperature of 4.2 K. With both the cryostat and STM head in place we look at the wiring of the STM and how the wires are precooled by the cryostat in (Sec. 3.4). Afterwards in Sec. 3.5 and Sec. 3.6 we look at two other key specification, the ultra-high vacuum system and vibration isolation, respectively.

3.1.1. OVERVIEW

The main strength of scanning tunneling microscopy is the ability to visualize conducting materials with subatomic resolution. That in itself has led to a tremendous amount of structural information of many materials at the atomic scale. One can think of several examples such as lattices, lattice deformations, structural phase transition, but also atomic ensembles. The latter is particularly interesting since it shows that the position of atoms on surfaces can also be manipulated by the tip. All of this is a result of the exponential current-distance dependence of tunneling process between tip and sample and clever engineering. The first gives rise to the extreme sensitivity of the tunneling current to height changes. To resolve a so-called topography, a spatially resolved atomic height map, one needs to be able to approach the tip to within a nanometer (typical 0.5 nm) from the sample and scan it over the surface using a feedback circuit. The feedback between tip and sample can for example be used to keep the tip at a constant height throughout a scan to acquire a topograph.

STM is not just an advanced imaging technique for topography, it can also be used for spectroscopy. This is called Spectroscopic Imaging STM (SI-STM) or Scanning Tunneling Spectroscopy (STS). By measuring the differential conductance dI/dV we acquire information about the local density of states (LDOS) of the sample, given that the LDOS of the tip is constant in energy [1]. During such a measurement the feedback is switched off. The real strength lies in the acquisition of a spectroscopic map (a spectrum at each

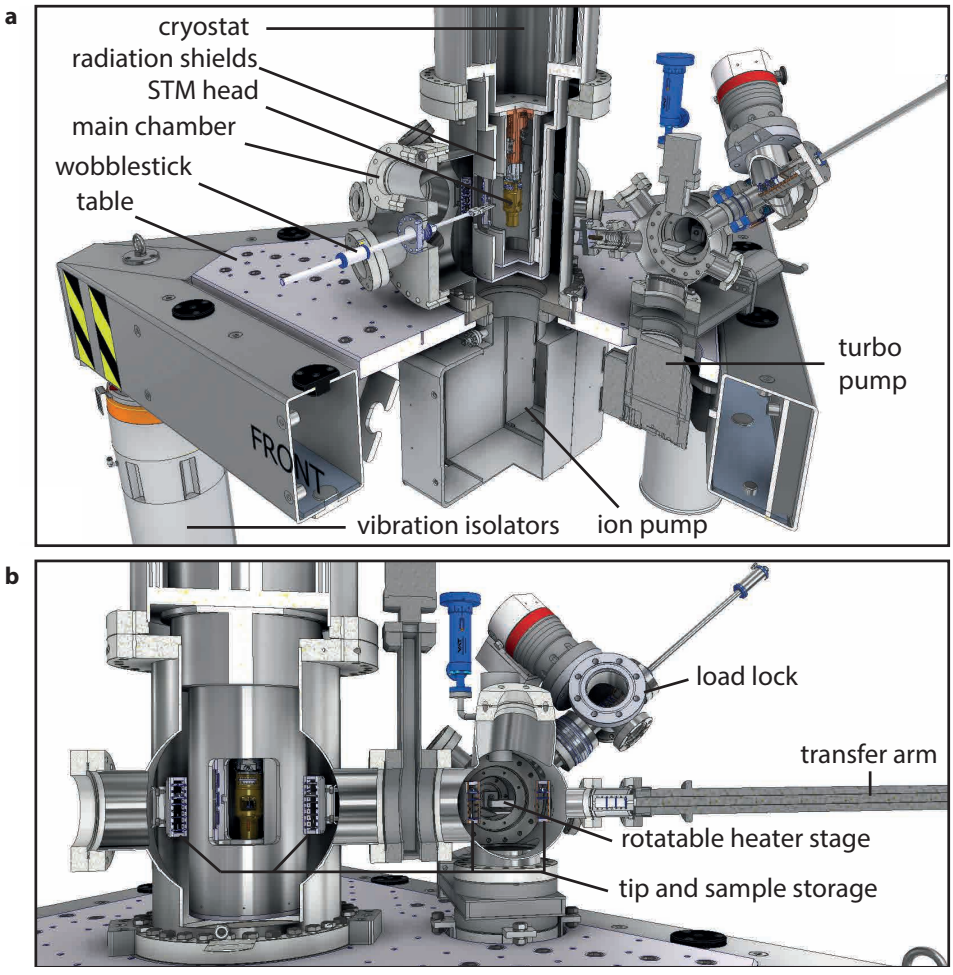

Figure 3.1: Overview of the full smart tip microscope. The inside of the cryostat and the STM head are made visible by virtually cutting open the CAD render. The main parts are individually labelled. **a** Inclined view to show the majority of the vacuum system, the vibration isolation table and the STM head including its surrounding radiation shields. **b** Front view render of the main chamber, preparation chamber and load lock.

point in space, i.e. 256x256 pixels) that consist of 10^4-10^5 spectra. These maps can provide a plethora of information about the electronic structure on the atomic scale. They typically take several days up to a week of continuous measurement with prolonged periods out of feedback demanding an extremely stable tip sample junction. The stability requirements are much more stringent than the ability to resolve atoms.

To prepare samples such as metal films, graphene based systems or other quantum materials such as cuprate high-T_c superconductors we need ultra-high vacuum (UHV) with pressures down to 10^{-10} mbar to prevent dirt from accumulating on the sample

surface. Most materials we want to study show interesting physics at low temperatures therefore we build the STM for operation down to 4.2 K. Low temperatures also helps the vacuum by condensing residual gasses to the cold surfaces, benefits the energy resolution of the spectra [1] and reduces drift in the piezo's.

3.2. STM HEAD

A key ingredient to low noise performance is a stable tip-sample junction. Therefore it is of great importance that the STM head, the construction containing the tip, the sample and everything that allows the scanning, is very rigid. Since the invention of STM by Binnig and Rorher in 1981 [2], several STM head designs have been developed. Two famous examples are the beetle type head and the Pan head pioneered by Besocke [3] and Pan et al. [4], respectively. The first is often adapted for multiprobe STM, where two or more metal wire tips can be individually manipulated. The latter has emerged as the preferred choice for spectroscopic imaging STM's due to its very rigid, compact and reliable design. Over the last two decades several innovations have lead to increasingly stable STM heads culminating in recent ultra-stable STM heads made primarily out of sapphire [5, 6].

The nature of the smart tip platform allows us to simply replace the metal tip wire with a chip based tip. The study of quantum materials by spectroscopic imaging STM requires stability over multiple days often out of feedback, therefore we prefer a Pan type STM head among other reasons. The examples of sapphire based STM designs given above [5, 6] show best in class stability, but they do sacrifice flexibility: a smaller and shorter piezotube has a higher resonance frequency but a smaller scan range and incorporating an exchangeable tip holder may prove very difficult. Instead the tip is directly mounted into a small cone on the piezo tube. The reduced scan range is not a problem, but the absence of a tip holder means the vacuum must be broken in order to exchange tips. Here we need to be able to replace tips frequently. In addition we want to be able to study a large variety of samples including exfoliated flakes such as (twisted bilayer) graphene, where we need to land the tip on a ~micron sized flake on a large chip. Therefore we need the sample to be on a piezo driven course motion XY stage with a range of several millimeter.

Besides the ability to exchange tips we also need multiple electrical contacts interfacing the tip holder to the of smart tip device. Fortunately it does not force us to custom build a STM head, since several commercially available Pan style STM heads are already equipped with three electrical contacts. This is due to the popularity of combined STM/AFM systems using a qPlus sensors [7]. Tip holders that are compatible with STM and AFM require three contacts.

Here we integrated the PanScan STM head made by RHK [8] into a 4 K bath cryostat described in Sec. 3.3. The head itself is shown in Fig. 3.2a and consist of the following main parts from bottom to top: the body, the slider for course Z motion, the piezo tube for the scanning, the tip holder receptacle, the sample stage that holds the sample and allows for course XY movement and finally the eddy current damper. The slider is a rigid prism clamped in the body by two piezo stacks on each of the three flat sides. The piezo stacks generate slip stick motion and thereby jointly make the slider move up to ~8 mm in Z direction towards/away from the sample. We typically apply pulses with an ampli-

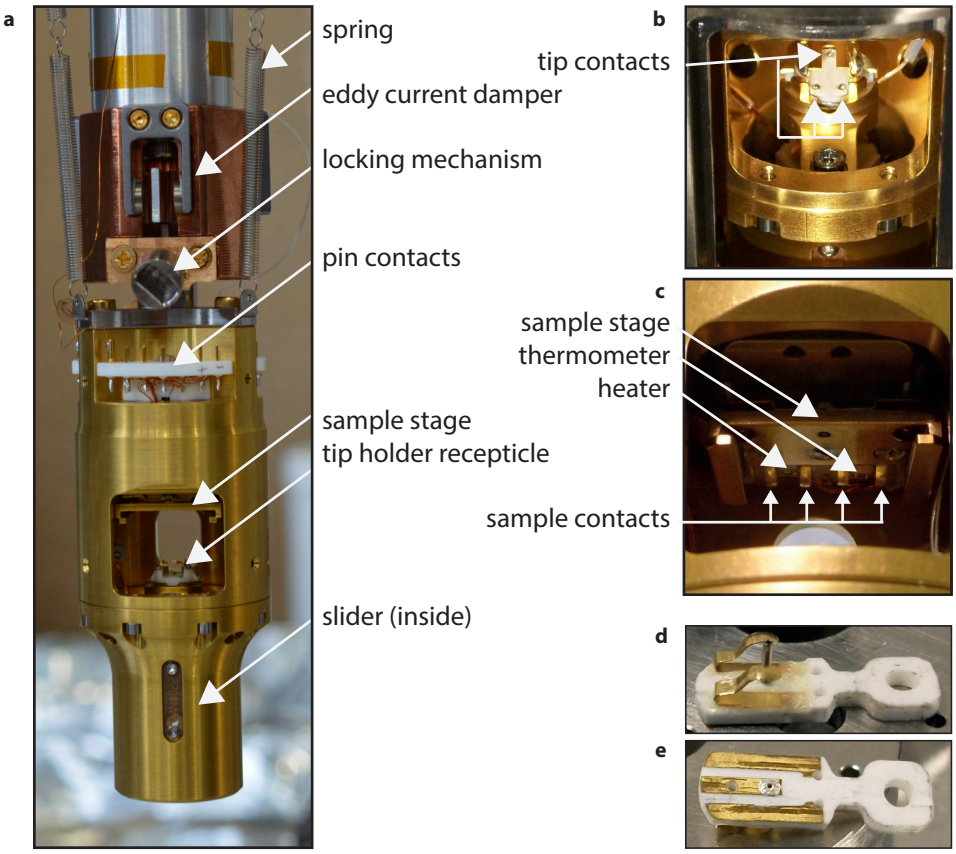

Figure 3.2: **a** Picture of the RHK STM head with all important parts indicated. Note that no sample or tip are loaded. **b** Close up of tip holder receptacle with three electrical contacts. **c** Close up of sample stage with four electrical contacts to the sample plate. **d,e** Pictures of the top (d) and bottom (e) of tip holder.

tude of ±150 V and a pulse duration of 1 ms at 4.2 K, in ambient conditions lower voltages typically suffice.

Protruding from the center of the slider is the piezotube that provides the scanning motion. The piezotube has four electrical contacts for de movement in the ±X, ±Y directions and one inner electrode responsible for the extension of the tube in Z. Typical driving voltages at 4 K are set by the calibration 5.18 nm/V for the X and Y direction and -1.2 nm/V for the Z direction with a maximum ±150V on all contacts, resulting at 4 K in a scanning range of around 1.2 μm^2. The tip holder and its receptacle glued on the piezotube together weigh less then one gram [9]

Samples are glued or clamped on a flag style sample plate [10]. With a wobblestick we can load it into the STM head where the plate is clamped by ruby balls pressed down by springs. Four additional metal springs contact the plate from the top side, these provide electrical contact. One of the contacts is the bias connection to the sample. Having

multiple electrical contacts expands the range of measurements available with this STM. By using an insulating sample plate with separate contacts one can add for example a gate electrode to the sample. Also attached to the plate are a heater (up to 150°C) and a thermometer (Si diode DT-670). The sample stage is also part of a course motion system that allows the sample to move up to 4 mm in the ±X and ±Y direction. This allows us to navigate the tip over large samples to find the exact location where we want to approach the tip to the sample.

The tip holder plays an integral role in the transition from traditional metal wire tips to the smart tip platform. The necessary adjustments to implement the chips will be discussed in Sec. 4.4. Here we take a look at the default tip holder provided by RHK. Their design consists of: a flag style Al_2O_3 plate to provide stiffness, strength and thermal conductivity; three gold contacts that slide over three metallic balls in the tip holder receptacle; a tube for the tip wire that connects to the center pad on the bottom; and, lastly, two BeCu spring that hold down the tip holder once we slide it in. Loading normal metal wire tips consist of three steps: (i) we make a slight bend in the tip wire such that is clamps itself in the tube, (ii) we load the tip holders into the parking and bake the load lock to reach the vacuum conditions, and (iii) we use the wobblestick to transfer the holder into the head when the slider is fully retracted. Only when the slider is fully retracted the piezotube is protected against deformation/breaking as we press in the tip holder.

3.3. CRYOSTAT

In the last section we have seen that the STM head is designed to be loaded from the front, using a wobblestick, and that the design is very open for good optical access. Therefore the head needs to be hanging inside the main vacuum chamber (see Fig. 3.1) where the center point between tip and sample lines up with the height of the wobblestick. As a consequence the cryostat situates on top of the vacuum system. STM's with optical access and the cryostat mounted under the STM head do exist, but keeping a constant base temperature is challenging as the liquid Helium level lowers over time.

Here we implemented a Cryovac 4.2K bath cryostat with two reservoirs: the inner contains 10L of liquid Helium and the outer 22L of liquid Nitrogen. The STM head is mechanically attached and thermally anchored to the oxygen free copper (OFC) bottom plate of the helium tank via an OFC construction (see Sec. 3.4). The full structure is enclosed by an aluminum 4 K radiation shield that is screwed into the 4 K plate and shields it from nearly all radiation hotter than 4 K. All the open spaces between the tanks and around the STM are part of the UHV system making radiation the foremost heat transfer mechanism.

The He tank and shields would have a large area exposed to room temperature radiation leading to high consumption if it wasn't for the liquid N_2 tank around it. To fully enclose the He tank and its radiation shield, there is also a radiation shield (at 77 K) around the STM as well as above the He tank. The shields around the STM both have doors that can be opened to load samples, release the STM locking mechanism (Sec. 3.6.3) or for optical access to approach the tip to a sample. Inevitably this will lead to a temporary increase in base temperature at the STM and elevated consumption. In fact, for maximal efficiency the otherwise wasted cooling power of the evaporated He is used to cool two

additional shields: one ~20 K shield between the two tanks and a ~200 K shield between the outside of the cryostat (room temperature) and the N_2 tank.

Some heat transfer via conduction is unavoidable. Both tanks are hanging from top on stainless steel tubes. The helium tank is connected to the top of the cryostat only via a single tube. This tube act as a He in- and outlet and allows us to fill the liquid He tank using a special transfer line and recollect the evaporated He. The two shields using the cooling power of the He gas connect to copper parts of the tube. The top connection of the tube to the outer body is where the whole tank and STM hang on. Using three screws on the top of the helium tank can be slightly tilted if necessary to prevent the inner tank to touch the outer. This would cause strong thermal link between the two. The outer liquid N_2 tank has minimal conductive paths to any parts at room temperature and also has inlets and outlets on top for filling/emptying and an over pressure valve.

Another source of heat conduction are the electrical wires. They extend from the vacuum feedthroughs on the top at room temperature all the way down to the STM head at 4 K and thereby form a direct path for heat conduction. In the next section we will discuss the wires we need, what materials we choose and how we thermalize the wires down to 4 K.

Finally that brings us to the overall consumption of the STM in operation. The consumption is important for two reasons: operational cost of the STM, due to the high price of liquid He, and the hold time that determines how long we run a single measurement. The first depends strongly on how long and often the shields are open and how many (warm) samples are loaded. On average use, with about two sample and tip changes in a week, the He last for 10-12 days corresponding to a consumption of <1 liter/day. The liquid N_2 needs to be refilled once every 4-5 days and is therefore the limiting factor for the hold time.

3.4. WIRING

With the STM head as the heart of this system the wiring must be the aorta: while a stable tip sample junction is vital due to the exponential nature of the tunneling current, that tunneling current remains a small signal prone to interference if not transported and amplified properly. In this section we look at the full wiring of the STM. What (type of) wires do we need? How do we minimize electrical noise? What materials do we choose? How do we thermalize the wires? And, lastly, how do we connect them to a STM head suspended by springs?

Fig. 3.3 provides the overview of all the wires inside the STM from the feedthroughs on the top of the cryostat down to the STM head. We use three types of wires to connect the STM head through inside the cryostat to the UHV feedthroughs: twisted pair wires, flexible coax cables and semi-rigid coax cables. The twisted pair wires are mainly used as general purpose wires. The twisting helps to reduce electromagnetic interference because it is equal and opposite in the two wires that make the pair. These wires are thin and flexible, an advantage we will discuss later in this section. As indicated by Fig. 3.3 we use them for thermometers, the heater, sample contacts and to ground the (hanging) STM head body to the copper body. We also use two twisted pairs for the piezotube contacts, one pair for ±X and one pair for ±Y to prevent any voltage asymmetries along the respective direction induced by interference.

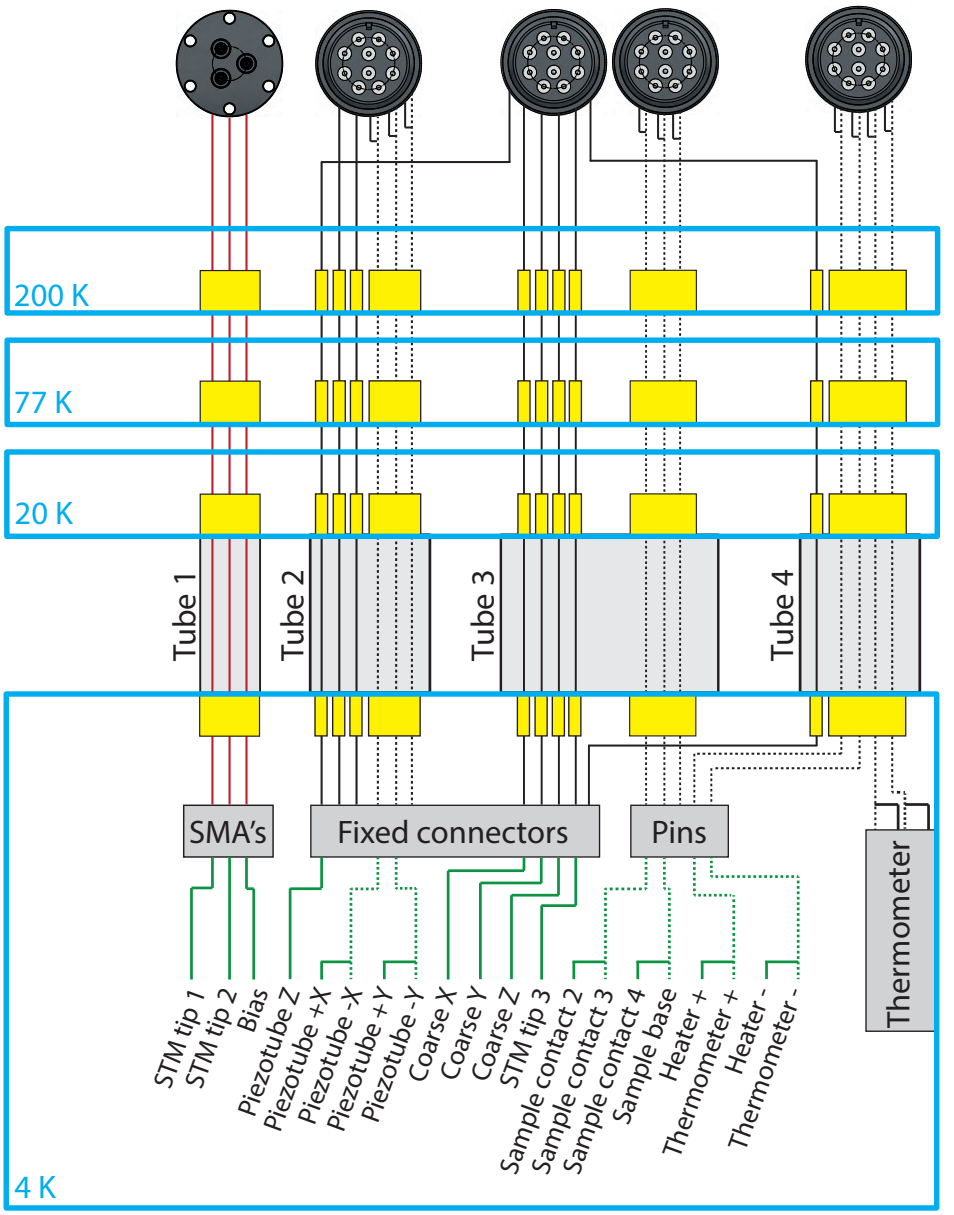

Figure 3.3: Schematic of full wiring of the STM including thermal anchors. From top to bottom: UHV feedthroughs, three thermal shields (blue) with attached bobbins (yellow), the four tubes (gray) through the helium dewar followed by the 4 K stage. The fixed connectors block consists of a row of SSMCX connectors fixed to the hexagonal OFC block and the pins are connected via a UHV compatible gender adapter. The line colors are indicated in Tbl. **??**.

For the rest of wiring we either use flexible coax cables or semi-rigids. The semi-rigids consist of a solid metal inner conductor and solid shields separated by a dielectric. Therefore they are not flexible and need some force to be bend into shape. We use three semi-rigids, two for tips and one for the bias, for several reasons. The coaxial nature of the cables shields them from outside noise, they are mechanically more stable and they have lowers attenuation for high frequency signals (depending on the material and diameter). With the latter we ensure future compatibility for high frequency STM [11]. These, and coax cables in general, have a larger metal cross section and will transport more heat than the twisted pairs. To minimize the heat load we decide opt for the small diameter stainless steel cables (SC-086/50-SS-SS) from Coax. Co. There is however, a trade-off between thermal conduction and the attenuation of the cable: thicker, well conducting cables have lower losses at high frequencies.

The three semi-rigid cables are all split into two parts and connected via SMA connectors. On the top of the cryostat all three connect to an ultra-high vacuum feedthrough for 3 SMA connectors. At the 20 K shield the two parts are joined via a SMA bulkhead connector that is attached to the shield. This helps with thermalization (more on that later) and significantly eases their placement into the cryostat compared to a single piece. At the 4 K stage we connect them to flexible copper coax wires to reduce the transmission of vibrations to the suspended STM head.

The flexible stainless steel coax cables (from CMR-direct) are also small diameter with a braided shield and non-solid core and are therefore easier to handle and thermalize. We use them for driving course motion piezos (X,Y and Z), the third tip wire and the inner electrode of the piezotube (fine Z motion). They are differently connected than the semi-rigids. Here we don't use SMA on either side, rather we simply connected the inner conductor to one of the vacuum feedthrough pins leaving the shield unconnected and for the connection to flexible copper coax cables at 4 K we use SSMCX connectors. The shields are connected to ground as we connect the outside of the SSMCX connectors to the body via the OFC clamp that holds them in place (Fig. 3.4e).

Proper grounding of the system by creating low ohmic connections to ground and avoiding ground loops is essential for the reduction of electronic noise, in particular 50 Hz noise. Starting from the STM head, we connect the body of the head to the hexagonal copper rod shown in Fig. 3.4a,e using thin copper wires to provide good electrical connection once the STM head is hanging on the stainless steel springs. The cryostat, the vacuum system and the vibration isolation table are all well connected electrically. All the shields of the coax cables are also connected to this body that acts as a central ground point. With a several mm thick copper cable we connect the STM table to a central ground in the building. All electronics such as the STM controller are also grounded with thick cables to the STM table.

The STM is controlled by an R9 controller from RHK. They provide an additional box called the IVP-R9 that provides the bias that we connect via a coax cable. The tip signal is amplified by a FEMTO DCLPA-200 variable gain transimpedance amplifier. The FEMTO is mounted very close to the SMA feedthrough to keep the cable short to minimize the input capacitance for the amplifier. We notice that firmly screwing the FEMTO on a thick copper plate connected to the feedthrough significantly reduces 50 Hz noise in the system.

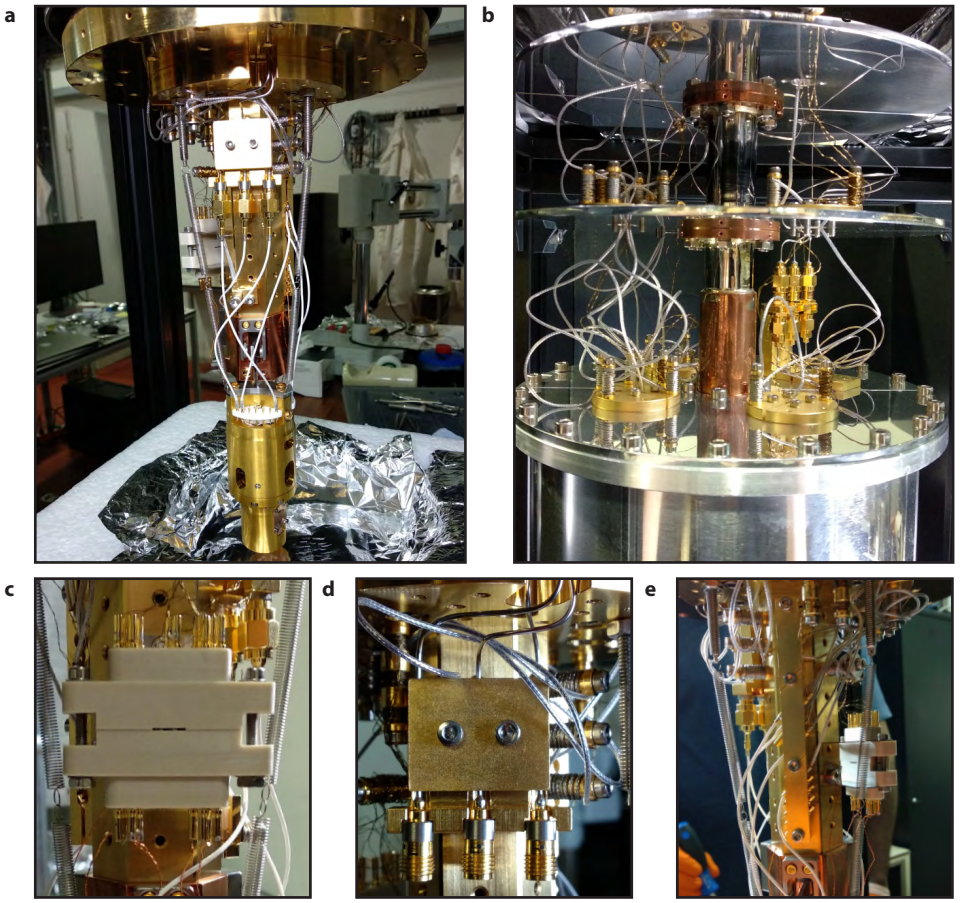

Figure 3.4: **a** Picture the 4 K plate (top) with the OFC construction and the STM head (bottom). It also shows the clamp to thermalize the semi-rigids that connect via the SMA connectors to flexible copper coax cables (white) running to the STM head. We see several bobbins on the top plate and the hexagonal support and two of the three springs holding the STM head on either side. **b** Picture of the three thermal shields inside the cryostat and the attached wires (before bundling) that include OFC plates and bobbins around each hole/tube and the SMA bulkhead connectors that connect the semi-rigids on the bottom right. **c,d,e** Pictures of the wiring ensemble at the 4 K plate. It includes an additional copper plate full of bobbins to thermalize wires and a hexagonal solid OFC support for the STM head with on three side different cable mounts. **c** UHV compatible gender adapter where the constantan twisted pairs coming from top are connected to copper twisted pairs going to the STM. **d** Three stainless steel semi-rigid coax cables fixed to the copper support by a custom made clamp to thermalize and ground the shields. Via SMA connectors the semi-rigid wires are connected to flexible coax wires going to the STM (not connected here). **e** Custom made OFC clamp to mechanically fix, thermalize and ground the SSMCX connectors of the flexible coax cables coming from top. They connect via copper coax cables (white) to the STM.

3.4.1. THERMALIZATION

In Sec. 3.3 we elaborated on the contributing factors to the transport of heat. It became apparent that for minimal consumption of cryogenic liquids and maximum hold time

	SS semi-rigid (Coax. Co.)	SS flexible coax (CMR-direct)	Constantan twisted pair (CMR-direct)	Copper flexible coax (Coonerwire)	Copper twisted pair (Accuglass)
Color/symbol in Fig. 3.3					
OD shield [mm]	1.19±0.0254	1	-	1	-
OD core [mm]	0.287±0.013	0.2	0.11	0.15	0.16
Impedance [Ω]	50	40	-	50	-
Attenuation @1 GHz,RT [dB/m]	7.4	18	-	?	-
Attenuation @1 GHz,4 K [dB/m]	4.7	-	-	?	-

Table 3.1: Properties of all five cables types used.

we aim to minimize the heat conduction from room temperature down to 4 K. We do this by optimizing the wiring, i.e. reducing thermal conductance by minimizing the wire diameter, and choosing materials with a good balance between good electrical conductance and bad thermal conductance.

The heat flow is simply given by Eq. (3.1).

$$\dot{Q} = \frac{A}{L}\int_{T_1}^{T_2} \kappa(T)\,dT \tag{3.1}$$

Where A is the cross-sectional area, L is the length of the wire, T_2, T_1 are the temperatures at the anchor points and $\kappa(T)$ is the thermal conductivity of the material. For large temperature differences one needs to integrate over $\kappa(T)$ since it is temperature dependent. To minimize the heat load at 4.2 K we need wires that (i) have low thermal conductivity, (ii) have a small cross-sectional area and (iii) are long. Also the reduction of T_2 makes a big difference, we achieve this by thermalizing the wires at intermediate temperatures along its path through the cryostat. The first step however is to select materials with low heat conductivity. For all the cables running from room temperature to 4 K we used either stainless steel (flexible and semi-rigid coax cables) or constantan (twisted pairs) with a low thermal conductivity of 16.3 W/m/K and 21.2 W/m/K at room temperature, respectively. Constantan has the advantage that the thermal conductivity is nearly constant over the large temperature range.

Both the twisted pairs and coax cables connecting the 4 K stage to the (suspended) STM head are made out of copper to create an optimal thermal link from the head to the cryostat. We also added two bundles of thin copper wires to the STM head body to further improve the thermal link.

The cryostat has four tubes running through the He tank each with a diameter of

10 mm. The three aluminium shields above the tank (20 K,77 K,200 K) each have four holes slightly offset with respect to each other to prevent a direct path for radiation. All wires run from the feedthroughs on top through these holes and tubes to the STM. We thermally anchor the wires each shield by using (homemade) bobbins or clamps. Bobbins are hollow rods made out of gold plated OFC where we wrap the wires around with as many windings as possible to create a large contact area. We can screw them into the small OFC plate we made around each hole on the shields where we can mount up to six bobbins at a time (Fig. 3.4b). To compensate for the thermal contraction of the copper with respect to the stainless steel screws we use Molybdenum washers. To fixate the wires on the bobbins we use non-conducting epoxy (Epotek H20E). Due to the high density of wires around the bobbin and their close proximity to the bobbin (connected to ground) any defect in their insulation layer may lead to a short if one was to use conducting epoxy, a risk we are not willing to take. We use the bobbins for both twisted pair wires and flexible coax cables, also at the 4 K plate.

The semi-rigids are also connected to all the shields in the top part of the cryostat. We use in-house designed clamps very similar to the one shown in Fig. 3.4d but horizontal. The main difference is that here the clamp has six grooves, so the each cables runs back and forth through the clamp to double the contact length. As mentioned before the semi-rigids are made out of two parts that are joined together by a SMA bulkhead connector. This connector is screwed firmly into a gold plated OFC piece we made that connects to the 20 K shield (Fig. 3.4b). Between the shields where the wires are fixed we keep about 20 cm excess wire, for convenience, and, because additional length also lowers the heat conduction following 3.1.

At the 4 K stage the wires come out of the four tubes and are thermalized again using bobbins and a clamp for the semi- rigids, see Fig. 3.4a,d,e. The constantan twisted pairs are soldered to pins and are connected to the copper twisted pairs via a UHV compatible gender adapter (by Accuglass) shown in Fig. 3.4c. We fix the SSMCX connectors at the end of the flexible coax cables in a custom clamp under 45° angle as shown in (Fig. 3.4e). The clamp fixes them, but also helps with thermalization and grounds the shields. The flexible copper coax cables then connect to the STM head's pin connectors. In the last few centimeters of coax cable before the pins the shield and dielectric are removed to further reduces the stiffness of the cables.

3.5. ULTRA HIGH VACUUM SYSTEM

SI-STM is surface sensitive technique and therefore we require extremely clean sample surfaces over prolonged periods of time. To prevent even a monolayer of dirt forming on our samples we utilize ultra-high vacuum (UHV) in combination with the low temperature to condense residual gasses to the cold surfaces. STM's that rely on low temperature in-situ cleaving of samples do not necessarily require such high vacuum in their loading chambers, the cryopumped area where the sample is exposed to after cleaving simply suffices [4, 6, 12]. Here, because of the optical access to the STM head, the temperature can vary after loading the sample, but also the cleaving does not happen in a cold area. On top of that we want to be able to investigate a wide variety of samples not only the ones that rely on cleaving; for example, the cleaning of metal films or the evaporation of thin films ideally requires ultra-high vacuum.

The vacuum system we describe here consists of several main parts: the cryostat described above, the main chamber for the STM, the preparation chamber and a small load lock. The cryostat is connected on top of the main chamber via a CF300 flange. The main chamber encloses the STM head with the 4 K and 77 K shields around it, two homebuilt tip/sample storage units on either side and a wobble stick to exchanges tips and samples. We have equipped the main chamber with many viewports, especially on the front side, both for ease of use and for multiple potential camera angles to approach tip and sample. The main chamber is pumped by a Gamma Vacuum 300T ion pump (with included titanium sublimation pump) during measurements. It is assisted by the turbomolecular (turbo) pump on the preparation chamber that we use to pump down the system before we can run the ion pump and to pump on the load lock/preparation chamber individually. The base pressure we obtain in the main chamber is approx. P=3 × 10^{-10} mbar.

The preparation chamber is a separate vacuum chamber specifically designed for sample preparation. It contains a transfer arm, tip/sample storage, a heating stage, a pressure gauge, a sputter gun with argon gas handling system and an additional flange to install an evaporator in the future. The chamber is pumped by a Edwards nEXT300 turbo pump connected at the bottom and situated under the table plate (see Fig. 3.1). The central part of the sample preparation is the resistive heating stage (OmniVac SHR 40H) for sample heating up to 800°C. The stage is mounted on a rotatable flange, this way we can rotate the sample plate towards or away from the sputter gun on top or the (future) evaporator on the side. This also allows us to set the sputter angle (typically 45° angle). For the sputtering, bombardment of the sample with accelerated Ar^+ ions to remove the top layers of the sample, we use a Prevac Ion Source IS 40C1. The base pressure we obtain here is also approx. P=3 × 10^{-10} mbar.

Initially we used the preparation chambers to load samples. We would vent the chamber, load tips and samples, pump it down and bake the chamber until we would reach a base pressure in the order of ~ 10^{-10} mbar. Even though we managed to minimize the volume of the chamber and utilized primarily UHV compatible materials, the baking time often exceeds 2-3 days. To speed up the process we replace a viewport with a VAT valve and attached a small, custom cross together with a short stroke transfer arm (Ferrovac) as a load lock. The load lock is pumped by its own Pfeiffer Hipace 80 turbo pump down to a pressure of P=5 × 10^{-8} mbar after 1 hours of baking at T=150°C and 2 hours cool down. The elevated pressure in the preparation chamber due to loading the sample is relieved within few tens of minutes. The newly added load lock therefore makes a dramatic impact on the operation speeds of the full system, especially when frequent replacement of tips and samples is needed.

3.6. VIBRATION ISOLATION

3.6.1. CONCRETE ISLAND

Our microscope is part of and constructed in the recently completed Leiden University Ultramicroscopy Hall specifically built for ultra low vibration microscopy facilities. Its main assets are the 30 ton reinforced concrete measurement islands or blocks. Their weight combined with the four vibration isolators on each corner under the blocks yields

a very low resonance frequency of about 0.9 Hz. The STM table with its own vibration isolators discussed in the next section are directly placed on such an island.

3.6.2. VIBRATION ISOLATION TABLE

The vibration isolation table is adapted from the table described in the thesis of Irene Battisti [13], see Fig. 3.1a. It consist of a triangular, hollow, but rigid stainless steel frame and a 40-mm-thick triangular aluminum plate that is screwed on the three support attached to the frame. We adapted the original design by adding a large opening in the center of the table to accommodate the ion pump that hangs under the main vacuum chamber. We further added another (smaller) opening to create space for the turbo pump connected on the bottom of the preparation chamber. The complete vacuum system is firmly screwed to the plate around the two openings. The table frame rests on three 28 inch tall Newport S-2000A-128 pneumatic vibration isolators with a resonance frequency down to 1 Hz at maximum weight load. To increase the weight of the table and to dampen acoustic vibrations in the frame we fill the compartments inside the frame with close to a ton of lead shots that should bring the resonance frequency down to approx. 1.6 Hz

3.6.3. EDDY CURRENT DAMPER

The combination of the high mass with the soft springs gives rise to the very low resonance frequencies for the concrete island (0.9 Hz) and the vibration isolation table (1.6 Hz), allowing only low frequency vibrations to be transmitted like a low pass filter. Convolution of that frequency response with that of a very rigid STM head (i.e. high pass filter) with a resonance frequency in the order of several kHz shows how we obtain the lowest possible vibration levels between tip and sample [14].

The STM head is often rigidly connected to the vacuum system and hence the table via an insert that also holds the head in a liquid Helium dewar. The main challenge for these inserts is to use as little material as possible to reduce the thermal load (and therefore liquid He consumption) while still making the construction very stiff [4, 6, 12]. The STM head is screwed on the bottom of the insert to obtain a system with low damping, but a high resonance frequency. In the system described here, the STM head hangs on springs and is equipped with an eddy current damping system [8] as indicated in Fig. 3.2. Extra damping is not always desirable since it worsens the efficiency of vibration isolation for frequencies beyond the natural frequency [14]. However the STM and the attached He tank are (indirectly) connected to the N_2 tank. The boiling of N_2 is known to be more violent than He and introduces white noise close to the STM. The eddy current damping system helps to reduce the impact of these vibrations. It consists of three vertical plates attached on top of the STM head each separated by 120° and hanging in between two small magnets as shown in Fig. 3.2a. The movement of the conducting plates through the magnetic field as it vibrates induces eddy currents that create an opposing magnetic field that counters the original field. That leads to damping of the field, a drag force on the plates and heat induced via the currents [15].

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4

PROOF OF PRINCIPLE EXPERIMENTS

Parts of this chapter have been published in Nanotechnology **30(33)**, 335702 (2019) [1].

4.1. INTRODUCTION

On our path towards an ultra-stable smart tip STM and thereby also a future double-tip STM we first want to demonstrate a few individual elements with these proof of principle experiments. For example, it is *a priori* unclear whether a nanofabricated tip will function for STM measurements, as several challenges arise: the stability needs to be below the picometer scale, stringent requirements exist on the shape and sharpness of the freestanding tip, and contamination from fabrication residues need to be absent. In the first section of this chapter, we demonstrate the feasibility of nanofabricated tips and the novel smart tip platform. We do this by implementing the single tip devices described in the previous chapter in a commercial STM system using a custom tip holder. Next we investigate the performance of the tips using low temperature measurements on a Au(111) surface. We further show that in-situ tip preparation such as voltage pulsing and mechanical annealing work; an important extra feature.

As we move from a single-tip device to devices with multiple contacts we also require an STM that houses multiple electrical contacts to the tip. This, among others, is one of the reasons that motivated us to build a dedicated STM for our new platform. The STM, its design and its features are extensively described in Ch. 3. The performance of the new homebuilt STM is another key part towards a fully functioning smart tip system. We therefore want to highlight its performance using traditional metal wire tips (here we use commercial PtIr tips). We commence with a detailed look at measurements taken on Au(111) samples at 4.2 K and under UHV conditions. We then look at the noise we measure on the tip sample junction to demonstrate it's stability.

Lastly we implement a double-tip device into the newly built STM in an attempt to verify its performance as we tunnel from *one of the tips*. It is in this section where we also present our in-house developed tip holder with three contacts to the chip. We will see that some of the choices made during its development turn out to have implications for the original metal wire tip holders as well. We aim to look at the *single tip* performance of the devices because at this stage to get both tips into tunneling requires further effort. The devices used here are the result of the next chapter where we discuss the remaining steps that need to be addressed to get both tips into tunneling simultaneously. The necessary preparations to get one of the two tips into tunneling and how to select which tip that is, are reported in this section as well.

4.2. SINGLE SMART TIP IN A COMMERCIAL STM

4.2.1. IMPLEMENTATION

Our microfabricated tips rely on and are compatible with existing STM systems and only requires the modification of the tip holder. Here we loaded the tips into a modified commercial Unisoku 1500 ultra-high vacuum STM with an operating temperature down to 2.3 K. We customized the original Unisoku tip holder to fit the smart tips. The original holder is made out of a single piece of BeCu that holds the tip and provides the electrical contact. As we start by using a single tip device described in the previous chapter, we do not yet address the additional complications that arise from having multiple contacts on the tip and consequently the tip holder. That means we can use a holder that is similar to the original and is made out of a single metal part and simply replace the hole for the

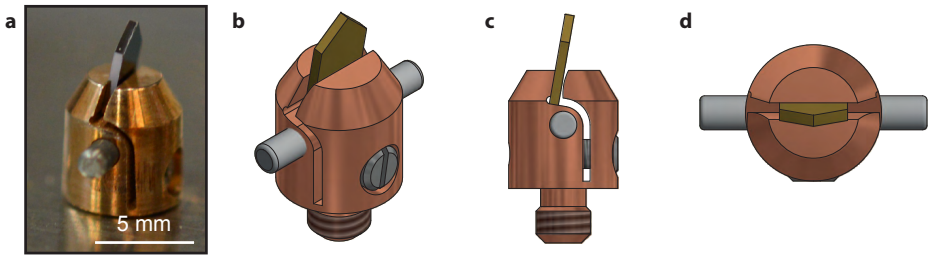

Figure 4.1: **a** Photograph of custom made smart tip holder for the (modified) Unisoku 1500 STM. **b** CAD render of the same holder. **c** Side view render that shows the clamp on the right fixed by a screw and shows the angle of the chip. The metallized top plane of the chip is on the left. **d** Top view render of the holder, here the metallized plane is on the top side.

metal wire tip with a slit in which we clamp the chip. The design and resulting holder are shown in Fig. 4.1. The metal covered top side of the chip is placed against the body of the holder and thereby creates a large metal-to-metal surface to ensure good electrical contact (few Ohms) and a clamp pushes against the bottom of the chip. The chip is placed under an angle of 10° to avoid contact between the Si sidewall of the chip and the sample. As the metal tip is electrically isolated from the Si by the SiN layer and because Si is highly resistive at low temperatures, tunneling can only originate from the metal tip itself.

4.2.2. SMART TIP PERFORMANCE

Next, we demonstrate the performance of the nanofabricated tips, and show that they are fully compatible with STM. For this, we use a single tip smart tip covered by a 20 nm gold film. After having verified that such tips routinely achieve atomic resolution without any tip preparation in ambient conditions on freshly cleaved graphite, we move to atomically flat Au(111) for more reliable tests. We use an Au(111) film on mica at 5.8 K under UHV conditions. The gold surface is prepared by cycles of Ar^+ ion sputtering (1 kV at 5×10^{-5} mbar) and subsequent annealing at 600°C for 1 min. We use standard tip cleaning procedures, such as voltage pulsing up to −3 V and mechanical annealing [2, 3]. The latter procedure consists of repeated and controlled indentation of the tip into the surface up to several conductance quanta and leads to a crystalline, atomically sharp tip apex [3]. All these procedures worked repeatedly with our microfabricated tips.

Fig. 4.2a shows a typical STM image (99×99 nm^2) of the reconstructed Au(111) surface obtained with the fabricated tip (setup conditions 100 mV, 300 pA). The herringbone reconstruction characteristic to these gold surfaces is resolved in great detail. Several of the kinks of the reconstruction lines house a single adatom identified as bright spots. Around the three contiguous adatoms in the center of the image, we can observe rings that show the waves of electron scattering, also known as Friedel oscillations. Similarly, quasiparticle interference spectroscopy [4] allows us to measure the dispersion of the surface state, shown in Fig. 4.2b. To quantify the lateral resolution of the tip we extract line traces over the atomic step from the topographic data. The width of the step edge is 1.3 nm, matching with values obtained from measurements with a conventional tip on

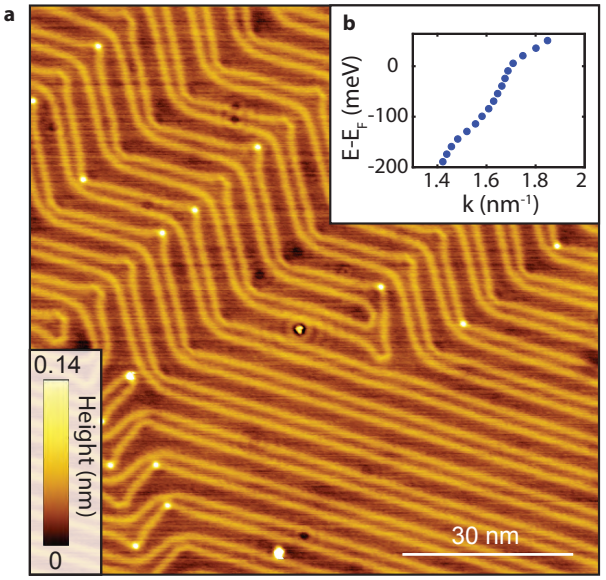

Figure 4.2: **a** Topograph of Au(111) surface taken with a fabricated tip at 5.8 K (V_b = 100 mV, I = 300 pA). We observe the herringbone surface reconstruction as well as single adatoms (bright dots). In the center a cluster of three adatoms is surrounded by Friedel oscillations. **b** Dispersion of the surface state measured by quasiparticle interference.

the same system.

The lateral stability of these tips could be a reason of concern, given their planar nature. Finite element simulations show, however, that the resonance frequency is very high, for both oscillations in the plane and perpendicular to the plane of the tip. Experimentally, we verified that changing the scan direction in the our of plane direction of the tip does not show any difference in the performance of the tip.

We have thus established the functionality of smart tips and that they are fully compatible with existing (commercial) STM systems. We have tested their performance and demonstrated that common tip preparation techniques such as voltage pulses and mechanical annealing can be applied to improve the tip quality in situ, which is an important aspect when using STM.

4.3. SMART TIP STM PERFORMANCE

Before we can start testing smart tips with two protruding tips, we first need to test the performance of our newly built microscope. Here, we briefly demonstrate the performance. We do this by taking topographical data on atomically flat Au(111). We further measure noise spectra on the tunnel junction to give an indication of the mechanical and electrical noise in the system.

4.3.1. SCANS

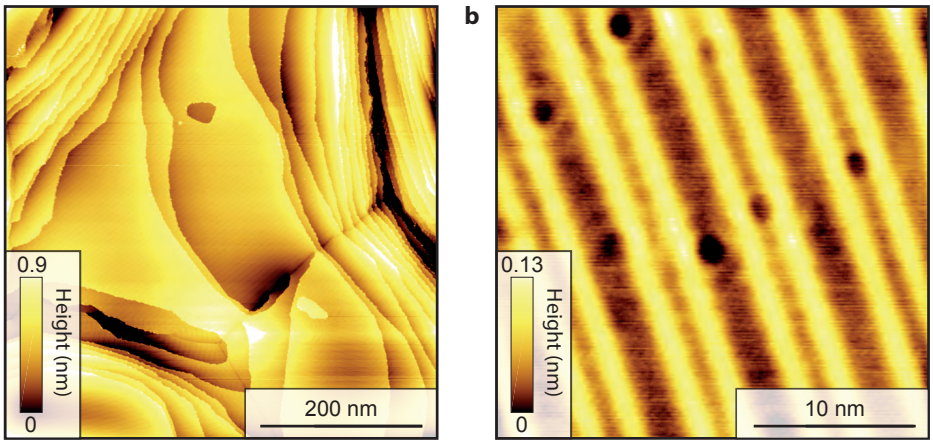

Figure 4.3: Two topographs taken with the new smart tip STM using a conventional PtIr tip at 4.2 K. Both images are not filtered and we have only removed the top few percent brightest and darkest spots for improved clarity and performed a line subtraction. **a** Large area topograph of Au(111) surface taken at $V_b = -100$ mV, $I = -70$ pA. We clearly resolve many step edges as well the herringbone reconstruction on the flat terraces. **b** Topograph of Au(111) surface taken at $V_b = 100$ mV, $I = 101$ pA. The striped pattern is again the herringbone reconstruction and the dark spots are adsorbed CO molecules.

First we show the topographic capabilities of the microscope by obtaining topographical data on atomically flat Au(111). For these measurements we use the default tip holder (Fig. 3.2d,e) together with 250 μm diameter PtIr wire tips that are hand cut. The preparation of the Au(111) surface differs slightly from the preparation described in the previous section since in this microscope we use a different heating mechanism and the ion source is closer to the sample. The parameters we use are indicated for every measurement.

For the topograph in Fig. 4.3a we clean the gold film with three cycles of Ar^+ sputtering (0.75 kV, 3 mA at 5×10^{-5} mbar for 15 min) and subsequent annealing around 390°C for 30 min under UHV conditions. The topograph shows the Au(111) surface over a large field of view of 533x533 nm^2 and is taken with setup conditions $V_b = -100$ mV, $I = -70$ pA. Many step edges are visible over the full range of the image, likely indicating that the annealing has not sufficed to create large flat terraces. However the gold is mostly clean, the tip exhibits no major changes despite the large scanning range and high pixel density. We can also clearly resolve the herringbone reconstruction especially on the larger terraces in the center of the image. Fig. 4.3b shows another topographic image taken on a different Au(111) sample that was slightly differently prepared. Here we decreased the ion acceleration voltage for the sputtering to 0.5 kV and slightly increased the annealing temperature to around 420°C for approx. 30 min. The field of view here is much smaller (27x27 nm^2, setup conditions $V_b = 100$ mV, $I = 101$ pA) and provides us with a clearer and more detailed look on the herringbone reconstruction. Like before, we again resolve Friedel oscillations around the adsorbed CO molecules (dark spots).

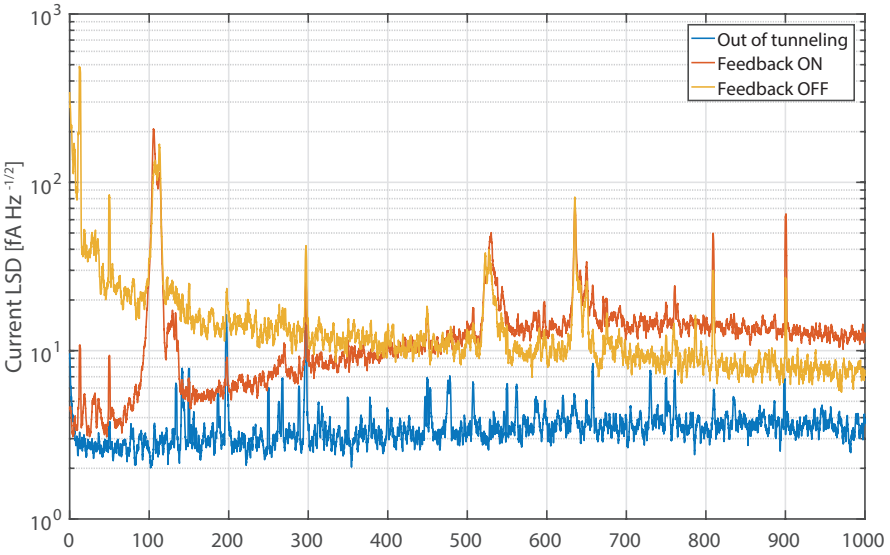

Figure 4.4: Linear spectral density (LSD) of the tunneling current obtained on a Au(111) sample with setup conditions V_b = 300 mV, I = 300 pA. We include data for the out-of-tunneling current and the in-tunneling current with feedback on and off.

4.3.2. CURRENT AND VIBRATIONAL NOISE

We continue with a brief analysis of the (combined) current and height noise measured at the tunnel junction. We do this by fourier transforming real time (averaged) current measurements and we thereby obtain the linear spectral density (LSD) of the tunneling current up to a kHz as shown in Fig. 4.4. This data was taken on a Au(111) similar to Fig. 4.3a,b but with setup conditions V_b = 300 mV, I = 300 pA and an integral gain of 0.8 km/As. All data presented here is an average of 2 spectra consisting of 131072 data points that we smoothed with a moving average over 50 data points for clarity.

We start by concluding that the overall noise is below 1 pA/$\sqrt{Hz}$ even at low frequencies. However we need to be somewhat cautions with the conclusion to the data presented here as they may require further offset corrections. The out of tunneling noise is largely flat as expected but is slightly below the 4.3 fA/$\sqrt{Hz}$ noise floor of the FEMTO pre-amplifier used to detect the signal, indicating that an offset may indeed be present. The noise in tunneling range with feedback *on* shows a 6-8 fA/$\sqrt{Hz}$ increase over the noise floor at frequency over 400 Hz. At the low frequencies the feedback can reduce noise below the noise floor (which can be slightly higher here as mentioned) [5]. For spectroscopic imaging STM the out of feedback performance is of great importance and is therefore also included in Fig. 4.4. The noise level drops to below 40 fA/$\sqrt{Hz}$ at frequencies over 15 Hz and decays to 7-8 fA/$\sqrt{Hz}$ around 1 kHz. The spectra for both in and out of feedback feature narrow peaks of electronic nature (typically harmonics of 50 Hz and 150 Hz) as well as broader -likely mechanical- resonances. These appear at primarily around 12 Hz, 110 Hz, 530 Hz and 635 Hz, but do not exceed 100 fA/$\sqrt{Hz}$ with

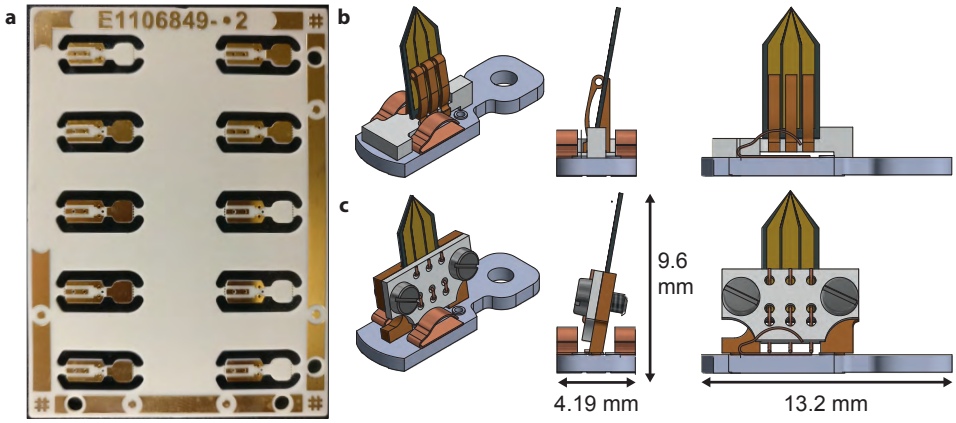

Figure 4.5: **a** Photograph of the bottom side of the UHV compatible printed circuit board containing 10 tip holder base plates of various designs. **b,c** CAD renders with dimensions of the two types of custom smart tip holders.

the exception of the first two.

Taking the presented characterization data into account we are confident that we can obtain good quality topographic and spectroscopic data in future measurement and hereby provide a good foundation to start the implementation of the fabricated tips into this new microscope.

4.4. DOUBLE TIP DEVICE IN SMART TIP STM

4.4.1. IMPLEMENTATION

One of the beneficial features of our smart tip platform is the ability to integrate it into many existing (commercial) STM systems given they have multiple tip contacts. In Sec. 4.2.1 we adapted a Unisoku 1500 tip holder to accommodate a 500 μm thick fabricated tip with a single metal plane as the top surface/contact. Now we take the next step to implement a more versatile and general smart tip design that contains three large contact pads and integrate it into the smart tip STM that uses the RHK PanScan STM head [6]. The main advantages of using our homebuilt system and the RHK head are: (i) we have optical access to the tips and their holders, (ii) the tip holders are already designed for three contacts, therefore they consist of an insulating base plate with the appropriate electrical contacts unlike in the Unisoku STM and (iii) the tip holders are clamped by springs allowing us a little more flexibility in base plate material.

Before we address the changes we have made we will first look at the original tip holder provided by RHK shown in Fig. 3.2d,e. It consists of an insulating Al_2O_3 (white ceramic) base plate that combines an excellent stiffness and good thermal conductivity. BeCu springs are glued on either side to clamp down the holder inside the tip holder receptacle that is glued on the piezo tube of the STM. On the bottom of the base plate we find three electrical contacts made out of approx. 50 μm thick gold that slide over three

conducting balls inside the STM head (Fig. 3.2b). The contacts can be accessed from the top via the three holes that are placed such that they don't slide over on any of the ball contacts. The contact is generally established by filling the hole with conducting UHV compatible epoxy as shown in Fig. 3.2d,e, where we see the metal tube that holds the tip wire connect to the center contact on the bottom of the base plate.

Redesigning this tip holder to fit the smart tips is challenging for many reasons most of which are related to the small dimensions, the fragility of parts and hard to machine materials. The latter finds it origin in the notoriously hard to machine and brittle Al_2O_3. As mentioned it is a very well suited material for this application, but its brittleness can result in breaking of the "flag" of the holder i.e. the little handle where we grab it with a wobblestick. The base plate also has two thicknesses, 0.8 mm under the springs and 1 mm in the center and at the flag, making it a difficult and expensive part to produce. Another challenge is the addition of the gold foil contacts on the bottom and the holes.

We address many of these complication at once with a simple yet effective solution: we switch from Al_2O_3 base plates to UHV compatible printed circuit board (PCB) that combines glass fibers with ceramic materials (Rogers RO 4003 via Eurocircuits). The beauty of this solution is that much of the machining is done by the high quality standard of machining of Eurocircuits, allowing for addition of bottom contacts and accurately aligned drilled holes/vias. We designed the PCB's such that a single board houses ten tip holders (see Fig.4.5a) with various designs providing us with a lot of design flexibility. The difference in cost between a single board and many is relatively small since the fabrication process is highly automated. More information on the different designs will follow shortly.

PCB DESIGN

Let's take one step back. We start with a 0.8 mm thick PCB. That means the full base plate of the tip holder will be 0.8 mm thick. Our motivation for this is to keep the spring forces the same as in the original holder by using the same springs and the same base thickness under the springs. The part of the plate most prone to breaking, the flag, is now 0.2 mm thinner than before. Therefore we also added a holder design where the flags are reinforced by metal plating, 70 μm on each side adding up to an overall thickness of 0.94 mm, very close to the 1 mm in the old design. The idea is that in case of breaking the flag still hangs on the metal and the broken part doesn't fall into the STM head near the piezo's. In addition we removed the hole in the flag which also improve its strength. The gold bottom contacts are now replaced with the 70 μm thick gold plated copper films. The three holes are replaced with vias of the same dimensions, also metallized on the inside. We further added two extra non-metallized holes where the holder for the smart tips can be glued.

CLAMPING MECHANISM

The main challenge for the mechanism that holds the tips is to make it fit within the 2 mm between the springs and to make the loading as convenient as possible given the fragile nature of the tips. To allow for maximum space to make the mechanism we choose to use 200 μm thick chips for the smart tips. The tips themselves and their fabrication are the subject of Ch. 5. We have designed and produced two mechanisms to hold the chips shown in Fig. 4.5b,c. The first is the most straightforward approach, a

back plate with a guiding slot the width of the chip that is mounted in two holes in the base plate under a 10 degree angle (Fig. 4.5b). A second plate can be screwed on to press the chip into the back plate. That second plate has six holes where we run through three gold plated copper wires that we fix in the vias with epoxy. The three wires press onto the contact pads on the chip as we fix the plate and they connect to the three vias. First tests using an Al_2O_3 pressing plate failed because the force caused it to crack. PEEK provides a successful solution due to its flexibility. The alternative design (Fig. 4.5c) consist of three individual clamps made out of phosphorous bronze that can be held open using a special jig. They are all mounted on an Al_2O_3 base part between the springs and connected to the vias using gold plated copper wire. The benefit of this design is that we can see the contact pad once the chip is mounted, however overall it seems more fragile and the loading is harder due to the lack of guiding.

Apart from the two smart tip holders we developed using the PCB base plates we now also use them to replace the standard Al_2O_3 based holder for normal tips. This allows us to mount larger diameter tubes to hold tip of 500 μm mechanically grinded PtIr tips that are commercially available.

4.4.2. APPROACHING WITH A DOUBLE-TIP DEVICE

With all elements in place we attempt to approach the double-tip devices to a Au(111) surface inside the smart tip STM. Our aim here is to bring one of the two tips into tunneling, since simultaneous tunneling from both tips will require further effort (see Sec. 5.4).

Despite us taking great care into mounting the smart tips as parallel to the sample as possible the two tips will not be the same length down to the nanometer and a slight tilt in the sample will occur since it is bottom mounted with epoxy. The main challenge compared to a single tip device is to detect the tunneling current from the tip closest to the sample i.e. that arrives within tunneling range first. We will see in the next chapter that we could estimate which of the tips is longest based on SEM images of the tips and determine which is likely to tunnel first. Given their precious nature we want to avoid such a risk. Rather we want to connect the two tips in parallel to obtain a current that originates from the foremost tip. Once detected we will then need to turn off the feedback (freeze the tip), measure the current on the individual tips, reconnect the foremost tips and resume the feedback. Having the tunnel junction in range but out of feedback makes it very sensitive to vibrations and therefore we initially added a home built switch box to *remotely* (i) connect both tips in parallel during approach, (ii) disconnect both after freezing of the tip and (iii) select individual tips. Unfortunately the relays based switch box introduces significant noise despite being nicely shielded and using a battery as a power supply. It turns out, connecting the two tips in parallel to a single amplifier works to detect the current and perform measurements with one of the tips. Once tunneling is established we can freeze the tip (as far from surface as possible) and manually connect the amplifier to the individual tips and detect a current on one of them despite early concerns.

4.4.3. CHALLENGES

We have attempted to approach the surface with several devices with very limited success, both with the above described switch box, but also with the two tips connected in

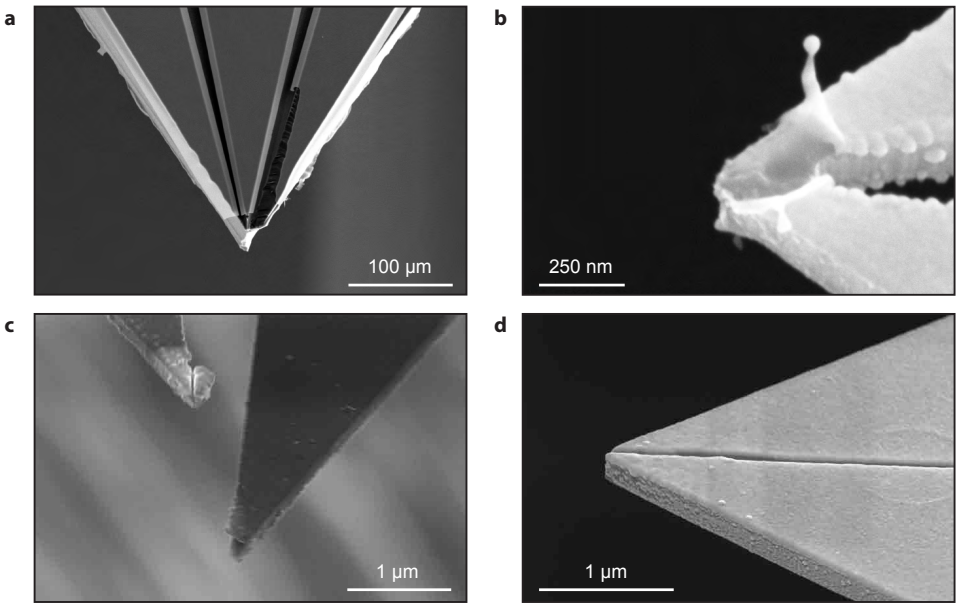

Figure 4.6: SEM images of various double-tip devices. **a** Double-tip device after unsuccessful approach, both the Au/SiN tips as well as some of the Si has been damaged by the impact of the crash. **b** Device loaded into the STM head and taken back out after cool down, showing damage reminiscent of electrostatic discharge. **c** Damaged device after erratic tunneling contact. The two tips have separated and both bent differently. The break did not happen at the milled line between the tips. **d** Prototype device with a larger adjoined area in case fragility turns out to be a major issue.

parallel via coax cables. Typically we do not obtain any tunneling current within a reasonable approach duration and we then abort the approach. Once unloaded from the STM, we inspect the tips with in SEM without taking the chips out of their holder to make sure the damage does not originate from the unloading. An example of the tip after the approach and subsequent crash is shown in Fig. 4.6a. This damage makes it harder to identify the cause of the failed approach.

To identify the cause of the damage we loaded a device into the STM load lock, baked it for several hours to over 150°C, loaded it into the STM head and simply let it cool down to 5 K. Without performing any measurements or approach procedure we then take it out again for inspection. The resulting SEM image is shown in Fig. 4.6b. The ripped off metal layer is reminiscent of damage that occurs via electrostatic discharge (ESD) that is not uncommon in structures with small scale gate electrodes. Fig. 4.6b shows slightly different damage on a very similar device, however the circumstances are different. With this device we managed to get a tunneling contact with a set current of 200 pA at a bias voltage of 0.5 V with the tip we expected from the SEM data (right in Fig. 4.6b). We made the following observations about the tunneling current: (i) current is not stable in time, (ii) the piezotube needs to make nanometer scale adjustments to keep the current at 200 pA, (iii) it is difficult to increase the current beyond 200 pA and

(iv) the current does not scale exponentially with the tip sample distance. This indicates that we are either have large dirt between tip and sample or we are pressing tip and sample together while just getting the metal in tunneling range but not further. The SEM image taken afterwards, shown in Fig. 4.6c, shows that the SiN/Au is broken next to the apex. Whether this results from ESD or forces acting on the tips during contact with the sample remains unclear. If the latter would apply we can simply opt for a tougher design like the one shown in Fig. 4.6d.

Throughout the full fabrication process (Ch. 5) we do not observe any sign of ESD damage. Most likely the discharge occurs when we connect the chips to the tip holder. To eliminate the ESD damage we want to keep both tips at the same potential after the deposition of the metal layer. We achieve this by wire bonding the three contact pads together after deposition. SEM images after wire bonding show no ESD damage after bonding. We proceed to load the tips into their holder while keeping the three contact pad grounded to the body of the STM and remove the wire bonds with tweezers under an optical microscope. Inside the vacuum all three contacts on the bottom of the holder are connected except for when we load the holder into the STM head. The three connections in the head will be grounded to the body using BNC ground plugs on the outside.

The measures proposed above to prevent any ESD related damage to the tips have been implemented and will likely resolve the main obstacle for testing the double-tip devices.

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5

TOWARDS DOUBLE-TIP STM

5.1. INTRODUCTION

A particularly exciting application of our smart tips is to create a chip that protrudes into two electrically isolated tips, with the goal of probing spatial electron correlations and Green's functions related properties. Original theoretical proposals [1–7] and (nearly all) early experiments are based on bringing two or four individual tip into close proximity [8–13], which, to a large extent, has been a long term goal within the multiprobe STM community. Here we aim to use our newly developed smart tip platform to overcome some of the technical challenges that double-tip STM brings, such as navigation of the tips and their tip-to-tip distance to name a few. From a theory perspective two individual tips or a single double-tip device makes little difference as long we have good control over parameters such as the tip-sample coupling and we know the tip separation, both of which we aim to obtain experimentally. The biggest and most fundamental difference lies in the individual control of the tips: being able to move the tips with respect to one another gives more freedom and is, at the moment, better served by theory and simulations [1–4]. In such an experiment the tip-to-tip distance of two individual tips is limited to approximately twice the radius of each tip. In this chapter we aim to address this by using our smart tip platform to create joined double-tip devices with potentially smaller tip separation and increased stability.

We start this chapter with the fundamentals of double-tip STM. What happens if we extend the transport principle from single-tip STM to double-tip? What do we aim to measure? What does it tell us? Specifically we want to highlight two types of experiments, from the outset both very interesting but also challenging. In Sec. 5.2.1 we start with what can be called Green's function STM proposed in the 1990's by [1] and [2] around the same time. The second experiment, described in Sec. 5.2.2, aims to circumvent some of the shortcoming of the first by performing a fundamentally different approach of measuring with two tips. This section results from a collaboration with and is based on (earlier) work by Y.M. Blanter. The experimental range of this method is somewhat limited, however we focus on a single application and provide a feasibility assessment in this section.

In Sec. 5.3.1 we describe the fabrication process of double-tip devices and rapidly it becomes apparent that we build heavily on the groundwork laid in Ch. 2. From there on, in some way, the remainder of this chapter will follow through on the promise of the smart tip as a platform. But not without its challenges as shown in Sec. 5.3.2. Even with the well fabricated double-tip devices at hand, a fully working double-tip experiment, with both tips into tunneling simultaneously requires further effort. What that effort entails we outline in Sec. 5.4.

5.2. PRINCIPLES OF DOUBLE-TIP STM

5.2.1. GREEN'S FUNCTION STM

There are multiple ways to envision a double-tip setup. The most straightforward is to have two tips touching the sample and measure locally the electrical conductivity of the sample between the tips. To eliminate contact resistances that are very large compared to that of the small sample area, these measurements are now often done using a four-probe setup [14] that are commercially available for some time now. Bringing the tips to the tunneling regime unlocks the ability to probe the resistance as a function of position

and avoids damaging the sample [15]. All these measurements rely on clever electronics and switches to assign roles to each probe, to ground (for scanning) the sample or unground (for the measurement) it.

Fig. 5.1 shows that the setup discussed here looks differently. We explore a three terminal setup with tip 1 (μ_1), tip 2 (μ_2) and the sample at a constant μ_0 following [1, 2]. Similar to single probe STM, both tips are voltage biased (V_1, V_2) and the current is individually measured (I_1, I_2) as shown in Fig. 5.1. The individual junction conductances are given by Eq. (5.1).

$$\sigma_i = \frac{\partial I_i}{\partial V_i} = \frac{2\pi e^2}{\hbar}\Gamma_i \rho(\vec{r}_i, \mu_i) \tag{5.1}$$

Where Γ_i includes both the tip-sample coupling and the LDOS of tip i and $\rho(\vec{r}_i, \mu_i)$ is the LDOS of the sample at the chemical potential of tip i. When we consider the properties we probe using two tips in terms of the single electron green's function, the LDOS at each tip are the diagonal elements (see Appx. A) G_{11} and G_{22}. With a three terminal setup like this we can also obtain the off diagonal elements G_{12} and G_{21} that contain further transport properties of the electrons inserted at one tip and collected on the other. In fact, this complementary information should allow -in principle- to obtain the full single electron green's function [1].

This works through a coherent cotunneling process from tip 1 via the sample to tip 2. The transport properties of this process can be derived using Fermi's golden rule to second order and result in a transconductance $\frac{\partial I_2}{\partial V_1}$ we derive in Appx. A following [16]. The same expression, albeit in slightly different form was obtained in the original work [1, 2] when looking at second order transport:

$$\sigma_{21} = \frac{\partial I_2}{\partial V_1} = \Gamma_1\Gamma_2 \frac{2\pi e^2}{\hbar} |G(\vec{r}_1, \vec{r}_2; \epsilon = \mu_1)|^2 \tag{5.2}$$

where $G(\vec{r}_1, \vec{r}_2; \epsilon)$ is the retarded Green's functions of the sample for non-interacting electrons at zero temperature. Inclusion of electron-electron and/or electron-phonon interaction yields the same result if the chemical potential of both tips are equal. When measured at $\mu_1 = \mu_2 = \mu_0$, the retarded Green's functions can indeed be measured according to [1].

Given the second order nature of the tunneling process the signal size is predicted to be small and highly dependent on the tip-sample distance, the band structure of the material under investigation and the dimensionality of the states involved. Explorations [2–4] and very recent measurements [17] concerning the double-tip setup discussed here have focussed on 2D and (quasi) 1D systems mostly where the amplitude green's function is well suited to gain maximum signal. A 1D system is a fine starting point as the signal does not decay with increased tip separation, for 2D, it scales with the inverse of that distance.

Measurements on quantum materials such as (2D) high-T_c superconductors may prove difficult because the surface of these materials is prone to breaking when the tip sample distance becomes too small. To our knowledge only one direct simulation (and no measurements) of the transconductance has been performed on these materials [2]

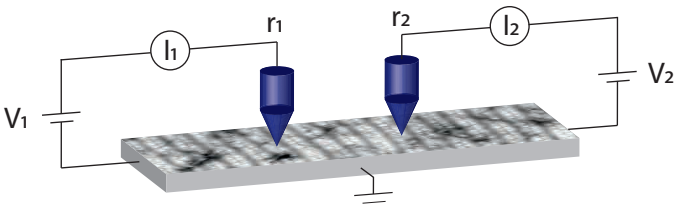

Figure 5.1: Schematic of setup with two tips and a sample (not to scale).

and shows that magnitude of the signal is around 1% of the signal through a single contact, but it is unclear what contact resistance was used (especially since they start of with a contact and a tip instead of two tips).

Another instructive and the most detailed example is provided by Settnes *et al.* [3, 4]. They developed methods to compute the single electron Green's function of graphene in a double-tip setup, leading to real and reciprocal space conductance maps independent of the sample size and thereby revealing scattering information beyond the reach of single-tip STM. Given the long inelastic mean free path of graphene, these conductance maps are predicted to show anisotropies in pristine graphene and quantum interference effects around defects.

5.2.2. DIFFUSION PROPAGATOR ON FINITE SYSTEMS

In order to complement our new experimental platform and explore the feasibility of our approach, we further outline the theory for a novel experiment using two tips on a nano-island for probing the diffusion propagator $\Pi(\mathbf{r_1}, \mathbf{r_2})$ at the nanoscale. We note that this is just one example of accessing Green's functions with double-tips, others are mentioned above [1–7]. Our example has the advantage of being simpler and yielding an improvement of the signal size under specific circumstances. It is based on correlating the two measured single tip currents in order to obtain correlations between electron states at the respective tip positions and to ultimately measure the electronic diffusion propagator.

In this section, we will first describe the specific setup we are considering here. We then derive an explicit expression of the diffusion propagator as a function of our experimental observables. By exploiting the formalism of level and wavefunction statistics developed earlier [18, 19], we show that the correlations of the amplitude of the same wave function are sustained even at these relatively large distances (much larger than the Fermi wavelength), while the correlations between different wavefunctions decay, resulting in the expression that relates the measured currents to the diffusion propagator. Finally, we apply the formalism to metallic nano-islands (Fig. 5.2) and provide some numerical estimates that yield the required sizes of the double-tips.

PRELIMINARIES

The scenario considered here consists of two tips held at individual bias eV_i while measuring the individual currents I_i. The sample is grounded, which considerably simplifies the experiment. We assume a smart tip consisting of two tips located at $\mathbf{r_1}$ and $\mathbf{r_2}$

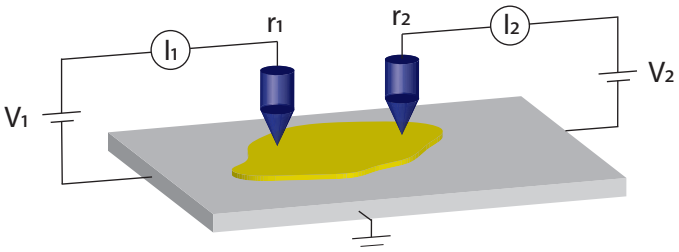

Figure 5.2: Schematic of setup with two tips and a mesoscopic island.

(Fig. 5.2), with the distance between the tips being much longer than the Fermi wavelength. In addition, the tip-to-sample coupling is the same for both tips. As a starting point for the theoretical description of the tunneling process we consider the Tersoff-Hamann model of STM [20], with the tunneling current from each tip to the substrate being [21]

$$I(\mathbf{r},V) = A\int_0^{eV} n^s(\mathbf{r},E)dE\,. \tag{5.3}$$

Here, E is the energy and A is the tip-sample coupling which includes details of the tunneling process, of the tip, and is exponentially dependent on the tip-to-sample distance. The order of magnitude of A is G_T/ν, with G_T and ν being the tunneling conductance (tip to substrate) and the density of states (per volume) in the substrate. The information about the substrate is encoded in the function n^s,

$$n^s(\mathbf{r},E) = \sum_k \delta\left(E-E_k\right)\left|\psi_k(\mathbf{r})\right|^2, \tag{5.4}$$

where E_k and ψ_k are the exact eigenvalues and eigenfunctions of an electron in the substrate.

In the following, we focus on weakly disordered metals, where $k_F l \gg 1$, k_F and l being the Fermi wave vector and the mean free path, respectively. In this situation, the exact energies and wave functions in Eq. (5.4) depend on the disorder configuration, and it makes sense to look at the averages values.

Before treating the double-tip situation, we will calculate the disorder averaged tunneling current for a single tip. The average square modulus of the wavefunction is a constant and, due to the normalization condition, equal to the inverse area vol of the substrate (assuming the geometry is 2D). Then

$$\left\langle n^s(\mathbf{r},E)\right\rangle = \frac{1}{vol}\left\langle\sum_k \delta\left(E-E_k\right)\right\rangle = \nu,$$

and thus $\langle I(\mathbf{r},V)\rangle = AveV$. It is position independent and proportional to the voltage.

CORRELATIONS OF THE TUNNELING CURRENT

Next, we derive an expression for the diffusion propagator in a double-tip configuration. This corresponds to the grounded substrate and the voltages V_1 and V_2 applied to the two

tips. Our aim is to bring the expression to a form that relates it directly to the observables of the experiment, which are the individual currents and their cumulant, defined as

$$\begin{aligned} J(\mathbf{r_1},\mathbf{r_2};V_1,V_2) &= \langle\langle I(\mathbf{r_1},V_1)\, I(\mathbf{r_2},V_2)\rangle\rangle \\ &= 2A^2\int_0^{eV_1} dE_1 \int_0^{eV_2} dE_2 \left\langle \langle n^s(\mathbf{r_1},E_1) n^s(\mathbf{r_2},E_2)\rangle\right\rangle. \end{aligned} \tag{5.5}$$

The double brackets $\langle\langle\,\rangle\rangle$ are defined by $\langle\langle UW\rangle\rangle \equiv \langle UW\rangle - \langle U\rangle\langle W\rangle$. In this expression, the key term to calculate is

$$\begin{aligned} \langle\langle n^s(\mathbf{r_1},E_1) n^s(\mathbf{r_2},E_2)\rangle\rangle = -\nu^2 + \delta(E_1-E_2)\left\langle \textstyle\sum_k \delta(E_k-E_1)\left|\psi_k(\mathbf{r_1})\psi_k(\mathbf{r_2})\right|^2\right\rangle \\ + \tfrac{1}{\Delta} R(E_1-E_2)\times\left\langle \textstyle\sum_{k\neq l}\delta(E_1-E_k)\delta(E_2-E_l)\left|\psi_k(\mathbf{r_1})\psi_l(\mathbf{r_2})\right|^2\right\rangle, \end{aligned} \tag{5.6}$$

where $\Delta = (\nu\cdot vol)^{-1}$ is the mean level spacing for electrons in the substrate, and $R(\omega)$ is the level-level correlation function. The first term in Eq. (5.6) is just a product of the averages – it creates a contribution to J which is proportional to V_1V_2 and is otherwise position independent and can therefore be ignored. It is the second term that is of interest here and we will refer to it as the same-level correlation term. It describes the correlations of the same state at different points in space and we will estimate it in the following paragraphs. The last term describes the correlations of different states and hence contains the level-level correlation function. We show in Appx. **??** that it can also be neglected.

The averages that form the same-level correlation term have been calculated previously in the context of level and wavefunction statistics [18, 19] and we only want to sketch the main steps here. For low energies $|E_1-E_2| \ll E_c$, with $E_c \equiv 2\pi\hbar D/L^2$ being the Thouless energy, and for magnetic fields strong enough to break the time-reversal symmetry for a typical electron trajectory, we obtain

$$\begin{aligned} \left\langle \sum_k \delta(E_k-E_1)\left|\psi_k(\mathbf{r_1})\psi_k(\mathbf{r_2})\right|^2\right\rangle = \\ \Delta\nu^2\left\{k_d(r)\left[1+\Pi(\mathbf{r_1},\mathbf{r_1})\right]+\Pi(\mathbf{r_1},\mathbf{r_2})\right\}, \end{aligned} \tag{5.7}$$

and

$$\begin{aligned} \left\langle \sum_{k\neq l} \delta(E_k-E_1)\delta(E_l-E_2)\left|\psi_k(\mathbf{r_1})\psi_l(\mathbf{r_2})\right|^2\right\rangle = \\ \nu^2 k_d(r)\Pi(\mathbf{r_1},\mathbf{r_1}). \end{aligned} \tag{5.8}$$

Here $r = |\mathbf{r_1}-\mathbf{r_2}|$ and D is the diffusion constant. The short-ranged function $k_d(r) = \exp(-r/l)J_0^2(k_F r)$ decays at the scale of the Fermi wavelength and, since the tips cannot be arranged so closely, does not play a significant role in the correlations. The diffusion propagator Π, introduced earlier, is the solution of the diffusion equation with the corresponding initial and boundary conditions. We disregard the terms with k_d and Eq. (5.7) becomes

$$\left\langle \sum_k \delta(E_k-E_1)\left|\psi_k(\mathbf{r_1})\psi_k(\mathbf{r_2})\right|^2\right\rangle = \sigma\Delta\nu^2\Pi(\mathbf{r_1},\mathbf{r_2}). \tag{5.9}$$

We will see below that the correlation function of the currents is proportional to the voltage allowing us to directly obtain the diffusion propagator. Note that in Eq. (5.9) we included both the situation where the external magnetic field is present to break the time-reversal symmetry ($\sigma = 2$), as well as the case where it is absent ($\sigma = 1$).

We now calculate the contribution of the term with $\delta(E_1 - E_2)$ in Eq. (5.6). The frequency integral is easily calculated, giving

$$\begin{aligned} & J_1(\mathbf{r_1}, \mathbf{r_2}; V_1, V_2) \\ = \; & A^2 \nu^2 \left[\sigma \Delta \min(eV_1, eV_2) \Pi(\mathbf{r_1}, \mathbf{r_2}) - e^2 V_1 V_2 \right]. \end{aligned} \tag{5.10}$$

The second term is the product of average currents, and thus the first one (which is much smaller) contains information about the electron states. Note that this term trivially depends on the voltage and on the magnetic field. The presence of the correlations proves that the states spatially extend from $\mathbf{r_1}$ to $\mathbf{r_2}$. The dependence on the tip-to-tip distance given by the diffusion propagator can be probed by repeating the experiment with different double-tip separations.

As we are interested in the autocorrelations of the shared energy levels between the two tips obtained from the current on each of the individual tips, it is not necessary to measure small currents like the transconductance suggested by Niu *et al.* [1] and Byers and Flatte [2]. We normalize the correlation function with the individual currents $\langle I_i \rangle = A_i \nu \cdot eV_i$ for $i = 1, 2$ and setting $V_1 = V_2 = V$, Eq. (5.10) then reduces to our final result:

$$\frac{J(\mathbf{r_1}, \mathbf{r_2}, V_1, V_2)}{\langle I_1 \rangle \langle I_2 \rangle} = \frac{\sigma \Delta}{eV} \Pi(\mathbf{r_1}, \mathbf{r_2}) - 1. \tag{5.11}$$

This equation directly relates the diffusion propagator to the current correlation normalized by the individual currents. We also note that while the correlations can be long-ranged, one needs nanometer range separation of the tips to measure the diffusion propagator (see numerical estimates below).

NUMERICAL ESTIMATES & FEASIBILITY

Finally, we present some numerical estimates to show the feasibility of our approach. We consider a Pb nano-island on which we scan with the double-tip probe (Fig. 5.2). We set the tip spacing to $r = 30$ nm, a spacing that we consider experimentally viable and that fits within the island. Kim *et al.* [22] concluded that for Pb nano islands of only a few monolayers thickness, the mean level spacing approaches the superconducting gap ($\Delta_s = 1.35$ meV) as the islands in lateral size is reduced to ~50 nm. Our aim is to find an estimate for the signal in Eq. (5.11) in such a scenario.

We start by estimating the diffusion coefficient, $D = \frac{1}{2} v_F^2 \tau$, with τ the scattering time of the electrons. From the residual resistivity ratio in thin film lead we can determine its low temperature resistivity [23], and, using Ohm's law, we find the scattering time for Pb: $\tau = m/(ne^2 \rho_{4K}) = 5.3 \times 10^{-13}$ s. Here, e is the electron charge and we used the low temperature resistivity $\rho_{4\text{Kelvin}} = 9.7 \times 10^{-2}$ $\mu\Omega cm$, the effective electron mass $m = 1.9 \times m_e$ [24] and the total density of valence electrons $n = 13.2 \times 10^{22}$ cm^{-3}. Taken together, this gives us the diffusion coefficient of $D = 223$ cm^2/s.

The size of the island and the diffusion constant, as calculated above, result in a Thouless energy $E_c = (2\pi\hbar D)/L^2 = 36.9$ meV, and, together with the mean level spacing, the dimensionless conductance $g = \frac{E_c}{\Delta} = 27.3$. This value satisfies the condition

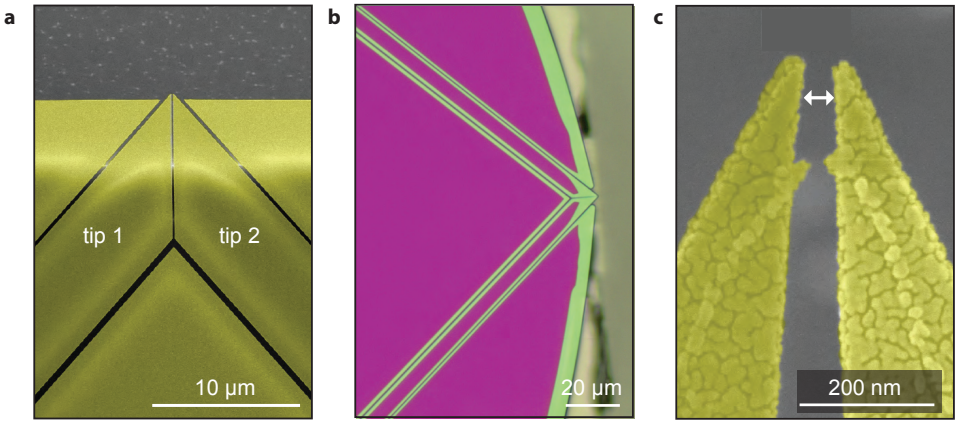

Figure 5.3: **a** (Coloured) SEM image of a double-tip test devices. The full top layer of SiN is covered in gold (yellow) and the trenches (dark gray) create the electrical separation. **b** Optical microscope image of the SiN layer with in purple the SiN attached to the Si and in green the released parts. **c** Third test device using thinner 50 nm thick SiN allowing a tip-to-tip separation of approx. 45 nm (white arrow).

$g = E_C/\Delta \gg 1$ to make the approximation: $\Pi(\mathbf{r_1}, \mathbf{r_2}) \approx \frac{1}{g} \ln \frac{L}{r} = 0.019$. Including the prefactors, in the absence of a magnetic field, we expect the measured ratio in Eq. (5.11) to be on the order of 0.05. We have thus shown that it is in principle possible to measure the diffusion propagator using realistic double-tip parameters. We would also like to note that this is only one example for an experiment using our new platform amongst many others [1–7].

5.3. FABRICATION OF DOUBLE-TIP DEVICES

5.3.1. EXTENDING THE SINGLE-TIP FABRICATION

The fabrication of a relevant double-tip device based on our previously introduced smart tip platform boils down to one main challenge: how do we create two stable and electrically isolated STM tips as close to each other as possible? Many solutions may spring to mind, but here, to start with, we want to stay close to the fabrication described in Ch. 2. That means we stick to using the SiN layer to form the tips but this time also to define the two contact.

The principle is readily demonstrated by three initial test devices shown in Fig. 5.3. Fig. 5.3a catches the essence: using electron beam lithography (EBL) and plasma etching like before, we now simply define a pattern into the SiN containing two tips that each have a pathway down to a large contact pad. We again use the isotropic SF_6 based etch to remove Si from all direction, creating the overhang of the tips together with the trenches we use to cut out the contact pads and the connecting paths clearly visible in Fig. 5.3a,b. This allows us to make both tips and their respective contact pads with a single lithography step. Then we coat the full chip with -in case of Fig. 5.3a,c- a 30 nm layer of sputtered gold.

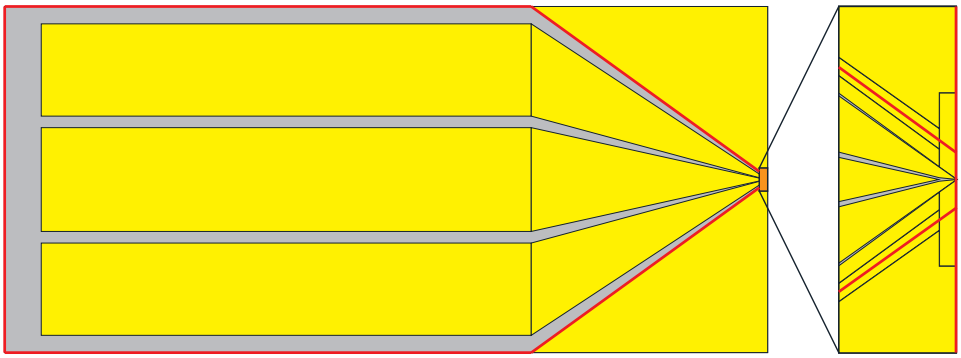

Figure 5.4: (Scaled) Double-tip pattern used for electron beam lithography. The gray areas represent underlying Si and yellow areas the SiN. From the three contacts pads (yellow) only the outer two connect to tips; the centre one, at this stage, is mostly to reduce the exposed area. The inset on the right represents a second smaller pattern we write in the orange block. Here one can see the two tips, the two shields next to the tips and two additional shields on each side. The dice line are indicated in red.

The devices we show in Fig. 5.3 are not fully functioning yet. One element that we want to add is the shields next to the tips, to make the tips protrude beyond the micron shown in Fig. 5.3a,b while keeping as much SiN attached to Si as possible (in other words we want the green parts next to the tips in Fig. 5.3b to drop off). But there is more. The narrow trenches shown here are prone to electrical shorts mostly formed by accidental leftover traces of resist inside the trenches or small pieces of dirt connecting the pads after deposition of the metal. In the final design shown in Fig. 5.4; we have enlarge the spacing between the tips and pads as we move away from the apices of the two tips.

Fig. 5.4 shows the final design is split up in two parts: the contacts pads and the (small) structures including the tips and shields. These two patterns are written using EBL in a single exposure but each with a different beam size and beam step size. The exposed areas are the gray ones in Fig. 5.4. These regions are where the resist is washed away and the SiN is etched to expose the underlying Si. Presently the centre pad is used to reduce the exposed area to speed up the process and to minimize proximity effects of the exposure near the two tips. For future applications it can also connect to the centre of the three contacts on our homemade tip holder (Sec. 4.4.1). We expose the big areas with a 40 nm electron beam with a beam step size of 20 nm and a dose of 400 μC/cm^2. For the small structure we use a smaller beam size of 18 nm together with a step size of 2.5 nm and a dose of 320 μC/cm^2. The SiN layer we transfer the pattern into is unchanged at 194 nm thick and therefore the SiN etch remains the same also.

The dicing of the chips to make them pointy barely deviates from the process described in Sec. 2.3.3. In fact, back in Fig. 2.6, we already used a double-tip devices to demonstrate the principle. The individual dices are also indicated in Fig. 5.4 in red. The only notable distinction is dice lines that create the pointy shape of the chip, they now run through the shields to the side of the tips and simply follow the pattern we wrote. Note that the contact pads never fully extend to the edge of the chip, this is to avoid damage caused when picking it up with a pair of tweezers or by the residue of liquids on

them.

METALLIZATION

After the overhang is created we deposit a metal film. In Ch. 2 we used sputtered Au films to ensure maximum sidewall coverage, meaning that the sidewalls of the SiN are also properly covered. This increases the probability we land with the metal on the sample (even though we but the chip under a small angle). The evaporation of Au films is more directional, but should in combination with a Cr layer underneath show better adhesion to the SiN. We use a Temescal FC-2000 electron beam evaporator to deposit films typically between 3-5 nm and 45-60 nm thick for the Cr and Au respectively. To counter the effects of the directionality of evaporation over sputter deposition we can place the chip under an angle, typically up to 45° and rotate it at 10 RPM to obtain a similar if not better side coverage on the SiN.

5.3.2. OPTIMIZATIONS AND CHALLENGES

Before we demonstrate the final devices we introduce three (optional) optimizations we applied. (i) We can shorten the etch time to reduce the thinning of the SiN during the etch by loading the chips on a Si carrier wafer covered with 4.3 μm SiO_2 instead of the bare Si wafer used before. Because the SiO_2 on the carrier is not etched, the overall etch duration is shortened from ~3-4 min to ~45 s compared to a bare Si carrier. (ii) We can minimize the overhang created on all edges of the contact pads as described below. These overhanging areas -if they break- can cause shorts to the lower lying metal on the Si especially during mounting in their holder. (iii) The third addition involves thorough cleaning of the chip to remove the ebeam resist (ARP6200.13), a problem that increasingly diminishes the yield of the recipe described above. A problem that has become more apparent since we implement the aforementioned tweaks.

Up until now we have simply created both the protrusion of the tips and the overhanging sides of the contact pads with the same isotropic Si etch used throughout this thesis, see Fig. 5.5a. We do this after dicing and subsequent removal of the protective photoresist with acetone and IPA. However, we can also choose to leave the resist used during dicing on and perform the etch, this process we illustrate in Fig. 5.5b. Now only the sidewalls of the chip retract while the top layer is protected, therefore we create the

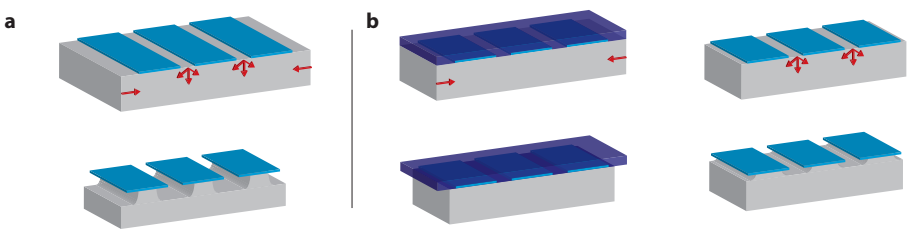

Figure 5.5: Two different fabrication schemes to create trenches between contact pads. **a** Original procedure where we expose the SiN (blue) to isotropic Si etch. **b** Optimized procedure to minimize trench depth and SiN overhang on contacts by covering the top surface by a layer of photoresist (purple).

protrusion of the tip, but no overhang on the contact pads. However we do need that overhang to create electrical separation of the pads. Once the tip overhangs and (almost) all shields are now "hanging" only on the resist, we spray acetone and IPA in the direction away from the tip to prevent the shields from landing on top and clean off the resist. Finally we can perform a very short additional etch to isolate the contact pads, typically between 7-15 s, when using a SiO_2 covered carrier wafer. The result is smaller overhanging regions around the side of the contacts pad. How much smaller is determined by how short the last etch is. The length of the initial (and second) etch we usually determine by optical inspection under the microscope in combination with the approximate etch rate of the Si. The second etch which determines the size of the overhang is typically around 50% shorter when performed in a single etch step without resist.

The full fabrication method for the double-tip devices detailed in this chapter so far suffers from a significantly lower yield than for their single-tip counterparts. This is surprising because apart from the extra steps we described above the fabrication is largely the same. The main cause for the reduced yield is the frequently poor release of the shields around the tips, where they either land on the tips, short two contacts or protrude beyond the tips. The shields are not a strict necessity for the final devices to function and could perhaps be circumvented. However, the underlying reason has become more apparent once we started spraying acetone (and IPA) to remove the protective photoresist. Optical images taken after removal of the photoresist (Fig. 5.6c,d) show sheets/traces of resist residue at the apex of the chip. We hypothesize that this is leftover ARP6200.13 (EBL) resist we know to react with acetone and change consistency. We have no indication of the photoresist being poorly removed by acetone. Surprisingly the resist residue is hardly -if at all- visible with the optical microscope before using acetone. We encountered one example where we managed to see residual resist after cleaning with for 10 min with DMF and 10 min with Positive Resist Stripper (PRS) both at 80°C. However after immersion in 135°C piranha solution for 8 min, which we always perform to clean the ebeam resist, it seems fully removed. Why exactly the resist removal has become more problematic is still unclear. One possibility is bad heat management during the SiN etch, either we etch too long creating more heat than necessary or the thermal conduction of the chip to the SiO_2 covered carrier wafer is worse than before.

Note that although we have a clear understanding of what the problem is, its origin remains somewhat unclear, let's therefore walk through the procedure we use to work around the problem and increase the fabrication yield. We simply add and prolong cleaning steps throughout the fabrication process. It starts by cleaning the ARP6200.13 (ebeam) resist after it is used for the SiN etch. Instead of the two short DMF dips followed by the boiling piranha clean we now add more steps: directly after the etch we perform a 10 min O_2 plasma clean with 0V DC bias in the same machine, then we replace the two dips by two 10 min immersions in DMF and PRS, respectively, both at 80°C followed by the same boiling piranha clean as before. Then, after applying the protective photoresist and dicing of the chip we start with the Si etch. In Fig. 5.6 (from top to bottom) we follow two nearly identical devices after the first Si etch. Fig. 5.6c,d shows that despite the added cleaning steps we still encounter residue near the tips after we removed the protective resist (this is the moment the residue becomes clearly visible). We add another O_2 plasma until satisfied with the cleaning, however beyond 20 min we risk thinning the

SiN slightly. The result is shown in Fig. 5.6e,f and from there we proceed with the final Si etch to release the shields and create the overhang on the contact pads (Fig. 5.6g,h). Finally we obtain a clean device in approx. 60% of cases ready for metallization.

5.3.3. FOCUSSED ION BEAM MILLING

WHY FIB MILLING

The minimum tip-to-tip distance we achieved by having to separate SiN tip coated by a thin layer of (sputtered) Au is >60 nm for 194 nm SiN and 45 nm for the test device using 50 nm SiN. The tip separation is not merely determined by the EBL resolution together with the SiN etch, but also by the thickness and grain size of the metal film; the SiN tips may be very close together, the metal film coverage can join them again. Slightly thicker films also create a radius of curvatures around the two tips and thereby limits the tip-to-tip distance to more than twice that radius, a similar problem to bringing two individual tips in close proximity. Moving towards 50 nm thick SiN and very thin metal films helps (Fig. 5.3c) but brings some uncertainties. First, depending on the length of the overhanging tips, the thin SiN tends to bend upwards more due to the intrinsic stress of the film. While this bend may not be a problem it may not always be equal for both (first indication suggest they are fairly equal if the geometry of the overhanging SiN is equal). Future work may well prove the use of 50 nm to be fruitful, here we want to proceed using the thicker 194 nm SiN in combination with slightly thicker evaporated Au films.

As a result of the excellent control we have over the shape of the tips we can also create devices where the two apices are joined together, both the SiN and Au film, and separate the tips using Focused Ion Beam (FIB) milling. The aim is to mill only the metal layer and keep the SiN attached. A priori this method present several advantages: (i) FIB milling has the ability to achieve higher resolution than EBL [25] especially when combined with a 194 nm deep etch through the SiN, (ii) tip separation is not merely determined by the film thickness, (iii) the mechanical connection formed by the SiN eliminates possible height or tip-to-tip distance fluctuations and (iv) may improve the overall (macroscopic) stability of the tips. Another possibility we leave completely unexplored is the use of electromigration to create the tip separation to possibly even smaller distance down to 5 nm [26], although sufficient control over where the separation occurs seems a priory challenging.

FOCUSSED ION BEAM MILLING

What is focused ion beam milling (and imaging)? FIB imaging is much like a scanning electron microscope (SEM), except instead of an electron beam it uses an ion beam. Secondary electrons are generated by the interaction of the ion beam with the sample surface and can be used to obtain high resolution images [25]. It utilizes Ga^+ ions to interact with the sample for imaging and milling. The milling (and imaging) is done by a highly focused bundle of ions extracted from Ga on a tungsten tip by field emission and is focused by a set of lenses. Here we want to achieve high resolution milling, this requires extensive focussing at high magnification, a low beam current (2 pA) and the smallest aperture available.

The system we use here is the FEI Helios G4 CX: a dual beam system where we can

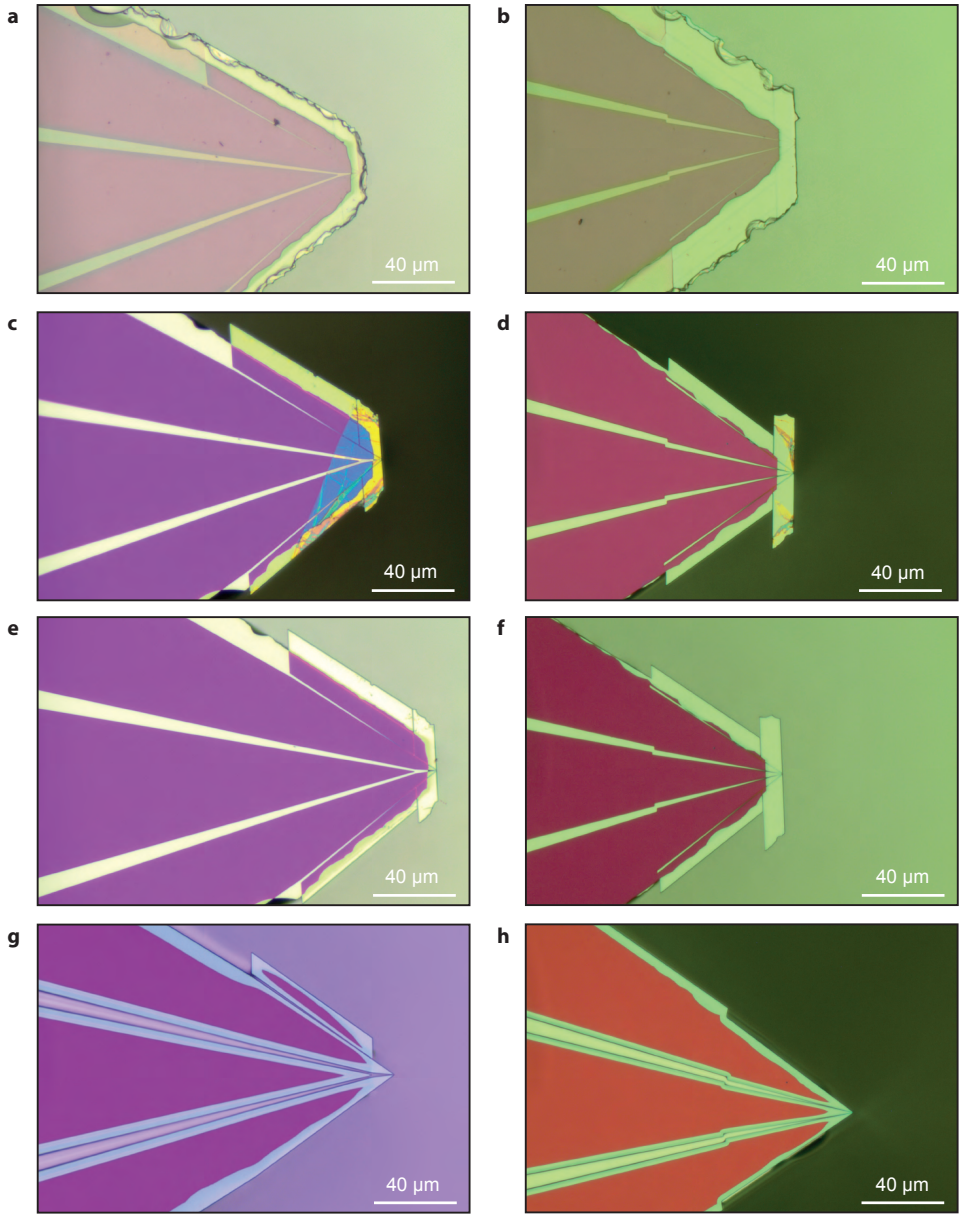

Figure 5.6: Optical microscope images of two nearly identical devices after consecutive fabrication steps. **a,b** Images taken after dicing and a Si etch for 20 s (a) and 40 s (b), respectively. Both still have the protective photoresist on top. Note that (b) has a slight design irregularity. **c,d** The devices after removal of resist with acetone and IPA with various degrees of (EBL) resist residue clearly visible. **e,f** Result after newly added O_2 plasma clean for 5 min (e) and 10 min (f). **g,h** Final device after the second Si etch. (h) has been sprayed with acetone and IPA again, which removed the side shields that stuck due to the design irregularity.

switch between the electron and ion beam mode by tilting the sample. The main caveat of imaging with the ion beam is that it will always mill your sample within the field of view. Having access to the electron beam for imaging significantly reduces the need to image with the ion beam thereby preserving the already thin metal layer on the sample as much as possible. Most of the imaging and navigation on the sample we perform using the electron beam. The ion beam is only used in a few instances: when we check the concentric conditions and alignment between electron and ion beam field of views such that both overlap, when we focus the ion beam at high magnification close to where we want to mill and lastly when we perform the milling itself.

Another well know side effect of FIB milling is the implementation of Ga ions a few nanometers into the exposed top layer of your sample. The Ga^+ enter the sample with high kinetic energy causing a cascade of collision within a volume within the sample. After this has come to a stand still (milling has taken place) what remains is lattice defects, incorporated Ga, and heat [25]. The range of implemented Ga ions can be between 10-100 nm deep and 5-50 nm wide. Although the Ga^+ ions inside the tip material may be cause for concern to whether this has a effect on the quality of the STM tips or on their LDOS, previous experiments have used tips modified by FIB before [27, 28]. In addition we generally pick up (clean) gold from the sample when preparing our tips in-situ using mechanical annealing as described in Ch. 4.

FIB MILLING PROCEDURE & SETTINGS

The milling procedure works as follows. We adhere the fabricated chips, with two metallized tips that are joined together at the apex, to a holder using a piece of carbon tape. It is important that the chip is nicely flat and the tape not very sticky since it also has to come of without breaking. We then pump down the dual beam system to a pressure of ~10^{-6} mbar with the sample holder firmly screwed in to prevent tiny displacements during tilting. We adjust the focus of the electron beam repeatedly as we move the stage to its working distance of 4 mm from the objective. We also correct for stigmatization, make sure the beam is not shifted with respect to the ion beam and take images. Then we pick a reference point at high magnification and tilt the sample 52° towards the ion beam while imaging with the electron beam. The reference point should stay at the same

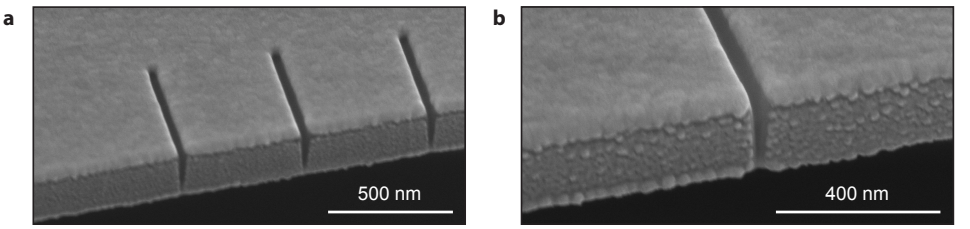

Figure 5.7: SEM images of milled lines on a double-tip device away from the tips taken with FEI Helios G4 CX dual beam system. The gold layer a is 55 nm thick film evaporated under a near 45° angle. The tips of the same device are shown in Fig. 5.8f. All milling is done using pre-set Au milling recipe, we simply adjust the milling depth here. **a** Three line cuts with mill depths of 150 nm, 200 nm and 250 nm from left to right. **b** Closer view on milled line with a depth of 300 nm.

location upon tilting the stage, if not we can slightly correct the height of the stage. Once we turn on the ion beam and image it will start milling, therefore we first find an area close but away from the tip. We can set up such that the field of views of the electron and ion beam are the same and the magnifications are linked. Before we mill we focus the ion beam at 100.000x magnification. Using the electron beam we navigate to the tip we want to mill, take a single scan with the ion beam and place the milling path. After the alignment we often take a second scan to check and compensate for a slight drift in the image. Then we perform the milling over a length of 1-2 μm in less than a second.

Fig. 5.7 shows test lines milled using different settings. As we mill deeper through the Au and into the SiN the cuts become only slightly wider, but the trench width on the sides of the SiN plane increases. With shallower milling we risk the two tips connecting on the very bottom of the sidewall where the width of the trench decreases with respect to the top. For the final devices we present in the next section we stick to either 200 nm or 300 nm milling depth using a preset milling recipe for Au (the SiN is denser).

5.3.4. FINAL DEVICES

Fig. 5.8 gives an overview of several devices we fabricated using the method describe in this chapter. All images are made with a SEM at various magnifications. Fig. 5.8a,b show a macroscopic view on the chips. In Fig. 5.8a we can identify the three contacts pads separated by trenches that are slightly brighter in the image. The narrow bright lines along the pads are the undercut regions consisting of undercut SiN covered in gold (remember the full chip is metallized). In Fig. 5.8b we show the pointy part of the chip under an angle from the side where on the top two out of the three contact pads join to form the two tips. The side view allows us to clearly see the tips protruding from the chip.

We continue with images taken at higher magnification to provide a more detailed view of the apices of the tips. The first example is a test device, shown in Fig. 5.8c, where we follow the same fabrication procedures and design as for the double-tip devices but we omit the FIB step to create a device that has the two contact pad connected and will act as a single-tip device. With this we could test the single-tip performance using the sample tip holder as for the double-tip devices.

Fig. 5.8d shows the apices of two tips from the front under a 52° angle. We can therefore clearly see the metal film also on the side of the SiN layer as well as the separation between the tips that is approx. 35 nm. Another observations worth noting is the slight drift in the FIB milling line that makes it slightly off centre resulting in one tip protruding further than the other. This becomes even more apparent from the top view image of the same device, Fig. 5.8e. What also becomes more apparent is the slight rounding of the gold film near the apex of the SiN, more so than on the other end of the milling line. This raises concerns as to whether the gold film protrudes beyond the SiN. To remove this uncertainty we proceed to deposit a thicker 55 nm (on top of a 5 nm Cr layer) under an angle of approx. 45°, resulting in Fig. 5.8e,f. The thicker film becomes more chunky, especially near the apex of the SiN (the film on the pad for example is smoother) and we set the milling depth to 300 nm. Even though the chuncks of metal make the exact location of the tip more uncertain (therefore also the tip-to-tip distance) we do see the metal reaching beyond the SiN with certainty.

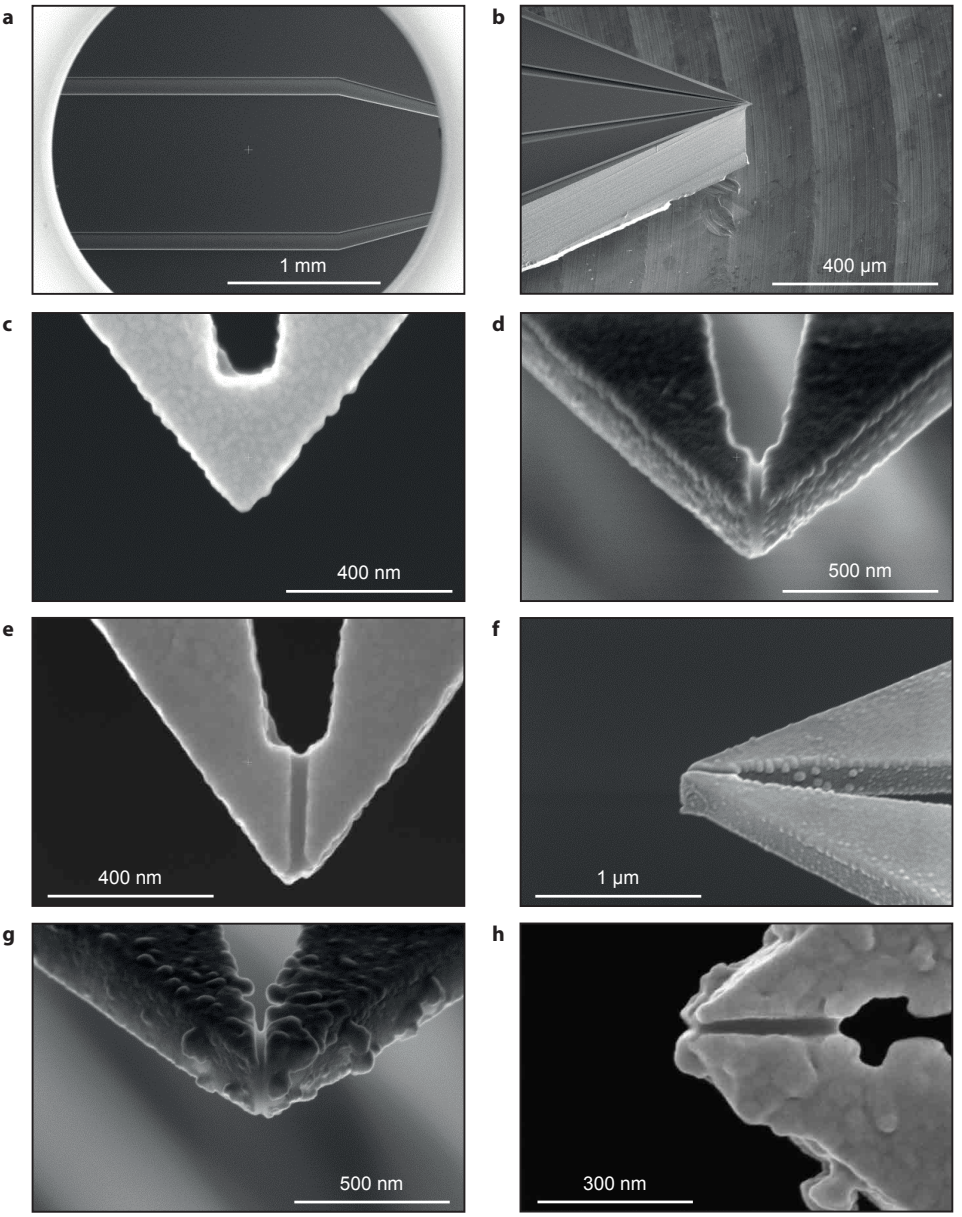
a
1 mm
b
400 µm
c
400 nm
d
500 nm
e
400 nm
f
1 µm
g
500 nm
h
300 nm

Figure 5.8: SEM images of several final double-tip devices with the exception of (c). **a** Top view of the three contact pads separated by trenches. **b** Tilted profile of the device with the protruding tips. **c** Device without any FIB milling. **d** (Angled) front view on the two tips after FIB milling. The tip separation is approx. 35 nm. The tip visible on the left hand side protrudes the furthest. **e** Top view of the same device as (d) showing a slight rounding of the metal film at the apex. **f** Side view on device with 45 nm of gold deposited under a 40° angle. The image clearly shows the gold also covers the sides of the SiN. **g** Front view on two tips with a separation of approx. 30 nm (can be larger depending on where the tunneling arises from) and an even thicker 55 nm gold layer evaporated under a 45° angle creating bigger lumps of material but better side coverage. **h** Top view of the same device as (g) showing clear protrusion of the metal film beyond the SiN.

5.3.5. CONCLUSION

In this section, we have demonstrated that we are able to fabricate double-tip devices with tip-to-tip distances in the order of 35 nm based on the platform presented in Ch. 2. The fabrication method developed here is simply an extension of the single tip fabrication with a focus on geometry: by etching contact pads and the (two) tip geometry into the SiN layer, we can move from single-tip to double-tip devices without adding many fabrication steps. Even though we have shown that the fabrication of two separate tips works and moving to thinner SiN allows us to reduce the tip separation, here we choose to keep the two tips attached via the SiN and only split the metal layer in two at the apex. In principle this should give us more mechanical stability, better alignment of the tips with respect to eachother and remove any electromechanical actuation [29]. It also allows us the exploit the benefits of FIB milling of the relatively thin metal film (compared to the SiN and the metal film together) to make tips that are even closer.

5.4. TOWARDS THE EXPERIMENT

With our newly developed devices and the dedicated, fully functioning, homebuilt STM we have made significant steps towards the realization a double-tip experiment. There are however a few more key ingredients necessary to properly apply the double-tip devices in such a way that we can get both tips into the tunneling regime. In the fabrication process for the devices together with the design and manufacturing of our tip holders we have taken great care to position the tips such that their height is as equal as possible. The difference in length of the two tips will however not be within 1 nm, the requirement for having both tips into tunneling range. Even if that would occur we want to be able to control the tip sample distance for various reasons: (i) in-situ for tip preparation, (ii) to create an optimal setup for imaging and spectroscopy and, (iii) to determine the tip sample coupling for future calculations (this can be obtained by measuring current as a function of tip-sample distance).

We mentioned before that using two individual tips is conceptually straightforward but technically challenging. Both tips have their own "copy" of a single STM setup including a piezo tube, a slider, a pre-amp and a controller. This asks for a complete redesign of the STM head. A separate slider for each tip is not strictly necessary, one could also use two piezo tubes with the tips under an angle as previously demonstrated using a beetle type STM head [8]. Difficulty lies in the navigation of the multiple probes with respect to each other, which used to require either a SEM column for additional visual input [8] or special navigation samples [30]. However over the past decades great progress has been

made to an extend that we can consider it successful. Recent work demonstrating very small tip-to-tip distances manages navigation well: once the field of view of the two tips overlap, the obtained images can be overlain and navigation becomes more clear [17].
Using our approach, both tips also require amplification and a controller, but they share a single piezo tube and slider, making them compatible with systems using a Pan type STM head. Their joined nature demands a more complicated feedback procedure for imaging. To get two tips of unequal length into tunneling requires tilt of several degrees, either on the side of the smart tip or the sample. This may prove to be a large technical hurdle for the joined double-tip approach. One solution would be tilting the sample using additional piezo's for fine tilt motion together with course tilt system, most of which require mechanical rotation of (large) parts [31] and therefore may prove to be impractical. Any such system would also have a large footprint will be hard to implement on sample plates of non-dedicated systems. Piezo stacks that provide slip-stick motion may provide a more compact solution as they are already incorporated in the course motion of the slider and the course XY motion. Other solutions include approaching on (specifically designed) samples with for example a rounded surface such that both tips can achieve tunneling by walking in the XY direction or developing on-chip actuators to retain individual control over both tips [32]. Picking up metal from the sample and reshaping both tips using mechanical annealing may help to reduce unequal tip length in the future but so far has not proven to systematically lengthen/shorten tips with great accuracy.
In conclusion, even with the significant steps made in this work, getting two tips fixed together into tunneling simultaneously remains a challenge and requires further effort. For this reason using a second tip as a local gate (does not require tunneling on both) seems an appealing option for the near future from a technical standpoint and will be the subject of Ch. 6.

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6

SCANNING TUNNELING MICROSCOPY WITH A LOCAL GATE

6.1. INTRODUCTION

In this chapter we briefly explore the possibility of using a second tip as a local top gate to change the carrier density of the materials we aim to study. We are motivated by the prospect of adding an extra "knob" to STM and the simpler experiment it yields compared to double-tip STM. Double-tip STM requires two tips in tunneling simultaneously and that makes it significantly more challenging than getting a single tip into tunneling while having the second tip close by. The second tip is then used to apply a (large) voltage to induce or deplete charge carriers from the surface under the primary tip. The main aim of this chapter is explore whether we can actually create a strong enough electric field to do so and if the experiment is overall worth pursuing.
Having an extra knob to tune the carrier density at the surface allows us -in principle- to probe a larger parameter space (probe more physics) without having to change the sample to adjust doping level. In addition we may be able to induce extra carriers in materials where this has been out of reach so far. Several gating techniques such as top gating, ionic liquid gating or back gating provide the tuning of electronic properties using an external voltage. The first two are not compatible with STM since the gate is on top of the surface. A priori the most suitable electrostatic gate for STM is a back gate, however we will see in the next section that they cannot always be added to a sample or do not achieve sufficiently strong fields. Our focus will be on quantum materials with relatively low carrier densities and, as we will see, in particular Mott insulators at low chemical doping. We will then look at what we need in order to obtain carrier modulation via the second tip whilst performing STM measurements and look at initial simulations of the electric field in a two probe setup. Lastly we will demonstrate a fabricated device optimized for the local gating experiment.

6.2. ELECTROSTATIC GATING IN QUANTUM MATERIALS

Field effect transistors (FET's) have had a nearly unprecedented impact on the field of condensed matter as well as our daily lives. They are not only one of the cornerstones of modern electronics but have also lead to a plethora of findings in modern experimental physics. Their working principle is as follows. The application of an external electric field to a material attracts or repels charge carriers, creating a thin charge accumulation or depletion layer at the surface that modifies the electrical conductivity between a source and a drain contact. The electric field is applied across a gate insulator using a gate electrode [1]. This three terminal setup allows the logical switching by pinching the conduction channel between source and drain, leading to a transistor. The control over the number charge carriers opens up the possibility to study electronic states of matter of the gated material, for example strongly correlated systems among others.
Fig. 6.1, reprinted from [1], illustrates various electronic states of correlated systems as a function of the 2D charge carrier density and includes Mott insulators, semiconductors and organic compounds among others. It demonstrates how the control over the charge density -in many systems- leads to rich phase diagrams, thereby showing the strength of electrostatic gating based on the field effect. Unfortunately most of the interesting phases occur a high carrier densities above 10^{13} e/cm^2. To induce such charge densities one needs to apply a strong electric field which is hard to achieve using the industry

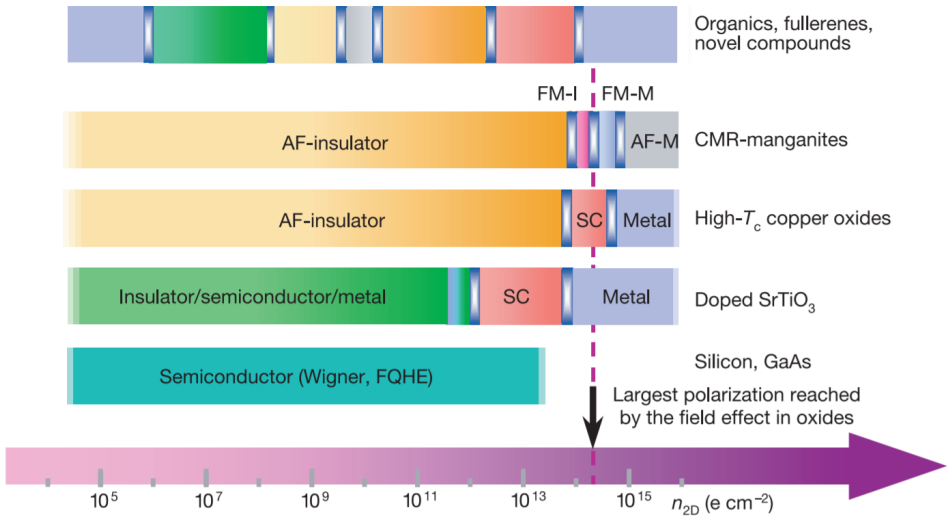

Figure 6.1: Illustration of the zero-temperature behavior of various correlated materials as a function of sheet charge carrier density, reprinted from [1]. That carrier density is indicated by the purple arrow on a logarithmic scale. The colors indicate different electronic phases. We clearly see that at low carrier concentrations most materials indicated here are either in an (antiferromagnetic) insulator or a semiconductor. For the cuprate high-T_c superconductors and the manganites most of the phase transitions occur around 10^{14}-10^{15} e/cm^2. Approaching a superconducting or metallic state is especially important here since STM requires sufficient conduction.

standard SiO_2 as the gate insulator. While nearly perfect as a gate insulator, SiO_2 has a dielectric breakdown voltage of around 10 MV/cm^2 and a relatively low dielectric constant preventing the FET to induce more than 2×10^{13} charges per centimeter squared [1]. More recently significant progress in the development of new gate insulators, often using ferroelectric and complex oxide based materials, has succeeded in gating experiments beyond the capability of SiO_2 [1, 2].

Another recent and initially successful attempt to induce high carrier densities in for example high-T_c superconductors is ionic liquid gating, where a liquid consisting solely of ions is polarized and a layer of ions sits directly on the channel forming. Up to several volts can be applied over a distance of ~1 nm leading to extremely high electric fields at the surface capable of probing the the majority of the phase diagram of a cuprate superconductor [3]. The ionic liquid gating the experiment is generally not limited by a dielectric breakdown but the nature of the doping may no longer be electrostatic but chemical in certain cases [4].

COMBINING GATING EXPERIMENTS WITH STM

In this chapter we want to explore the possibility of combining a local (STM) probe with the electrostatic gating of quantum materials. Traditional top gates using either a dielectric or an ionic liquid cover the surface and are therefore unsuited for high precision STM. We envision a local top gate in the form of a second tip very close to the primary tip.

The study of -for example- cuprate superconductors with STM often relies on chemical (bulk) doping of crystals that require in-situ cleaving to obtain an atomically flat, clean surface. The use of a FET type configuration has the obvious advantage that it does not require many samples with different chemical doping levels but rather a single sample that can be tuned by simply setting a voltage on the gate electrode. That same simplicity holds for a local gate on the second tip and makes it a very attractive experiment from the outset.

TWISTED BILAYER GRAPHENE

An obvious candidate for the application of our newly proposed gating method would be graphene for its low carrier density [5] and compatibility with STM (when cleaned well). Even more exciting would be very recently discovered magic angle twisted bilayer graphene (TBLG) that exhibits numerous interesting physical properties including a Mott state and superconductivity at temperatures below 1.7 K [6]. Transport measurements have uncovered a rich phase diagram that shows similarities to that of the cuprates while structurally less complex and with lower carrier densities of around 10^{11} electrons per square centimeter [6]. Already from the first experiments on magic angle TBLG, the low carrier density has allowed conventional back gating using SiO_2 to probe the (full) phase diagram. More recently TBLG has also been studied by STM to uncover its microscopic details despite that fabricated devices like these are often hard to clean sufficiently well for STM [7, 8]. The ability to clean the surface and therefore allow back gate experiments in low temperature STM makes our proposed probe redundant except perhaps to study the effect of probing tip on the low carrier density material. As a test material graphene based system seems well suited.

CUPRATES AND IRIDATES

Other highly interesting quantum materials that have been widely and successfully studied by STM are for example the high-T_c superconductors like the cuprates or iridates. When undoped, in the parent compound, they are Mott insulators and become superconducting at sufficiently low temperatures by adding carrier via (chemical) doping. There are however many challenges when studying these materials using an STM and electrostatic gate simultaneously. The first challenge is the fabrication of a device with a back gate that can be used to achieve atomic resolution imaging and spectroscopy. To incorporate a back gate the sample would most likely be a heterostructure consisting of a back gate, a gate dielectric and the cuprate top layer. Generally such a structure would be deposited by Molecular Beam Epitaxy (MBE) or Pulsed Laser Deposition (PLD). However in-situ cleaving does not seem to work and significant effort is now made to transfer these layer-by-layer grown material under UHV conditions. Even then, making a device with at least two contacts (top to ground surface and bottom to contact gate electrode) may prove difficult without breaking the vacuum at any step in the process. With the gate electrode next to the STM tips as proposed here we can simply rely on (currently available) crystals that we cleave in-situ under UHV conditions to obtain atomically flat clean surfaces. On a side note, recent progress in isolating monolayer thick cuprate flakes can be combined with a back gate as well [9, 10], but cleaning of the surface may prove challenging.

DOPING A MOTT INSULATOR

As mentioned in the previous section, electrostatic gating of Mott insulators is hard since they require strong fields to induce enough carriers. This brings us to the second reason a vacuum separated top gate in the form of a tip may be helpful: if it can generate a strong enough field it does not suffer from some of the shortcomings of a back gate. We want to stress that, especially for (doped) Mott insulators, engineering a heterostructure with a highly polarizable gate insulator with a clean, lattice matched interface to the Mott insulator remains a challenge even without the inclusion of STM. Limited success has been achieved with Mott insulator based FET's, but often with limited range compared to chemical doping and carefully chosen materials [11]. One of the reasons for the limited success is that the density of trapped interface states can rival the modulated carrier density for the more modern gate materials with a high dielectric constants such as $SrTiO_3$ or $Pb(Zr, Ti)O_3$, but progress is being made [1]. It turns out that gate tunable Mott insulators are an interesting challenge by themselves (also from a commercial point of view) and the payoff would be high especially when combined with a local probe.
If our gating tip will generate a sufficiently large field and if the field has the desired effect, there is one material that we will be an ideal candidate: the strontium doped iridate $(Sr_{1-x}La_x)_2IrO_4$. This material is an electron doped Mott insulator that becomes metallic upon doping and largely resembles the cuprates despite being chemically very different [12]. On top of all the previously mentioned reasons why back gating on these materials is hard in combination with STM, this crystal also requires low temperature in-situ cleaving. Using our tip based top gate this would not make a difference. Secondly, the La doping level in this material has not exceeded 5.5% and the potential presence of superconductivity (mimicking the cuprates) has remained undiscovered. Electrostatic gating could help induce extra electrons locally, but this again requires relatively carrier large modulation.

6.3. PRELIMINARY ELECTRIC FIELD SIMULATIONS

GATE VOLTAGE LIMIT

Before we discuss the simulations of the electric field we can generate with the local gating tip we first need to consider the factors that limit the voltage we can set on the tip. Following Ch. 5 we prefer double-tip devices with the two tips mechanically attached via the LPCVD SiN. The SiN acts as a dielectric separating the two tips by only few tens of nanometers. The maximum voltage we can apply to the gating tip is most likely limited by the dielectric breakdown of the bridging SiN that we estimate below. Following the dielectric breakdown the voltage set on the gating tip will in that case (largely) also be applied on the measurement tip causing it to crash. Arcing between the gating tip and the sample through the ultra-high vacuum is less likely: for samples with weak interlayer coupling it is more likely that the layers tear than any breakdown between tip and sample occurring. At what voltage the sample is damaged, is highly sample dependent and needs to be investigated when performing the experiment. Here we assume that about 2V/nm is still manageable on this material.
The dielectric breakdown voltage of LPCVD SiN at low temperatures is hard to precisely estimate. Here we work with a previously obtained value for room temperature

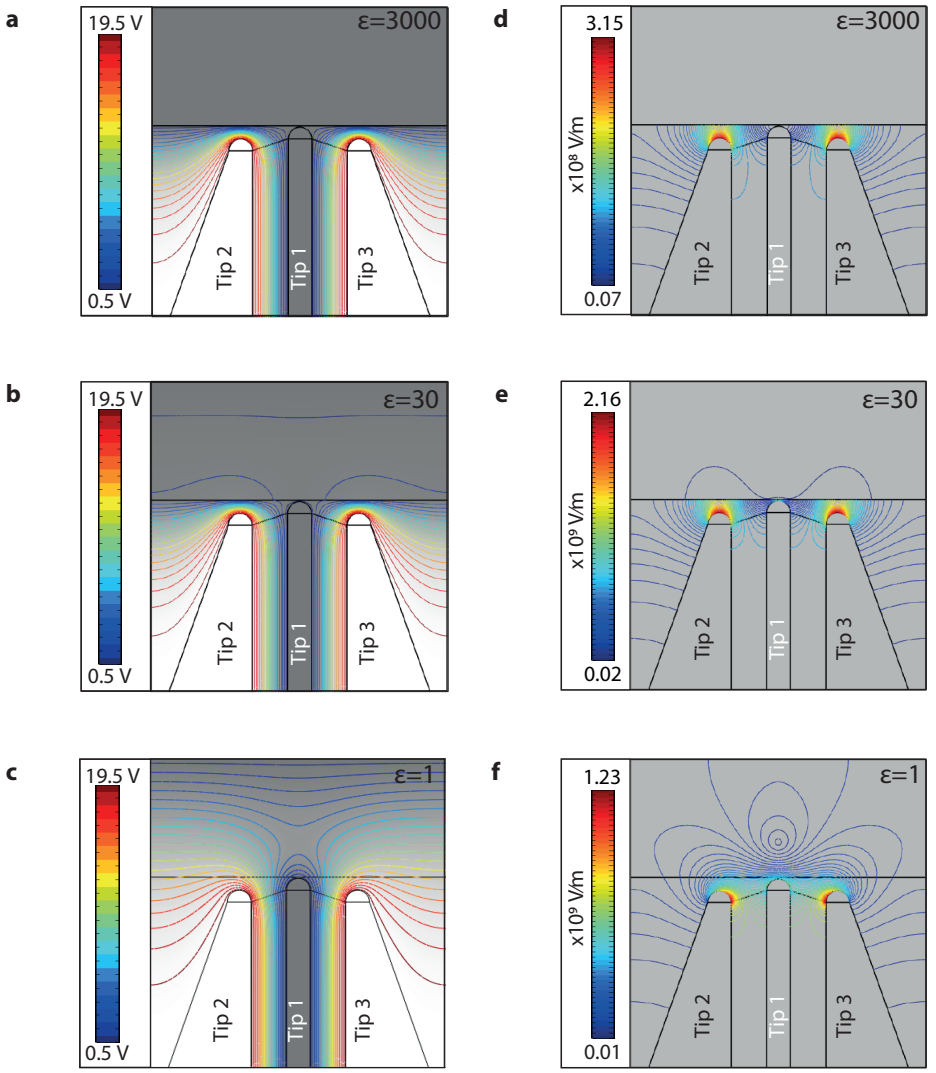

Figure 6.2: Results of finite element analysis performed with Comsol showing the electrical potential (**a,b,c**) and the electric field strength (**d,e,f**) between the three tip geometry and the sample for various dielectric constants. The sample in **a,d** represents a metal (ϵ = 3000) and we clearly see the electric field generated by the gating tips at 20 V is screened almost perfectly at the interface. Moving down, we do observe the field penetrating the sample for $\epsilon = 30$ and the absence of any shielding for ($\epsilon = 1$). Note that for $\epsilon = 1$ the boundaries of the simulation domain affect the shape of the field.

of 10 MV/cm [13]. Since we want to determine a conservative upper limit to the voltage we consider a tip-to-tip distance 20 nm at their closest point. The resulting breakdown voltage should therefore be in the order of 20 V. Although this number may not be very

accurate is does indicate that we can at least apply a significantly larger voltage compared to the measurement tip.
For double-tip devices that are not connected via SiN the dielectric is replace by the ultra-high vacuum and therefore if any breakdown would occur it will likely happen between the gating tip and the sample (they should be closer together). However they may be prone to electromechanical actuation at high voltages.

ELECTRIC FIELD SIMULATION

The two main element in modeling the effect of the local gate electrode on a material like $(Sr_{1-x}La_x)_2IrO_4$ are the electric field strength it induces under the probing tip and what happens inside the material under the influence of the field. Here we report elementary simulations of the electric field resulting from the gating tip. We do this by performing finite element analysis in 2D using Comsol Multiphysics. The geometry and results are presented in Fig. 6.2. At the bottom of each figure we have not two but three tips: in the center the unbiased probing tip (tip 1) and on each side a gating tip (tip 2 and 3). The geometry roughly the shape of the tips we observe in SEM image and we have included the SiN ($\epsilon = 7.4$). Both gating tips are set to 20 V, 30 nm removed from the center tip and kept at 11 nm from the sample. The ground is defined at the bottom of the sample (top of each image).
Fig. 6.2a,d nicely demonstrates that the electric field generated by the gating tips is fully shielded by the sample that is set at an arbitrary, but large, dielectric constant of $\epsilon = 3000$ to represent a metal. The free carriers in a metal efficiently screen the coulomb potential with a characteristic screening depth λ_s =0.5 Å, the same holds for the probing tip and to some extent the SiN between the tips. At 2×10^7 V/m, the field strength at the surface under the probing tip (tip 1) is two order of magnitude lower the under the gating tip due to the shielding. When we assign $\epsilon = 1$ to the sample (Fig. 6.2c,f), setting it equal to the vacuum, we effectively remove the shielding provided by the sample and see that the field penetrates the sample the same way as the vacuum.
In Fig. 6.2b,e we set $\epsilon = 30$ to model the dielectric behavior of $(Sr_{1-x}La_x)_2IrO_4$ following [14] naively treating it as an insulator and see that the field can in fact penetrate the sample. Here, the field strength at the surface under the probing tip is close to 1×10^9 V/m, a similar value to what can be obtained using a SiO_2 based back gate. The field here is a result from the voltage inside the dielectric and the probing tip that is very close at zero bias. The sign of the field here is therefore opposite, from the sample to the tip. The conclusions we can draw from these preliminaries explorations of the electric field generated by two gating tips are limited. The field profile we have shown with a metal sample seems the closest to what the surface will feel from the gating tips and it is heavily shielded by the probing tip. To achieve the electronic changes we desire, we should first look at the carrier density we can induce via the tip field and then focus on what happens within the sample.

ESTIMATION OF INDUCED CHARGE

We can estimate the carrier density at the sample surface using Gauss' law,

$$\sigma = \epsilon\epsilon_0 E \tag{6.1}$$

where σ is the surface charge per unit area, ϵ the dielectric constant between gate and surface, ϵ_0 the vacuum permittivity. Using Gauss' law we assume a conducting surface in equilibrium something we may obtain (locally) when the field ends up strong enough to change the material to metallic. For the electric field we take the local value from the simulations in the previous section and we obtain a charge density around 0.9 $\mu C/cm^2$ or, equivalently, a carrier density of $6 \times 10^{12} cm^{-2}$. This is even lower than the maximum carrier modulation obtained using a SiO_2 gate which is typically around 3 $\mu C/cm^2$. This is to be expected because the field we -optimistically- use here, 1×10^9 V/m, is exactly the breakdown field of a SiO_2 gate, but the SiO_2 has a dielectric constant of 3.9. To obtain a carrier modulation of around 1% in for example $(Sr_{1-x}La_x)_2IrO_4$ we would need a charge density of about 1 $\mu C/cm^2$. For these and the cuprates to trace significant parts of the phase diagram we would require an order of magnitude larger field. The doping level required to reach the onset of superconductivity in $(Sr_{1-x}La_x)_2IrO_4$ -if at all present- is not clear, but above $x = 5\%$. Naturally one could start with a chemically doped sample at $x = 5\%$ that are available.

Utilizing the vacuum instead of a dielectric to perform this type of top gating has the advantage of circumventing -to large extent- the dielectric breakdown. Our calculation reveals a weakness in this approach and that is the low dielectric constant. The vacuum is not a dielectric in the traditional sense. Both have no free moving charge but a real dielectric can be polarized by a slight net shift in the bound charge. That does not occur in a vacuum. Therefore we lose a factor of 3.9 in terms of induced charge compared to a SiO_2 gate and up to 40 to complex oxide and ferroelectric oxide based dielectrics that have been moderately successful in this type of materials [1].

6.3.1. ELECTRIC FIELD INSIDE A MOTT INSULATOR

To confidently assess whether we can achieve any relevant carrier modulation in a lightly doped Mott insulator we need to understand what happens in the material, especially since it appears the purely electrostatic interaction between the gating tip and the sample is likely insufficient. The surface potential that modifies the carrier density decays inside the material with a characteristic length scale known as the screening length λ_s. For semiconductors this screening length can be more than 10 nm [15, 16]. The screening mechanism of a Mott insulator can effectively follow the band bending picture used for semiconductors [17]. From the Poisson equation we can get an expression for the screening length:

$$\lambda_s = \frac{\epsilon \epsilon_0}{e^2 \chi_c} \tag{6.2}$$

where e is the electron charge and $\chi_c = dn/d\mu$ the charge compressibility. The latter can vary strongly upon application of the external electric field and is generally not very well understood in strongly correlated systems. For very low chemically doped Mott insulators the screening length would be very long at zero temperature and gets smaller with increasing temperature. In the very low (chemical) doping limit these materials (at $T = 4\ K$) are too insulating to perform STM measurements. We discussed before that the amount of carriers in Mott insulators as we approach the metallic phase is relatively high ($\sim 2 \times 10^{14} cm^{-2}$). When one applies the screening length for semiconductors for the car-

rier concentration one typically finds in these materials we obtain a screening length in the order of few nanometers only [1]. This seems to be in line with recent measurements on $(Sr_{1-x}La_x)_2IrO_4$ that show the formation of nanometer sized bubbles caused by tip induced band bending (TIBB) [14].
A priori the charge modulation does not seem to extend into the sample beyond a few nanometers. From the experiment mentioned above [14] we know that the STM (probing) tip can have a significant effect on the electronic properties of the $(Sr_{1-x}La_x)_2IrO_4$. So far we have disregarded the field effect of the probing tip altogether because we are interested in what the gating tips add. With a local electric field of approx. 1 V/nm between tip and sample, similar to the (optimistic) value we used above, variation of the energy gap is clearly observed giving some reason for optimism.

6.4. DEVICES

For maximum change in carrier density under the probing tip we aim to achieve an electric field that is as strong and close as possible using a local gate. Here we demonstrate a prototype device that is likely to achieve stronger local electric fields than the device presented in the previous chapter. We do this starting a similar gold coated SiN tip that now connects to all three contact pad already installed before. We again use FIB milling, this time to create three tips as shown in Fig. 6.3. They remain prototypes as the SiN still protrudes beyond the metal. This can be resolved by further optimizing the deposition and fine tuning the milling that now requires two very precisely spaced cuts. Again we also notice a slight misalignment of the two cuts as they tend to shift to the right (see image).

6.5. CONCLUSION

In short, we have shown that electrostatic back gating doped Mott insulators is not only practically challenging but also not very well understood theoretically. Achieving the strong electric field required to modulate the carrier density in the material proves difficult and, to our knowledge, only few experiment have succeeded to some degree. To

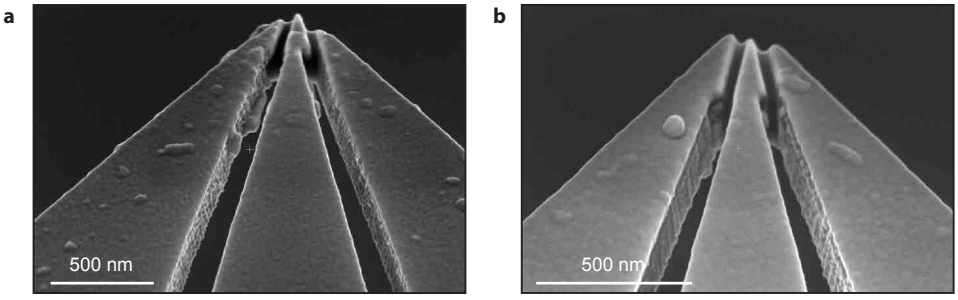

Figure 6.3: **a,b** SEM images of two devices with a primary tip in the center and a gating tip on each side to provide more electric field than a double-tip device.

bring this experiment to the field of STM the additional requirement of an extremely clean surface emerges. To achieve such a clean surface we traditionally rely on in-situ cleaved crystals that do not allow for a back gate. Here, we explored the possibility to use a second probe few tens of nanometers from our primary probe to apply a strong electric field locally and thereby avoiding some of the technical difficulties mentioned above. Preliminary electric field simulations indicate that for poorly screening doped Mott insulators such as $(Sr_{1-x}La_x)_2IrO_4$ the electric field strength under the probing tip can be around 10^9 V/m for a tip-to-tip distance of 30 nm and a sample-to-gate distance of 10 nm at 20 V. Because the material is poorly conducting it does allow the field to penetrate the sample like in a dielectric. The field we simulate is however also a result of the voltage drop inside the material and is likely not representative for the field applied by the gating tip. Apart from the field strength, the key element here is to understand the complex behavior of the Mott insulator which is not very well understood. The screening length however seems to be in the order of few nanometers only. However given the relative simplicity of the experiment and the poorly understood relation between the electric field and the induced carriers in Mott insulators we remain somewhat optimistic that new things can be learned.

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7

CONCLUSION

The main aim of this thesis is to develop a new type of microfabricated on-chip STM tips that we call smart tips, demonstrate their performance and explore their future potential for double-tip experiments and beyond.
Our approach that is the subject of Ch. 2, has largely been bottom up; we have developed a new, relatively uncomplicated, fast and high yield fabrication method to create our smart tips. One of the key ingredients has been the use of LPCVD SiN as a base material to create the tips since they are highly (silicon) etch resistant, straightforward to clean and mechanically rigid. Although the tips we present at the end of Ch. 2 are elementary due to their lack of advanced features such as multiple contacts, their simplicity allowed for easy implementation in a commercial UHV low temperature STM demonstrated early on in Ch. 3.
As a result we have been able to perform important tests to show the performance of the tips on an atomically flat Au(111) surface at 5.8 K. To our knowledge the performance is on par with traditions metal wire tips used in the same system. We also discovered that common in situ tip preparation methods such as voltage pulsing and mechanical annealing work, a very important side note for real world use. After these proof-of-principle experiments, the majority of effort has been focussed on the development and integration of more complex smart tip devices that house two tips separated by only few tens of nanometers.
A large part of that effort consists of the design and construction of a dedicated home-built low temperature STM. One of the requirements for adding extra functionality to the tips beyond the capabilities of a single tip, is to have multiple contacts from the STM wiring to the tip. For the latter we decided to build a dedicated system ourself as described in Ch. 3. However we want to stress that one of the main benefits of our platform is that it only requires multiple contacts and a redesigned tip holder. The STM has been designed for ease of use, low operational cost, stability and with optical access to the tips. The ultra high vacuum system together with the included sample preparation techniques make it capable of preparing many samples including atomically flat metals films that are ideal for testing the new tips. Optical access with an advanced camera system

provides us great control and speed enhancement in approaching tips to the sample. We demonstrate the performance of the STM on Au(111) surface using a traditional metal wire tip by taking topographic images as well as vibration measurements.
In Ch. 5 we succeeded in extending the previously developed fabrication to allow separate contacts and multiple tips without adding a lot more complexity to the process. Unfortunately, even though the fabrication is largely similar, the yield has suffered for reasons still to be determined. Yet we were able to show devices that consist of two tips that are electrically isolated while mechanically still attached. We achieved this by keeping the SiN that forms the base material of the tip attached, cover it fully with gold and lastly use FIB milling to separate the tips down to ~35 nm apart.
Our double-tip smart tips already incorporate three contact pad (two of which connect to the tips) for future applications. To integrate them into our newly built STM we re-engineered the existing tip holder to accommodate the smart tips, see Ch.3. We overcame many of the challenges by switching from an Al_2O_3 tip holder to one made out of UHV compatible printed circuit board made by a specialized company in a largely automated process. The benefits include time savings, low cost (because of the bulk production) and, therefore, more design flexibility. One of the derived designs we now even use to replace the traditional wire tip holders in our system.
At the time of writing, the definitive tests of the double-tip devices in the STM, part of Ch.3, are still ongoing. Several challenges have presented themselves in preliminary tests such as suspected electrostatic discharge that destroys the apex of the two tips. However, we remain confident that these challenges can be overcome and that we can maintain a stable tunneling contact with one of the two tips in the (very) near future.
We end Ch. 5 with the next steps that will be required to get two tips simultaneously into tunneling and scanning. Questions arise whether getting two fixed tips functioning is in fact more straightforward than using two traditional wire tips that was successfully demonstrated recently [1]. However to have one tip in tunneling and the other out of tunneling but only few tens of nanometers away presents new opportunities. We could use the second tip to apply an strong electric field to locally induce or deplete charge carriers at the surface. At first glance this yields a more straightforward experiment and may allow us to provide electrostatic gating from the top to samples where back or liquid gating is impossible in combination with STM. The gating will be ideally suited for electron systems with low carrier densities such as (twisted bilayer) graphene or underdoped high-T_c (like) materials such as the cuprates or iridates. Graphene systems do not require in situ cleaving to obtain clean atomically flat surfaces and often included a back gate capable of tuning the carrier density significantly while performing STM measurement. We believe the Iridate $(Sr_{1-x}La_x)_2IrO_4$ may prove to be a fine candidate because it requires in situ low temperature cleaving [2], it has already been shown the electric field of a tip can bend the bands[3] and adding more dopants chemically has proven difficult. However, preliminary electric field simulations indicate that the field strength that can be applied via the gating tip may not be sufficient for any large effect. We believe that the simplicity of the experiment and mysteries surrounding the relation between the field and the induced carriers in Mott insulators still makes for an interesting experiment.
Beyond the local gating and the actual double-tip experiments we want to outline another application that finds its origin in and expands on recent work performed around

high frequency STM [4–8]. In the next section we outline the potential benefits that our smart tip platform may bring to this emerging field and take a closer look at the challenges that lay ahead. In the last section we elaborate on the improvement in fabrication of the tips in particular with upscaling the production in mind. Larger scale fabrication would increase speed of testing, lower cost and hopefully move the smart tips towards the mainstream.

7.1. TOWARDS ON-CHIP HIGH-FREQUENCY STM

SCANNING NOISE SPECTROSCOPY

STM has long been a technique that utilizes a DC current between tip and sample (with a bandwidth up to few kHz) to study topographical and electronic properties at the atomic scale. Only very recently a new field has been emerging to study electron systems using STM at increasingly high frequencies up to the MHz regime [4–8]. In conventional STM the current noise of the tunnel junction is dominated by 1/f noise while in the MHz regime the thermal noise and shot noise dominate giving access to a new information formerly hidden to STM. The (potential) applications include ultrafast STM, local thermometry [8] and local shot noise measurements. The latter was first reported by Birk et al. [4] for low tunnel junction resistances. Recently Bastiaans et al. [6] and Massee et al. [7] have created low temperature MHz amplifiers that allow shot noise measurements at higher junction resistances making them capable of scanning shot noise measurements with atomic resolution. These are the types of experiments that may benefit from our smart tip platform in the foreseeable future, the challenges and benefits of which we will outline in this section.

Both examples of the so-called scanning noise spectroscopic mentioned above use LC circuits to amplify the signal from the tunnel junction. The tunnel junction itself can be modelled by a resistor and a parallel capacitance. Together with the capacitance interfacing coax cable they form a low pass filter that restricts the bandwidth of conventional STM to the kHz regime [8]. The cable capacitance can be minimized by placing the LC resonator and the impedance matching circuit close to the tip. The impedance matching is done by low noise high-electron mobility transistor (HEMT) that converts the voltage fluctuations over the LC resonator into a current fluctuations sent through a 50 Ω resistor to match the cable and the lock-in amplifier input impedance. The resonance measured by the lock-in amplifier contains contributions from both thermal and shot noise, but the latter is zero at zero bias and can thus be eliminated. The shot noise measured at each point in space is given by $S_p = 2q|I|$ with e as the electron charge and I as the current. We can then obtain the Fano factor F which measures the deviation of the noise from the Poissonian noise of independent tunneling events of electrons. For uncorrelated electrons the Fano factor is unity and for strongly correlated electrons it will deviate [6].

The first experiments using scanning noise spectroscopy have already made an impact in understanding correlated electron systems at the atomic scale [5, 7, 9]. For example they have revealed noise centers, local hot spots where the noise is up to 40 times higher, on very select sites on lead doped BSCCO. The elevated noise level indicates significant charge bunching at these sites and have thereby shed new light on the insulating be-

havior of these macroscopic superconductors [5, 7]. Another pedagogical example is the ability to observe doubling to the charge in superconducting Pb as we move the bias into the superconducting gap. The implications are perhaps more substantial than they appear first glance. This experiment shows that noise spectroscopy could act as a local and direct probe to show the presence of preformed cooper pairs in the poorly understood pseudogap regime [10].

ADDITIONAL BENEFITS OF HIGH FREQUENCY STM

Atomic resolution noise spectroscopy is not the only benefit of high frequency STM. There are more features we want to highlight here that may appeal to a broader community and both are a result of the increased frequency and bandwidth compared to conventional STM. The circuit splits the signal using a bias tee to separate a DC component with a similar bandwidth to normal STM and a high frequency component that goes to the MHz tank circuit. The DC part is necessary for the feedback on the tip sample junction. Not only does this allow to perform the shot noise and conventional spectroscopy at the same time, it also allows to do spectroscopy using a lock-in scheme at MHz frequencies thereby largely avoiding the influence of 1/f noise and vibrations [5, 7]. Moreover the larger the frequency separation between the DC and the high frequency line the more they are decoupled. This decoupling -in principle- enables spectroscopy while in feedback and seems worth exploring especially given the rise of pulse tube based cryogen free STM's [11].

MOVING TO THE GHZ REGIME

We already stressed that the main intrinsic limitation to the bandwidth of any high frequency amplifier in the tunneling regime is the combination of the GOhm junction resistance combined with the capacitance of the coax cable leading to the amplifier that creates a low pass filter in the kHz regime [8]. Therefore the newly developed MHz amplifiers have, among other reasons, moved close to the STM head reducing the length and thereby the capacitance of the coax cable to the actual tunnel junction [6]. To get to even higher frequency regimes and (therefore) gain bandwidth moving the circuitry closer to the tip comes to mind, further reducing the capacitance. This is where our smart tip platform may play a role.

Silicon has been a long standing leading technology when it comes to small scale electronics in both industry and research. On chip high frequency (100 MHz-5 GHz) electronics has become a widely studied and well established field in recent decades. To our knowledge however, there exist only few examples that combines high frequency compatible circuitry with scanning probe techniques [12, 13], non of which include STM. Here we consider two possible implementations of circuits integrated directly on the tip. The first exploits low loss, superconducting coplanar waveguide (CPW) stub tuner circuit to match the impedance of the tunnel junction to 50 Ohm and therefore obtain maximal signal from the junction. The principle has been readily demonstrated on quantum point contacts in the kHz regime [14].

However, a few questions arise whether this is truly feasible both from an fundamental and fabrication point of view. We believe the fabrication of such devices is in fact feasible, but requires additional steps. We could choose to continue with the same design philosophy we use to create the double-tip devices and etch away the SiN between the

center conductor and the ground planes of the CPW. The undercut and subsequent metallization would then create the (superconducting) CPW's separated by vacuum. However it is a priori unclear how the metal in the trenches and sidewall coverage of the SiN would affect the CPW's performance. The size of the undercut we need to create the overhanging tip as well as the stress in the SiN films will put constraints on the geometry, in particular the width of the center conductor. Furthermore we would first strive to have a non-superconducting tip (at first), which would require an extra lithography and deposition step. At this stage it seems therefore more straightforward to first create the circuitry on the chip and connected it to the tip that we create by adjusting the fabrication detailed in Ch. 2.

Even with the fabrication likely to succeed, using CPW based stub tuner suffers a few drawbacks. Most importantly preliminary calculations have shown that matching the tunnel junction impedance requires extreme precision in the length of the stub, has limited bandwidth and is sensitive to capacitance noise [15]. Furthermore the footprint of stub tuners is large given the long wavelength at these frequencies making it challenging to fit on the chips at this size.

A second implementation that utilizes lumped elements shows more promise at first glance. It centers around an on-chip superconducting LC resonator demonstrated recently [16]. The resonator is a planar superconducting coil that has a (relatively) small inductance and parasitic capacitance that together lead to a high resonance frequency ($f = 1/(2\pi\sqrt{LC})$). Here the authors developed it to measure quantum dots with a load of approx. 15 kΩ. Immediately several benefits come to mind both of which are beneficial for our application. Firstly, the coils are very compact with a total size in order to 200 μm and, secondly, they achieve a higher bandwidth compared to their stub tuner counterpart. Simulations will have to show the feasibility of such a matching circuit at around 1GΩ junction resistance.

A perhaps more exciting prospect is the same planar coil as a replacement for the superconducting coils in the circuit used by Bastiaans et al. [6] where they use a HEMT to circumvent the impedance matching of the LC resonator. One can imagine the small coil(s) on the chip and the HEMT and its surrounding circuitry on the -now slightly larger- tip holder. The main questions that need to be addressed are: (i) how do we incorporate the bias tee since it requires a large inductance? (ii) Is there enough cooling power available at the tip holder for the HEMT? (iii) Can we manage with only three contacts (we require an RF line, a DC line, a HEMT power line and a ground)?

7.2. FABRICATION IMPROVEMENTS AND UPSCALING

Among the main strengths of the smart tip platform is the (potential) compatibility with existing commercial STM system, given they have multiple contacts to the tip and enough space to facilitate a custom tip holder. We have also demonstrated two tip holder designs that use a printed circuit board base plate that can easily be made in large quantities at low cost while maintaining good performance and a lot of design flexibility. That leaves the smart tips themselves as the main investment when compared to conventional metal wires tips. To some extent this will always be the case since the fabricated tips are intrinsically more valuable given the amount of fabrication steps and care that goes into them. We believe the benefits they bring can be well worth the extra effort,

especially since that effort can be greatly reduced as we will discuss here.
One of the strengths of nanofabrication has always been reproducibility and scaling, two properties we can also use to our advantage here. So far we have concentrated on the production of few devices at a time with a relatively large amount of manual steps as a consequence of using individually diced chips. While at this stage of the development we believe this approach is justified and allows us to quickly implement design changes where necessary, the future will likely hold a different approach. Once a final device has been established it should be relatively straightforward to upscale the fabrication to produce many smart tips at a time by moving from single chip to full wafer processing. Naturally the production of AFM tips [17] comes to mind where hundreds tips can be fabricated on a single 4 inch wafer. In fact the fabrication of AFM requires more steps and a long KOH through wafer etch that may prove our tips to be even more time effective.
The key element for moving to full wafer processing has already been discussed and (to some degree) tested here (Sec. 2.2.2). It requires replacing the dicing of the chips, the most time consuming and least automated step in the fabrication, by a Bosch etch to cut out the chips. Again, we mostly switched towards dicing because changes can be quickly made and we struggled with the removal of the resist mask after the Bosch etch. The latter can be easily solved by switching to a SiO_2 hard mask instead of the resist mask. The process would work as follows. We use the EBL (now on a full wafer) to define all the tips, we etch the SiN and cover the wafer with a layer of Plasma Enhanced Chemical Vapor Deposition (PECVD) grown SiO_2. Then using EBL or an optical lithography process combined with a SiO_2 etch we can define the chip shapes into the SiO_2. In this step, the alignment of the chips to the tips within a few micron is essential and should be straightforward even optically, since the SiO_2 is transparent. We continue with a through wafer Bosch etch as described in Sec. 2.2.2, which requires about 30-40 min for a 200 μm thick wafer. The SiO_2 is easily, quickly and cleanly removed by immersion into a HF solution [18]. Finally we can undercut the SiN with the isotropic SF_6 etch and deposit the metal.
We expect two main challenges when implementing this process. The first and perhaps most obvious is the uniformity of the etches over the full wafer range. It is know that near the edge of the wafer the etch can give slightly different results than in the centre leading to inconsistent results. If this turns out problematic and optimization of the etches proves difficult, one could always discard the tips near the edges and write as many as possible in the center of the wafer. The second main challenge is the removal of the chip out of the wafer. When we etch through the wafer the chips would become separate entities if we would not keep a small connection from the chip to the wafer. Like with AFM tips the chips can then be taken out from the wafer by breaking the small connecting piece of Si. The location of this connection can be slightly problematic, because it can leave a piece of Si protruding from the edge of the chip. We should avoid the side opposite from the tips because that ensures the chip is nicely parallel to the holder and sample when standing upright. One of the sides is also not ideal depending on the design of the holder; in one of our designs the chip is guided by the mounting plate leaving little to no room for any protrusions on either side. The breaking point of the bridging silicon is therefore ideally confined within the outer dimensions of the chip, or the holder design does not use a guiding slit.

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A

DERIVATION OF THE TRANSCONDUCTANCE

FERMI'S GOLDEN RULE

In this section we take a detailed look at the derivation of the so-called transconductance between two tips following the work of Y. S. Chan [1]. We start with Fermi's golden rule. From Brennan [2] we take the transition rates to first order (given by Fermi's golden rule)

$$W = \frac{2\pi}{\hbar}\left|\left\langle k\middle|V\middle|s\right\rangle\right|^2 \rho_f(E_s) = \frac{2\pi}{\hbar}\left|\left\langle k\middle|V\middle|s\right\rangle\right|^2 \delta(E_k - E_s), \tag{A.1}$$

where s is the initial state, **k** is the final state, **V** the perturbation and ρ_f the final Density of States (DOS).
The transition rates to second order read

$$W_{s\to k} = \frac{2\pi}{\hbar}\left|\sum_m \frac{\left\langle k\middle|V\middle|m\right\rangle\left\langle m\middle|V\middle|s\right\rangle}{E_s - E_m}\right|^2 \delta(E_k - E_s), \tag{A.2}$$

where m are the intermediate states over which we need to sum before taking the square. There is no need for the intermediate states to be real. Note that the transition probability scales with product of the first order transitions and is therefore small.

SINGLE TIP TUNNELING CURRENT

Both tips have their own location r_i, chemical potential μ_i, bias voltage V_i and a measured current I_i. The sample has states ν with a chemical potential μ_ν and energy E_ν. M is the tunneling matrix element of the wavefunctions of tip and sample. For direct tunneling from a single tip to sample Eq. (A.1) now reads:

$$W_{|\mu_i\rangle\to|\nu\rangle} = \frac{2\pi}{\hbar}\left|\left\langle \nu\middle|M\middle|\mu_i\right\rangle\right|^2 \delta(E_{\mu_i} + eV_i - E_\nu) \tag{A.3}$$

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Where we know that $\langle \nu|M|\mu_1\rangle = C_i\psi_\nu(r_i)$ with C_i the tip sample coupling without the DOS of the tip. The tip sample current is then given by:

$$I_{|\mu_i\rangle\to|\nu\rangle} = \frac{2\pi e}{\hbar}\sum_{\mu_i,\nu}\Big[f(E_{\mu_i}) - f(E_\nu)\Big]\Big|C_i\Big|^2\Big|\psi_\nu(r_i)\Big|^2\delta(E_{\mu_i}+eV_i-E_\nu) \tag{A.4}$$

Or equivalently, as shown below,

$$I_{|\mu_i\rangle\to|\nu\rangle} = \frac{2\pi e}{\hbar}\sum_{\mu_i,\nu} -\Big[f(E_{\mu_i}) - f(E_\nu)\Big]\Big|C_i\Big|^2\frac{1}{\pi}Im[G(r_1,r_1,E_{\mu_1}+eV_1)]\delta(E_{\mu_i}+eV_i-E_\nu) \tag{A.5}$$

LOCAL DENSITY OF STATES

The local density of states (LDOS) can be written as:

$$n_\nu(r_i,E_{\mu_1}+eV_1) = \sum_\nu\Big|\psi_\nu(r_i)\Big|^2\delta(E_{\mu_1}+eV_1-E_\nu) \tag{A.6}$$

The general form of the (retarded) Green's function following is:

$$G(r,r',E) = \sum_k \frac{\psi_k(r)\psi_k(r')^*}{E-E_k+i\eta} \tag{A.7}$$

With $\eta\to 0+$ and using $Im[E-E_k+i\eta]^{-1} = -\pi\delta(E-E_k)$ (see below). By combining all this information we immediately get

$$n_\nu(r_i,E_{\mu_1}+eV_1) = -\frac{1}{\pi}Im[G(r_1,r_1,E_{\mu_1}+eV_1)]. \tag{A.8}$$

From Coleman[3] we learn that we can use Cauchy's principle part equation to derive the identity above.

$$\frac{1}{x-i\delta} = P(\frac{1}{x}) + i\pi\delta(x) \tag{A.9}$$

where we multiply both sides by -1 and chose $x = E_k - E$ such that

$$\frac{1}{E-E_k+i\delta} = -P(\frac{1}{E_k-E}) - i\pi\delta(E_k-E)) \tag{A.10}$$

after taking the imaginary part on both sides and realizing that $\delta(x) = \delta(-x)$ we retrieve the identity used above.

DOUBLE TIP CURRENT

We again look at Fermi's golden rule to second order (Eq. (A.2)) and rewrite it for our experiment:

$$W_{\mu_1\to\mu_2} = \frac{2\pi}{\hbar}\Big|\sum_\nu\frac{\Big\langle\mu_2\Big|M\Big|\nu\Big\rangle\Big\langle\nu\Big|M\Big|\mu_1\Big\rangle}{E_{\mu_1}+eV_1-E_\nu}\Big|^2\delta(E_{\mu_1}+eV_1-(E_{\mu_2}-eV_2)) \tag{A.11}$$

With $\langle \nu | M | \mu_i \rangle = C_i \psi_\nu(r_i)$ the direct tunneling from tip-to-sample, where C_i consists of the tip sample coupling without the density of states of the tip.

$$W_{\mu_1 \to \mu_2} = \frac{2\pi}{\hbar} \left| \sum_\nu \frac{C_1 C_2 \psi_\nu^\dagger(r_2) \psi_\nu(r_1)}{E_{\mu_1} + eV_1 - E_\nu} \right|^2 \delta(E_{\mu_1} + eV_1 - (E_{\mu_2} - eV_2)) \tag{A.12}$$

Comparing this to Eq. (A.7) we see that the tip-to-tip transition probability is:

$$W_{\mu_1 \to \mu_2} = \frac{2\pi}{\hbar} \left| C_1 C_2 G(r_1, r_2, E_{\mu_1} + eV_1) \right|^2 \delta(E_{\mu_1} + eV_1 - (E_{\mu_2} - eV_2)) \tag{A.13}$$

Now the total current from tip 1 to 2 becomes:

$$I_{1 \to 2} = \frac{2\pi e}{\hbar} \sum_{\mu_1, \mu_2} [f(E_{\mu_1}) - f(E_{\mu_2})] \delta(E_{\mu_1} + eV_1 - (E_{\mu_2} - eV_2)) \left| C_1 C_2 G(r_1, r_2, E_f + eV_1) \right|^2 \tag{A.14}$$

TOTAL TRANSCONDUCTANCE

The total current between tip 1 and the sample to second order is determined by $I_1 = I_{1 \to S} + I_{1 \to 2}$ (add Eq. (A.4) and Eq. (A.14)).

$$\begin{aligned} I_1 = {} & \frac{2\pi e}{\hbar} \sum_{\mu_1, \nu} \Big[f(E_{\mu_1}) - f(E_\nu) \Big] \Big| C_1 \Big|^2 \Big| \psi_\nu(r_1) \Big|^2 \delta(E_{\mu_i} + eV_i - E_\nu) + \\ & \frac{2\pi e}{\hbar} \sum_{\mu_1, \mu_2} [f(E_{\mu_1}) - f(E_{\mu_2})] \delta(E_{\mu_1} + eV_1 - (E_{\mu_2} - eV_2)) \Big| C_1 C_2 G(r_1, r_2, E_f + eV_1) \Big|^2 \end{aligned} \tag{A.15}$$

We now look at the differential conductance dI_1/dV_1, insert Eq. (A.8) and write $A_i = C_i^2 n_t$ where n_t is the DOS of the tip.

$$\frac{dI_1}{dV_1} = \frac{2\pi e^2}{\hbar} \Big[-A_1 \frac{1}{\pi} Im[G(r_1, r_1, E_{\mu_1} + eV_1)] + A_1 A_2 \Big| G(r_1, r_2, E_f + eV_1) \Big|^2 \Big] \tag{A.16}$$

The first order term can be made positive by using $(-1/\pi) Im(A) = (1/\pi) Re(iA)$.

$$\frac{dI_1}{dV_1} = \frac{2\pi e^2}{\hbar} \Big[A_1 \frac{1}{\pi} Re[iG(r_1, r_1, E_{\mu_1} + eV_1)] + A_1 A_2 \Big| G(r_1, r_2, E_f + eV_1) \Big|^2 \Big] \tag{A.17}$$

Equivalently for tip 2:

$$\frac{dI_2}{dV_2} = \frac{2\pi e^2}{\hbar} \Big[A_1 \frac{1}{\pi} Re[iG(r_2, r_2, E_{\mu_1} + eV_1)] + A_1 A_2 \Big| G(r_2, r_1, E_f + eV_2) \Big|^2 \Big] \tag{A.18}$$

The current between tip 1 and sample as a function of voltage on tip 2 is:

$$\frac{dI_1}{dV_2} = \frac{2\pi e^2}{\hbar} \Big[A_1 A_2 \Big| G(r_1, r_2, E_f + eV_1) \Big|^2 \Big] \tag{A.19}$$

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B

LEVEL-LEVEL CORRELATIONS

This appendix is to consider the contribution of the second term in Eq. (5.8) and is work done by Y.M. Blanter based on earlier work [1, 2] but in a new context. We will see that its contribution to J is less important than the first term in Eq. (5.10), but that it has non-trivial voltage dependence. Since for a single experiment the distance between the two tips is fixed, we can use this non-trivial voltage dependence to look at correlations between different states in the system.
For this we need to consider the last term of Eq. (5.6), where $R(\omega)$ is the level-level correlation function, that in the lowest order is given by the Wigner-Dyson statistics. The theory of random matrices, from where the Wigner-Dyson statistics originates, discriminates between two situations — the absence of external magnetic field (Gaussian Orthogonal Ensemble, of GOE, $\sigma = 2$) and the presence of magnetic field (Gaussian Unitary Ensemble, or GUE. $\sigma = 1$). In GUE we have

$$R(\omega) = 1 - \left(\frac{\pi\omega}{\Delta}\right)^{-2} \sin^2\left(\frac{\pi\omega}{\Delta}\right) . \tag{B.1}$$

The contribution of Eq. (5.8) was dismissed in the same-level correlations due to the strong decay of k_d with distance. To calculate the (small) contribution of the level-level correlations, we need higher order in g^{-1} terms in Eq. (5.8). We get [1, 2]

$$\begin{aligned} &\left\langle \sum_{k\neq l} \delta(E_k - E_1)\delta(E_l - E_2) \left|\psi_k(\mathbf{r_1})\psi_l(\mathbf{r_2})\right|^2 \right\rangle \\ = \quad &\frac{\sigma}{2}\nu^2\Pi^2(\mathbf{r_1}, \mathbf{r_2}) . \end{aligned} \tag{B.2}$$

Furthermore, for energies ω exceeding the Thouless energy E_c, $|E_1 - E_2| \gg \Delta$, we have (note that the two expressions coincide in the main order in $1/g$ where they both apply,

i.e. for $\Delta \ll |E_1 - E_2| \ll E_c$),

$$\left\langle \sum_{k\neq l} \delta(E_k - E_1)\delta(E_l - E_2) \left|\psi_k(\mathbf{r_1})\psi_l(\mathbf{r_2})\right|^2 \right\rangle = \frac{\sigma}{2}\nu^2 \mathrm{Re}\left[\Pi_\omega^2(\mathbf{r_1},\mathbf{r_2}) - \frac{1}{vol^2}\int d\mathbf{r_2} d\mathbf{r_2} \Pi_\omega^2(\mathbf{r_1},\mathbf{r_2})\right] \tag{B.3}$$

and $R_2 = 1$. We again have discarded the short-range terms proportional to k_d. Here,

$$\Pi_\omega(\mathbf{r_1},\mathbf{r_2}) = \frac{1}{\pi\nu}\sum_q \frac{\phi_q(\mathbf{r_1})\phi_q(\mathbf{r_2})}{\hbar D q^2 - i\omega}\,, \tag{B.4}$$

where Dq^2 and ϕ_q are the eigenfunctions and the eigenvalues of the diffusion operator $-D\nabla^2$ with appropriate boundary conditions.
To facilitate the calculations, we take $V_1 = V_2 = V$. Furthermore, as before, we assume that the distance between the tips is much longer than the wavelength. Since $R(\omega)$ and Π_ω are even functions of ω, we can reduce the double integral to a single one using

$$\int_0^{eV} dE_1 dE_2 F(E_1 - E_2) = 2\int_0^{eV} (eV - \omega) F(\omega) d\omega\,, \tag{B.5}$$

where F is an arbitrary even function of ω. Due to non-trivial dependences of our functions on ω, we consider different regimes in voltage.

REGIME 1: $eV \ll \Delta$

For $eV \ll \Delta$ in GUE we substitute Eq. (B.1) for $R(\omega)$, calculate

$$\int_0^{eV} (eV - \omega) R(\omega) d\omega \approx \frac{\pi^2}{36\Delta^2}(eV)^4\,, \tag{B.6}$$

and the contribution to j from the last term in Eq. (5.6) becomes

$$\delta J(\mathbf{r_1},\mathbf{r_2};V_1,V_2) = \frac{\pi^2\nu^2A^2}{36\Delta^2}(eV)^4\Pi^2(\mathbf{r_1},\mathbf{r_2})\,. \tag{B.7}$$

This differs from Eq. (5.10) by the factor of $g^{-1}(eV/\Delta)^3 \ll 1$.
For GOE, the level correlation function is cumbersome, but we only need the low-energy behavior, which is $R(\omega) \approx (\pi^2|\omega|)/(6\Delta)$. Calculating the current correlation function, we obtain

$$\delta J(\mathbf{r_1},\mathbf{r_2};V_1,V_2) = \frac{\pi^2\nu^2A^2}{36\Delta}(eV)^3\Pi^2(\mathbf{r_1},\mathbf{r_2})\,. \tag{B.8}$$

It is the same as Eq. (B.7) except for the additional factor $\Delta/eV \gg 1$, making it bigger than Eq. (B.7). It is still factor $g^{-1}(eV/\Delta)^2 \ll 1$ lower than the contribution of correlations of the same wavefunction.

REGIME 2: $\Delta \ll eV \ll E_c$

For $\Delta \ll eV \ll E_c$ we have $R = 1$, and, calculating the integral again, we find in both GOE and GUE

$$\delta J(\mathbf{r_1},\mathbf{r_2};V_1,V_2) = \frac{\pi^2\nu^2A^2\sigma}{2}(eV)^2\Pi^2(\mathbf{r_1},\mathbf{r_2})\,, \tag{B.9}$$

which is again small compared with Eq. (5.10) as $eV/E_c \ll 1$.

REGIME 3: $E_c \ll eV \ll \hbar D/r^2$

For $eV \gg E_c$, we still have $R = 1$ but now need to use Eq. (B.3) to calculate the current-current correlation. To get the results, we now explicitly calculate evaluate Π_ω in two dimensions. In (B.4), we take $\phi_q(\mathbf{r}) = (vol)^{-1/2}\exp(i\mathbf{qr})$ and replace the summation over q with integration. Integrating over the angle, we get the Bessel functions, and subsequently integrating over the length of q, and we obtain Kelvin functions kei and ker,

$$\begin{aligned} &\mathrm{Re}\,\Pi_\omega(\mathbf{r_1},\mathbf{r_2}) \\ = \;& \frac{1}{4\pi^6\nu^2\hbar^2D^2}\left[\mathrm{kei}^2\left(\sqrt{\frac{\omega}{\hbar D}}r\right)+\mathrm{ker}^2\left(\sqrt{\frac{\omega}{\hbar D}}r\right)\right]. \end{aligned} \tag{B.10}$$

In the case of $E_c \ll eV \ll \hbar D/r^2$, we can use the expansion of the Kelvin functions at low arguments, $\mathrm{kei},\mathrm{ker}(x) = C, C' - (x/2)^2\ln(x/2)$, where C and C' are two constants of the order one. We get

$$\delta J(\mathbf{r_1},\mathbf{r_2};V_1,V_2) \sim \frac{(C+C')\nu^2A^2\sigma}{2\pi^4g^2}\frac{(eV)^3}{\hbar D/r^2}\ln\frac{\hbar D/r^2}{eV}. \tag{B.11}$$

Comparing this with the first term in J, we get

$$\delta J/J \sim \frac{1}{\pi^4}\frac{(eV)^2}{E_c\hbar D/r^2}\ln\frac{\hbar D/r^2}{eV}, \tag{B.12}$$

which in principle can become big, but in practice it is unlikely due to the small factor π^{-4} in front of this ratio.

REGIME 4: $E_c \gg \hbar D/r^2$

In this case, we can replace $(eV-\omega)$ with eV in the integral over ω, and the remaining integral can be calculated exactly. The result is exponentially small $(\exp(-(2eVr^2/\hbar D)^{1/2}))$, and does not play any role.

Note that this regime only makes sense for $r \gg l$ — then $\hbar D/r^2 \ll 1/\tau$, where τ is the momentum relaxation time for scattering at impurities. If $eV \gg 1/\tau$, the electron motion at highest energies is not diffusive, and our approach is not valid.

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SUMMARY

This dissertation mainly describes the path to a new type of metal needle -or tip- for a so-called scanning tunneling microscope (STM). This type of microscope works by bringing a very sharp, conductive needle very close to a conductive surface. When we apply a voltage between the surface and the needle and the distance between them is less than a nanometer, a billionth of a meter, electrons can jump without a medium. This quantum mechanical phenomenon is called tunneling. Tunneling of electrons leads to a current that exponentially depends on the distance between the needle and the surface, so that we can measure the distance very accurately via the current. It is even possible to move the needle over the surface in a very controlled manner while keeping the current constant, this allows us to scan and map the surface. If the needle is so sharp that it ends in a single atom, then we can resolve the atoms of the surface. Traditionally, the needle is a thin metal wire that has been polished or etched at the end to form a sharp apex. Even at the nanoscale, the wire will not end in one atom but will have a certain radius of the order of 5-30 nanometers, but there is always a single atom that is closest to the surface from which the electrons tunnel.

Our goal in this thesis is to replace this metal wire with a microscopic needle that is integrated into a silicon chip that we know from the computer industry. These tips can serve as a platform for new applications, such as electrical circuits or multiple needles next to each other, that can be added via the micro and nanofabrication techniques that we use here. We call these tips smart tips. We also investigate which of the additional options we can implement and what promise they yield. We focus on a number of applications for studying so-called quantum materials. In particular, we are exploring the possibility of making two needles up to a few (tens of) nanometers apart and get both into tunneling in order to create a double-tip STM based on the smart tip platform.

In *chapter 2* we describe the development of the fabrication process of the smart tips and we show the resulting smart tip devices that consists of a single tip that protrudes from and connects to the entire surface of the chip that here serves as an electrical contact. The fabrication is based on a silicon chip covered with a layer of silicon nitride, known for its insulating and mechanically robust properties. By means of lithography with a very narrow beam of focused electrons instead of light, we can write structures on the nanoscale in a thin layer of polymers. We transfer this pattern, which defines the needle, into the silicon nitride by etching. With a very precise dicing machine we dice the shape of the chip, which is pointy, with the tip close to the edge at the apex of the chip. With a plasma we then etch the silicon from which the chip is made such that it shrinks on all sides to make the nitride tip protrude 10-12 micrometers at the apex of the chip. Finally, we cover the entire chip, including the tip, with a thin layer of gold for electrical conduction.

Chapter 3 describes the design, construction and performance of the smart tip scanning tunneling microscope developed here. Because we want to add new applications to the chip and have it serve as a platform, we need multiple electrical contacts. This applies to the chip but also to the microscope in which they are loaded. One of the advantages of our smart tip platform is that it -in principle- can be loaded into many commercially available microscopes, provided these have three contacts to the tip. Here we choose to design and build the system ourselves, but mostly with commercially available parts. The main objective of the microscope is to facilitate the smart tips and to be able to study as many types of samples as possible. For this we use an STM head, where the needle and surface are brought together in a compact, rigid housing. It also allows us to move the surface sideways. The STM head is cooled by the connection to a liquid Helium tank that cools it to 4.2 K. Due to the high cost of liquid Helium that evaporates, the Helium tank is enclosed by a tank with liquid nitrogen (77 K). All cables that connect the STM to the electronics outside the microscope are pre-cooled at different temperatures to minimize the heat transfer from room temperature. All of the components mentioned above are part of an ultra-high vacuum system with a final pressure of 3×10^{-10} mbar such that samples remain clean after preparation and virtually no heat conduction takes place via air and the STM remains cold.

Chapter 4 consists of a series of proof-of-principle experiments, each of which forms an important part towards the development of a fully functioning double-tip STM. First we test the performance of the developed STM by scanning over an atomic flat gold surface with a traditional metal needle and analyzing the fluctuations in the current. We demonstrate here that the performance is satisfactory for successful measurements of quantum materials in the near future. Next, we show that the smart tips developed in chapter 2 give comparable results to a traditional metal needle in a commercial low temperature and ultra-high vacuum STM, an important result. Finally, we attempt to test one of the needles of a double-tip device, a smart tip that ends in two seperate tips, on a gold surface. As a result of the sensitivity to electrostatic discharge between the two tips, causing them to blow up, these tests are still ongoing at the time of writing.

In *chapter 5* we explore in detail the possibility of a double-tip STM based on the platform introduced in Ch. 2. The idea is that we can measure correlations using the two needles by inserting electrons through one tip and measuring the fraction of them that arrives on the other tip. This allows one to acquire new information that is not available with a single tip. However, because two tunneling processes are involved, the signal can be very small. We also consider the possibility of calculating correlations between the individual currents of each tip and thus measuring a larger signal on certain specimens. In this chapter we also present the double-tip devices and the associated manufacturing methods. We show that we are able to make two tips with a separation of only a few tens of nanometers by splitting the metal needle with a focused ion beam. Finally, we conclude that in order to get both needles into tunneling simultaneously, a number of elements are still missing, in particular tilting the tips to compensate for the difference in length and, while doing so, navigating the surface.

In the final chapter, *chapter 6*, we explore a more straightforward experiment with the double-tip devices where we only require one tip in tunneling: STM with a local gate electrode. Here we use the non-tunneling tip, a few tens of nanometers away, to apply a strong electric field to modify the electronic properties of the surface. This could enable us -by simply applying a voltage from outside- to influence the electronic properties of quantum materials where this is otherwise impossible or impractical. We believe this is particularly the case with strontium iridates at low chemical doping levels. Initial simulations, however, show that the field that can be generated this way is probably on the low side to induce major electronic changes. However, because of the simplicity, we think it is likely that we can gain new insights with this experiment.

SAMENVATTING

Dit proefschrift beschrijft hoofdzakelijk het pad naar een nieuw type metalen naald voor een -zogenoemde- scanning tunneling microscope (STM). Dit type microscoop werkt door middel van een hele scherpe, elektrisch geleidende naald -ook wel tip genoemd- zeer dicht bij een geleidend oppervlak te brengen. Wanneer we een spanning aanleggen tussen het oppervlak en de naald en de afstand daartussen minder dan een nanometer, een miljardste meter, is, kunnen elektronen overspringen. Dit kwantummechanische verschijnsel heet tunnelen. Het tunnelen van elektronen leidt tot een stroom die exponentieel afhangt van de afstand tussen de naald en het oppervlak waardoor we -via de stroom- de afstand zeer nauwkeurig kunnen meten. Het is zelfs mogelijk om de naald zeer gecontroleerd over het oppervlak te bewegen terwijl we de stroom gelijk houden, dit stelt ons in staat het oppervlak af te tasten en in kaart te brengen. Als de naald dermate scherp is dat hij eindigt in één enkel atoom, dan is hij scherp genoeg om enkele atomen in het oppervlak te onderscheiden. Traditioneel is de naald en dunne metalen draad die gepolijst of ge-etst is aan het uiteinde om een punt te vormen. Op het oog zal de draad niet eindigen in één atoom maar een bepaalde radius hebben in de orde van 5-30 nanometer, echter er is altijd wel een enkel atoom dat het dichtste bij het oppervlak komt en waarvandaan de elektronen tunnelen.

Ons doel in dit proefschrift is om deze metalen draad te vervangen door microscopische kleine naald die is geïntegreerd in een silicium chip zoals wij die ook kennen uit de computer industrie. Deze tips kunnen dienen als een platform voor nieuwe toepassingen, zoals elektrische circuits of meerdere naalden naast elkaar, die kunnen worden toegevoegd via de micro en nanofabricage technieken die wij hier gebruiken. Wij noemen deze tips: smart tips. Verder onderzoeken wij enkele van de extra mogelijkheden die deze integratie op een chip met zich meebrengt. Wij richten ons hierbij op een aantal toepassingen omtrent het bestuderen van zogenoemde kwantum materialen. In het bijzonder verkennen wij de mogelijkheid om twee naalden tot op enkele (tientallen) nanometers van elkaar te maken en beide in tunneling te brengen om zo een double-tip STM te creëren gebaseerd op het smart tip platform.

In *hoofdstuk 2* beschrijven wij de ontwikkeling van het fabricage proces van de smart tips en tonen wij de resulterende smart tip devices die bestaan uit een enkele tip die uitsteekt en verbonden is aan het gehele oppervlak van de chip die hier slechts dient als enkel elektrisch contact. De fabricage is gebaseerd op een silicium chip bedekt met een laag silicium nitride, bekend om zijn isolerende en mechanisch sterke eigenschappen. Door middel van lithografie met een hele smalle bundel gefocuste elektronen i.p.v. licht kunnen wij op de nanoschaal structuren schrijven in een dunne laag van polymeren. Dit patroon, die de naald definieert, brengen we over in het silicium nitride door te etsen. Met een hele precieze zaagmachine zagen wij de vorm van de chip, die puntig

is met de zojuist geëtste tip vlak bij de rand aan het uiteinde. Vervolgens etsen we met een plasma het silicium waarvan de chip is gemaakt zodat deze aan alle kanten krimpt, waardoor aan het uiteinde van de chip de tip van nitride 10-12 micrometer uitsteekt. Tenslotte bedekken we de gehele chip, inclusief de tip, met een dunne laag goud voor de elektrische geleiding.

Hoofdstuk 3 beschrijft het ontwerp, de bouw en de prestaties van een door ons ontwikkelde smart tip STM. Omdat wij aan de chip nieuwe toepassingen willen toevoegen en hem te laten dienen als een platform hebben wij meerdere elektrische contacten nodig. Dat geldt voor op de chip maar ook voor de microscoop waar ze in geladen worden. Een van de voordelen van ons smart tip platform is dat zijn -in principe- in de meeste commercieel verkrijgbare microscopen kunnen worden geladen mits deze drie contacten naar de tip hebben. Hier kiezen wij ervoor om het systeem zelf te ontwerpen en bouwen, maar wel veelal met commercieel verkrijgbare onderdelen. Het hoofddoel van de microscoop is het faciliteren van de smart tips en zo veel mogelijk type preparaten te kunnen bestuderen. We gebruiken hiervoor een STM kop, waar naald en oppervlakte naar elkaar bewogen worden in een compacte, stijve behuizing. Hierbinnen kunnen we ook het oppervlak zijwaarts kunnen bewegen. De STM kop wordt gekoeld via de verbinding naar een vloeibaar Helium tank die het geheel koelt naar 4.2 K. Vanwege de hoge prijs van vloeibaar Helium dat verdampt is de Helium tank omsloten door een tank met vloeibaar stikstof (77 K). Alle kabels die de STM verbinden met de elektronica buiten de microscoop worden voorgekoeld op verschillende temperaturen om de geleiding van warmte vanaf kamertemperatuur te minimaliseren. Al de hier genoemde onderdelen maken deel uit van een ultra-hoog vacuüm systeem met een einddruk van 3×10^{-10} mbar zodat preparaten na bereiding schoon blijven en er nagenoeg geen warmtegeleiding plaats vind via lucht.

Hoofdstuk 4 bestaat uit een serie proof-of-principle experimenten die ieder een belangrijk onderdeel uitmaken richting de ontwikkeling van een volledig werkende dubbel-tip STM. Eerst testen we de prestaties van de ontwikkelde STM door met een traditioneel metalen naald over een atomair vlak goud oppervlak te scannen en de fluctuaties in de stroom te analyseren. We demonstreren hier dat de prestaties voldoen voor succesvolle metingen aan kwantum materialen in de nabije toekomst. Daarna laten we zien dat de in hoofdstuk 2 ontwikkelde smart tips vergelijkbare resultaten geven als een traditionele metalen naald in een commerciële lage temperatuur en ultra-hoog vacuüm STM, een belangrijk resultaat. Tenslotte pogen we één van de naalden van een dubbel-tip device, een smart tip die eindigt in twee aparte naalden, te testen op een goud oppervlak. Vanwege de gevoeligheid voor elektrostatische ontlading tussen de twee tips, waardoor zij opblazen, zijn deze testen nog gaande op het moment van schrijven.

In *hoofdstuk 5* onderzoeken we in detail de mogelijkheid van een dubbel-tip STM op basis van het platform geïntroduceerd in hoofdstuk 2. Het idee is dat we via de twee naalden correlaties kunnen meten door elektronen in te brengen via één tip en een fractie daarvan te meten met de andere tip. Hierdoor kan men nieuwe informatie

verwerven die niet beschikbaar met een enkele tip. Omdat er twee tunneling processen aan te pas komen kan het signaal echter zeer klein zijn. Wij bekijken tevens de mogelijkheid om correlaties uit te rekenen tussen de individuele stromen van elke tip en zo een groter signaal te meten op bepaalde preparaten. In dit hoofdstuk presenteren wij de dubbel-tip devices en de bijbehorende fabricage methoden. Wij laten zien dat we in staat zijn om twee naalden met een afstand van enkele tientallen nanometers van elkaar te maken door de metalen naald te splitsen met een gefocuste ionen bundel. Tenslotte concluderen we dat om beide naalden tegelijkertijd in tunneling te krijgen, nog een aantal elementen ontbreken, met name het tilten van de tips om het lengteverschil op te vangen en het navigeren over het oppervlak.

In het laatste hoofdstuk verkennen wij een eenvoudiger experiment met de dubbel-tip devices waar wij slecht één van de twee tips in tunneling hoeven te brengen: STM met een lokale stuurelektrode. Hier gebruiken we de naald die niet in tunneling is en op enkele tientallen nanometers afstand, om een sterk elektrisch veld aan te leggen om zo de elektronische eigenschappen van het oppervlak te beïnvloeden. Dit zou ons in staat kunnen stellen om -door simpelweg een spanning aan te leggen van buiten af- de elektronische eigenschappen van kwantum materialen te beïnvloeden waar dit op andere manieren onmogelijk of onpraktisch is. In het bijzonder is dit het geval bij de strontium iridaten bij lage chemische doping niveaus. Initiële simulaties laten echter zien dat het veld dat gegenereerd kan worden op deze manier waarschijnlijk aan de lage kant is om grote elektronische verandering te induceren. Vanwege de eenvoud achten wij het toch waarschijnlijk dat we tot nieuwe inzichten kunnen komen met dit experiment.

Curriculum Vitæ

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Education

2016–2020 PhD in Applied Physics
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List of Publications

5. **M. Leeuwenhoek** *et al., Fabrication of on-chip probes for double-tip scanning tunneling microscopy*, in preparation.

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