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Passive Cooling of mm-Wave Active Integrated 5G Base Station Antennas Using CPU Heatsinks

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***Abstract* — The challenge of cooling in mm-wave chip-integrated base station antenna arrays is addressed. Several approaches in thermal modeling of electronics are revisited and discussed. The two-resistor compact thermal model is applied to predict the junction temperatures of the beamformer chips. Thermal simulations are performed for two fabricated arrays having 16 chips (single-polarized) and 32 chips (dual-polarized). Two commercial passive CPU heatsinks with different capabilities are modeled and attached to the chips. The simulation results are validated through experiments using the temperature sensor readings. The reasons of discrepancies between the simulated and measured results are explained.**

***Keywords* — active integrated antenna, base station antenna, CPU cooler, fifth-generation (5G), millimeter-wave communication, passive cooling.**

I. Introduction

Due to the relatively small package sizes and low-efficiency chips at mm-waves, the 5G industry is currently facing serious thermal challenges [1]. As a rule of thumb, it is commonly accepted that every 10^oC rise in the integrated circuit (IC) junction temperature reduces the average life of the chip by 50% (through the Arrhenius equation [2]). Moreover, the average junction temperature should be kept below 125^oC under typical working conditions at steady state for a safe and reliable device operation [3].

At the Ka frequency band, in which most of the current 5G mm-wave work is conducted, the severe cooling issue is handled by active cooling strategies employing fans or water pumps [4]. However, high-volume and low-cost communication market demands fully-passive thermal management. For this purpose, making use of the commercial fanless CPU coolers was first proposed in [5] and the effect of increasing the chip layout sparsity on the maximum array temperature was investigated. Later, in [6], the impact of antenna substrate thermal conductivities on cooling extension was studied for chip-integrated antennas that are attached to CPU heatsinks. However, in both papers, the CPU heatsink was represented with a roughly estimated heat transfer coefficient (H.T.C.) on the order of 1000 W/m^2K, which is increased or decreased depending on the capabilities (i.e. conduction properties and dimensions) of the heatsink. In other words, modeling and integration of the specific coolers into the simulations was not performed.

In this work, two commercially available CPU heatsinks with different cooling capabilities are modeled and included in the thermal simulations. The simulations are performed for two antenna arrays: a single-polarized (single pol.) integrated antenna array with 16 chips on LTCC, and a dual-polarized (dual pol.) integrated antenna array with 32 chips on PCB. The results are verified by experiments with the fabricated arrays using temperature sensors.

The rest of the paper is organized as follows. Thermal modeling approaches in electronics design are revisited in Section II. The simulation settings and results are given in Section III. Section IV presents the experimental results and discussions. The paper is concluded in Section V.

II. Thermal Modeling in Electronics Design

The thermal models in electronics design can be grouped into two categories: detailed thermal models (DTMs) and compact thermal models (CTMs) [7]. DTMs present an almost-exact physical model of the chips with the actual package geometry. Despite being very accurate, DTMs are not suitable for system-level studies with large number of ICs due to their high computational burden. CTMs, on the other hand, do not try to mimic the package geometry and material properties. Instead, they aim to accurately predict the temperature at only a few critical points of the chip package (junction, case, etc.), mostly by using an equivalent thermal resistor network. Because of their high computational efficiency, CTMs are much more suitable for investigating system-level designs and exploring what-if scenarios.

Today, the most commonly used CTMs are the two-resistor [8] and DELPHI [9] models, which are shortly discussed next. It is worthy to note that both models are standardized by the JEDEC Solid State Technology Association.

A. Two-resistor CTM

In the two-resistor CTM, it is assumed that the heat can only leave the junction through two nodes: the case node and the board node. The heat flow through the package sides is not taken into account. Therefore, the equivalent thermal network is represented by two resistances, namely, the junction-to-case and the junction-to-board resistance. In a 3D model, the IC junction is represented by a high conductivity block with

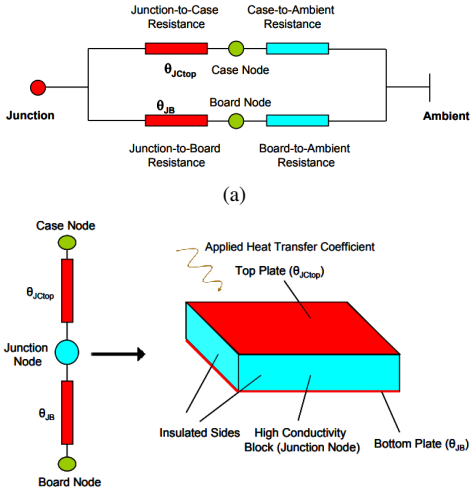


Fig. 1. Two-resistor CTM representation from [8], (a) model network, (b) 3D modeling.

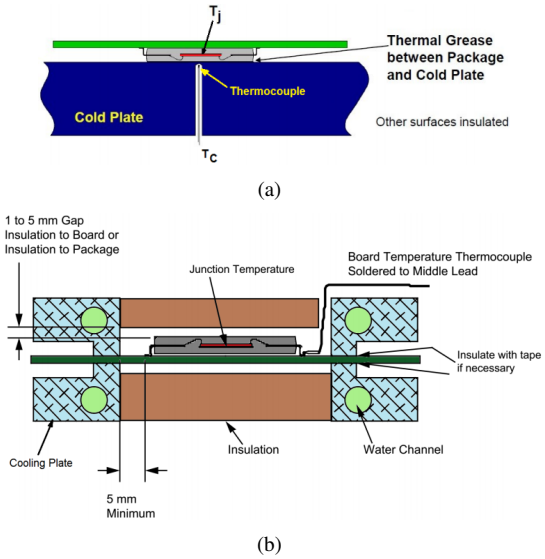


Fig. 2. Thermal resistance measurement setups from [10] for, (a) junction-to-case resistance, (b) junction-to-board resistance.

insulated sides and resistive plates at the top/bottom. An equivalent H.T.C. is applied at the solid-to-air interfaces. See Fig. 1 for visualization of the two-resistor model.

While calculating the junction-to-case resistance, almost all the heat is forced to be dissipated through a single surface of the chip (case top or bottom). A cold plate is attached to the top (or bottom) of the chip and works as a heatsink. The case temperature is measured via a thin thermocouple wire, as shown in Fig. 2(a). Similarly, for calculation of the junction-to-board resistance, it is ensured that almost all of the heat flows through the substrate. The chip top and bottom are covered with a thermal insulation material. A circular cooling plate holds the board (see Fig. 2(b)).

In general, the prediction accuracy of the two-resistor CTM is not very high, but the accuracy will be much higher in the cases where most of the heat flows through the heatsink (as in the CPU cooler integrated arrays) and/or the board.

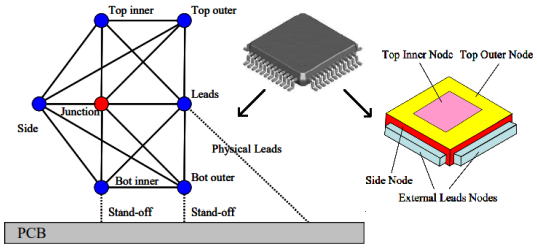


Fig. 3. DELPHI CTM representation from [9]

B. DELPHI CTM

As shown in Fig. 3, the DELPHI CTM consists of several thermal resistors connecting the junction node to the surface nodes. The resistor values are computed by a detailed simulation procedure followed by a statistical optimization process that minimizes the errors in the prediction of the junction temperature through averaging over a wide range of environmental conditions (free convection, fan cooling, cold plate, high/low conductivity substrate etc.).

A comparison between the two models is provided in Table 1. The DELPHI CTM has a relatively high accuracy with a reasonable computational efficiency, which makes it more advantageous than the two-resistor CTM. Yet, it is advisable to use the two-resistor CTM in the initial design stage to obtain the first predictions on the chip temperatures.

III. Simulation Results

In the simulations, the two-resistor CTM was used for the Ka band quad channel analog beamformer chip of NXP Semiconductors. The thermal model parameters commonly used in all the simulations are provided in Table 2. Two different fabricated antenna arrays (a single pol. and a dual pol.) were modeled with the properties summarized in Table 3. The arrays were integrated with two different CPU heatsinks (Mugen MAX and NH-L9x65) that are shown in Fig. 4 and have the properties listed in Table 4. The complete simulation models for the single pol. array with the two coolers are provided in Fig. 5 for better visualization. The damping in the heatpipes and the nickel-plating were not considered in the simulations for simplicity. Note that the chips (placed on the baseplate of the cooler) and patch radiators are located on the opposite sides of the substrate. Therefore, the radiation pattern is not significantly affected by the heatsink.

Table 1. A qualitative comparison of the CTMs

Two-resistor CTM	DELPHI CTM
Intuitive & Simple	Complex
Test-based	Simulation-based
Artifacts from the test environment	No environmental artifacts
No error analysis	Statistical optimization with low errors
Less accurate	More accurate
Well-developed (aerospace / defense applications etc.)	Not adopted universally
Lack of CTM data by the semiconductor manufacturers	

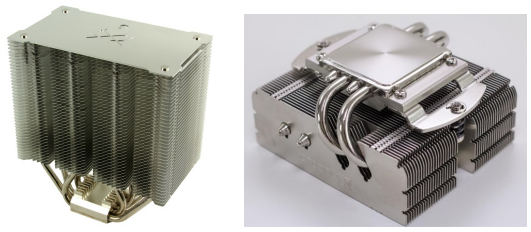
Table 2. Thermal model parameters

Heat produced per chip in idle mode	0.36 W
Heat produced per chip in Tx mode	2.3 W
Heat produced per chip in Rx mode	1.3 W
Chip dimensions	4.3 x 3.5 x 0.5 mm
IC junction-to-case resistance	10 W/K
IC junction-to-board resistance	14 W/K
H.T.C. at the air interfaces	10 W/m^{2}K
Surface emissivity	0.9
Ambient temperature	25°C

Table 3. Antenna array properties

Array type	Single pol.	Dual pol.
Operating frequency	28 GHz	28 GHz
Board material	LTCC	Isola Astra MT77
Board dimensions (length x width x height)	40.6 x 47.5 x 1.4 mm	88.8 x 43.4 x 2.4 mm
Board thermal conductivities (length x width x height)	11.53 x 11.53 x 3.06 W/mK	27.32 x 27.32 x 0.48 W/mK
Number of chips	16	32
Spacing of chips (along length x along width)	10 x 10 mm	5.35 x 10.7 mm
Number of patches	64 (8 by 8)	72 (8 by 9)
Patch dimensions	1.5 x 1.5 mm	2.9 x 2.9 mm
Inter-patch spacings	5 mm	5.35 mm

A summary of the CST MPS simulation results for the maximum chip junction temperature ($T_{j,\max}$) in different cases (depending on the type of the cooler, type of the array, work mode of the chips) is given in Table 5. For better visualization of the results, Fig 6 shows a few sample temperature distributions in the simulated antennas for the single pol. array in transmit (Tx) mode and the dual pol. array in half-active mode (in which the chips of one pol. are in Tx

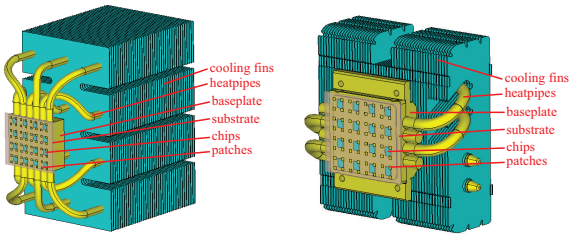


(a) (b)

Fig. 4. Commercial CPU heatsinks used in the paper, (a) Mugen MAX from Scythe [11], (b) NH-L9x65 from Noctua [12].

Table 4. CPU cooler properties

Cooler type	Mugen MAX	NH-L9x65
Overall dimensions	145 x 86 x 145 mm	95 x 95 x 50 mm
Heatsink weight	720 g	340 g
Heatpipe material	Copper (damped, nickel-plated)	Copper (damped, nickel-plated)
Number of heatpipes	6	4
Baseplate material	Copper (nickel-plated)	Copper (nickel-plated)
Baseplate dimensions	38 mm x 43 mm	42 mm x 45 mm
Fin material	Aluminum	Aluminum
Fin plate dimensions	86 x 145 mm	34 x 95 mm
Number of fin plates	40	43
Fin spacing	2.6 mm	1.65 mm
Fin plate thickness	0.5 mm	0.4 mm



(a) (b)

Fig. 5. CST model of the single-polarized integrated antenna array using (a) Mugen MAX, (b) NH-L9x65.

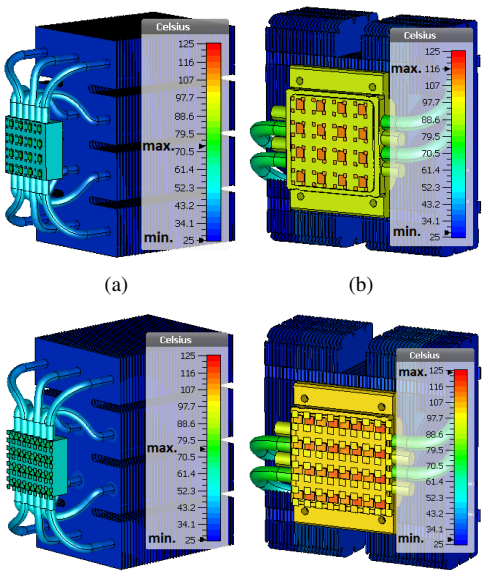
Table 5. Simulation results of the maximum IC junction temperatures in various cases*

Cooler type	Mugen MAX					NH-L9x65				
Array type	Single pol.		Dual pol.			Single pol.		Dual pol.		
Work mode	idle	Tx	full idle	half active Tx	full active Tx	idle	Tx	full idle	half active Tx	full active Tx
$T_{j,\max}$** (°C)	33	73	37	75	98	39	116	50	124	177

* Single pol. idle: 16 chips in idle mode, single pol. Tx: 16 chips in Tx mode, dual pol. full-idle: 32 chips in idle mode, dual pol. half-active Tx: 16 H-pol. (or V-pol.) chips in Tx mode and 16 V-pol. (or H-pol.) in idle mode, dual-pol. full-active Tx: 32 chips in Tx mode.

** The temperatures across the array do not vary much (only by a few degrees) as compared to the maximum value provided in the table.

while the other pol. chips are in idle) using the Mugen MAX and NH-L9x65 coolers. It was seen that due to its larger natural convection surface area and better heat conduction with larger number of heatpipes, the Mugen MAX has much better cooling capability compared to the NH-L9x65. This advantage comes at the expense of having a relatively bulkier/heavier cooling structure.



(a) (b)

(c) (d)

Fig. 6. Simulated array temperature distributions for (a) single pol. array with Mugen MAX in Tx mode, (b) single pol. array with NH-L9x65 in Tx mode, (c) dual pol. array with Mugen MAX in half-active Tx mode, (d) dual pol. array with NH-L9x65 in half-active Tx mode. (The substrates are hidden for a clear view of the chip temperatures.)

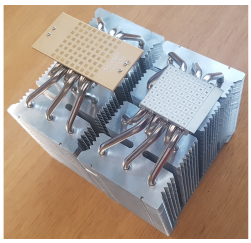


Fig. 7. Fabricated arrays with the Mugen MAX cooling module (right - single pol., left - dual pol. array).

86°C	82°C	78°C	81°C
77°C	73°C	71°C	77°C
76°C	73°C	73°C	74°C
76°C	75°C	73°C	75°C

Fig. 8. Temperature sensor readings for the fabricated single pol. array in Tx mode.

48°C	45°C	43°C	45°C
46°C	46°C	44°C	43°C
45°C	44°C	41°C	42°C
45°C	41°C	X	44°C
45°C	42°C	38°C	42°C
46°C	X	40°C	42°C
44°C	40°C	41°C	44°C
45°C	45°C	47°C	47°C

(a)

67°C	63°C	59°C	61°C
92°C	90°C	82°C	84°C
66°C	61°C	57°C	60°C
91°C	75°C	X	82°C
66°C	58°C	53°C	59°C
95°C	X	75°C	83°C
66°C	59°C	61°C	65°C
98°C	90°C	95°C	104°C

(b)

X	104°C	96°C	97°C
73°C	70°C	66°C	65°C
96°C	89°C	80°C	86°C
68°C	59°C	X	63°C
91°C	78°C	71°C	82°C
68°C	X	56°C	60°C
90°C	80°C	82°C	87°C
65°C	61°C	63°C	65°C

(c)

Fig. 9. Temperature sensor readings for the fabricated dual pol. array in (a) full-idle, (b) half-active Tx (H-pol.), (c) half-active Tx (V-pol.) mode. ('X' indicates that the temperature reading of the IC was not available during the experiment due to a loss of communication between the chip and the main computer. The chips inside the red and blue rectangles represent the V-pol. and H-pol. ICs, respectively.)

IV. Experimental Results and Discussion

The experiments were conducted using the fabricated single pol. and dual pol. arrays (see Table 3 for the details) integrated with the Mugen MAX cooler, which are shown in Fig 7. The junction temperatures were read from the temperature sensors integrated into the chips. Fig. 8 shows the measured temperatures for the single-pol. array in Tx mode. It was seen that the predicted 73^{o}C temperature in Table 5 is in very good agreement with the measured results. It was also realized that at some portions of the array the thermal connection between the chip and the heatsink becomes worse due to the substrate bending during the fabrication process (caused by the thermal expansion coefficient mismatch between the layers), which results in higher junction temperatures.

The experimental temperature readings for the dual pol. array are provided in Fig. 9 in the full-idle and half-active Tx with H-pol. and V-pol. It was seen that the results are again in good agreement with the predicted ones (37^{o}C in the full-idle mode (see Table 5), 60^{o}C and 75^{o}C in the half-active mode for the idle and Tx chips, respectively (see Fig. 6(c))), especially at the chips located in the middle of the array. Apart from the modeling inaccuracies, similarly to the previous case, the discrepancies at the surrounding chip temperatures are mainly due to the undesired bending of the substrate and the resulting poorer thermal connection to the CPU heatsink.

V. Conclusion

The use of commercially available, low-cost and fully-passive CPU heatsinks in the cooling of mm-wave chip-integrated 5G base station antennas has been shown and validated. Two different CPU heatsinks (Mugen MAX and NH-L9x65) have been modeled and thermal simulations have been performed using the two-resistor CTM of the fabricated single-polarized and dual-polarized arrays with 16 and 32 chips, respectively. A good agreement between the experimental junction temperature readings and the predicted values through the simulations has been observed, especially at the chips located in the center of the array with the best thermal connection to the heatsink. The main cause of the discrepancies between the measured and the simulated temperature results for the surrounding chips has been found to be the poorer thermal connection that occurs due to the substrate bending. From the simulation results, it has been observed that the Mugen MAX has better cooling capacity than the NH-L9x65 due to its larger air-interfacing surface area and better heat conduction with larger number of heatpipes. The experimental results verify that the Mugen MAX cooler can guarantee a safe and reliable operation for both arrays in the work modes used in the paper. The presented research provides valuable and useful guidelines for the selection of a proper cooler in the initial array design process.

Acknowledgment

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