An Energy-Efficient Current-Controlled Write and Read Scheme for Resistive RAMs (RRAMs)

Aziza, H.; Moreau, M.; Fieback, M.; Taouil, M.; Hamdioui, S.

DOI
10.1109/ACCESS.2020.3011647

Publication date
2020

Document Version
Final published version

Published in
IEEE Access

IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received July 9, 2020, accepted July 20, 2020, date of publication July 24, 2020, date of current version August 5, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3011647

An Energy-Efficient Current-Controlled Write and Read Scheme for Resistive RAMs (RRAMs)

H. AZIZA[1], M. MOREAU[1], M. FIEBACK[2], (Graduate Student Member, IEEE), M. TAOUIL[2], (Member, IEEE), AND S. HAMDIOUI[2], (Senior Member, IEEE)

[1]IM2NP, UMR CNRS 7334, Aix-Marseille University, F-13451 Marseille, France
[2]Computer Engineering Laboratory, Delft University of Technology, 2628CD, Delft, The Netherlands

Corresponding author: H. Aziza (hassen.aziza@univ-amu.fr)

ABSTRACT Energy efficiency remains one of the main factors for improving the key performance markers of RRAMs to support IoT edge devices. This paper proposes a simple and feasible low power design scheme which can be used as a powerful tool for energy reduction in RRAM circuits. The design scheme is exclusively based on current control during write and read operations and ensures that write operations are completed without wasted energy. Self-adaptive write termination circuits are proposed to control the RRAM current during FORMING, RESET and SET operations. The termination circuits sense the programming current and stop the write pulse as soon as a preferred programming current is reached. Simulation results demonstrate that an appropriate choice of the programming currents can help obtain *4.1X* improvement in FORMING, *9.1X* improvement in SET and *1.12X* improvement in RESET energy. Also, the possibility to have a tight control over the RESET resistance is demonstrated. READ energy optimization is also covered by leveraging on a differential sense amplifier offering a programmable current reference. Finally, an optimal trade-off between energy consumption during SET/RESET operations and an acceptable read margin is established according to the final application requirements.

INDEX TERMS Resistive RAM (ReRAM), RRAM, OxRAM, energy optimization, write termination, programming current, read current.

I. INTRODUCTION

Memory is an essential component of today's electronic systems. It is used in any equipment using a processor such as computers, smart phones, tablets, digital cameras, entertainment devices, global positioning systems, automotive systems, etc. Moreover, the unprecedented growth in Internet of Things (IoT) devices across all industry verticals continuously generates a massive amount of data which increases the demand for even more physical space for memory. To accommodate multi-media and other data-intensive applications, mobile battery-operated systems embed high-performance and large capacity memories; and thus the memory system becomes a dominant energy consumer, which motivates energy efficient information storage solutions [1]. Today's dominant memory technologies are DRAM and Flash, for performance and storage purposes. Both technologies are facing severe scaling issues [2]. DRAM offers very high endurance (approximately 10^{14} cycles) but it is volatile. Flash is non-volatile and can be seen as an ideal solution as it requires no additional power to retain the data. But its endurance is limited (approximately 10^6 cycles), and its operation access frequency is very slow, with program/erase time in the order of microseconds to milliseconds [2]. Moreover, Flash devices need high voltages for storage operations which is hardly compatible with ultra-low power applications [3]. In the quest for low power non-volatile memory solutions, different technologies have emerged in research over the last 15 years [4]. Among these technologies, Resistive RAMs (ReRAMs or RRAM) are believed to be a good choice for low power embedded applications [5]. It is worth noticing that in literature, the generic term RRAM is often used to refer to both Oxide Random Access Memory (OxRAM) and Conductive-Bridging Random Access Memory (CBRAM). In the rest of the paper, OxRAM technology will be considered, as it is one of the most competitive candidates for future non-volatile memory applications due to its simple structure offering low manufacturing costs, fast switching speed ($\sim$10 ns), great scalability ($<$10 nm), compatibility with current CMOS technology, and low voltage operation [6].

The associate editor coordinating the review of this manuscript and approving it for publication was Aimin Song.

However, when it comes to ultra-low power designs to enable the deployment of RRAM technology for IoT edge devices, efficient and flexible energy reduction solutions are highly desirable.

Although several RRAM energy optimization techniques have appeared in the literature [7]–[9], they still suffer from several issues related to integration cost, strict control of the operating currents, and flexibility. Moreover, most of the work focus on the programming operations [10], [11]. The READ operation is completely forgotten as well as an analysis of the impact of the proposed energy reduction schemes on the memory cell functionality. From a reliability point of view, OxRAM is mostly affected by switching variability [12]: OxRAMs suffer from intrinsic Device-to-Device (D2D) and Cycle-to-Cycle (C2C) variability resulting in wide distributions of switching parameters for FORMING (FMG), RESET (RST) and SET programming operations. OxRAM variability negatively impacts power consumption. To illustrate this effect, the conventional OxRAM write scheme is presented in Fig.1a. A one-pulse voltage with a fixed-pulse duration is used for RST and SET operations [13], with V_R representing the voltage across the cell and I_R the cell current. As a result, the time width of the applied voltage pulse T_{SET} and T_{RST} must cover the worst cases during RST (T_{RST_slow}) and during SET (T_{SET_slow}). These worst cases correspond to the tail bits in the switching parameter distributions [12]. Fig.1b shows that this conventional write scheme results in wasted energy for fast-switch cells requiring short RST (T_{RST_fast}) and SET (T_{SET_fast}) pulse widths. Indeed, as the voltage across the memory cell V_R is maintained after the switching event, the current I_R keeps flowing through the cell. Also, these fast cells can be over-RST or over-SET resulting in an uncontrolled spread of High Resistance State (HRS) and Low Resistance State (LRS) distributions. Moreover, the READ current can be relatively large for over-SET cells (tens of μA) as these cells end in a very low LRS resistance. The latter can limit performances of read-intensive applications generally associated with in-memory processing and more specifically with Neural Network (NN) applications where synaptic weights are constantly and simultaneously read during inference [14]. Thus, READ energy optimization needs to be addressed to support the adoption of RRAM-based NN accelerators.

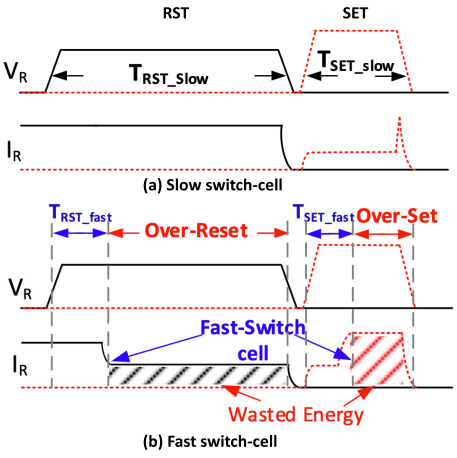


FIGURE 1. Conventional one-pulse programming approach for a) worst-case coverage of slow switching cells and b) fast switching cells, resulting in wasted energy.

In this context, we propose a new design scheme that addresses attractive properties that are missing or poorly achieved in other previously proposed works, including:

1) A minimal area overhead.
2) A dynamic and strict control of write and read currents (provided by programmable current sources).
3) A tight control of post-programming HRS and LRS resistances.
4) An evaluation of the read currents and energy.
5) An discussion regarding the impact of the energy reduction scheme on the memory cell functionality.

In particular, all OxRAM's operation currents including FMG, RST, SET and READ currents will be monitored. We will focus on circuit level considerations from an energy efficiency point of view. To the authors' knowledge, this is the first work presenting a full low-power design-scheme targeting all operating modes of RRAM memory circuits.

The remainder of this paper is organized as follows. Section II presents the OxRAM technology along with conventional energy optimization approaches. In Section III, the low-power design scheme is presented. Section IV presents simulation results. Section V discusses the proposed energy optimization strategy versus reliable READ operations (i.e. R_{ON}/R_{OFF} ratio optimization). Finally, Section V concludes this paper.

II. BACKGROUND

A. OXRAM TECHNOLOGY

An OxRAM memory cell consists of two metallic electrodes that sandwich a thin dielectric layer serving as a permanent storage medium. This Metal-Insulator-Metal (MIM) structure, denoted RRAM in Fig. 2a, can be easily integrated in the Back-End Of Line (BEOL) on top of the CMOS subsystem. The MIM structure is integrated on top of the Metal 4 copper layer (Cu). A TiN Bottom Electrode (BE) is first deposited. Then, a 10nm-HfO_2/10nm-Ti/TiN stack is added to form a capacitor-like structure [15]. Fig. 2b shows the basic

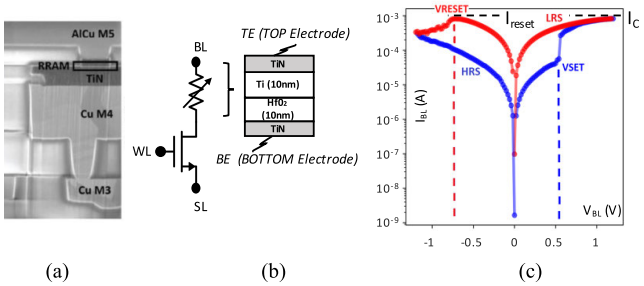


FIGURE 2. a) TEM cross-section of an OxRAM device [10] b) symbol view of a 1T-1R cell c) OxRAM I-V characteristic in log scale.

1T-1R memory cell where one MOS transistor is connected in series with an OxRAM cell. Fig. 2c presents a typical 1T-1R OxRAM I-V characteristic in logarithmic scale. Based on the I-V curve, the memory cell behavior can be seen as follows: after an initial electroforming step (not presented here), the memory element can be reversibly switched between HRS and a LRS. Resistive switching in an OxRAM corresponds to an abrupt change between the HRS and the LRS. The resistance change is triggered by applying specific biases across the 1T-1R cell, i.e., V_{SET} to switch to LRS and V_{RST} to switch to HRS.

In the 1T-1R configuration, the transistor controls the amount of current flowing through the cell according to its gate voltage bias. The maximum current allowed by the select transistor is called the compliance current and is referred to as I_C in Fig. 2c. I_C controls the LRS resistance value in the SET state as well as the maximal RST current I_{reset}, and thus plays an essential role in limiting the memory cell power consumption [16]. Table 1 presents the different voltage levels applied to the OxRAM cell during the different operating stages. During the OxRAM cell characterization, the extraction of V_{SET} and V_{RST} values is achieved using 1ms DC voltage sweeps instead of voltage pulses to precisely extract the threshold voltages; the applied voltage increases step by step and the current flowing through the cell is measured [17]. Thus, BL and SL voltage values presented in Table 1 refer to the maximal sweep ramp values.

TABLE 1. Standard Operating voltages (cell level).

	FMG	RST	SET	READ
WL	2V	3V	2V	3V
BL	2V	0V	1.2V	0.2V
SL	0V	1.2V	0V	0V

B. ENERGY REDUCTION CONVENTIONAL TECHNIQUES

Programming algorithms and write assist circuits play a crucial role for efficient RRAM programming [18]. Program-verify algorithms have been developed to ensure distinct resistance distributions; they adjust the write signal (width or amplitude) until the cell resistance reaches the target resistance state [19]. However, in this scheme, the writing is interrupted periodically to allow for the read operations to verify that switching has occurred, which increases the write-time significantly. An alternative to avoid the use of read operations, is to implement a write-termination scheme at the memory driver level where the write pulse is cut-off right after the resistance transition completes. This prevents wasting write energy but introduces an important area overhead. For instance, in [10], such a scheme is implemented using an op-amp, a differentiator and additional capacitors and resistors, resulting in significant area overheads. In this study, a cost-efficient self-terminated write driver based on a strict control of the FMG/SET and RST currents is introduced. Instead of detecting the resistance state transition, the driver compares the memory cell current with a reference current and terminates the programming operation when the RRAM cell current matches the reference current. No read operation is required in the process. Moreover, controlling the programming currents allows to control post-programming resistance values.

III. ENERGY EFFICIENCY SCHEME IMPLEMENTATION

A. IMPACT OF VARIABILITY ON SWITCHING PARAMETERS

To extract FMG, RST and SET switching parameter distributions, an 8 × 8 elementary 1T-1R array presented in Fig. 3a is considered for measurements. Memory cells are grouped to form eight 8-bit memory words. Word Lines (WL_X) are used to select the active row, Bit Lines (BL_X) are used to select active columns during a SET operation and Source Lines (SL_X) are used to RST a whole memory word or an addressed cell. Fig. 3b presents the layout view of the memory array.

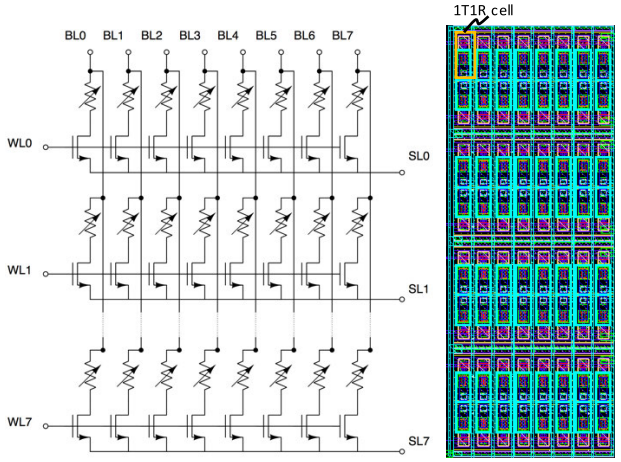


FIGURE 3. a) 8 × 8 OxRAM memory array and b) corresponding layout view.

The experiments are performed using a Keysight B1500 semiconductor parameter analyzer. The studied memory array is embedded on an 8-inch wafer, connected to the B1500 through a probe card and a low resistance switching matrix. The matrix connects the Source/Measure Units (SMUs) to the memory array pads during the FMG, SET, RST and READ operations. Python programs control the equipment and 1ms DC sweeps are used to extract switching parameters. Before any operation, the memory array is first formed. Then, memory cells are RST one by one to extract V_{RST} threshold and the corresponding T_{RST}. After RST, cells are SET to extract V_{SET} threshold and the corresponding T_{SET}. The RST/SET process is repeated 750 times for the whole array in order to catch C2C as well as D2D variability.

Fig. 4.a and Fig. 4.b present the resulting V_{RST} and V_{SET} distributions. T_{RST} and T_{SET} switching times are also reported in Fig. 4.c and Fig. 4.d. Table 2 reports V_{SET}, V_{RST}, T_{SET} and T_{RST} main distribution parameters. V_{RST} and V_{SET} exhibit large distribution spreads with median values located

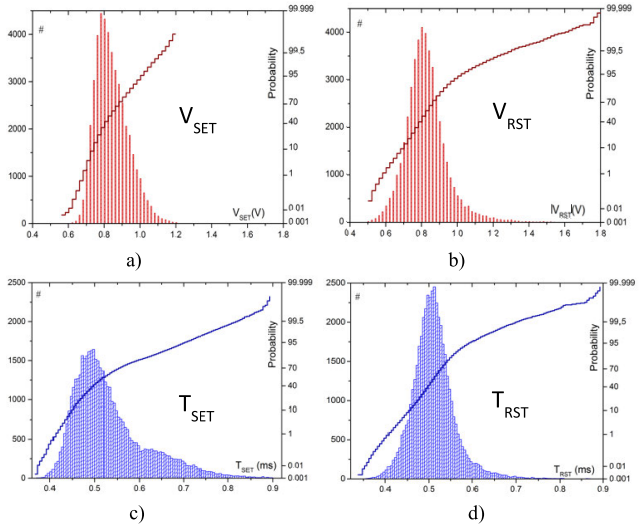


FIGURE 4. Measured a) V_{SET} and b) V_{RST} voltage distributions and corresponding c) T_{SET} and d) T_{RST} timing distributions obtained from the 8 × 8 memory array presented in Fig.3 after 750 RST/SET cycles (51 000 data).

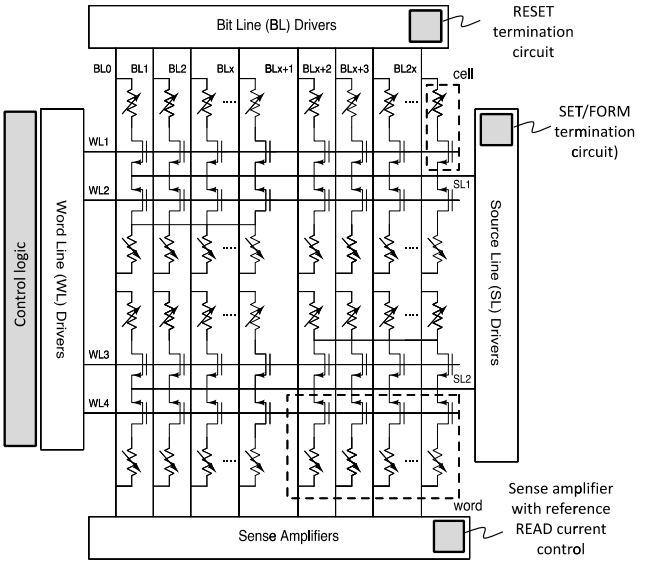


FIGURE 5. Elementary memory array architecture used for simulations including modifications required for the implementation of the low power design scheme.

TABLE 2. V_{RST}, V_{SET} and V_{FMG} distribution parameters.

	#	σ	Min	Median	Max
V_{SET}	48000	0.091V	0.57V	0.840V	1.21V
$\|V_{RST}\|$	48000	0.117V	0.51V	0.823V	1.80V
T_{SET}	48000	0.0827ms	0.368ms	0.512ms	0.899ms
T_{RST}	48000	0.0491ms	0.339ms	0.507ms	0.895ms

at 0.823 V and 0.840 V respectively. The V_{RST} distribution shows tail bits and varies in the range [0.51 V-1.80 V] contrasting the V_{SET} distribution which varies in the range [0.57 V-1.21 V]. Regarding T_{SET} and T_{RST}, a large time dispersion between fast and slow cells is observed in the range [0.368 ms-0.512 ms] for T_{SET} and [0.339 ms-0.507 ms] for T_{RST}, making the use of long programming pulses mandatory for proper cell programming.

Prior to performing SET or RST, a FMG step is required, which is achieved one time in the device life [12]. Thus, only 64 values are available for the FMG operation providing an average V_{FMG} value of 1.95 V and an average T_{FMG} value of 0.745 ms.

B. HIGH LEVEL ARCHITECTURE IMPLEMENTATION

In this section, the write termination structures applied during FMG, SET and RST operations are introduced. Fig. 5 presents the OxRAM memory array, considered in this work, which is composed of a word line driver to select the active row (WL_X), a bit line driver to select active bit lines (BL_X) during a FORM/SET and READ operations and a source line driver to select a specific source line (SL_X) during RST. Sense amplifiers are used to convert the cell current into a logical value at the circuit output during a READ operation. Memory cells are usually grouped into 8, 16 or 32 bits to form a memory word (dashed line). Fig. 5 highlights the changes made to the OxRAM memory array to implement our low power design scheme. A FMG/SET termination circuit is used to monitor the FMG/SET current at the SL driver level and a RST termination circuit is used to control the RST current. A modification of the control logic circuitry is implemented to end the programming pulses when predefined threshold currents are reached. During the READ operations, the sense amplifier compares the cell current to a strictly controlled reference current. Note that all the reference currents will be derived from a single current source for all memory operations (FMG/SET, RST and READ operations).

For memory array simulations, a compact OxRAM model [20] calibrated on measurements presented in Section III.A is implemented. The model accurately reproduces the stochastic switching nature of OxRAM cells. The variation is chosen to fit experimental data as presented in Fig. 6 where the model (lines) is consistent with experimental data (symbols) for SET (blue), RST (red) and FMG (green) operations. A good agreement with experimental data is obtained with a ±5% standard deviation on parameters α and Lx of the model [21].

The proposed OxRAM modeling approach relies on electric field-induced creation/destruction of oxygen vacancies within the switching layer. The model enables accounting for both FMG/SET and RST operations into a single master equation in which the resistance is controlled by the radius of the conductive filament (r_{CF}) [21]:

$$\frac{dr_{CF}}{dt} = \left(r_{CF_{\max}} - r_{CF}\right) \cdot 10^{\beta_{RedOx}} \cdot e^{-\frac{Ea - q\cdot\alpha_{red}\cdot V_{cell}}{k_b\cdot T}} - r_{CF} \cdot 10^{\beta_{RedOx}} \cdot e^{-\frac{Ea + q\cdot\alpha_{ox}\cdot V_{cell}}{k_b\cdot T}} \quad (1)$$

where β_{RedOx} is the nominal oxide reduction rate, E_a is the activation energy, α_{red} and α_{ox} are the transfer coefficients

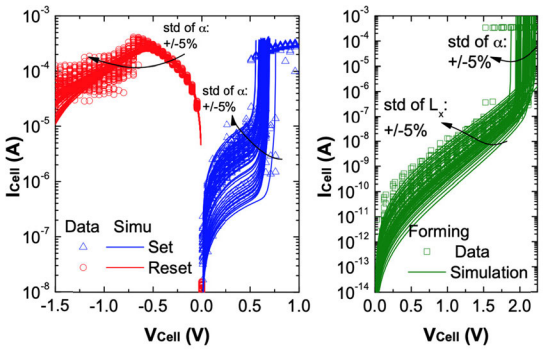


FIGURE 6. Measured and corresponding simulated I-V characteristic obtained from TiN/Ti/HfO_2/TiN devices showing R_{LHS} and R_{HRS} variations and switching parameters variation after SET, RST and FMG operations.

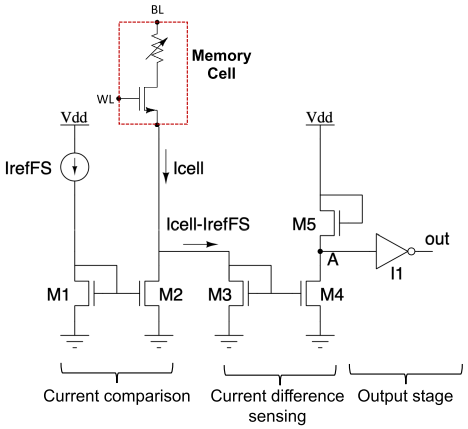


FIGURE 7. Built-in current comparator for FMG/SET operations.

for respectively reduction an d oxidation (ranging between 0 and 1), k_b is the Boltzmann constant, r_{CFmax} is the maximal size of the conductive filament radius, T is the temperature and V_{cell} the voltage across the cell.

Moreover, the model makes assumptions of a uniform radius of the conduction pathways, a uniform electric field in the cell and temperature triggered acceleration of the oxide reduction reactions (''redox''). Finally, the total current in the OxRAM includes two components, i.e., one that is related to the conductive species (I_{CF}) and the other one to the conduction through the oxide (I_{OX}).

$$I_{CF} = \frac{V_{Cell}}{L_x} \cdot \left(\pi \cdot r_{CF}^2 \cdot (\sigma_{CF} - \sigma_{OX}) + \pi \cdot r_{CF\,\max}^2 \cdot \sigma_{OX}\right) \tag{2}$$

$$I_{OX} = A_{HRS} \cdot S_{Cell} \left(\frac{V_{Cell}}{L_x}\right)^{\beta_{HRS}} \tag{3}$$

Here, L_x is the oxide thickness, S_{Cell} is the total area of the device, σ_{Ox} the oxidation rate and σ_{CF} the reduction rate. To take into account I_{OX} trap assisted current (Poole-Frenkel, Schottky emission, Space Charge Limited Current (SCLC)), a power law between the cell current and the applied bias is considered with two parameters A_{HRS} and β_{HRS}. Finally, the total current flowing through the cell is given by:

$$I_{Cell} = I_{CF} + I_{OX} \tag{4}$$

I_{CF} is the main contributor to LRS current (I_{LRS}) and I_{OX} is the main contributor to HRS current (I_{HRS}).

C. LOW LEVEL ARCHITECTURE IMPLEMENTATION

1) FMG/SET OPERATIONS

The self-terminated structure used for FMG/SET operations is based on current level detection in a current comparator. The FMG/SET current is monitored during the FMG/SET operation and the write pulse is stopped when the cell current reaches a pre-defined threshold current referred to as I_{refFS} (where '*F*' stands for FMG and '*S*' stands for SET). Fig. 7 presents the circuit diagram of the built-in current comparator including the OxRAM cell. The current comparator is inserted in series between the OxRAM and GND in order to monitor the memory cell current, I_{cell}. It consists of a current differential amplifier (M2, M3) and two current mirror pairs (M1, M2 and M3, M4). The n-MOS current mirror (M1, M2) is used to mirror the current from a constant current source delivering a reference current I_{refFS}. The current mirror (M3, M4) is used to mirror and amplify the current difference (I_{cell}-I_{refFS}) to the output inverter I1. The differential pair (M2, M3) calculates the difference between the reference current I_{refFS} and the cell current I_{cell}. Hence, the current through M3 is equal to I_{cell}- I_{refFS}. If (I_{cell}-I_{refFS}) < 0, then I_{cell} flows through M2 and no current flows through M3. The inverter input *A* is set high and the comparator output *out* is set to low. When I_{cell} just exceeds I_{refFS}, a current starts to flow through M3. This current is amplified and the inverter input *A* is grounded. As a result, the comparator output *out* switches from a low level to a high level. At this point, the current through the cell is equal to I_{refFS}. The *out* signal is used to terminate the write signal as soon as I_{refFS} is reached.

The proposed FMG/SET termination circuit implementation is presented in Fig. 8. For clarity, only the current comparison stage of the current sensor is included and four memory cells are considered with one cell addressed. *WL0* is activated and a write pulse is applied to *BL0* through the *BL* driver. As current flows through the selected cell, the cell resistance is reduced, and as such, more current flows as the write pulse is maintained. This positive feedback mechanism causes large currents to flow, which impacts drastically current consumption, especially for fast cells. Therefore, current monitoring in the FMG/SET direction is a strong requirement at the circuit level. Note that the write pulse termination is handled by the control logic when I_{refFS} current is reached (*stop pulse* signal triggered).

2) RST OPERATION

The proposed RST termination circuit is presented in Fig. 9. First, the cell current I_{cell} is copied by an n-MOS current mirror (M1, M2). The current mirror (M3, M4) is used to mirror the reference current I_{refR} which feeds the input

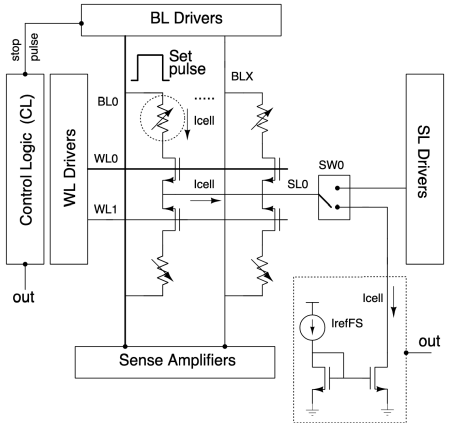


FIGURE 8. FMG/SET termination implementation.

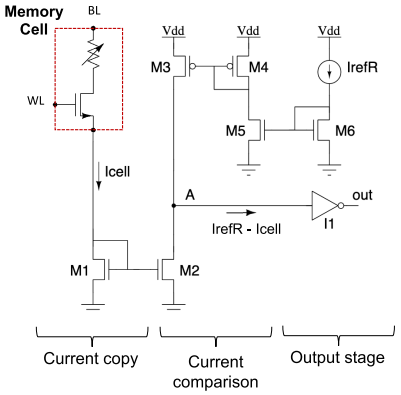


FIGURE 9. Built-in current comparator for RST operations.

of inverter I1. If (I_{cell}-I_{refR}) $>$ 0, the inverter input *A* is set low and the comparator output *out* is set to high. If (I_{cell}-I_{refR}) $<$ 0, input *A* is set high and *out* is set to low. The RST operation is terminated when I_{cell} decreases down to I_{refR}. Typically, I_{refR} is set to a few micro amperes to limit the HRS resistance increase to a few hundred kilo ohms.

The proposed RST termination circuit implementation is presented in Fig. 10. For clarity, only the current copy stage of the RST termination is included. Compared to the FMG/SET operation, the RST operation is performed by biasing the memory cell in the opposite polarity. *WL0* is activated and a RST pulse is applied to *SL0* through the *SL* driver. *BL0* is connected to the current sensor. When I_{cell} equals I_{refR}, the write termination signal is triggered (*out* signal) and the control logic terminates the RST operation. During a RST operation, as the current flows, the resistance of the cell increases, causing current to reduce. Therefore, the RST operation is a negative feedback mechanism and a current limitation during a RST operation is not mandatory. However, terminating the RST operation when the RST current reaches a minimal value can be valuable in terms of variability reduction as a lower limit is set for the HRS resistance, i.e., the lower limit of the current is the upper limit of the HRS resistance.

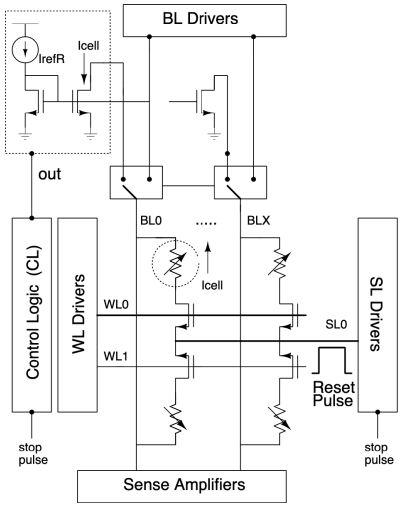


FIGURE 10. RST write termination implementation.

3) READ OPERATION

One of the major components in a memory architecture is the sense amplifier. The function of a sense amplifier is to read out the values in the cell array by sensing a voltage or current difference between two bit-lines and producing a full-swing rail-to-rail output. In the present paper, the Pre-Charged Sense Amplifier (PCSA) presented in Fig. 11a is applied. The PCSA has been extensively used in the literature as it improves significantly the reliability and sensing latency [22]. Conventionally, when reading an OxRAM cell, the resistance of the addressed cell is compared against a reference resistance. In our approach, the reference resistance is replaced by a current mirror to provide a strict and dynamic control of the reference current.

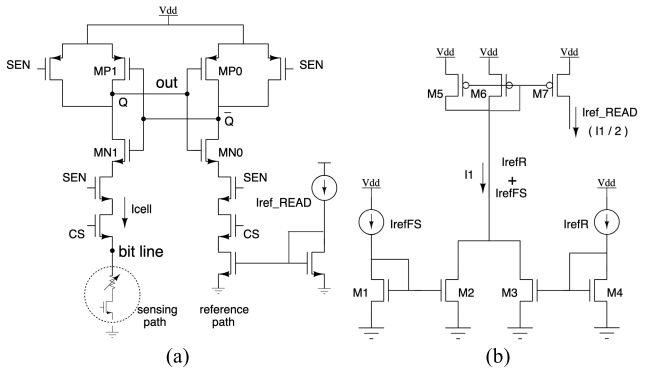


FIGURE 11. a) PCSA circuit with reference current control and b) read current generation technique according to SET and RST programming conditions.

Main components of the proposed PCSA are two inverters (MP0, MN0 and MP1, MN1) making a latch circuit. The PCSA requires two operating phases depending on the *SEN* (Sense Enable) control signal. When *SEN* is set to '0', the *Q* and *Qb* nodes are pre-charged to V_{dd}. When *SEN* signal is switched to '1', these pre-charged nodes start discharging, provided that *CS* (Column Select) signal used to activate the

addressed bit line is enabled. As the discharge current controls the latch circuit, a small difference between the currents is turned into a large output voltage. Note that the sensing path current is fixed by the resistance of the addressed cell, whereas the reference path current is forced to I_{ref_READ}.

To obtain an optimal read margin, I_{ref_READ} should be set exactly between the current provided by a LRS cell and the one provided by a HRS cell. To this aim, we propose to calculate the reference current by averaging the SET and RST threshold currents I_{refS} and I_{refR} respectively as presented in Fig. 11b. Indeed, the LRS resistance is the image of the I_{refS} current ($R_{LRS} = V_{cell}/I_{refS}$) and the HRS resistance is the image of I_{refR} current ($R_{HRS} = V_{cell}/I_{refR}$). V_{cell} being the voltage across the cell just before SET and RST pulses are interrupted. This technique provides an optimal read margin regardless of the SET and RST programming conditions. Note that the cell current I_{cell} is fixed by the previous RST/SET operation. Thus, post-RST and post-SET resistance values have a direct impact on current consumption.

IV. CIRCUIT LEVEL EVALUATION

A. SIMULATION SETUP

We implemented the memory circuit presented in Fig. 5 using a 0.13μm High Voltage CMOS technology offering a 3.3 V supply voltage. A 3.3 V technology is required as the FMG operation involves high voltages. To verify the operation of our design scheme, SPICE simulations are performed using the *Eldo* simulator. In order to discuss the energy efficiency of OxRAM memory devices, both reading/programming currents and reading/programming times need to be considered. Table 3 presents typical values for I_{refF}, I_{refS}, I_{refR}, I_{ref_READ} and FMG, SET, RST and READ typical resistance values referred to as R_{eq}. For the read operation, R_{eq} is obtained by averaging R_{LRS} and R_{HRS}.

TABLE 3. Reference current values during FMG, RST, SET and READ.

	I_{refF}	I_{refS}	I_{refR}	I_{ref_READ}	R_{eq}
FMG	75 µA	-	-	-	10.5 kΩ
SET	-	55 µA	-	-	10 kΩ
RST	-	-	3 µA	-	600 kΩ
READ	-	-	-	29 µA	305 kΩ

According to the literature, a minimal current of 55 μA is chosen for the SET operation as it is still considered as a reliable programming current for the considered technology [23]. Regarding the FMG operation, the limit has to be increased to 75 μA in order to reach a LRS value close to 10 kΩ for acceptable programming time with programming voltage close to 3.3 V [16]. For the RST operation, a threshold of 3 μA is chosen in order to limit the HRS resistance decrease to a value close to 600 kΩ, preventing uncontrolled HRS variations.

In order to accurately evaluate the benefits of our proposed scheme on large memory arrays, BL and WL lengths have been modelled to mimic a 1 Mbyte array (made of 1024 WLs and 1024 × 8-bits BLs). As a BL is characterized by a parasitic capacitance distributed through its length, a 1 pF bit line capacitance is used according to the targeted technology and the array architecture, presented in Fig.5. Additionally, parasitic resistances distributed along BLs and WLs have been inserted in the design based on the considered technology, following the methodology developed in [24].

Based on the proposed simulation setup, different pulses are applied to the memory array and the energy per cell and post programming resistance values are extracted. More specifically, word programming is performed in 2 steps. Once a 8-bit word is addressed, all cells are RST in parallel (logical '0') through the SL. Then, memory cells are SET (logical '1') through the BLs according to the data bus values. During RST, multi-bit access is guaranteed as one write termination is associated with a single BL (Fig. 9). During SET, multi-bit access is allowed only if the current mirror circuit presented in Fig. 8 is connected to the BL (i.e., current comparator located at the BL driver side). This last configuration is adopted.

B. TRANSIENT SIMULATION RESULTS

Transient simulation results are presented in Fig. 12 after FMG, RST and SET operations considering the reference currents presented in Table 3. During FMG (Fig.12a), the cell current I_{cell} is sensed and compared to the reference current I_{refF}. When I_{cell} reaches the reference current value set to 75 μA, the FMG pulse V_{FMG} is terminated. The standard fixed width FMG pulse V_{FMG_std} is also reported. One can notice that terminating the FMG pulse results in significant energy savings, as it prevents a large current to flow through the cell just after the switching event. Moreover, a high control over the final resistance is possible, preventing over-forming the cells. The proper working operation of the FMG stage is assessed by monitoring the cell resistance which reached a LRS value equal to 10 kΩ just after the FMG pulse termination.

During RST (Fig.12b), the cell current I_{cell} gradually decreases down to I_{refR} set to 3 μA. Beyond this point, the RST pulse is terminated limiting the HRS resistance value to 600 kΩ. The standard RST pulse V_{RST_std} is also reported, showing that the energy reduction obtained after terminating prematurely the RST pulse is much less compared to the FMG operation. The SET operation (Fig.12c) is comparable to the FMG operation as the memory cell ends in a LRS with a value close to 10 kΩ. However, the I_{cell} current change is abrupt and induces an important current overshoot leading I_{cell} to immediately exceed I_{refS} current set to 55 μA, which in turn terminates the SET operation. It is noteworthy that the standard 100 ns SET pulse is very short, which is common for SET operations [19]. This short pulse highlights the latency of the SET write termination as the SET pulse is not immediately terminated when I_{cell} exceeds I_{refS}. The coupling between the SET pulse and I_{refS} is discussed in the next sections.

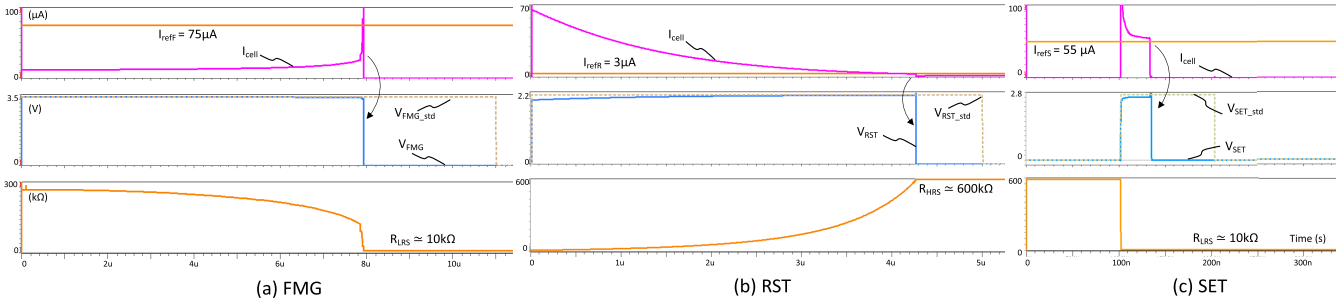


FIGURE 12. Transient simulation results after a) FMG, b) RST and c) SET operations.

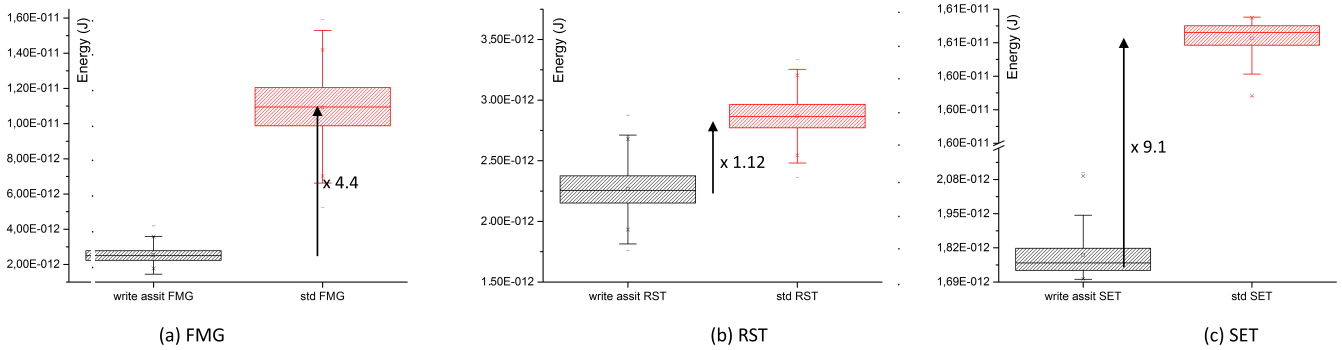


FIGURE 13. Energy/cell box plots obtained after MC simulation (5000 runs) after a) FMG, b) RST and c) SET operations.

C. MONTE CARLO ANALYSIS

To assess the impact of our design-scheme on energy consumption, a Monte Carlo (MC) analysis is conducted. In this analysis, only actual possible variations are reported, because cell variability is generated based on a targeted technology (i.e., a calibrated model featuring a variability dependency, see Fig.6). Moreover, the variability (including transistor mismatch) also targets the CMOS subsystem and especially the memory cell access transistor as its impact on the memory cell electrical characteristics is

dominant [25]. Process variation parameters used for CMOS transistors are provided by ST-Microelectronics (Crolles facility, France). On each simulation run, the MC analysis calculates every parameter randomly according to statistical distribution models. These statistical models are provided for active devices (MOSFETs) as well as for passive devices and cover corner cases.

It is worth noticing that current references are derived from a 'golden' current source provided by a bandgap voltage reference circuit included in the design [26]. Thus, the impact of PVT variations on the reference currents is mitigated as the bandgap produces a fixed (constant) current regardless of power supply variations, temperature changes and circuit loading.

During programming operations, two design configurations are considered. The first one takes advantage of the write assist circuits and is referred to as "write assist" or "wa". The second one, referred to as "standard" or "std" uses the conventional program scheme with fixed time duration.

Fig. 13 presents the impact of the memory cell variability after 5000 statistical runs following FMG (Fig. 13a), RST (Fig. 13b) and SET (Fig. 13c) operations. The energy distributions per memory cell are extracted and presented using box-plots. An overall trend is observed where the energy consumption is higher for the conventional scheme compared to the proposed write assist scheme. Energy consumption is reduced by a factor 4.4 during FMG. During RST, a reduction of 1.12 times is obtained and during SET, the write termination provides impressive results as the energy consumption per cell is reduced 9.1 times. Simulation results are summarized in Table 4.

TABLE 4. Energy/cell box plot distributions main parameters obtanined after 5000 statisctical runs.

Operation	Runs	Std. deviation	Median Value (J)	Energy reduction
wa FMG	5000	$3.960E^{-13}$	$2.499E^{-12}$	**x 4.4**
std FMG	5000	$1.565E^{-12}$	$1.094E^{-11}$	-
wa RST	5000	$1.650E^{-13}$	$2.255E^{-12}$	**x 1.2**
std RST	5000	$1.413E^{-13}$	$2.865E^{-12}$	-
wa SET	5000	$8.958E^{-14}$	$1.762E^{-12}$	**x 9.1**
std SET	5000	$2.784E^{-14}$	$1.611E^{-11}$	-

It is worth mentioning that no programming failure is detected after MC runs, which means that all the memory cells were able to cross the reference currents during FMG,

RST and SET operations (i.e., the write termination signal is triggered). In the case where the write termination signal would not be triggered, a stuck-at '0'/'1' fault would be detected (i.e., cell unable to SET/RST). Moreover, beyond being able to detect or not a proper write operation, the proposed write termination scheme also mitigates bit cell resistance uncontrolled variations as the reference currents are linked to specific HRS/LRS values (see Table 3).

V. DISCUSSION

A. READ OPERATION ENERGY

In this section, the READ energy is discussed versus R_{HRS} and R_{LRS} variations as well as variability. During the READ operation, two configurations are considered. The first one considers a memory cell in HRS state with a resistance value equal to 600 kΩ. The second one considers a memory cell in LRS with a resistance value equal to 10 kΩ. Fig. 14 presents transient simulation results. The PCSA presented in Fig. 11a is considered along with the read current generation circuit presented in Fig. 11b. Fig. 14a is a post-RST read operation. The READ window, fixed by the *SEN* signal is set to 20 ns. I_{ref_READ} is set to 29 μA according to Table 3. Note that the current consumption is mainly due to the current reference making the contribution of the cell current I_{cell} neglectable. Also, the reference current is provided to the sense amplifier only when *SEN* is high (for clarity, I_{ref} is represented as a straight line).

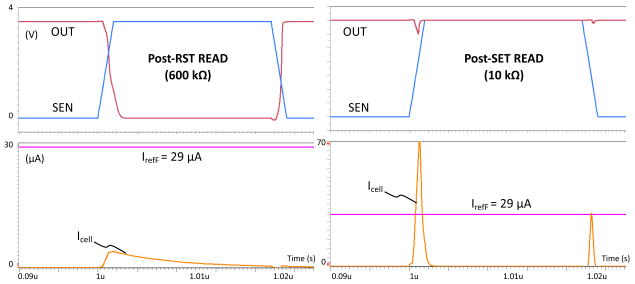


FIGURE 14. Transient simulation results of a READ operation for a) a 600 kΩ HRS cell and b) a 10 kΩ LRS cell.

Fig. 14b presents a post-SET read operation. Here again, I_{ref_READ} is set to 29 μA. When the *SEN* signal is high, the output of the PCSA switches to '1'. In this configuration, the cell current consumption increases and shows two peak values equal to 72 μA and 29 μA.

Post-RST and post-SET PCSA currents are also evaluated versus variability. Current distributions are extracted after 5000 MC runs and presented in Fig. 15. As expected, the LRS current is higher than the HRS current. However, it is worth noticing that the energy dissipation is mainly attributed to the reference path which provides the 29 μA current. Note that for the READ operation, current distributions are preferred to energy distributions as the energy is time dependent and can vary according to the READ window defined by the

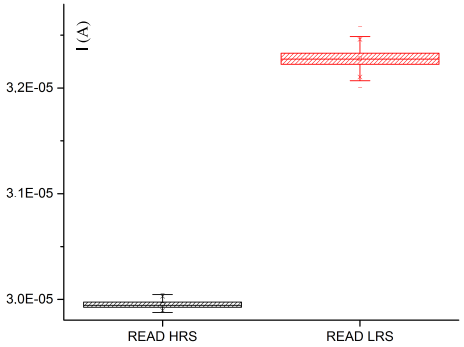


FIGURE 15. Current distributions extracted after 5000 MC runs for a 600 kΩ HRS cell and for a 10 kΩ LRS cell.

SEN signal. The latter is generally adjusted according to the considered technology, the memory array architecture as well as the sense amplifier topology.

Current consumption is also evaluated against R_{HRS} variation. Fig. 16 presents the evolution of the PCSA sensing path current during a READ operation for different R_{HRS} values. As R_{HRS} increases from 100 kΩ to 1 MΩ, the consumed current decreases from 32.55 μA to 31.55 μA, showing that R_{HRS} variation has a low impact on current consumption during a READ operation. If the reference current is not taken into account, the consumed current decreases from 3.55 μA to 2.55 μA (a 28% reduction). A study against R_{LRS} variation is not conducted as the variation of R_{LRS} versus the applied pulse width is neglectable. This last point will be further developed in the next section.

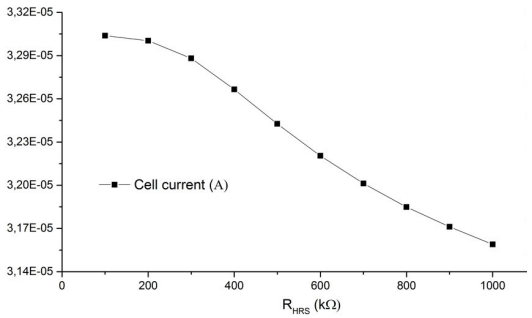


FIGURE 16. Evolution of the PCSA current consumption during a READ operation for different R_{HRS} values ranging from 100 kΩ to 1 MΩ.

B. ENERGY REDUCTION VERSUS RELIABLE READ OPERATION

In addition to providing major benefits in terms of energy reduction, the proposed design scheme offers the possibility to monitor post-RST and post-SET resistance values, which is a critical point, as HRS and LRS values need to be properly controlled to guarantee a reliable read operation. Indeed, as already mentioned, the sense amplifier reference current value should be set exactly between the current delivered by a LRS cell and the one delivered by a HRS cell, provided that the read margin, referred to as $\Delta R = R_{HRS}$-R_{LRS} in

this study, is large enough. Thus, an energy reduction versus reliable read operations co-optimization scheme needs to be developed.

Before developing the co-optimization scheme, a few observations can be made. Fig 17 shows the impact of the SET reference current I_{refS} on the SET pulse width. When I_{refS} decreases from 55 μA to 5 μA, the SET pulse width decreases from 100 ns to 11 ns, potentially resulting in a huge impact on power consumption with a neglectable change in the final LRS resistance. In contrast to the SET operation, the RST threshold current I_{refR} has a strong impact on the final HRS resistance value (i.e., the higher the I_{refR} value, the narrower the RST pulse and the lower the HRS resistance). These trends have been experimentally validated in [23] for the considered technology. Fig. 17 also highlights the latency of the write termination (i.e., delay between the I_{refS} threshold current detection and the SET pulse termination).

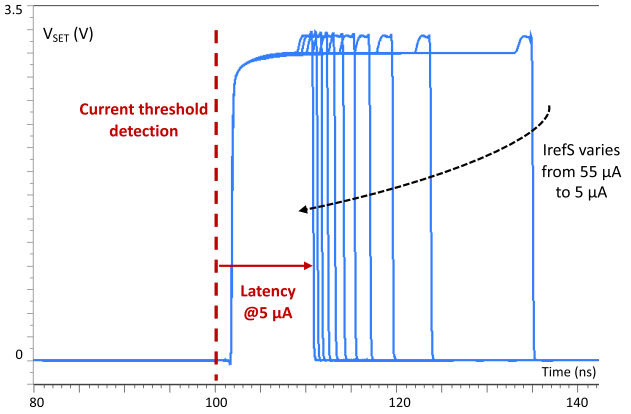


FIGURE 17. I_{refS} versus SET pulse width. When I_{refS} decreases from 55 μA to 5 μA, the pulse width decreases from 100 ns to 11 ns. The write termination latency is also highlighted (in red) for I_{refS} = 5 μA.

Fig.18 presents the evolution of the HRS resistance as well as the LRS resistance for different RESET (I_{refR}) and SET (I_{refS}) currents. I_{refR} ranging from 2 μA to 12 μA and I_{refS} ranging from 5 μA to 55 μA.

The R_{LRS} final value is not affected by I_{refS} variation (a few ohms-range variation is observed), although the SET pulse decreases with decreasing I_{refS} values (see Fig. 17). Regarding the HRS resistance, its value decreases as I_{refR} increases. Note that increasing I_{refR} limits R_{HRS} variation range, but at the cost of decreasing the read margin ΔR which starts at 962 MΩ and drops to 115 kΩ. To achieve a reliable READ operation, the reference current tracking technique presented in section III.C is used to dynamically set the read reference current I_{ref_READ} (average of I_{refS} and I_{refR}). The image of I_{ref_READ} referred to as R_{eq} is reported in Fig. 18, demonstrating the dynamic reference current tracking capability of the proposed PCSA.

At this point, the co-optimization process consists in finding the best trade-off between energy efficiency and an acceptable read margin. To this aim, MC simulations are

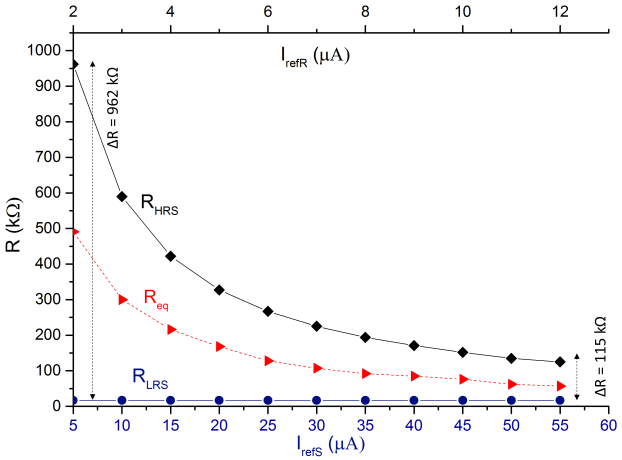


FIGURE 18. Evolution of HRS and LRS resistances for different SET (I_{refS}) and RESET (I_{refR}) current reference values. The read margin ΔR and the equivalent read resistance R_{eq} (image of I_{ref_READ}) are also reported.

performed for specific I_{refR} and I_{refS} currents picked from Fig. 18 in order to track the evolution of the read margin versus variability. R_{LRS} and R_{HRS} resistance distributions are extracted after 500 MC simulations and presented in Fig. 19. Although the read margin ΔR is reduced to 792 kΩ and 113 kΩ (compared to 962 kΩ and 115 kΩ respectively in Fig. 18), no distribution overlap is observed.

Regarding the energy reduction versus reliable read operation co-optimization process, it appears clearly that the best threshold currents choice is associated with I_{refS} = 5 μA, I_{refR} = 2 μA along with $I_{refREAD}$ = 3.5 μA and ΔR = 792 kΩ. Indeed, minimal threshold current values reduce write and read operations energy and provide a optimal read margin at the same time. However, a minimal I_{refR} value increases the RST pulse length, hence, degrading the RST speed.

C. COMPARISON WITH STATE-OF-THE-ART

Table 5 summarizes the proposed write-assist scheme and compares it to state-of-the-art write termination schemes. Comparison metrics include energy reduction (in %) during FMG, RST and SET, READ energy tracking and proper operation evaluation, the ability to propose a strict control of the operating currents, the area overhead (expressed in terms of number of transistors) along with the use of passive components.

In [7], the authors propose a low-dc-current voltage-mode write termination (LDC-VWT) module, including SET and RST terminators allowing 70% and 92% energy reduction in RST and SET respectively. A 65-nm RRAM macro was fabricated to confirm the developed concepts. For the RST operation, the proposed termination includes many analog and digital blocks including an ac-coupling capacitor, a voltage-swing detector and a voltage-controlled write driver resulting in a large area. In contrast, for the SET operation, only 3 transistors are needed. In [8], only the FMG operation is addressed along with a pulse programming

TABLE 5. Comparison to state of the art architectures.

	Energy reduction (%)						
	FMG	RST	SET	READ	Current Control	Area*	Pass. Comp.
[7], 19	-	70%	92%	yes	no	~150	1C
[8], 18	27%	-	-	yes	yes	~30	-
[9], 13	-	40%	99%	yes	no	~150	1R
[10], 16	-	63%	21%	no	no	~70	3R,2C
[11], 19	97%	93%	65%	no	no	~50	-
Work	**44%**	**1%**	**91%**	**yes**	**yes**	**22**	**-**

[a]C: Capacitor [b]R: Resistor
*Analog/Digital blocks have been converted to transistors

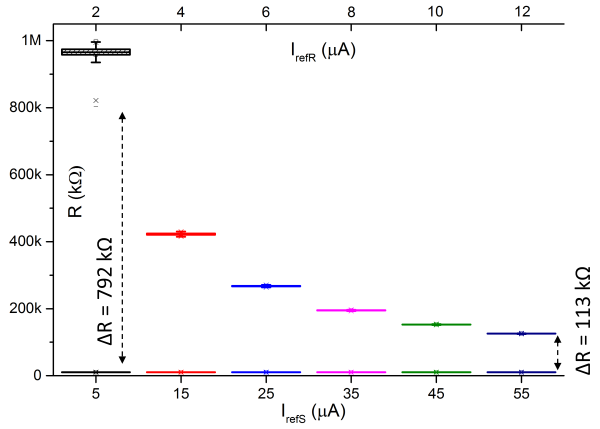


FIGURE 19. Read margin evolution after MC simulations for different I_{refR} and I_{refS} currents.

approach. Authors achieved a 27% energy reduction along with a 57% reduction of the standard deviation of post-FMG distributions. In [9], adaptive write and read assist circuits are proposed to fix yield and power consumption issues. A 99% SET energy reduction is achieved at the cost of using two op-amps, delay circuits and bias generators. In [10], 63% and 21% energy reduction are obtained for RST and SET operations respectively, and an original programming technique based on pulse series with controllable amplitude and duration is used. However, the presented scheme uses an op-amp, a differentiator and additional capacitors and resistors, resulting in a substantial area overhead. In [11], high energy reduction factors are obtained (97% reduction for FMG and 93% for SET). However, the READ operation is completely missing as well as the impact of the proposed termination circuits on read performances. Moreover, no strict control of the programming currents is provided, preventing the monitoring of post-programming resistance values.

Compared to state-of-the-art write termination schemes, our solution excels with its minimal area overhead and important energy reduction for the SET operation. Moreover, the strength of our approach relies on the possibility to adjust dynamically the FMG, RST, SET and READ currents. For instance, in the best case, the SET energy reduction can be increased by a factor close to 10 if I_{refS} decreases from 55 μA to 5 μA (as the SET pulse width decreases from 100 ns to 11ns, see Fig. 17). This adjustment technique based on the control of the memory cell current during all operating modes advances the state of the art and is missing in previous works.

VI. CONCLUSION

This paper proposes a simple and feasible solution to mitigate two of the most challenging issues in filamentary-based Resistive RAM (RRAM) devices which are energy consumption, and HRS and LRS resistance control. A new energy saving design approach based on a strict control of RRAMs programming and reading currents is introduced. Its implementation offers a minimal area overhead along with a minimal number of control signals compared to state-of-the-art write termination implementations. The presented design methodology can be extended to any resistive RAM technology such as Phase-Change Memory or Spin-Transfer-Torque Magnetic Random Access Memory. Extensions of the current work will address the impact of high programming current control on reliability. Indeed, it has been demonstrated that high endurance and retention are closely linked to the programming currents since excessive and insufficient currents can result in RRAM memory cell failures.

REFERENCES

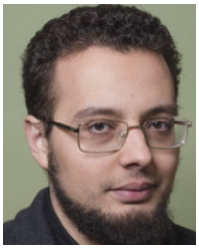
[1] K. Prall, "Benchmarking and metrics for emerging memory," in *Proc. IEEE Int. Memory Workshop (IMW)*, May 2017, pp. 1–5.
[2] S. Yu and P.-Y. Chen, "Emerging memory technologies: Recent trends and prospects," *IEEE Solid StateCircuits Mag.*, vol. 8, no. 2, pp. 43–56, Dec. 2016.
[3] W. S. Ngueya, J.-M. Portal, H. Aziza, J. Mellier, and S. Ricard, "An ultra-low power and high performance single ended sense amplifier for low voltage flash memories," *J. Low Power Electron.*, vol. 14, no. 1, pp. 157–169, Mar. 2018.
[4] E. I. Vatajelu, H. Aziza, and C. Zambelli, "Nonvolatile memories: Present and future challenges," in *Proc. 9th Int. Des. Test Symp. (IDT)*, Dec. 2014, pp. 61–66.
[5] G. Molas, G. Sassine, C. Nail, D. A. Robayo, J.-F. Nodin, C. Cagli, J. Coignus, P. Blaise, and E. Nowak, "Resistive memories (RRAM) variability: Challenges and solutions," *ECS Trans.*, vol. 86, no. 3, pp. 35–47, 2018.
[6] D. Ielmini, "Resistive switching memories based on metal oxides: Mechanisms, reliability and scaling," *Semicond. Sci. Technol.*, vol. 31, no. 6, pp. 1–25, 2016.
[7] C.-P. Lo, W.-Z. Lin, W.-Y. Lin, H.-T. Lin, T.-H. Yang, Y.-N. Chiang, Y.-C. King, C.-J. Lin, Y.-D. Chih, T.-Y.-J. Chang, and M.-F. Chang, "A ReRAM macro using dynamic Trip-Point-Mismatch sampling current-mode sense amplifier and low-DC voltage-mode write-termination scheme against resistance and write-delay variation," *IEEE J. Solid-State Circuits*, vol. 54, no. 2, pp. 584–595, Feb. 2019.
[8] H. Aziza, B. Hajri, M. Mansour, A. Chehab, and A. Perez, "A lightweight write-assist scheme for reduced RRAM variability and power," *Microelectron. Rel.*, vols. 88–90, pp. 6–10, Sep. 2018.
[9] X. Xue, W. Jian, J. Yang, F. Xiao, G. Chen, S. Xu, Y. Xie, Y. Lin, R. Huang, Q. Zou, and J. Wu, "A 0.13 μm 8 mb logic-based Cu_xSi_yO ReRAM with self-adaptive operation for yield enhancement and power reduction," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1315–1322, May 2013.
[10] J. Yang, "A self-adaptive write driver with fast termination of set-up pulse for ReRAM," *IEICE Electron. Express*, vol. 13, no. 7, pp. 1–6, 2016.
[11] M. Alayan, E. Muhr, A. Levisse, M. Bocquet, M. Moreau, E. Nowak, G. Molas, E. Vianello, and J. M. Portal, "Switching event detection and self-termination programming circuit for energy efficient ReRAM memory arrays," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 5, pp. 748–752, May 2019.
[12] S. Ambrogio, "Statistical fluctuations in HfOx resistive-switching memory: Part I—Set/RST variability," *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2912–2919, d2014.

[13] W.-H. Chen, W.-J. Lin, L.-Y. Lai, S. Li, C.-H. Hsu, H.-T. Lin, H.-Y. Lee, J.-W. Su, Y. Xie, S.-S. Sheu, and M.-F. Chang, "A 16Mb dual-mode ReRAM macro with sub-14ns computing-in-memory and memory functions enabled by self-write termination scheme," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2017, p. 28.
[14] D. Garbin, E. Vianello, O. Bichler, Q. Rafhay, C. Gamrat, G. Ghibaudo, B. DeSalvo, and L. Perniola, "HfO_2-based OxRAM devices as synapses for convolutional neural networks," *IEEE Trans. Electron Devices*, vol. 62, no. 8, pp. 2494–2501, Aug. 2015.
[15] A. Grossi, E. Nowak, C. Zambelli, C. Pellissier, S. Bernasconi, G. Cibrario, K. El Hajjam, R. Crochemore, J. F. Nodin, P. Olivo, and L. Perniola, "Fundamental variability limits of filament-based RRAM," in *IEDM Tech. Dig.*, Dec. 2016, pp. 4–7.
[16] D. M. Nminibapiel, "The efficacy of programming energy controlled switching in resistive random access memory (R5M)," Ph.D. dissertation, Elect./Comput. Eng., Old Dominion Univ., Norfolk, VA, USA, 2017.
[17] G. Wang, "Operation methods of resistive random access memory," *Sci. China Technol. Sci.*, vol. 57, no. 12, pp. 2004–2295, 2014.
[18] G. M. Wang, "Improving resistance uniformity and endurance of resistive switching memory by accurately controlling the stress time of pulse program operation," *Appl. Phys. Lett.*, vol. 10, Oct. 2015, Art. no. 092103.
[19] S. Ning, T. O. Iwasaki, and K. Takeuchi, "50 nm al o ReRAM program 31% energy, 1.6× endurance, and 3.6× speed improvement by advanced cell condition adaptive verify-reset," *Solid-State Electron.*, vol. 103, pp. 64–72, Jan. 2015.
[20] M. Bocquet, H. Aziza, W. Zhao, Y. Zhang, S. Onkaraiah, C. Müller, M. Reyboz, D. Deleruyelle, F. Clermidy, and J.-M. Portal, "Compact modeling solutions for oxide-based resistive switching memories (OxRAM)," *J. Low Power Electron. Appl.*, vol. 4, no. 1, pp. 1–14, Jan. 2014.
[21] M. Bocquet, D. Deleruyelle, H. Aziza, C. Muller, J.-M. Portal, T. Cabout, and E. Jalaguier, "Robust compact model for bipolar oxide-based resistive switching memories," *IEEE Trans. Electron Devices*, vol. 61, no. 3, pp. 674–681, Mar. 2014.
[22] W. Zhao, C. Chappert, V. Javerliac, and J.-P. Noziere, "High speed, high stability and low power sensing amplifier for MTJ/CMOS hybrid logic circuits," *IEEE Trans. Magn.*, vol. 45, no. 10, pp. 3784–3787, Oct. 2009.
[23] A. Grossi, E. Vianello, C. Zambelli, P. Royer, J.-P. Noel, B. Giraud, L. Perniola, P. Olivo, and E. Nowak, "Experimental investigation of 4-kb RRAM arrays programming conditions suitable for TCAM," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 12, pp. 2599–2607, Dec. 2018.
[24] J. Liang, S. Yeh, S. S. Wong, and H.-S.-P. Wong, "Effect of Wordline/Bitline scaling on the performance, energy consumption, and reliability of cross-point memory array," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 9, no. 1, pp. 1–14, Feb. 2013.
[25] H. Aziza, "Evaluation of OxRAM cell variability impact on memory performances through electrical simulations," in *Proc. Non-Volatile Memory Technol. Symp. Process.*, 2011, pp. 1–5.
[26] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, May 1999.

H. AZIZA received the B.S. and M.S. degrees in electrical engineering from the University of Marseille, France, and the Ph.D. degree from the University of Marseille, in 2002. He is currently an Associate Professor with the IM2NP Laboratory (Institute of Materials, Microelectronics and Nanosciences of Provence), Aix-Marseille University. He has (co)authored more than 120 articles in international conferences and journals and is a (co)inventor of five patents. He was involved in the French National Research Agency project DIPMEM dedicated to hybrid circuit design (CMOS-ReRAM). Since 2017, he has been the IM2NP's "Memory Team" Leader. IM2NP's "Memory Team" is composed of 12 permanents. Research thematics conducted by the group are fully dedicated to Resistive RAM technology, design, and test. His research interests include the design, test, and reliability of conventional non-volatile memories (Flash and EEPROM) as well as emerging memories (Resistive RAM).

M. MOREAU received the M.Sc. and Ph.D. degrees in micro and nanoelectronics from Aix-Marseille University, France, in 2007 and 2010, respectively. His doctoral research at the Institute of Materials Microelectronics and Nanosciences of Provence (IM2NP) covered numerical simulation and compact modeling of advanced nano-devices, such as FinFET, based on new materials (high-k and III–V semiconductors). From 2010 to 2011, he was a Teaching Assistant at polytech'Marseille and work on the compact modeling of organic thin-film transistors (OTFTs). Since 2012, he has been an Associate Professor at Aix-Marseille University and conducts his research at IM2NP in the field of hybrid circuit design based on emerging non-volatile memories (ReRAM and MRAM). He was a recipient of the Newcas 2013 Best Paper Award and the 2017 IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS Guillemin-Cauer Best Paper Award.

M. FIEBACK (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees from the Delft University of Technology, The Netherlands, in 2015 and 2017, respectively, where he is currently pursuing the Ph.D. degree. His research interests include device and defect modeling, and test and reliability of emerging memories.



M. TAOUIL (Member, IEEE) received the M.Sc. and Ph.D. degrees (Hons.) in computer engineering from the Delft University of Technology, The Netherlands. He is currently an Assistant Professor at the Computer Engineering Laboratory, Delft University of Technology. His current research interests include hardware security, embedded systems, 3D stacked integrated circuits, VLSI design and test, built-in-self-test, design for testability, yield analysis, and memory test structures.

S. HAMDIOUI (Senior Member, IEEE) received the M.S.E.E. and Ph.D. degrees (Hons.) from the Delft University of Technology (TU Delft), The Netherlands. He was with Intel Corporation, CA, USA, with Philips Semiconductors Research and Development, Crolles, France, and with Philips/NXP Semiconductors, Nijmegen, The Netherlands. He is currently the Chair Professor of dependable and emerging computer technologies, the Head of the Computer Engineering Laboratory (CE-Lab), and the Head of the Quantum and Computer Engineering Department, TU Delft. He is also the Co-Founder and the CEO of Cognitive-IC, a start-up focusing on hardware dependability solutions. His research interests include two domains: dependable CMOS nano-computing (including testability, reliability, and hardware security) and emerging technologies and computing paradigms (including memristors for logic and storage, in-memory-computing, and neuromorphic computing).