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RESEARCH ARTICLE

Strategy to mitigate the dipole interfacial states in (i)a-Si:H/MoO_x passivating contacts solar cells

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Abstract

Molybdenum oxide (MoO_x) is attractive for applications as hole-selective contact in silicon heterojunction solar cells for its transparency and relatively high work function. However, the integration of MoO_x stacked on intrinsic amorphous silicon (i)a-Si:H layer usually exhibits some issues that are still not fully solved resulting in degradation of electrical properties. Here, we propose a novel approach to enhance the electrical properties of (i)a-Si:H/MoO_x contact. We manipulate the (i)a-Si:H interface via plasma treatment (PT) before MoO_x deposition minimizing the electrical degradation without harming the optical response. Furthermore, by applying the optimized PT, we can reduce the MoO_x thickness down to 3.5 nm with both open-circuit voltage and fill factor improvements. Our findings suggest that the PT mitigates the decrease of the effective work function of the MoO_x (WF_{MoO_x}) thin layer when deposited on (i)a-Si:H. To support our hypothesis, we carry out electrical simulations inserting a dipole at the (i)a-Si:H/MoO_x interface accounting the attenuation of WF_{MoO_x} caused by both MoO_x thickness and dipole. Our calculations confirm the experimental trends and thus provide deep insight in critical transport issues. Temperature-dependent *J-V* measurements demonstrate that the use of PT improves the energy alignment for an efficient hole transport.

KEYWORDS

(i)a-Si:H/MoO_x hole transport contact, interfacial dipole layer, plasma treatment, TCAD electrical modeling

1 | INTRODUCTION

Silicon heterojunction (SHJ) solar cells are attractive for their high-efficiency potential and simple structure processing.¹ The key element of this technology is the use of the Si thin-film technology based on hydrogenated amorphous silicon (a-Si:H) films grown by plasma-enhanced chemical vapor deposition (PECVD).² By stacking together

intrinsic and doped silicon thin films, it is possible to combine excellent surface passivation and carrier selectivity reaching open-circuit voltage up to 750 mV.³ The potential of the SHJ concept results in record conversion efficiency (η) of 26.7%⁴ in all-back contacted architecture. This device configuration can benefit from very high current density of 42.5 mA/cm²,⁴ but the higher fabrication complexity strongly limits its market uptake. The two-side contacted SHJ solar

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cell instead has a lean and cost-effective production process⁵ with η of 25.1%.⁶ The front layer stack is responsible for 2.1 mA/cm² current losses caused by parasitic absorption in a-Si:H layers and transparent conducting oxide (TCO).⁷ Many groups devoted efforts to minimize those losses by carefully optimizing layer thickness/properties and developing wider band gap layers to replace intrinsic and/or doped a-Si:H films. The most explored approaches consist in alloying the silicon films with oxygen or carbon,^{8–14} developing doped hydrogenated nanocrystalline silicon oxide^{15–21} or silicon carbide films via hot-wire chemical vapor deposition (CVD).²² Alternatively, highly transparent TCO electrodes^{23–25} or improved antireflective stack²⁶ are used. Furthermore, others suggested to replace the (i)a-Si:H passivation layer with SiO₂ obtaining remarkable η .^{22,27}

In recent years, a new explored route consisted in replacing doped layers with the so-called dopant-free materials.²⁸ Within this category, transition metal oxides (TMOs) exhibit a wide range of work function (WF) values enabling several applications in photovoltaic technologies especially in combination with organic semiconductors.^{29,30} Those materials are similarly attractive in SHJ solar cells for their ability to induce an efficient carrier selectivity for both hole and electron transport layers.^{31–38} When TMO films replace the highly doped silicon-based layers on the illuminated side of the device, parasitic absorption losses can be strongly mitigated, resulting in clear current gain.^{31,33,34,39,40}

Among TMOs, molybdenum oxide (MoO_x) is promising for applications as hole transport layer (HTL) in replacement of the traditionally used (p)a-Si:H in SHJ device.^{31,41} MoO_x layer, in combination with a thin (i)a-Si:H layer and a TCO, has in fact demonstrated conversion efficiency of 23.5%.⁴²

MoO_x is an n-doped material and can act as HTL owing to its large work function as compared to Si. In particular, the difference in WF induces a band bending in the c-Si absorber with a surface inversion layer at the c-Si interface promoting a proper hole transfer (typical of a p-contact) and a barrier for electrons.⁴³ Furthermore, MoO_x has particularly low absorption coefficient in the visible wavelength range as compared to Si layers⁴⁴ that makes the material promising for application as window layer. MoO_x exhibits variable WF in the range of 6.9 to 4 eV depending on the deposition processing and stoichiometry.^{45–48}

Additionally, several groups^{49–52} report the formation of a relatively thick 2- to 3-nm sub-stoichiometric silicon oxide (SiO₂) interlayer at the (i)a-Si:H/MoO_x interface in the as-deposited state. More controversial is the instance of MoO_x in stack with (i)a-Si:H or indium tin oxide (ITO). On one hand, transmission electron microscopy (TEM) inspection suggests that SiO₂ does not increase in thickness with annealing up to 180°C.⁴⁹ On the other, when the device-relevant (i)a-Si:H/MoO_x/ITO stack undergoes annealing, the contact resistivity drastically increases for relatively low temperature (150–210°C).⁵³ No changes are instead observed when the (i)a-Si:H is omitted.¹⁷ In this respect, as degradation mechanism, others⁵⁴ propose the WF reduction of MoO_x triggered by the observed H effusion from (i)a-Si:H.

Usually, electrical performances of cells featuring MoO_x as HTL are below the record SHJ device.⁶ Those devices exhibit typically

lower fill factor (FF) and possibly S-shaped J-V characteristics,^{40,49} indicating carrier selectivity issues. A strategy to overcome this limitation and fabricate solar cells with MoO_x free from S shape was proposed by Essig et al.⁵⁴ They optimized a pre-annealing treatment at 250°C of the (i)a-Si:H passivation layer followed by a chemical removal of the surface oxidation. Nevertheless, the reasons behind device degradation mechanisms of MoO_x at device level are not fully understood yet.

In this work, we study the device degradation by focusing on the (i)a-Si:H/MoO_x interface and propose an alternative and industrial compatible treatment to successfully integrate MoO_x in SHJ solar cells. In fact, the strong difference in work function between the two adjacent materials affects the accumulation/depletion of holes at this interface with formation of an interface dipole.⁴⁵ To address this point, we manufacture high-performance solar cells integrating the MoO_x layer after a practical plasma treatment (PT). To support our findings, we investigate the potential sources of degradation by means of technology computer-aided design (TCAD) simulations and relate the calculations to the experimental trends to identify the optimal MoO_x thickness.

2 | EXPERIMENTAL AND SIMULATION METHODS

We fabricated SHJ solar cells using 4-inch double-side polished n-type float-zone (FZ) wafers with <100> orientation, resistivity of 3 Ω cm, and initial thickness of 280 μ m. After texturing and wet chemical cleaning procedures, the wafers are dipped in 0.55% hydrofluoric acid for 5 min to remove the native oxide prior layer deposition. For all cells, the electron transport contact at the rear side is kept constant and consists of a (i)a-Si:H/(n)a-Si:H stack. On the illuminated side, three different types of front HTL stacks are fabricated as depicted in

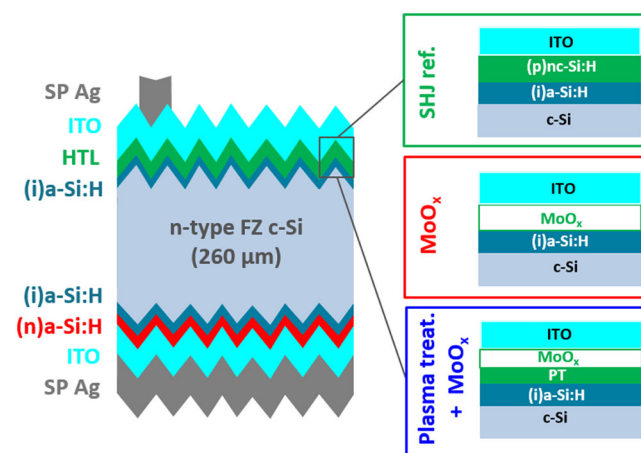


FIGURE 1 Cross-sectional sketch of front/back-contacted SHJ solar cells fabricated with three different front HTL as depicted in the zoom box: SHJ reference with 20 nm thick (p)nc-Si:H (green), MoO_x (red), and plasma-treated + MoO_x (blue). Layers not to scale. FZ, float zone; HTL, hole transport layer; ITO, indium tin oxide; SHJ, silicon heterojunction

Figure 1. The reference SHJ device is completed with 20 nm thick (p) nc-Si:H as optimized in Zhao et al.,¹⁷ while the other two configurations are completed with MoO_x layer with variable thicknesses. In the last variation, the (i)a-Si:H layer surface is treated with a plasma of SiH₄, H₂, CO₂, and B₂H₆ (PT) for variable time at the pressure of 2.2 mbar and power 90 mW/cm² in the same PECVD tool prior MoO_x deposition. For all configurations, a nominally 5 nm thick (i)a-Si:H layer is deposited by PECVD. The contacts are completed with sputtered In₂O₃:Sn (ITO)²⁵ as TCO layers and screen printed Ag cured in an oven at 170°C for 30 min, defining cells with area of 3.92 cm² and front metal coverage of 4.4%. All samples with exposed MoO_x films are kept under high vacuum when possible or, alternatively, in a N₂ flow cabinet to minimize exposure in atmosphere.

The sub-stoichiometric MoO_x is thermally evaporated from a MoO₃ powder source (Aldrich Chemistry, 99.98%) at a deposition rate of 0.1 nm/s after reaching a base pressure of 5·10^{−6} mbar. MoO_x thickness was determined on wafer samples by means of angle-dependent spectral ellipsometry using a J.A. Woollam Co., Inc. setup at incident angles between 50° and 70°. We modeled the MoO_x layer using the Tauc–Lorentz dispersion model as reported in Sacchetto et al.⁴⁹

The passivation quality of solar cell precursors is measured by Sinton WCT-120 under transient photo-conductance decay mode to extract implied open-circuit voltage (*i*-V_{OC}). The current–voltage characteristics are measured using a Wacom WXS-156S-L2 solar simulator under standard test conditions through a shadow mask. Illumination-dependent open-circuit voltage (SunsV_{OC}) curves are measured on completed cells using a Sinton Instruments WCT-150 to acquire the pseudo-fill factor (*p*-FF).

An in-house external quantum efficiency (EQE) setup is used to obtain the integrated *J*_{SC,EQE}, thus analyzing the spectral response of the device without the influence of the front metal grid.

The simulations are carried out using TCAD Sentaurus device simulator⁵⁵ running drift-diffusion models previously validated for

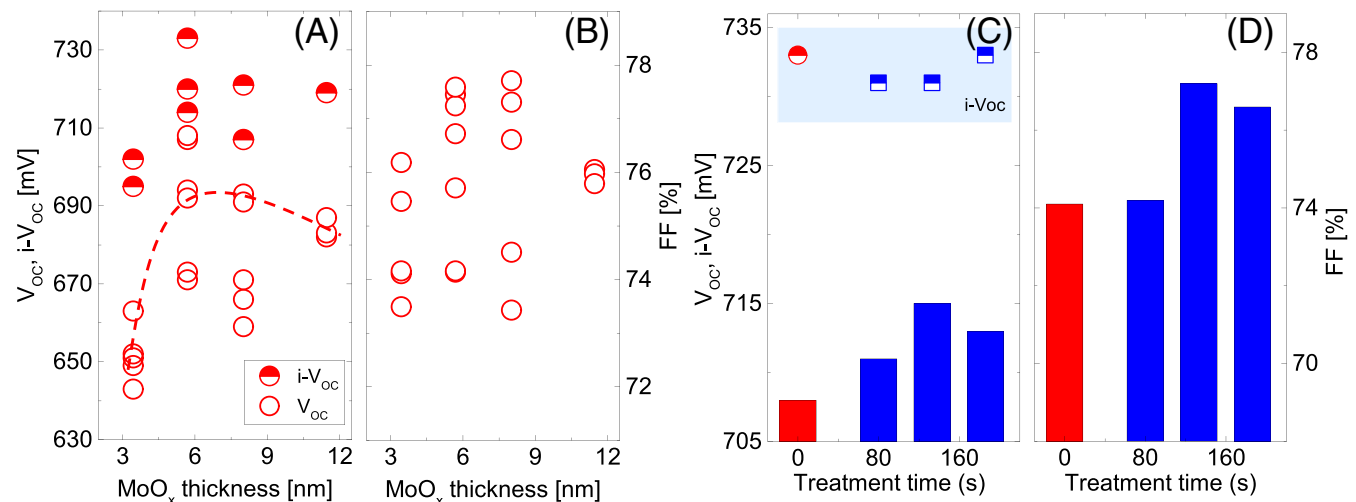
SHJ solar cells.^{56,57} The structure includes a n-type c-Si absorber passivated by a 5 nm thick (i)a-Si:H layer and coated by a MoO_x (3–9 nm) and a thin SiO₂ layer at the (i)a-Si:H/MoO_x interface that is formed during the evaporation process as confirmed by other groups.^{49–51,58} The front contact is then completed with ITO film (65 nm).

3 | SOLAR CELL RESULTS

Figure 2A,B shows open-circuit voltage (*V*_{OC}), *i*-*V*_{OC}, and fill factor (*FF*) as a function of the MoO_x thickness. The data show a *V*_{OC} dependency on the MoO_x thickness despite the large distribution observed. Particularly, poor *V*_{OC} are measured (<665 mV) for the thinnest MoO_x layer tested, while *V*_{OC} increases when thicker layers are used. As similarly reported in Cho et al.,⁵⁰ in the range of 5–8 nm, the *V*_{OC} reaches a maximum. Above this value, *V*_{OC} decreases. In the same figure (Figure 2A), a comparable trend is observed for the *i*-*V*_{OC} values measured on the cell precursors after ITO depositions. Besides that, we measure a drastic drop in *V*_{OC} in the range of 25–40 mV by comparing the *i*-*V*_{OC} to the value measured on the completed device which indicates a sort of material degradation. The *FF* data in Figure 2B follow a similar tendency as *V*_{OC} with higher *FF* for MoO_x of 5.7–8 nm.

We do not ascribe these low parameters to the thermal budget during the metallization because the process temperature is kept at a relatively low temperature (170°C) which is identified as optimal.⁵⁰

The results reported in Figure 2A for *i*-*V*_{OC} reveal that the (i)a-Si:H/c-Si heterointerface remains in similar conditions for MoO_x > 6 nm. Therefore, we explore the (i)a-Si:H/MoO_x interface where the charge transfer is based on recombination between electrons from the MoO_x and holes from the c-Si absorber.^{56,59} Such a recombination is essential for an efficient transport and the (i)a-Si:H/MoO_x interface is critical because of the abrupt changes in energy caused by the large difference in *WF* of (i)a-Si:H and MoO_x.



To address this specific aspect, we treat the (i)a-Si:H layer surface with a PT prior to the MoO_x deposition. While the PT time is varied, the MoO_x thickness is kept constant at 5.7 nm. The results are summarized in Figure 2C,D for devices fabricated within the same batch. For all the cells, we measure i -V_{OC} values (prior metallization) above 730 mV. In particular, the cell with no treatment and only 5.7 nm of MoO_x exhibits the lowest V_{OC} of 708 mV and the FF limited to 74.2%.

The data show that there is a clear impact of the interfacial PT of the (i)a-Si:H on electrical properties. The measured V_{OC} is consistently

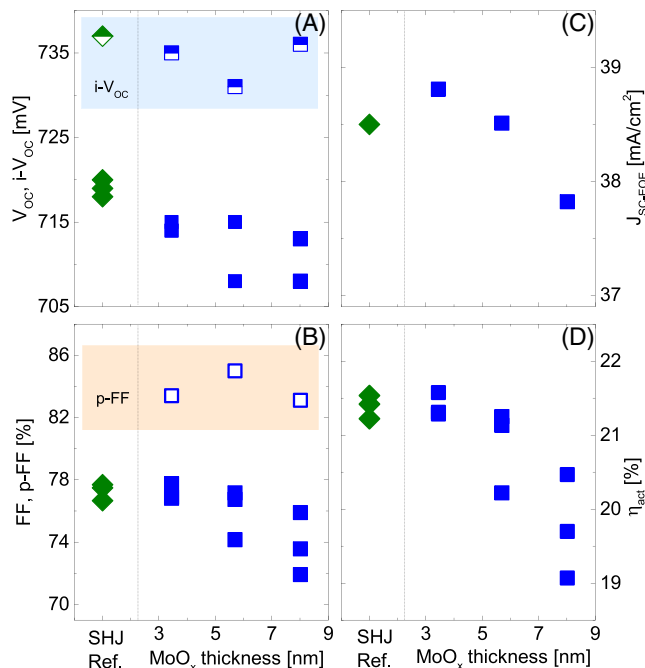


FIGURE 3 Solar cell parameters with different MoO_x thickness and constant interfacial plasma treatment (130 s) compared to silicon heterojunction (SHJ) reference. (A) V_{OC} and i -V_{OC}, (B) FF and p-FF, (C) J_{SC-EQE}, and (D) η_{act}. Note that all the cells (except the SHJ reference) feature an unintentionally thicker indium tin oxide (90 nm) that reduces J_{SC} by ~0.55 mA/cm². All the cells have an area of 3.92 cm²

higher with respect to the not treated cell, while the benefit on FF is appreciable only for longer PTs. We identify the optimum for PT at 130 s with measured V_{OC} of 715 mV and FF above 77%. X-ray photoelectron spectroscopy (XPS) spectra in Figure S1 show that the PT does not result in boron incorporation.

In Figure 3, we report the thickness optimization for the (i)a-Si:H/MoO_x stack featuring a PT time of 130 s. The results in Figure 3A,B indicate that MoO_x layer thickness can be reduced down to 3.5 nm without V_{OC} loss (715 mV) and with a linear gain in FF up to 77.7%. The device endowed with the optimized PT + MoO_x stack reaches FF equal to the SHJ reference cell with only 5-mV losses in V_{OC}.

In Figure 3C, J_{SC-EQE} progressively increases by thinning the MoO_x layer, but the values are still limited by the relatively thick ITO layer on the front side that shifts the antireflection pick away from the optimum wavelength with an estimated current loss of ~0.55 mA/cm² calculated by optical simulation using GenPro4.⁶⁰ Consequently, the gains observed for the optimized PT combined with a thin MoO_x lead to a η of 21.6% comparable to the value measured for the reference SHJ cell, as shown in Figure 3D.

4 | DISCUSSION

Here, we discuss the experimental results of Section 3 supported by TCAD electrical simulations aiming at identifying the critical elements and how they contribute to the device electrical performances. Furthermore, these calculations help to better understand the trends observed for solar cells' electrical parameters and to explain the dominating transport mechanisms behind.

4.1 | Effect of MoO_x thickness

The relatively low electrical parameters observed in Figure 2A,B reveal a degradation in selectivity and transport of the HTL. In particular, the low V_{OC} values indicate high recombination and therefore

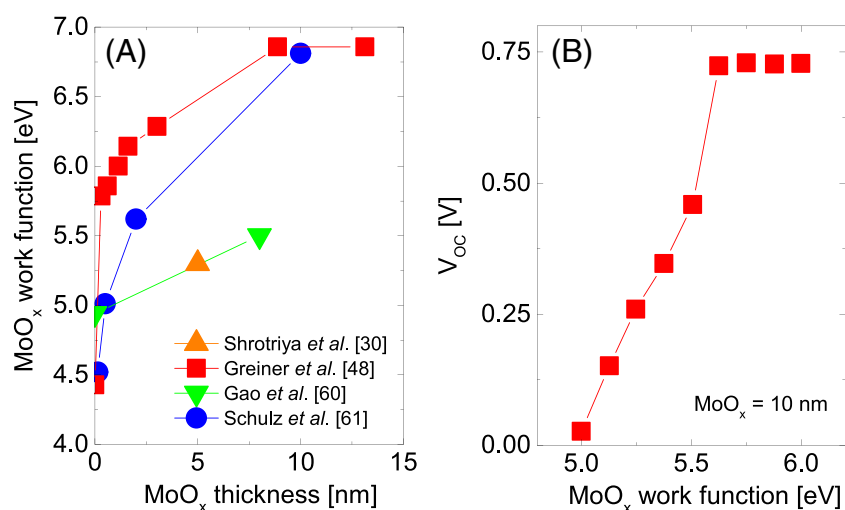


FIGURE 4 (A) Literature values of MoO_x work function as a function of MoO_x layer thickness. (B) Numerical simulation for V_{OC} as function of W_FMoO_x and for a fixed thickness of MoO_x equal to 10 nm. The lines are guides to the eye

poor selectivity, while poor *FFs* suggest issues with transport of holes. Those observations can be explained by *WF* variation of MoO_x thin films. As depicted in Figure 4A, many groups^{30,48,58,61} report a clear reduction of *WF* for thinner MoO_x layers. The great variability among the data may depend on the different deposition methods, material quality, and eventual reaction with air. Irfan et al.⁶² observe similar trend after exposing MoO_3 to oxygen and air with a resulting *WF* of 5.8 and 5.3 eV, respectively. Similarly, Battaglia et al.⁴¹ report for thermally evaporated MoO_x films a *WF* of 6.6 eV that is drastically reduced to 5.7 eV after air exposure. A *WF* reduction is furthermore observed in case of temperature exposure of MoO_x material with deteriorated passivation performances.⁶³

One reason for *WF* attenuation can be ascribed to the oxygen deficiency in MoO_x . As a consequence, the material is reduced with an increase in the concentration of lower cation oxidation states (Mo^{5+} and Mo^{4+}) that accounts for a linear reduction of WF_{MoO_x} .⁴⁸ A second contribution is related to the oxygen vacancies with an energy close to the Fermi level (E_F) that act as n-type dopants. This results in a drastic decrease of *WF* with oxygen deficiency as compared to the stoichiometric MoO_3 .⁶⁴

Furthermore, it has been observed that oxygen deficiency occurs preferentially at the interface with (i)a-Si:H and in the initial stage of growth leading to a sub-stoichiometric SiO_x layer.^{48,50,58} Similar to what was discussed above, the reduced layer thickness (i.e., further reduced *WF*) can negatively influence the transport, explaining the low V_{OC} measured for the 3.5 nm thick MoO_x cells in Figure 2A.

To investigate the effect of reduced WF_{MoO_x} on V_{OC} , we report in Figure 4B electrical simulation results obtained with 10 nm thick MoO_x with variable *WF* values. As the *WF* increases, we calculate an

increase in V_{OC} until it reaches a saturation. The observed trend in Figure 4B can be explained as higher *WF* implies higher band bending at the c-Si interface.⁶⁵

Consequently, it induces higher accumulation of holes at the interface with a more efficient carrier separation. Furthermore, for low WF_{MoO_x} values, we observe that a relatively weak band bending inside c-Si results in carrier recombination along (i)a-Si:H/ MoO_x heterointerface. On the contrary, for higher WF_{MoO_x} values, we detect improvements in c-Si band bending and carrier population with the consequent reduction of recombination.

We stated above that material composition can be responsible for reduction of the *WF* in MoO_x . We expand here the discussion about *WF* attenuation of MoO_x layers to include such an effect in our calculations. Assuming a classical depletion approximation for the heterojunction under investigation, the energy of the valence band can bend up to reaching the Fermi energy. Under such conditions, the inverted potential inside c-Si (V_{bi}) is favorable for positive charge accumulation at (i)a-Si:H/ MoO_x interface that accounts as traps for negative charge from n-type MoO_x ,⁴³ thus forming the so-called dipole. We assume such an effect as work function attenuation due to dipole ($\Delta WF_{\text{dipole}}$) at the (i)a-Si:H/ MoO_x interface. Following the approach suggested in Gerling et al.⁴³ and Bisquert,⁶⁶ we have

$$WF_{\text{MoO}_x}(t) - WF_{(\text{i})\text{a-Si:H}} = qV_{\text{bi,max}} - \Delta WF_{\text{dipole}}(t) \quad (1)$$

where t is the thickness of MoO_x layer. We assume the $WF_{(\text{i})\text{a-Si:H}}$ as a constant parameter, while $V_{\text{bi,max}}$ is set at 0.87 eV, as the energy difference from valence band to Fermi level in equilibrium conditions

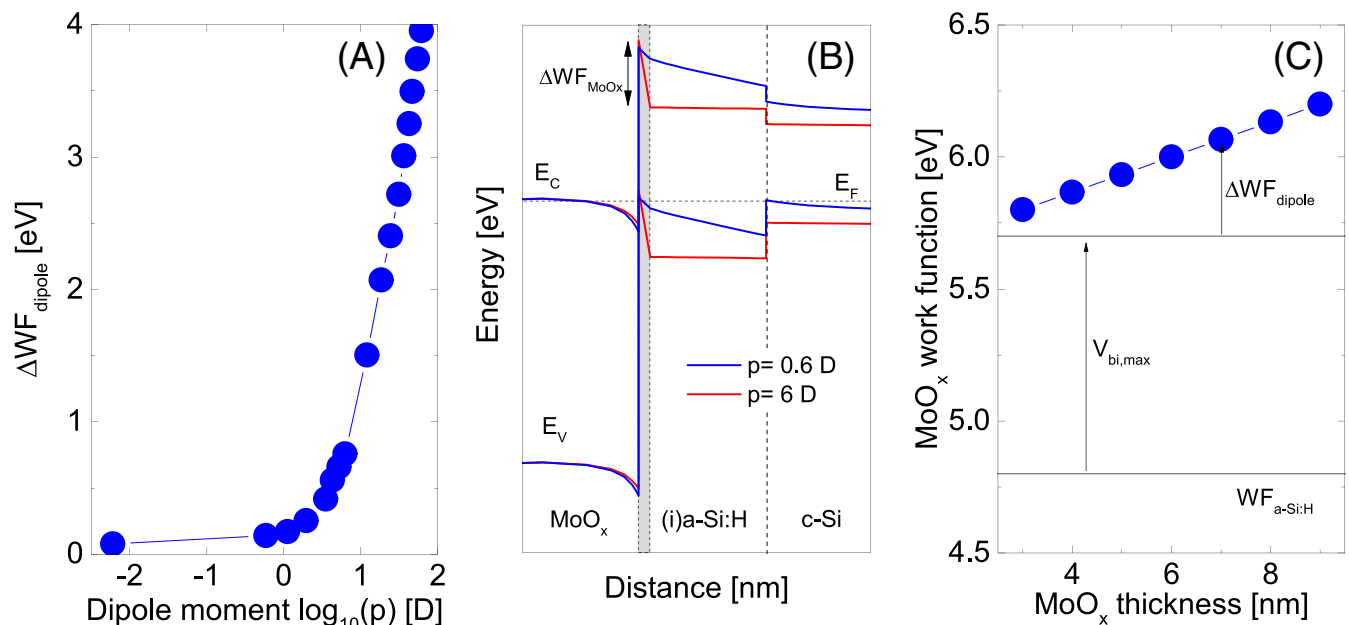


FIGURE 5 (A) Work function attenuation due to dipole as a function of the dipole moment. (B) Simulated band diagram of the hole transport layer contact for two values of dipole moment (in debye, D). The gray area indicates the interfacial dipole. (C) From values extracted from simulations, a graphical determination of $\Delta WF_{\text{dipole}}(t)$ is provided for the chosen $WF_{\text{MoO}_x}(t)$ used in simulations. $V_{\text{bi,max}}$ is equal to 0.87 eV as the energy difference from valence band to Fermi level in equilibrium conditions

allocated on the silicon bulk. Furthermore, WF_{MoO_x} is a function of the MoO_x thickness (see Figure 4A),⁶⁷ and therefore, $\Delta WF_{\text{dipole}}$ is similarly thickness-dependent to respect the equality axiom of Equation 1.

To identify the role and the effect of the $\Delta WF_{\text{dipole}}$ on cell parameters, we introduce in our simulations a virtual layer representing the dipole placed at the (i)a-Si:H/ MoO_x interface. The dipole is assumed with negative charge at the MoO_x side, while the positive charge arises at (i)a-Si:H side. To emulate the effect of the MoO_x thickness in WF_{dipole} , we tune the magnitude of the WF_{dipole} attenuation as described by Equation 1 through the dipole moment (p), as depicted in Figure 5A. We conduct simulations assuming variable interface dipole (p), and in Figure 5B, we report band diagrams for selected dipole moment values. For large dipole moment ($p = 6$ D), the band diagram changes considerably (see Figure 5B) as compared to the case with lower p , with the appearance of a large ΔWF_{MoO_x} at the (i)a-Si:H/ MoO_x interface.

Figure 5C reports a graphical representation of Equation 1 where we observe that $\Delta WF_{\text{dipole}}$ changes according to the WF variation and becomes stronger with the increasing of MoO_x layer thickness. Therefore, the accumulation of holes at the (i)a-Si:H/c-Si interface decreases, hindering the charge transport.

Based on these assumptions, we performed TCAD calculations including a variable dipole at the (i)a-Si:H/ MoO_x interface as shown in the inset of Figure 6A following the approach reported in Würfel et al.⁶⁸ In the calculation of WF_{MoO_x} and $\Delta WF_{\text{dipole}}$, we assumed the scaling trend as reported in Figure 5C.

The simulation results of cell parameters are reported in Figure 6A,B for MoO_x layer thickness varied in a range of interest for device application (3–9 nm). We observe a maximum V_{OC} of 730 mV for 4 nm thick MoO_x layer. Below and above this thickness, the V_{OC} slowly decreases. When the MoO_x is thicker than 5 nm, the V_{OC} drops down to ~ 670 mV. Similarly, the FF in Figure 6B shows a maximum value of 78.4% for a MoO_x layer of 4–5 nm and decreases to 73% for thicker MoO_x layers. By increasing MoO_x thickness, WF_{MoO_x} and ΔWF_{MoO_x} increase.

For carrier separation inside c-Si, the increment of WF_{MoO_x} is favorable, while the rise of ΔWF_{MoO_x} is opposing. Accordingly, for MoO_x thickness values lower than 4 nm, the decrement of FF is explained by the low WF_{MoO_x} . The decrease in FF for thicker MoO_x than 4 nm is ascribed to ΔWF_{MoO_x} . These outcomes are in agreement with the WF dependency assumed in Figure 5C: the thicker the MoO_x layer is, the stronger the dipole contribution of the WF attenuation is with reduced band bending as shown in Figure 5A,B. In conclusion, two competitive mechanisms lead to an optimal MoO_x thickness: WF_{MoO_x} and ΔWF_{MoO_x} . Indeed, the optimal MoO_x of ~ 4 nm results from a trade-off between the WF dependency on the thickness and on the dipole.

4.2 | Effect of interfacial treatment

Here, we discuss the results of solar cell devices with the application of the interfacial PT providing a physical interpretation about the role of PT for the HTL in view of the analysis of interfacial WF attenuation discussed in Section 4.1. Based on the results reported in Figure 2C, we can infer that passivation is similar among experiments as $i\text{-}V_{\text{OC}}$ is almost constant above 730 mV. However, V_{OC} and FF trends in Figure 2C,D reveal that the optimized PT improves the collection of holes (increase in FF) by improving the induced field effect inside the c-Si as V_{OC} trend consistently increases. Such improvement is not triggered by B-doping at the interface as confirmed by XPS analysis (see Figure S1). For PT treatment longer than 130 s, both V_{OC} and FF slightly decrease for reasons that are still under investigation. Further analyses (e.g., XPS) have been started to understand the mechanism of the PT at the (i)a-Si:H/ MoO_x interface. However, the deposition of a thin film is not precluded at this point. Similarly, the solar cell without treatment exhibits lower FF and V_{OC} , revealing that the flow of holes at the (i)a-Si:H/ MoO_x interface is blocked, possibly due to a band misalignment caused by low WF_{MoO_x} . In general, V_{OC} and FF values in Figure 2C,D proved that our PT is a good strategy to improve the contact. Comparing the FF and V_{OC} data presented in

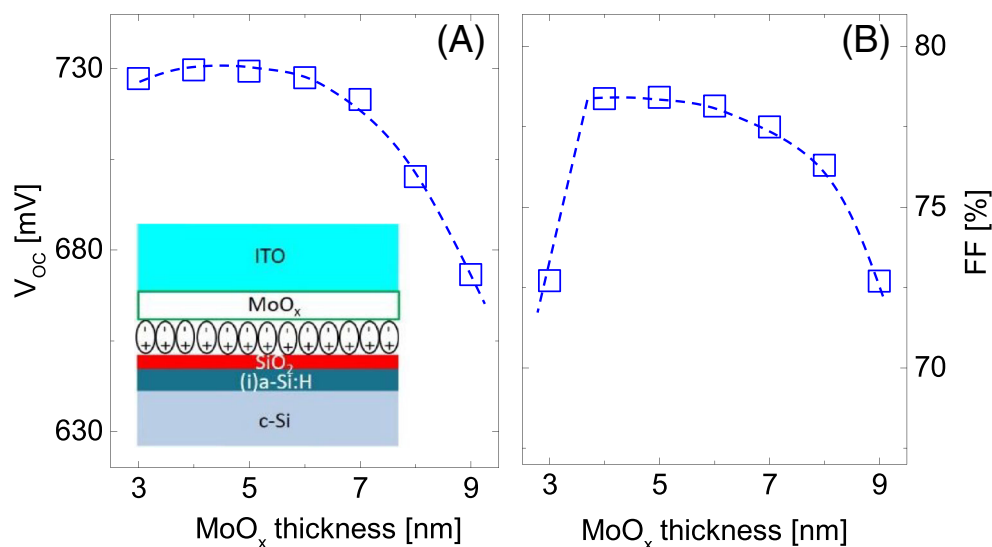


FIGURE 6 Simulated electrical performance of silicon heterojunction solar cells endowed with MoO_x -based hole transport layer (HTL) as function of MoO_x thickness: (A) V_{OC} and (B) FF . The lines are guides to the eye. The sketch in (A) represents the simulated HTL contact stack. ITO, indium tin oxide

Figure 3 to the ones of Figure 2A,B, we observe that the proposed approach leads to the opportunity to thin down the MoO_x layer to 3.5 nm with a simultaneous gain FF and V_{OC} . The use of such thin MoO_x layer is only possible thanks to the PT as discussed in Figure 2C,D. Interestingly, a similar trend and optimal thickness (4 nm) is reported in Dr  on et al.⁴² for the current record efficiency MoO_x -based device by applying the pre-annealing of the (i)a-Si:H.⁵⁴ This observation might suggest that both treatments can be explained by similar mechanisms even though the pre-annealing at the relatively high temperature of 250  C aims at reducing the excess of unbounded H from the passivation layer to avoid reduction of the MoO_x layer.⁵⁴ On the contrary, with our optimized PT, the H content in the (i)a-Si:H layer is not expected to be reduced based on the plasma parameters used (see Section 2).

Furthermore, comparing the experimental results in Figure 3 to the simulations in Figure 6, we observe a similar trend for both V_{OC} and FF as function of the MoO_x thickness with a similar optimum thickness at about 4 nm. Based on those observations, we conjecture that the interfacial PT of the (i)a-Si:H can provide positive fixed charge at the (i)a-Si:H/ MoO_x interface that relaxes the amount of negative charge in n-type MoO_x , thus mitigating the WF attenuation due to dipole once the MoO_x layer is deposited on top of the (i)a-Si:H.

4.3 | Transport mechanisms

To elucidate the nature of transport mechanisms and to deeper understand the role of the PT on the transport mechanisms of the

HTL, we measure the light J - V characteristics of selected cells as function of the temperature.

The device with MoO_x contact, shown in Figure 7A, is characterized by an S-shape profile that straightens out for higher temperatures.⁴⁰ On the contrary, the cell with PT + MoO_x in Figure 7B shows well-shaped J - V characteristics in the whole range of temperatures tested. Both cells show the expected decrease in V_{OC} caused by the increased recombination at higher operative temperature, as reported in Figure 7C with a negative temperature coefficient of 1.6 mV/  C. Looking at Figure 7D, we observe that the device fabricated with MoO_x and without PT shows an improved FF for higher temperature, as also reported by other group.⁴⁰ This FF trend, together with the presence of S-shape J - V curve in Figure 7A, confirms a not efficient transport of holes through HTL contact already at room temperature.

As the temperature increases, holes can more easily recombine with electrons from MoO_x , and therefore, we observe an improved FF up to 74% in Figure 7D.^{11,69} As recombination increases with temperature,^{70,71} the FF improvement reveals that the dominant transport mechanism is recombination via trap-assisted (TAT) process.

On the contrary, for the cell featuring the optimized PT and MoO_x in Figure 7D, we observe that FF only slightly decreases for higher temperature which results in an inverted trend compared to the device with only MoO_x . The J - V curves in Figure 7B and the FF trend clearly indicate that the PT plays a key role in the energy alignment for positive charge collection at the MoO_x /(i)a-Si:H interface leading to a tendency that is commonly observed for many types of c-Si including SHJ ones.^{72,73} Therefore, we can infer that for plasma-treated cell, the energy band alignment among c-Si/(i)a-Si:H/ MoO_x

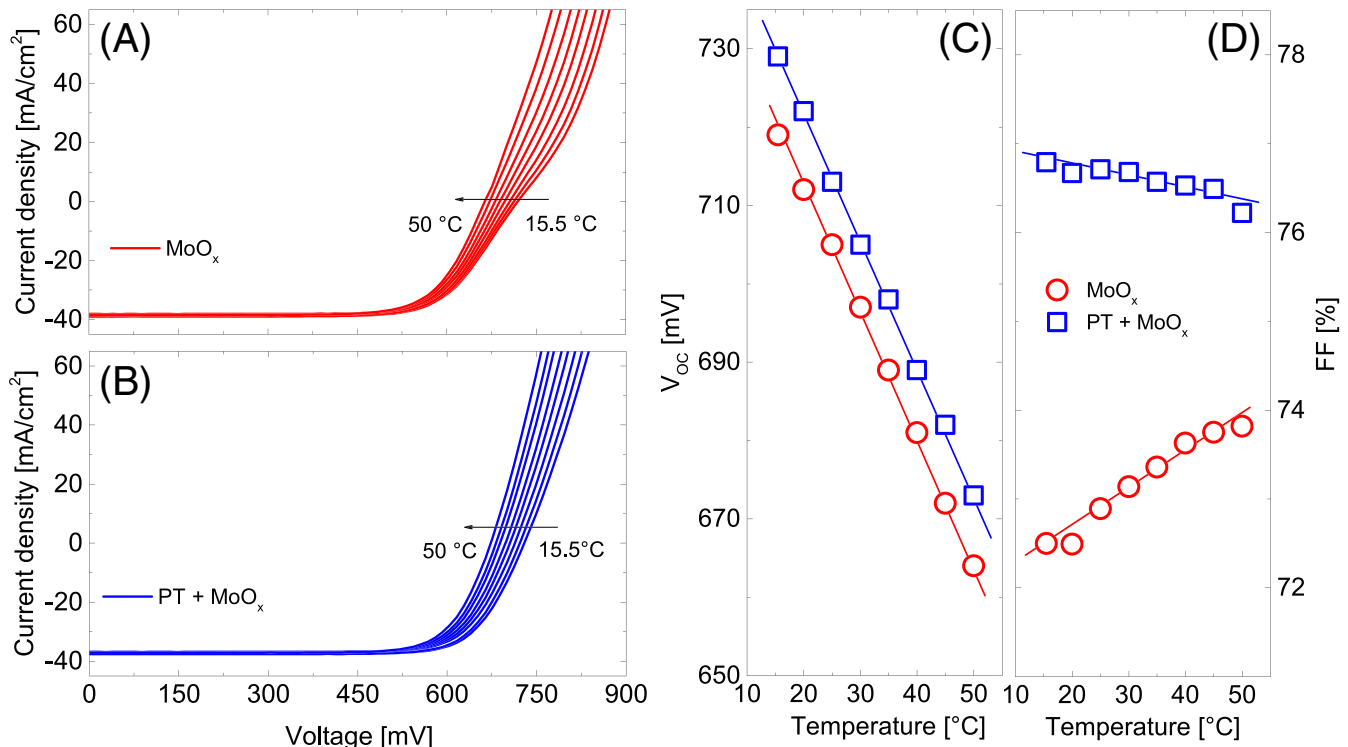


FIGURE 7 Temperature-dependent light J - V characteristics of cells with 5.7-nm MoO_x HTL (A) without and (B) with plasma treatment. (C) V_{OC} and (D) FF evolution as function of temperature extracted from the curves in (A) and (B). PT, plasma treatment

allows transport based on direct energy transitions as band-to-band tunneling (B2B), since the core of such energy alignment is the Fermi level which remains almost constant within the temperature variation range (15.5–50°C).

5 | CONCLUSIONS

We have investigated the critical role of the (i)a-Si:H/MoO_x interface for the hole carrier selectivity of c-Si heterojunction solar cells by means of experiments and electrical simulations. We have experimentally demonstrated that the application of a PECVD PT at the (i)a-Si:H layer surface is a powerful strategy to overcome open-circuit voltage (V_{OC}) and fill factor (FF) limitations observed for MoO_x cells without any treatment. For the optimum PT time, we have measured consistently higher V_{OC} and FF with respect to the not treated cell. Thickness optimization demonstrates that, by applying the PT, we can reduce the thickness of MoO_x to 3.5 nm without apparent electrical losses, therefore enhancing FF and V_{OC} . By means of electrical simulations, we have demonstrated that the experimentally observed electrical degradation could be attributed to the work function attenuation of the MoO_x layer caused by a dipole formation at the interface with the (i)a-Si:H passivation layer. We discuss the interdependency of MoO_x thickness and its WF , identifying an optimal MoO_x layer of about 4 nm for conversion efficiency maximization. Based on those observations, we suggest that the interfacial PT can mitigate the formation of a dipole, thus improving the WF of MoO_x. Finally, temperature-dependent J - V curves confirm that the optimized PT changes the dominant transport mechanisms at the hole transport stack from recombination-based (TAT-dominant) to direct energy transitions (B2B-dominant) resulting in a clear inversion of the FF trends. We deduce that PT mitigates the dipole strength at the (i)a-Si:H/MoO_x compared to the device with only MoO_x with a typical S-shape characteristic. The use of such thin MoO_x layer is only possible thanks to the PT.

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