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RF CMOS Oscillators for Cellular Applications

Shahmohammadi, Mina

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RF CMOS Oscillators for Cellular Applications

Mina Shahmohammadi

RF CMOS Oscillators for Cellular Applications

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. ir. K.C.A.M. Luyben;
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op

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door

Mina SHAHMOHAMMADI

Master of Science in Electrical Engineering,
University of Tehran, Tehran, Iran
geboren te Teheran, Iran

This dissertation has been approved by the
promotor: Prof. dr. R. B. Staszewski

Composition of the doctoral committee:

Rector Magnificus	chairman
Prof. dr. R. B. Staszewski	Delft University of Technology

Independent members:

Prof. dr. ing L. C. N. de Vreede	Delft University of Technology
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Mina Shahmohammadi,
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Keywords: RF, oscillator, 1/f noise up-conversion, impulse sensitivity function, wide tuning range, Colpitts oscillator, coupled oscillators, all-digital phase-locked loop (ADPLL).

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Printed in the Netherlands.

To Maman, Babajan, Mohammad and Kaveh
And to my dearest Masoud

Contents

Contents **i**

1 Introduction **1**

1.1 Thesis Objectives 3

1.2 Thesis Outline 4

2 LC Oscillator Structures **9**

2.1 Introduction 9

2.2 Class-B Oscillator Topology 12

2.3 Class-C Oscillator Topology 15

2.4 Class-D Oscillator Topology 16

2.5 Class-F Oscillator Topologies 18

2.5.1 Class-F_3 Topology 19

2.5.2 Class-F_2 Topology 20

2.6 Conclusion 21

3 A 1/f Noise Up-Conversion Reduction Technique **27**

3.1 Introduction 28

3.2 Method to Reduce 1/f Noise Up-Conversion 31

3.2.1 Auxiliary Resonant Frequencies 31

3.2.2 Harmonic Effects on the Effective ISF 32

3.2.3 Resonant Frequency at $2\omega_0$ 37

3.2.4 ω_{CM} Deviation from $2\omega_0$ 38

3.3 Circuit Implementation 40

3.3.1 Inductor-Based F_2 Tank 44

3.3.2 Class-D/F_2 Oscillator 45

3.3.3 Transformer-Based F_2 Tank . . . 47
3.3.4 Class-$F_{2,3}$ Oscillator . . . 48
3.4 Experimental Results . . . 50
3.4.1 Class-D/F_2 Oscillator . . . 51
3.4.2 Class-$F_{2,3}$ Oscillator . . . 53
3.5 Conclusion . . . 54

4 A Wide-Tuning-Range DTC-Assisted Fractional-N All-digital PLL 61
4.1 Introduction . . . 62
4.2 Structure of the ADPLL . . . 64
4.3 Circuit Implementation . . . 66
4.3.1 Implementation of MASH $\Delta\Sigma$ TDC . . . 66
4.3.2 Implementation of Wide Tuning-Range DCO . . . 67
4.4 ADPLL Measurements Results . . . 73
4.5 Conclusion . . . 75

5 Tuning range extension of an oscillator through CM resonance 79
5.1 Introduction . . . 80
5.2 Common Mode Resonances . . . 82
5.3 Proposed Wide Tuning Range Oscillator . . . 86
5.3.1 Dual-Core Oscillator . . . 86
5.3.2 Phase Noise Analysis . . . 88
5.3.3 Center Tap Inductance . . . 96
5.4 Experimental results . . . 97
5.4.1 Supply and Ground Routing Inductances and Losses . . . 99
5.5 Conclusion . . . 100

6 Conclusion 107
6.1 Thesis Outcome . . . 107
6.2 Suggestion for Future Works . . . 109

List of Publications 111

Summary 113

Samenvatting 115

List of Figures 119

List of Tables **123**

Acknowledgment **125**

About the Author **127**

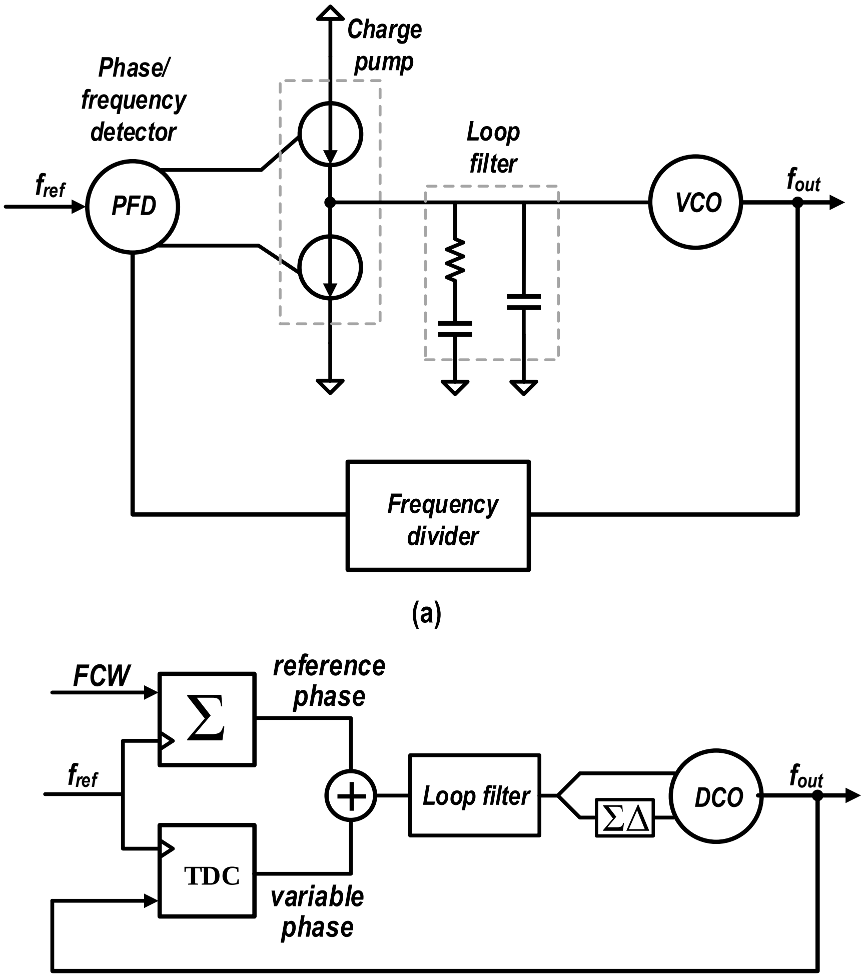
Chapter

1

Introduction

The steadily increasing growth of cellular and wireless communications motivates researchers to keep on improving the system performance, overcome limitations and face new challenges. One of the key building blocks in a wireless radio is an RF oscillator, whose purity limits the radio performance. The oscillator's phase noise in a transmit chain results in power emissions into adjacent channels. In the receive chain, downconversion of a large interferer via the noisy local oscillator (LO) causes reciprocal mixing. Furthermore, in orthogonal frequency-division multiplexing (OFDM) systems, the phase noise leads to inter-carrier interference and a degradation in bit error rate. The trade-off between oscillator's phase noise and its power consumption introduce many challenges for oscillator designers.

Table 1. 1 summarizes the frequency bands and the phase noise requirement specifications for some communication standards. GSM standard's phase noise requirements is the most stringent one. Lots of efforts in the literature is dedicated to improve the RF CMOS oscillator's thermal phase noise upconversion performances to meet such requirements. New classes of oscillation and multi core oscillators are introduced to fulfill this purpose [1]- [5] that we discuss about in Chapter 2. However, the efforts on reducing flicker noise upconversion in the oscillators are not as successful. The current solutions are sacrificing the thermal noise upconversion or sacrificing die area [6]- [8]. However,


Charge
pump
Phase/
frequency
detector
Loop
filter
fref
PFD
VCO
fout
Frequency
divider
FCW
Σ
reference
phase
fref
Loop filter
ΣΔ
DCO
fout
TDC
variable
phase

(a)

(b)

Figure 1.1: (a) Analog and; (b) digital phase locked loops [9].

since to achieve high frequency accuracy oscillators are incorporated in a phase lock loop (PLL) (as is shown in Fig. 1.1 for both analog and digital PLL), they can benefit from high pass nature of filtering of their noise by the loop. This reduction of the oscillator's low frequency noise in the synthesizer is highly dependent on the loop bandwidth. The loop bandwidth of the PLL is usually chosen to minimize the noise contribution of the frequency reference and charge pumps. However, if this bandwidth is less than the 1/f^3 corner of the oscillator then part of the oscillator's low frequency noise remains unfiltered.

Another challenge in the recent RF oscillator designers is to be able to design a wide tuning range oscillator while having low phase noise. The multi-standard applications that are the trend now demands for such oscillators. The trade-off between the quality factor of the switch capacitor bank that is tuning the LC oscillators and the oscillator's tuning range is the obstacle in wide tuning range oscillator design. The MOS transistor switch introduce a resistance that defines the switch capacitor bank quality factor in

Table 1.1: Communication standards requirements [10].

Standard	Frequency band (GHZ)	Required phase noise (dBc/Hz)
Bluetooth	2.402-2.480	-84 @ 1 MHz -114 @ 2 MHz -129 @ 3 MHz
GSM 900/1800	0.880-0.960 1.710-1.880	-122 @ 0.6 MHz -132 @ 1.6 MHz -139 @ 3 MHz
UMTS	1.920-2.170 1.900-2.025	-132 @ 3 MHz -132 @ 10 MHz -144 @ 15 MHz
WiFi	2.412-2.472 5.150-5.350 5.470-5.825	-102 @ 1 MHz -125 @ 25 MHz

on-state, consequently a less resistance and so larger MOS transistor is required for phase noise considerations, However, in the off-state the series combination of the capacitor in the tank and the switch parasitic capacitances defines the equivalent tank capacitance. Consequently a smaller switch is preferred to increase the tuning range. This trade-off makes it impossible to meet both wide tuning range and low phase noise at the same time. For a moderate phase noise the tuning range of the oscillator can hardly go beyond 50% [11]. Some designers tried to switch inductors or transformers instead of the capacitors in order to increase tuning range, however the equivalent tanks Q-factor and consequently phase noise is degraded due to the switches in the signal path. Furthermore, due to the reduced oscillation voltage that is tolerable by the nano metric oxide thickness of advanced technologies CMOS process, low phase noise design is even more challenging.

1.1 Thesis Objectives

The main objective of this dissertation is to address the requirements of RF CMOS oscillators in cellular applications. The first objective of this dissertation is to introduce a method to reduce the relatively high $1/f^3$ PN upconversion of CMOS oscillators. Due to the trade-off between the synthesizer loop bandwidth and the incorporated oscillator's $1/f^3$ noise, the cellular synthesizers with bandwidth of few hundred kHz cannot filter considerable amount of oscillator's low frequency noise. The introduced method reduces oscillator low frequency noise upconversion while not compromising die area or power consumption. The applicability of the method to different oscillator topologies allow the designer to choose the preferred topology and improve the low frequency noise

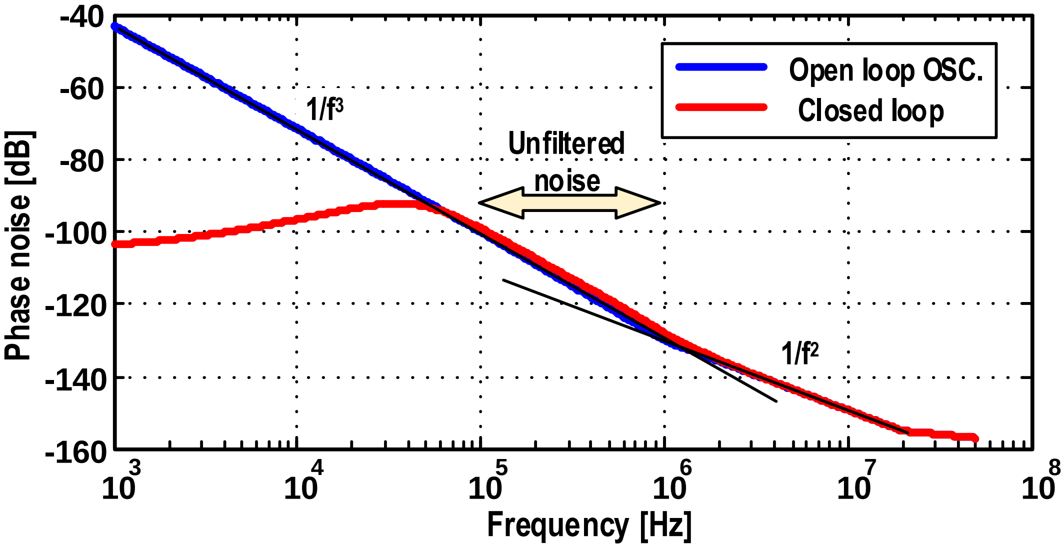


Figure 1.2: Oscillator's open loop and output frequency phase noise.

upconversion.

The second objective is to address the overgrowing interest in multi-standard communication devices by designing wide tuning range oscillators. The tradeoffs between tuning range, phase noise and area of mode switching oscillators are studied and one oscillator that shows promising tuning range-phase noise trade off is chosen to be incorporated in an all-digital PLL (ADPLL). Furthermore, we focused on optimizing die area of wide tuning range oscillators that seem to be missed in the literature. The ability of a transformer based tank to show different differential and common mode resonance frequencies are exploited to introduce a wide tuning range oscillator with a size of a conventional narrow tuning range oscillator for moderate phase noise applications.

1.2 Thesis Outline

In Chapter 2 we briefly introduce and compare different LC oscillator structures. Then the thesis is divided in two parts. The first part in Chapter 3 elaborates a method to reduce a flicker (1/f) noise upconversion in voltage-biased RF oscillators. Excited by a harmonically rich tank current, a typical oscillation voltage waveform is observed to have asymmetric rise and fall times due to even-order current harmonics flowing into the capacitive part, as it presents the lowest impedance path. The asymmetric oscillation waveform results in an effective impulse sensitivity function (ISF) of a non-zero dc value, which facilitates the 1/f noise upconversion into the oscillator's 1/f^3 phase noise. If the ω_0 tank exhibits an auxiliary resonance at $2\omega_0$, then the oscillation waveform would be symmetric and the flicker noise upconversion would be largely suppressed. The second part of the thesis is focused on designing wide tuning range RF oscillators. In Chapter 4 a dual mode transformer based oscillator is designed. A digitally controlled oscillator (DCO) based on this design is incorporated in a digital to time converter (DTC)-assisted fractional-N wide-bandwidth ADPLL. This wide tuning range oscillator suffers from large die area. To tackle this problem specially in the applications that do not demand low phase noise oscillators another method to broaden a tuning range of an LC-tank oscillator without sacrificing its area is presented in Chapter 5. The extra tuning range is achieved by forcing a strongly coupled transformer-based tank into a common-mode resonance at a much higher frequency than in its main differential-mode oscillation. The oscillator employs separate active circuits to excite each mode but it shares the same tank, which largely dominates the core area but is on par with similar single-core designs.

Finally, Chapter 6 concludes this dissertation and presents suggestions for future developments.

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CHAPTER

2

LC Oscillator Structures

2.1 Introduction

An oscillator is a key block used in both transmit and receive paths of a typical integrated transmitter/receiver (a.k.a., transceiver), see Fig. 2.1. Its spectral purity and efficiency highly affect the transceiver's performance. The phase noise of the oscillator results in reciprocal mixing in the receive path, where the blocker is mixed with the oscillator's phase noise and then can appear on top of the desired signal, thus degrading the receiver sensitivity [1]. This problem especially reveals itself in modern mobile phones that support 2G, 3G, 4G wireless standards as well as wireless connectivity (e.g., WiFi) standards with two or more very closely spaced antennas in one small handleld device [2]. It can also affect wideband CMOS receivers without off-chip SAW filters, in which powerful blockers can enter the IC without any prior attenuation [3].

In the transmit path, the oscillator phase noise gets amplified and can desensitize a nearby receiver [1]. Furthermore as one of the most power hungry blocks in the transceiver, its power consumption tends to limit the full system efficiency [2] [4]. Therefore, understanding and modeling the oscillator phase noise have been subjects of numerous studies [5]- [11]. A linear time-variant model through an impulse sensitivity function response of each noise source of the oscillator [9] is the most approached method since

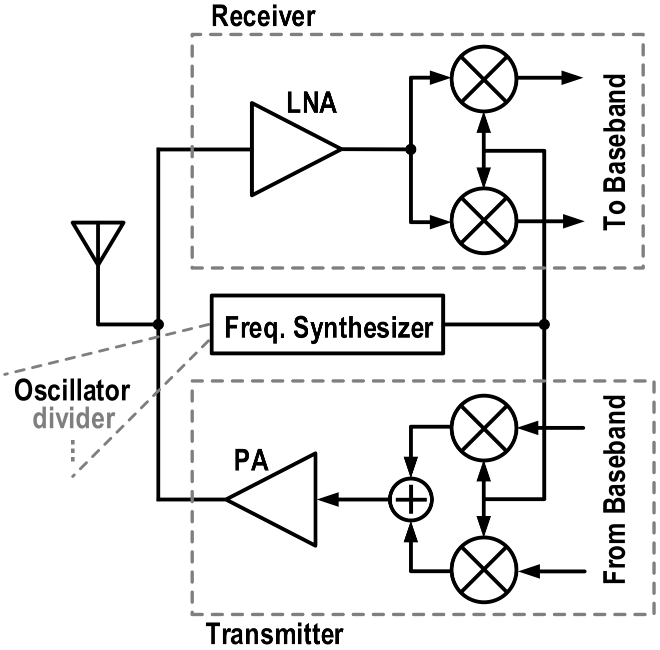


Figure 2.1: A generic RF transceiver [1].

its introduction. To understand this method, it should be noted that a current impulse injected to the tank of Fig. 2.2(a) can change the oscillating phase and/or amplitude depending of the injection time instant (see Fig. 2.2(b)-(c)). If the current impulse be injected when the oscillation waveform is at its maximum, oscillation amplitude will be disturbed but its phase will not. On the other hand, current impulses at zero crossings result in a minimum amplitude but maximum phase disturbance. The impulse response, however, is periodic with respect to the impulse injection time. The impulse sensitivity function (ISF), $\Gamma(\omega_0\tau)$, is a dimensionless, periodic function with period of 2π that describes the oscillation phase shift from injected current impulses during the period [9]. ISF is a periodic function and consequently,

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{i=1}^{\infty} c_n \cos(n\omega_0 t + \theta_n). \tag{2.1}$$

Parasitic phase modulation is then obtained by convolving the current noise source with ISF as

$$\phi_n(t) = \frac{1}{q_{max}} \left[\frac{c_0}{2} \int_{-\infty}^{t} i(\tau) + \sum_{i=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau) \cos(n\omega_0 t + \theta_n) \right], \tag{2.2}$$

where, q_{max} is the maximum charge displacement at the capacitance of the node that the noise is injected.

For a current, such as $i(t) = I_n \cos[(n\omega_0 + \Delta\omega)t]$, the excess phase can be found as,

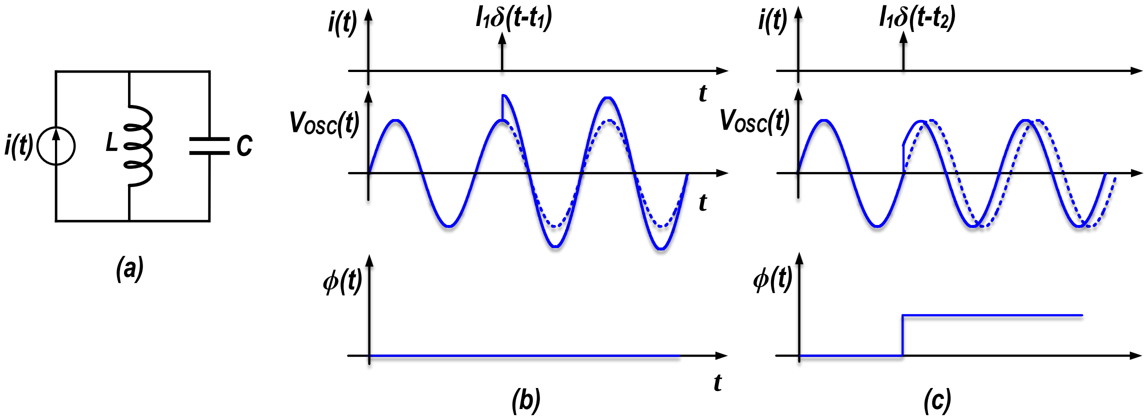


Figure 2.2: Phase response to an impulse current [9].

$$\phi(t) \approx \frac{I_n c_n \sin(\Delta\omega)}{2q_{max}\Delta\omega}. \tag{2.3}$$

The modulated phase shows itself in the phase noise spectrum since we can write

$$x(t) = A\cos(\omega_0 t + \phi_n(t)) \approx A\cos(\omega_0(t)) - A\phi_n(t)\sin(\omega_0 t), \tag{2.4}$$

and, consequently, this injected current results in two sidebands at $\omega_0 \pm \Delta\omega_0$ and $\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{I_n c_n}{4q_{max}\Delta\omega}\right)^2$.

The same method can be generalized for random noise sources and with applying the Parseval's relation to derive the phase noise for a white power spectral density noise as

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{\frac{\overline{i_n^2}}{\Delta f}\frac{1}{2\pi}\int_0^{2\pi}\Gamma^2(\phi)d\phi}{4q_{max}^2\Delta\omega^2}\right) \tag{2.5}$$

The most accurate method to calculate ISF of each noise source is by simulation. An impulse current should be injected to a node in the circuit at a certain time. The time shift of the oscillation should be measured after a few cycles and be converted to the phase shift. By sweeping the injection time of the current impulse over one oscillation period, ISF can be measured.

If the application demands a low phase noise, an LC-tank-based oscillator is to be chosen. The thermal to phase-noise upconversion (20 dB/dec region) of these oscillators can be found as,

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{R_t kT}{2Q_t^2 V_{OSC}^2}\cdot F\cdot\left(\frac{\omega_0}{\Delta\omega}\right)^2\right) = 10\log_{10}\left(\frac{kT}{2\,Q_t^2\,\alpha_I\,\alpha_V\,P_{DC}}\cdot F\cdot\left(\frac{\omega_0}{\Delta\omega}\right)^2\right), \tag{2.6}$$

where, R_t is the equivalent parallel resistance of the tank, k is Boltzmann's constant, T is the absolute temperature, $\alpha_V = \frac{V_{osc}}{V_{DD}}$ and $\alpha_I = \frac{I_{\omega_0}}{I_{DC}}$ are the voltage and current efficiency factors, and F is the noise factor and can be found as,

$$F = \sum_i \frac{R_t}{2kT} \cdot \frac{1}{2\pi} \int_0^{2\pi} \Gamma_i^2 \left(\phi\right) \overline{i_{n,i}^2(\phi)}\, d\phi, \tag{2.7}$$

in which Γ_i is the ISF of the i^{th} noise source.

2.2 Class-B Oscillator Topology

The traditional class-B oscillator, shown in Fig. 2.3(a), has been widely used in RF applications due its simplicity and robustness. The noise factor in a class-B structure is ideally equal to $\gamma + 1$ [11] if M_T tail current transistor would be an ideal current source. In this case, not only the current source does not contribute to phase noise but also provides an infinite impedance at the common source of the g_m transistors which, as we explain later, is beneficial for phase noise reduction. Let us investigate how the performance of this oscillator topology can be improved. The figure of merit (FoM) that is widely used for comparing oscillator performance is as

$$FoM = |PN| + 20\log_{10}(\omega_0/\Delta\omega) - 10\log_{10}(P_{DC}/1mW). \tag{2.8}$$

The objective is to reduce phase noise and/or power consumption of the oscillator.

Increasing the tank's quality factor, reduces the oscillator's phase noise. The tank's quality factor, Q_t depends on the both inductive and capacitive quality factors:

$$\frac{1}{Q_t} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{2.9}$$

The inductor's quality factor, Q_L, which usually limits Q_t, is mostly technology dependent and does not improve with CMOS technology scaling. The capacitive quality factor, Q_C, on the other hand, depends on the tuning range of the oscillator. A switched-capacitor structure, shown in Fig. 2.4, is used nowadays to tune the oscillators. When M_s is on, $C_{on} = \frac{C}{2}$, and the switch on resistance, r_{on} defines $Q_C = \frac{1}{2r_{on}C\omega}$. To improve Q_c, r_{on} should decrease and consequently M_s size should increase. However, larger M_s, adds to the parasitic capacitors and consequently increases the the switch capacitor equivalent capacitance when M_s is off: $C_{off} = \frac{CC_{par}}{2(C + C_{par})}$. Consequently, Q_t will be defined by the technology and oscillator's tuning range and is rarely a design parameter to improve phase noise.

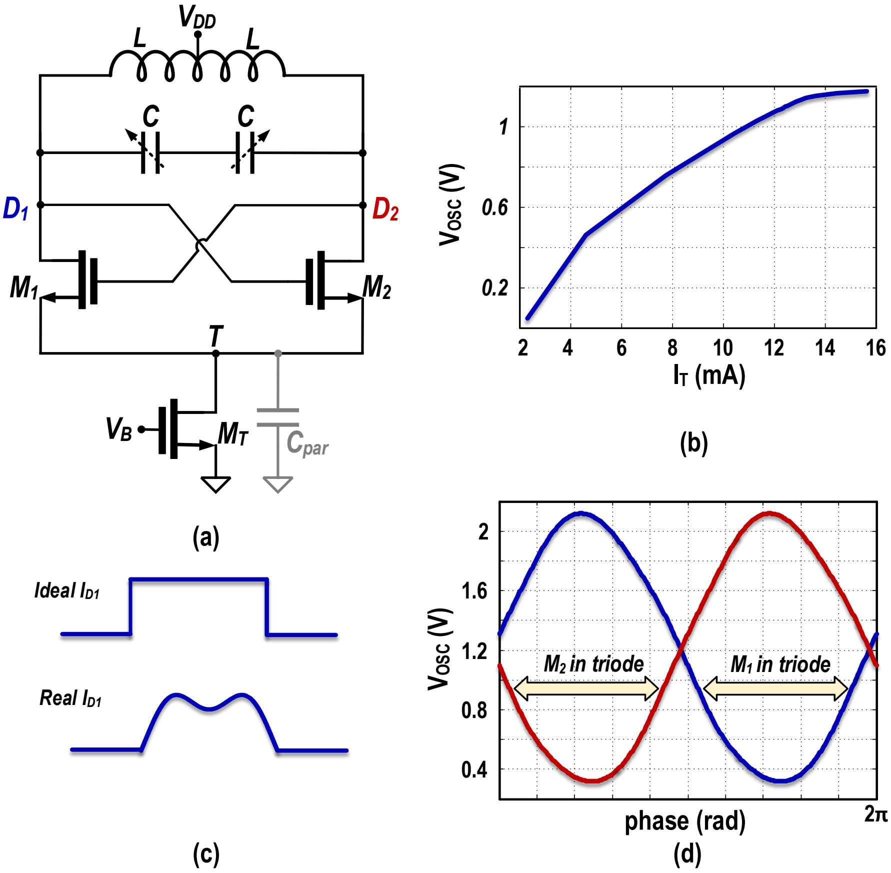


Figure 2.3: A class-B oscillator (a) schematic; (b) oscillation amplitude vs. tail current; (c) ideal and real drain current waveforms; (d) oscillation voltages waveforms.

Another approach to improve the oscillator's phase noise is reducing the tank's inductance while maintaining its quality factor. Doing so reduces $R_t = L\omega Q_t$; however, it increases the power consumption $P_{DC} = \dfrac{V_{OSC}^2}{\alpha_V \alpha_I R_t}$ at the same rate and so it keeps the FoM constant. Furthermore, by reducing the inductor size, the tank interconnection losses become more critical and at some point they limit its quality factor.

The class-B oscillator shows the best performance when its oscillation amplitude is around V_{DD} [13] [12] [25], and consequently $\alpha_V = 1$. After this point, for a typical oscillator with a tail current source M$_T$, the oscillation amplitude increase rate tapers off (see Fig. 2.3(b)) while its power consumption still increases linearly with the tail current, thus reducing FoM. The $M_{1,2}$ transistors' drain current exhibits almost a square waveform when the tail current source is ideal and $\alpha_I = \dfrac{2}{\pi}$ (see Fig. 2.3(c)). However, in a realistic scenario, the non-ideal current source brings up certain issues and limitations. First of all, the M_T transistor will contribute to the phase noise and increase the noise factor beyond $1 + \gamma$. The minimum tail node voltage, V_T, is also limited by the need to keep the M_T transistor in saturation; consequently the maximum oscillation voltage amplitude

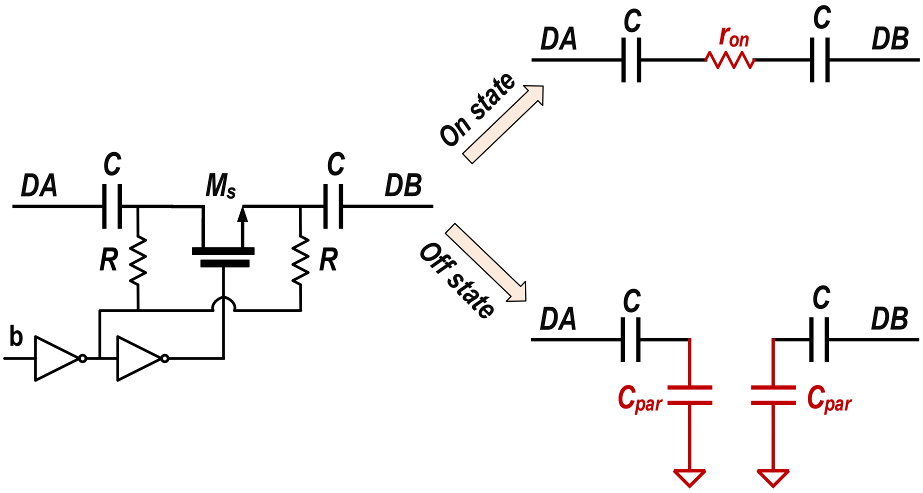


Figure 2.4: The switched-capacitor tuning circuit in on and off states.

reduces to $V_{DD} - V_{sat}$ and $\alpha_V < 1$ ($\alpha_V \approx 0.8$). The capacitance at node T tends to keep this node voltage at a constant level, consequently, for large oscillation amplitudes with $M_{1,2}$ entering the triode region, the ideal square wave of $M_{1,2}$ drain current experiences a dimple, as is shown in Fig. 2.3(c). As a result, α_I drops from the ideal value of $\frac{2}{\pi}$, thus increasing the phase noise. On the other hand, when M_1 or M_2 transistors enter the triode region for a portion of the oscillation period, they will exhibit a low channel impedance. Furthermore, the equivalent parasitic capacitance at node T creates a low impedance path from T to ground. Therefore the tank finds a discharge path to the ground for the time that either one of these transistors are in the triode region; consequently, its quality factor drops, increasing the oscillators phase noise. The M_T transistor size is usually relatively large to reduce its flicker noise; consequently the parasitic capacitor at node T is large enough to provide such a low frequency path. However, it is also helpful in partially filtering the M_T transistor's thermal noise.

Various solutions have been proposed in the literature to improve phase noise of the class-B topology or to improve trade-offs between its phase noise and power consumption. Consequently, new classes of oscillation have been introduced. One of the most effective techniques that could improve the class-B considerably is a noise filtering technique [29]. In this technique, M_T thermal noise is filtered by a relatively large capacitor and a high impedance path is inserted between the core transistors and M_T to prevent the discharge path to the tank. Although this technique is very effective, since the high impedance path is realized by another resonator, it significantly increases the die area. Another interesting technique to improve the oscillator's phase noise is to couple N oscillator cores together [17]. This technique has been used in microwave circuits [18] and is also

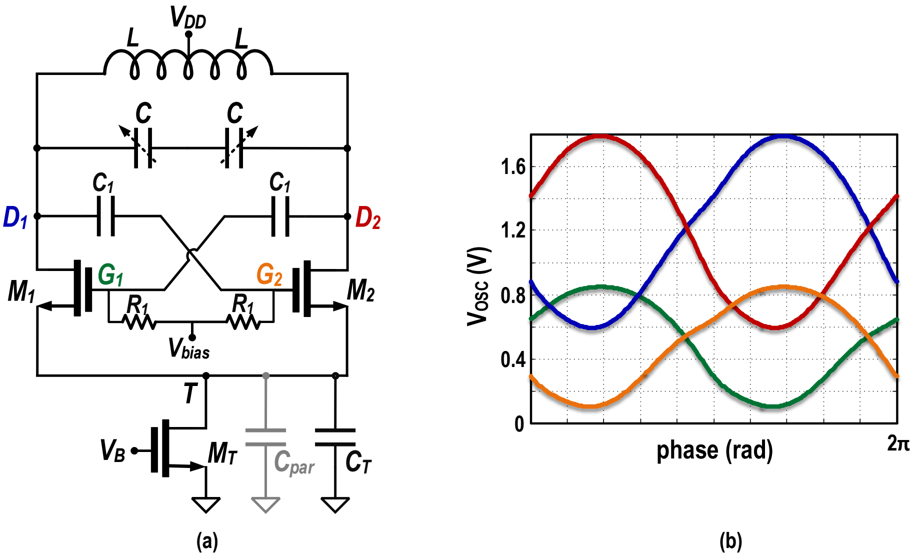


Figure 2.5: (a) A class-C oscillator schematic; and (b) its voltages waveforms.

employed to improve phase noise in RF applications [19]. With coupling N cores, phase noise reduces by a factor of N while power consumption increases by the same factor. Consequently although the phase noise is reduced, the FoM remains the same. However, the die area is increased N times.

In the following sections we briefly review other oscillator topologies that attempt to improve their phase noise / power consumption trade off. In a class-C structure, $M_{1,2}$ are biased in a way as to always remain in saturation during the whole oscillation period. In another strategy, the oscillation waveforms in class-D and class-F structures offer unique ISFs that prevent circuit noise from upconverting to phase noise.

2.3 Class-C Oscillator Topology

The class-C structure [20] is shown in Fig. 2.5(a). In this class of operation the core transistor are kept in saturation, and consequently they show a high impedance during the entire oscillation period. The tank does not find a discharge path to the ground and its quality factor is thus preserved. This structure also saves 36% of the power consumption for the same phase noise by changing the square pulses of $M_{1,2}$ drain current in the class-B operation to narrow and tall pulses with α_I=1. To ensure the saturation region operation, $M_{1,2}$ transistors' gates are decoupled from oscillation voltage and are biased to a value well below the V_{DD} voltage. A large capacitor in parallel with the M_T current source allows the class-C like tall and narrow current pulses for $M_{1,2}$ transistors.

However, the maximum oscillation amplitude is limited in this topology. If the

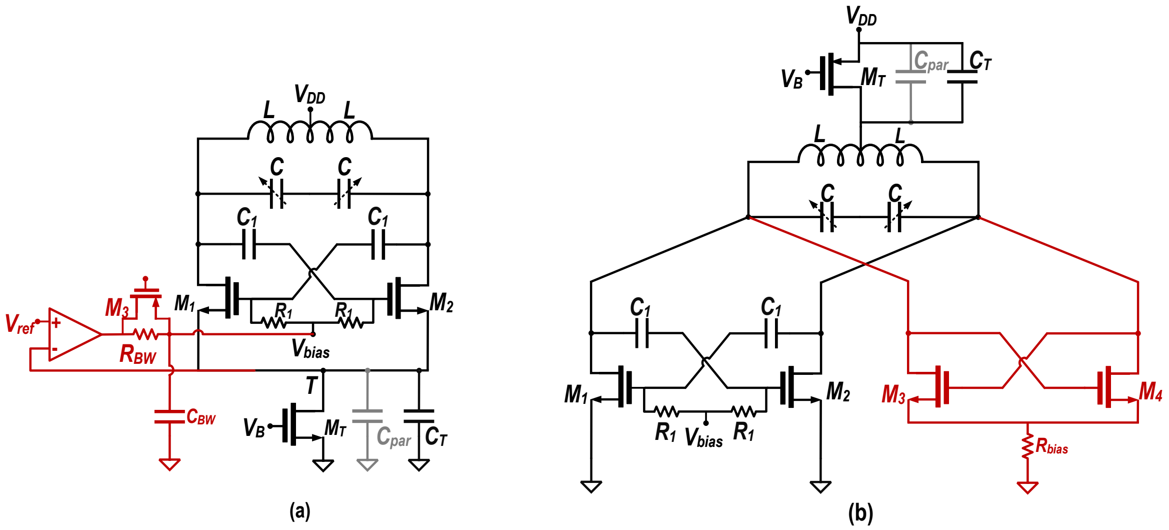
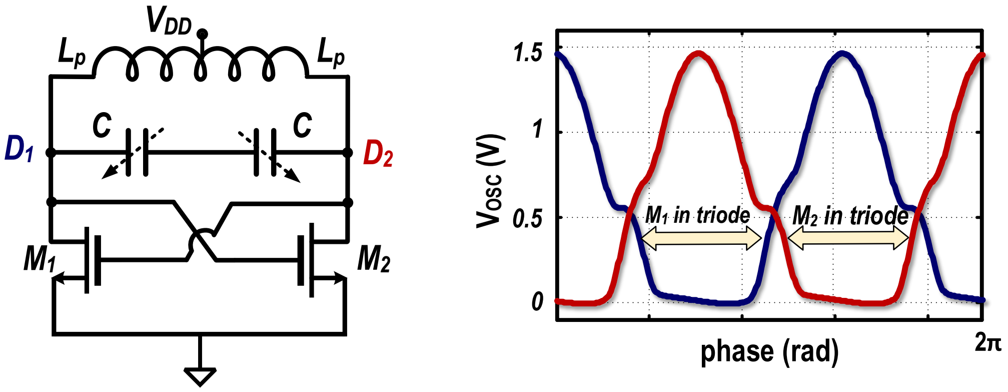


Figure 2.6: (a) A class-C with dynamic generation of V_{bias} [22]; (b) a hybrid class-B/class-C oscillator [26].

oscillation amplitude gets large enough to push $M_{1,2}$ into the triode region, not only the tank's quality factor would heavily drop due to the large C_T, but also $M_{1,2}$ drain current will no longer feature tall and narrow pulses, thus α_I would dramatically drop. Consequently, although the phase noise and power efficiency are improved for low oscillation amplitudes as compared to the class-B oscillator structure with the same amplitude, the minimum achievable phase noise here is limited. An attempt to increase the class-C swing is done by removing the current source transistor M_T and generating V_{bias} by an adaptable current mirror circuit [21]. This oscillator topology also suffers from a trade-off between its robust start-up and the maximum oscillation voltage in steady-state [22]. V_{bias} should be relatively large to facilitate the start-up, but large V_{bias} values limit the steady state oscillation amplitude. It is proposed to adjust V_{bias} dynamically in a negative feedback loop [22]– [24], which consumes extra power (see Fig. 2.6(a)), or employ class-B switching transistors in parallel with the class-C ones to ensure start-up for low V_{bias} values [25] [26]. This reduces α_I and consequently power efficiency (see Fig. 2.6(b)). The power efficiency of this structure has motivated designers in [27] to incorporate this oscillator topology in a Bluetooth Low Energy (BLE) transmitter.

2.4 Class-D Oscillator Topology

The schematic of a class-D oscillator topology is shown in Fig. 2.7(a). The tail transistor is removed, thus eliminating the overhead voltage necessary for its proper operation. Furthermore, the $M_{1,2}$ transistor sizes are chosen large enough to become



(a) (b)

Figure 2.7: (a) A class-D oscillator schematic; and (b) its voltages waveforms.

almost ideal switches. The relative oscillation voltage amplitude is maximized in this structure and reaches $\sim 3V_{DD}$. Doing so pushes $M_{1,2}$ transistors deep into the triode region (even more than in the class-B structure) and, consequently, they generate considerable amount of noise. However, as demonstrated in Fig. 2.7(b), the oscillation voltages, V_1 (at node D_1) and V_2 (at node D_2), are forced to ground for almost half the period. V_1 (V_2) is mostly grounded when M_1 (M_2) is in the triode region, and consequently the ISF of node D_1 (D_2) is almost zero for most of this period, preventing the M_1 (M_2) noise to be upconverted to phase noise.

The idea of voltage-switching oscillators was first proposed in 1959 [28], but discrete BJT implementations have turned out not to be suitable for RF applications. However, recent CMOS technologies make excellent switches with reasonable sizes and, consequently, this structure has been attracting some interest [29]- [31]. A high oscillation amplitude in this structure makes it suitable for low-voltage low phase-noise applications [31] [32]. The product of drain current and drain voltage of MOS switches is almost zero across the oscillation period, consequently the power efficiency of this structure could be beyond 90% [30]. This oscillator structure not only *can* but it also *must* work at low voltage supplies, otherwise the $M_{1,2}$ transistors, which should be thin-oxide devices to guarantee nearly ideal switching, will face breakdown. Another limitation of the class-D structure is its relatively severe low-frequency noise upconversion and supply frequency pushing. It has been attempted to minimize this problem by an on chip LDO in [33], which is rather power consuming. We elaborate on this problem in detail in Chapter 3 and propose a solution.

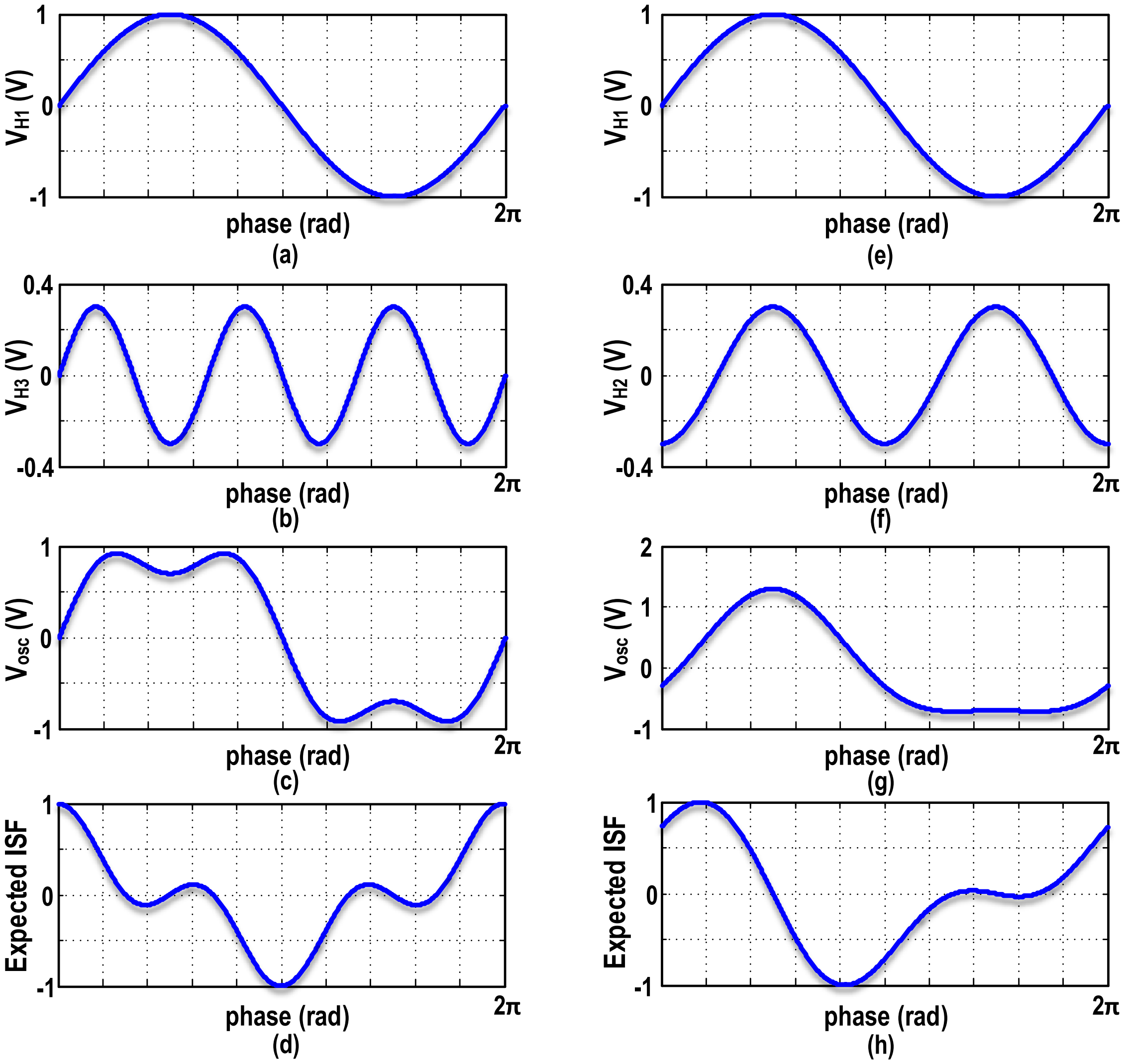


Figure 2.8: (a) Fundamental, V_{H1}; (b) 3rd harmonic, V_{H3}, voltage components; (c) oscillation waveform; and (d) expected ISF. (e) Fundamental, V_{H1}; (f) 2nd harmonic, V_{H2}, voltage components; (g) oscillation waveform; and (h) expected ISF.

2.5 Class-F Oscillator Topologies

If ISF of a certain oscillation waveform is negligible for some interval of an oscillation period, the circuit noise cannot be upconverted to phase noise during that time. This is beneficial in reducing the oscillator's phase noise. Class-F oscillators realize such oscillation waveforms by giving rise to either *third* or *second* harmonic of oscillation voltage, as we discuss in following sections.

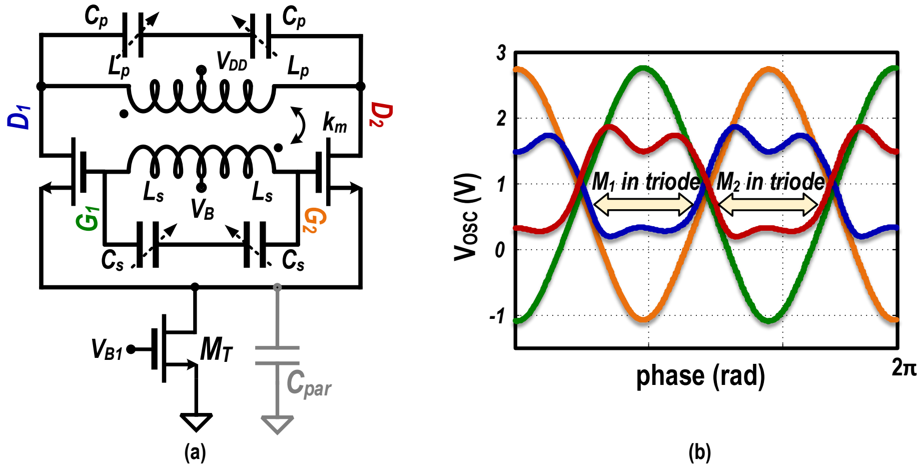
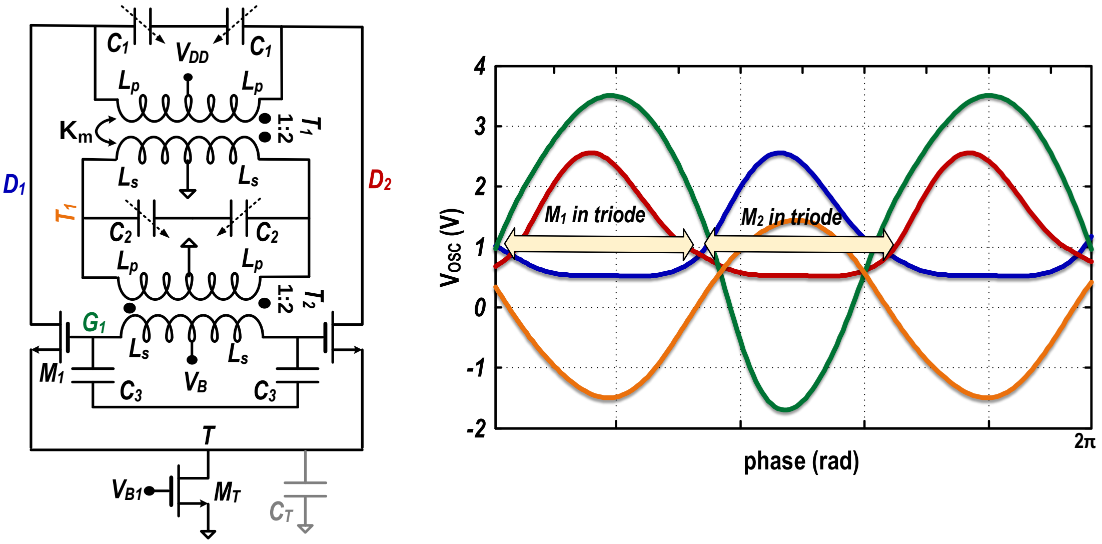


Figure 2.9: (a) A transformer based tank class-F oscillator schematic; and (b) its voltages waveforms.

2.5.1 Class-F$_3$ Topology

In this oscillator topology, a pseudo-square voltage oscillation waveform is realized by increasing the *third* harmonic component of the oscillation voltage and so the voltage ratio of the third harmonic to the fundamental is $\frac{V_{H3}}{V_{H1}} \approx 0.3$ (see Fig.2.8(a)-(c)). This waveform has an ISF as shown in Fig.2.8(d), which prevents the circuit thermal-noise to phase-noise upconversion. Since the drain current in an oscillator is rich in harmonics, the voltage third harmonic could arise if we could realize another resonant peak at $3\omega_0$ as an extra resonance to prevent filtering of the tank *current's* third harmonic component. An extra tank could be utilized for the $3\omega_0$ resonance [34] [35]. However, although the phase noise performance of the oscillator improves, the extra tank is not area efficient. It is proposed in [6] to realize a tank with a transformer instead of an inductor. A transformer-based tank input impedance shows two resonant frequencies. The tank can be designed with the second resonant frequency to be at three times the fundamental resonance and consequently realize the pseudo-square oscillation waveform. This oscillator structure and waveforms are shown in Fig. 2.9(a). The $M_{1,2}$ transistors in this structure spend more time in the triode region as compared to the class-B with sinusoidal oscillation waveform. Although the tank can find a discharge path to ground during this time span (see Fig. 2.9(b)), the very small ISF value there result in a reduced noise contribution of $M_{1,2}$ to the total phase noise. Voltage efficiency α_v of class-F$_3$ is about 0.8, which is similar to that in class-B, but the $M_{1,2}$ drain currents are almost square-wave and current efficiency α_I is very close to $\frac{2}{\pi}$. One drawback of this structure is that transformers have lower quality factor in the same technology as compared to an inductor with the same size. The promising phase noise performance of this structure has motivated the designers



(a) (b)

Figure 2.10: (a) A transformer based tank class-F oscillator schematic; and (b) its voltages waveforms [38].

to incorporate this oscillator in a synthesizer for 4G phones [37].

2.5.2 Class-F_2 Topology

The time span that the core transistors are in the triode region is contributing most to the 20 dB/dec phase noise. Consequently, if the ISF were to be negligible in this time span, the phase noise would reduce (see Fig. 2.8(h)). The oscillation voltage of Fig. 2.8(g) offers such a waveform. As demonstrated in this figure, increasing the *second* harmonic component of the oscillation voltage with a $\frac{V_{H2}}{V_{H1}} \approx 0.3$ constraint results in such a waveform (see Fig. 2.8(e)-(g)). As in the class-F_3 structure, an extra resonant peak, now at $2\omega_0$, prevents the current's second harmonic from being filtered and thus gives rise to a voltage harmonic component at $2\omega_0$. This waveform was realized in [38] with the help of two transformer-based tanks, as demonstrated in Fig. 2.10. α_I is almost $\frac{2}{\pi}$ in this structure and the tail transistor has more overhead with $\alpha_V \approx 0.9$. Furthermore, the tradeoff of power consumption and phase noise is improved by applying two 1:2-turn transformers, thus scaling down the equivalent resistance of the tank and oscillator's PN by a factor of 5. The drawback is, of course, the large area required to acommodate the two transformers.

2.6 Conclusion

In this chapter, we briefly introduce various oscillator structures and mention their benefits and drawbacks. We overview nonidealities that the traditional class-B oscillator faces and review how each structure tries to overcome them. The class-C oscillator improves phase noise at a given power consumption but only when its oscillation amplitude is low enough to keep the core transistors in saturation. The class-D oscillator reaches low phase noise in the thermal noise region without requiring large supply voltages but it is limited in operation to low supply voltages due to reliability concerns. The class-F oscillators raise voltage harmonics to create waveforms with special ISFs that prevent circuit thermal noise to phase noise upconversion. However, they are more complex to design and need simultaneous tuning of two capacitor banks.

All these oscillator structures attempt to improve the thermal or 20 dB/dec phase noise. In the next chapter we introduce a method to reduce the low-frequency noise upconversion in LC oscillator structures.

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CHAPTER

3

A 1/f Noise Up-Conversion Reduction Technique

In this chapter, we introduce a method to reduce a flicker (1/f) noise upconversion in voltage-biased RF oscillators[1]. Excited by a harmonically rich tank current, a typical oscillation voltage waveform is observed to have asymmetric rise and fall times due to even-order current harmonics flowing into the capacitive part, as it presents the lowest impedance path. The asymmetric oscillation waveform results in an effective impulse sensitivity function (ISF) of a non-zero dc value, which facilitates the 1/f noise upconversion into the oscillator's $1/\mathrm{f}^3$ phase noise. We demonstrate that if the ω_0 tank exhibits an auxiliary resonance at $2\omega_0$, thereby forcing this current harmonic to flow into the equivalent resistance of the $2\omega_0$ resonance, then the oscillation waveform would be symmetric and the flicker noise upconversion would be largely suppressed. The auxiliary resonance is realized at no extra silicon area in both inductor- and transformer-based tanks by exploiting different behavior of inductors and transformers in differential- and common-mode excitations. These tanks are ultimately employed in designing modified class-D and class-F oscillators in 40-nm CMOS technology. They exhibit an average flicker noise corner of less than 100 kHz.

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[1] Material of this chapter was published in IEEE Journal of Solid-State Circuits [1]

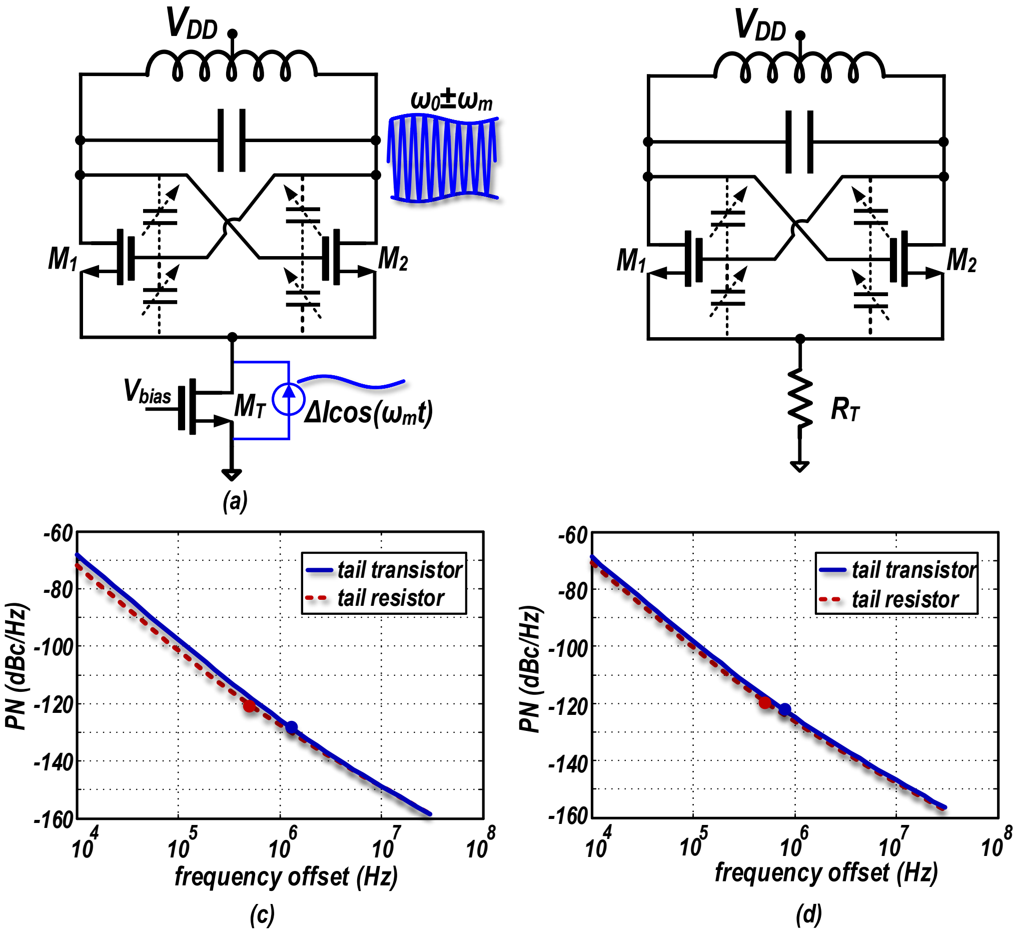
VDD
ω0±ωm
M1
M2
Vbias
MT
ΔIcos(ωmt)
(a)
VDD
M1
M2
RT
-60
-80
-100
-120
-140
-160
PN (dBc/Hz)
tail transistor
tail resistor
10^4
10^5
10^6
10^7
10^8
frequency offset (Hz)
(c)
(d)

Figure 3.1: Class-B oscillator: (a) with tail transistor M_T; (b) with tail resistor R_T; and their PN when (c) M_T is always in saturation; (d) M_T enters partially into triode.

3.1 Introduction

Close-in spectra of RF oscillators are degraded by a flicker (1/f) noise upconversion. The resulting low-frequency phase noise (PN) fluctuations can be mitigated as long as they fall within a loop bandwidth of an enclosing phase-locked loop (PLL). However, the PLL loop bandwidths in cellular transceivers are less than a few tenths to a few hundreds of kHz [2] [3], which is below the typical $1/f^3$ PN corner of CMOS oscillators [4]- [6]. Consequently, a considerable amount of the oscillator's low frequency noise cannot be filtered by the loop and will adversely affect the transceiver operation. In a current-biased oscillator, flicker noise of a tail transistor, M_T, modulates the oscillation voltage amplitude and then upconverts to PN via an AM-PM conversion mechanism through nonlinear parasitic capacitances of active devices, varactors and switchable capacitors [7] [8] (see

Fig. 3.1(a).)[1] An intuitive solution is to configure the oscillator into a *voltage-biased* regime, which involves removing the $\mathrm{M_T}$ [9], or replacing it with a tail resistor, $\mathrm{R_T}$, in Fig. 3.1(b). Such expected reduction is highly dependent on the tail transistor's operating region. If $\mathrm{M_T}$ in Fig. 3.1(a) is always in saturation, the amount of 1/f noise is considerable and the tail resistor $\mathrm{R_T}$ in Fig. 3.1(b) could improve the low-frequency PN performance, as shown in Fig. 3.1(c), However, in advanced CMOS process nodes with a reduced supply voltage, $\mathrm{M_T}$ partially enters the triode region, thereby degrading the oscillator's effective noise factor but improving the 1/f noise upconversion, see Fig. 3.1(d). In [4], class-C oscillators were designed with a tail transistor and a tail resistor. Measured $1/\mathrm{f}^3$ corners are almost the same, thus supporting our discussion. However, regardless of the $\mathrm{M_T}$ operating region, removing this source would still not completely eliminate the 1/f noise upconversion.

Another mechanism of the 1/f upconversion is due to Groszkowski effect [10]. In a harmonically rich tank current, the fundamental component, I_{H1}, flows into the equivalent parallel resistance of the tank, R_p. Other components, however, mainly take the capacitive path due to their lower impedance, see Fig. 3.2(a). Compared to the case with only the fundamental component, the capacitive reactive energy increases by the higher harmonics flowing into them. This phenomenon makes the tank's reactive energy un-balanced. The oscillation frequency will shift down from the tank's natural resonance frequency, ω_0, in order to increase the inductive reactive energy, and restore the energy equilibrium of the tank. This frequency shift is given by [11]

$$\frac{\Delta\omega}{\omega_0} = -\frac{1}{Q^2}\sum_{n=2}^{\infty}\frac{n^2}{n^2-1}\cdot\left|\frac{I_{Hn}}{I_{H1}}\right|^2 \tag{3.1}$$

where, I_{Hn} is the n^{th} harmonic component of the tank's current. The literature suggests that this shift is static but any fluctuation in I_{Hn}/I_{H1} due to the 1/f noise modulates $\Delta\omega$ and exhibits itself as $1/\mathrm{f}^3$ PN [12], see Fig. 3.2(c). Although this mechanism has been known for quite some time, it is still not well understood how the flicker noise modifies the I_{Hn}/I_{H1} ratio. Furthermore, (3.1) suggests all harmonics *indiscriminately* modulate the Groszkowski's frequency shift by roughly the same amount, without regard to their odd/even-mode nature, which could be easily misinterpreted during the study of the flicker noise upconversion in cross-coupled oscillators.

While recognizing the Groszkowski's frequency shift as the dominant physical mechanism in voltage-biased oscillators, we turn our attention to the impulse sensitivity function

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[1] It is shown in [7] that for certain values of varactor bias voltages this upconversion is almost eliminated.

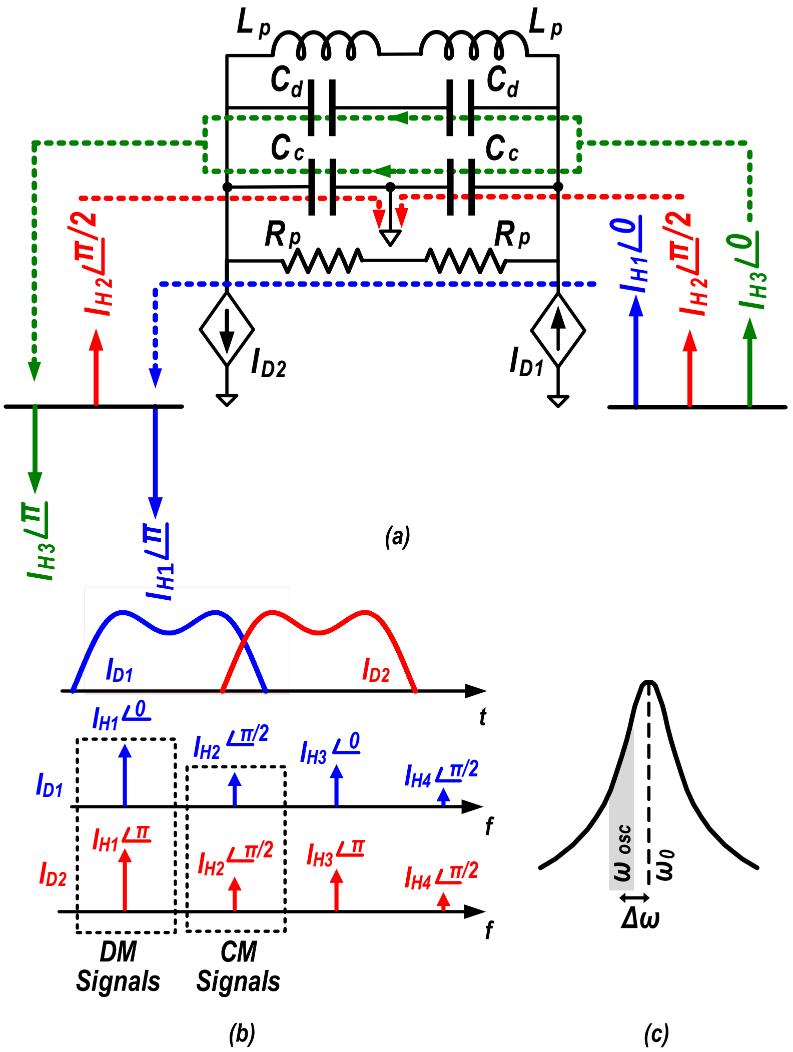

L p
L p
C d
C d
C c
C c
R p
R p
I D2
I D1
I H1∠0
I H2∠π/2
I H3∠0
I H2∠π/2
I H3∠π
I H1∠π
(a)
I D1
I D2
t
I H1∠0
I H2∠π/2
I H3∠0
I H4∠π/2
I D1
f
I H1∠π
I H2∠π/2
I H3∠π
I H4∠π/2
I D2
f
DM Signals
CM Signals
(b)
ω osc
ω0
Δω
(c)

Figure 3.2: (a) Current harmonics paths; (b) drain current in time and frequency domains; (c) frequency drift due to Groszkowski effect.

(ISF) theory in researching the above questions. Hajimiri and Lee [13] have shown that upconversion of any flicker noise source depends on the dc value of the related effective ISF, which can be significantly reduced if the waveform has certain symmetry properties [13] [14]. Another explanation was offered in [27] [16] suggesting that if the 1/f noise current of a switching MOS transistor is to be modeled by a product of stationary noise and a periodic function *w(t)* then this noise can upconvert to PN if *w(t)* is asymmetric.

In this chapter, we elaborate on a method proposed in [22] to effectively trap the second current harmonic into a resistive path of a tank in a *voltage-biased* oscillator topology. Doing so will reduce the core transistors' low frequency noise upconversion by making the oscillation waveform symmetric and reducing the effective ISF dc value. We further investigate the effects of harmonics on the core transistors' flicker noise upconversion by studying their impact on the oscillation waveform and on the effective impulse sensitivity function, $\Gamma_{eff,dc}$.

It should be mentioned that several solutions are proposed in literature to reduce the 1/f noise upconversion due to Groszkowski's frequency shift. The concept of a harmonically rich tank current degrading the close-in oscillator spectrum has been noticed for quite some time; however, the proposed solutions mostly include linearization of the system to reduce the level of current harmonics by limiting the oscillation amplitude by an AGC [17] [18], or linearization of gm-devices [19] [20], at the expense of the oscillator's start-up margin and increased $1/f^2$ PN. In a completely different strategy, a resistor is added in [21] in series with gm-device drains. An optimum value of the resistor minimizes the flicker noise upconversion; however, the 1/f noise improvement is at the expense of the 20 dB/dec degradation in oscillators with low V_{DD} and high current consumption.

The chapter is organized as follows: Section 3.2 shows how harmonic components of the drain current contribute to the flicker noise upconversion and shows how an auxiliary CM resonance at $2\omega_0$ mitigates this upconversion. Section 3.3 demonstrates how the auxiliary resonance is realized and proves the effectiveness of the proposed method by implementing two classes of voltage-biased oscillators. Section 3.4 reveals the details of circuit implementations and measurement results.

3.2 Method to Reduce 1/f Noise Up-Conversion

3.2.1 Auxiliary Resonant Frequencies

Let us start by focusing on reducing the Groszkowski frequency shift. As shown in Fig. 3.2(a), the oscillation frequency ω_{osc} fluctuates around the tank's natural resonant frequency ω_0 due to the flow of higher harmonics of the current $I_{D1,2}$ into the capacitive part of the tank. A voltage-biased class-B tank current in time and frequency domains is shown in Fig. 3.2(b). Odd harmonics of the tank current are differential mode (DM) signals, hence, they can flow into both differential- and single-ended capacitors. Even harmonics of the tank current, on the other hand, are common mode (CM) signals, and can only flow into single-ended (SE) capacitors. If the tank possesses further resonances coinciding with these higher harmonics (see Fig. 3.3(a)), these components can find their respective resistive path to flow into, as shown in Fig. 3.3(b). Consequently, the capacitive reactive energy would not be disturbed and the oscillation frequency shift $\Delta\omega$ would be minimized (see Fig. 3.3(c)). The input impedance Z_{in} of such a tank is shown in Fig. 3.3(d). The tank has the fundamental natural resonant frequency at ω_0 and auxiliary CM and DM resonant frequencies at even and odd-order harmonics, respectively.

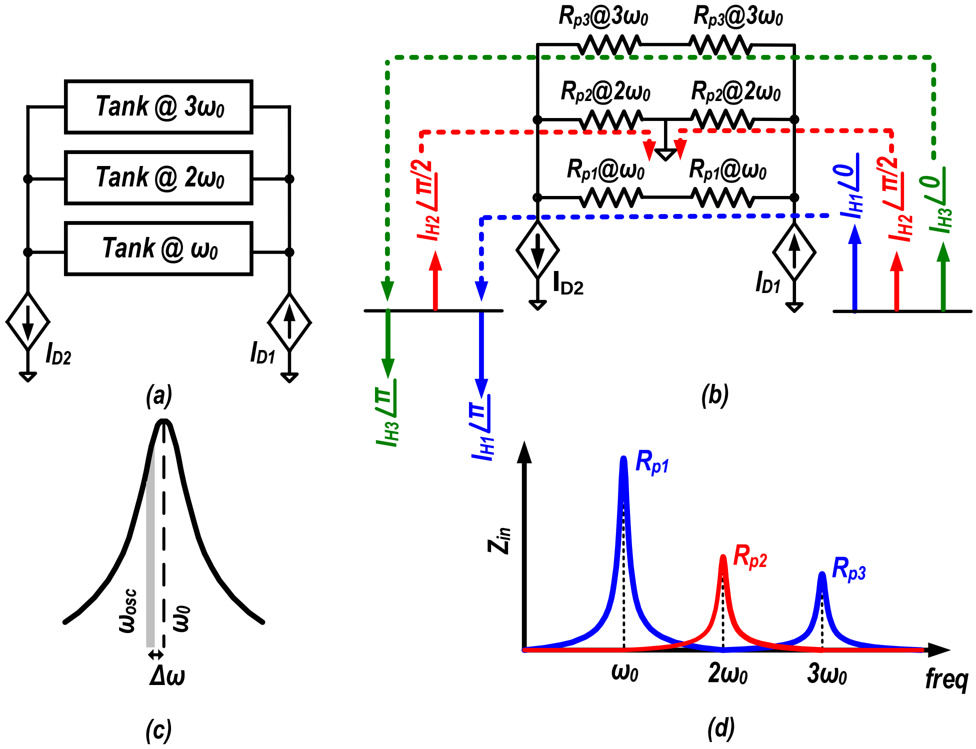


Figure 3.3: (a) Auxiliary resonances at higher harmonics; (b) current harmonic paths; (c) frequency drift; (d) input impedance of the tank.

Minimizing the frequency shift $\Delta\omega$ will weaken the underlying mechanism of the 1/f noise upconversion; however realizing auxiliary resonances at higher harmonics has typically been area inefficient and can also degrade the PN performance. Consequently, the auxiliary resonance frequencies have to be chosen wisely. Groszkowski frequency shift formula (3.1) indicates that all the contributing current harmonics I_{Hn} are weighted by almost the same coefficients. This means that, in practice, stronger current harmonics I_{Hn} contribute more to the frequency shift. Consequently, we can narrow down the required auxiliary resonances to these harmonics. On the other hand, ultimately, the low frequency noise upconversion depends on the oscillation waveform and the dc value of effective ISF. The various current harmonics contribute unevenly to the flicker noise upconversion since they result in different oscillation waveforms and effective ISF values. Investigating these differences reveals how many and at which frequencies the auxiliary resonances should be realized.

3.2.2 Harmonic Effects on the Effective ISF

A (hypothetical) sinusoidal resonance tank current $I_{H1}(t) = |I_{H1}|\sin(\omega_0 t)$ would result in a sinusoidal resonance oscillation voltage: $V_{H1}(t) = R_{p1} \cdot |I_{H1}|\sin(\omega_0 t) = A_1 \sin(\omega_0 t)$.

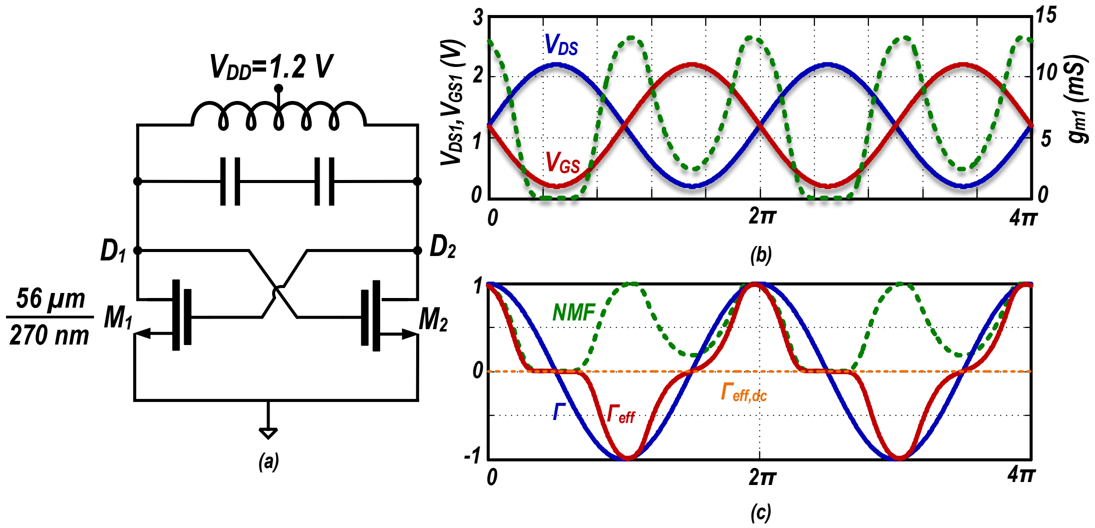


Figure 3.4: Oscillator example: (a) schematic; (b) V_{DS}, V_{GS}, and g_m of M_1 transistor when oscillation voltage contains only fundamental component; (c) its ISF, NMF, and effective ISF.

Its ISF is also a zero-mean sinusoid but in quadrature with $V_{H1}(t)$ [23]. The flicker noise of core transistors (e.g., $M_{1,2}$ in Fig. 3.4(a)) in a cross-coupled oscillator, is modeled by a current source between the source and drain terminals, and exhibits a power spectral density as

$$\overline{i_n^2(t)} = \frac{K}{WLC_{ox}} \cdot \frac{1}{f} \cdot g_m^2(\omega_0 t) \tag{3.2}$$

where, K is a process-dependent constant, W and L are core transistors' width and length, respectively, and C_{ox} is an oxide capacitance per area. Due to the dependency of current noise on g_m, the flicker noise source is a cyclostationary process and can be expressed as

$$i_n(t) = i_{n0}(\omega_0 t) \cdot \alpha(\omega_0 t), \tag{3.3}$$

in which $i_{n,0}(\omega_0 t)$ shows the stochastic stationarity. $\alpha(\omega_0 t)$ is the noise modulating function (NMF), which is normalized, deterministic and periodic with maximum of 1. It describes the noise amplitude modulation; consequently it should be derived from the cyclostationary noise characteristics [13]. In this case, an *effective* impulse sensitivity function is defined as $\Gamma_{eff}(\omega_0 t) = \alpha(\omega_0 t) \cdot \Gamma(\omega_0 t)$. $M_{1,2}$ flicker noise cannot up-convert to PN if effective ISF has a zero dc value.

Let us investigate the $M_{1,2}$ flicker noise upconversion when the oscillation voltage ideally contains only the fundamental component. In Fig. 3.4(a), $V_{D1} = V_{DD} - A_1 sin(\omega_0 t)$, $V_{G1} = V_{D2} = V_{DD} + A_1 sin(\omega_0 t)$. Assuming $V_{DD} = 1.2\,\text{V}$, and $A_1 = 1\,\text{V}$, the g_m of the M_1 transistor under such V_{DS} and V_{GS} is found by simulations and is shown as dotted line in Fig. 3.4(b). Under this condition, $\alpha(\omega_0 t) = \dfrac{g_m(\omega_0 t)}{g_{m,max}}$. ISF, NMF and the effective ISF of

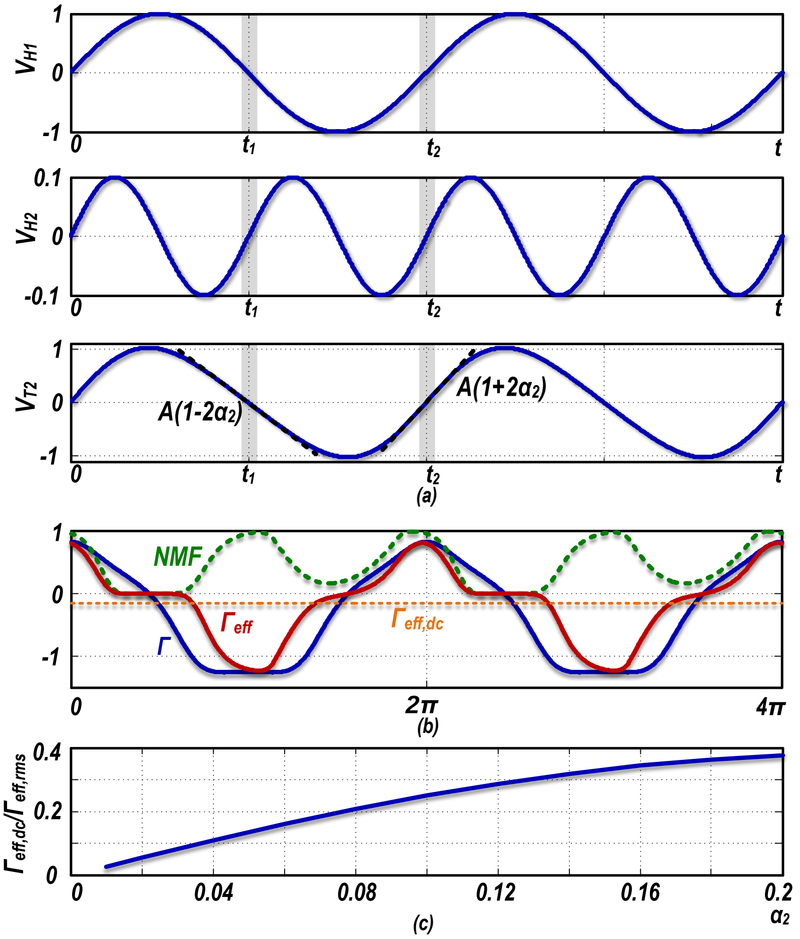


Figure 3.5: Conventional tank waveforms: (a) fundamental, V_{H1}, 2^{nd} harmonic, V_{H2}, voltage components and oscillation waveform, V_{T2}; (b) its ISF, NMF and effective ISF; (c) $\Gamma_{eff,dc}/\Gamma_{eff,rms}$ for different α_2 values.

the M_1 flicker noise source are shown in Fig. 3.4(c). The dc value of such an effective ISF is zero, resulting in no flicker noise up-conversion. This is a well known-conclusion and is referred to as a state where $M_{1,2}$ transistors' flicker noise cannot upconverted to PN [16].

In reality, the tank current of voltage-biased oscillators is rich in harmonics. Due to physical circuit constraints, the even-order current harmonics lead by $\pi/2$, while the odd-order current harmonics are in-phase with the fundamental current I_{H1}. The $\pi/2$ phase difference in even and odd-order current harmonics considerably changes the oscillation waveforms characteristics. For simplicity, we focus only on dominant harmonics, $I_{H2}{=}|I_{H2}|\sin(2\omega_0 t{+}\pi/2)$ and $I_{H3}{=}|I_{H3}|\sin(3\omega_0 t)$, as representatives of even and odd-order current harmonics, respectively; however, the following discussion can be easily generalized for all harmonics. We also assume for now that the tank only contains SE capacitors.

The differential current I_{H2} flows into the SE capacitors and creates a 2^{nd}-order voltage harmonic:

$$V_{H2}(t) = \frac{1}{C \cdot 2\omega_0} \cdot |I_{H2}| \sin\left(2\omega_0 t + \pi/2 - \pi/2\right) = \alpha_2 A_1 \sin\left(2\omega_0 t\right) \tag{3.4}$$

where, the $-\pi/2$ phase shift is due to the capacitive load. The oscillation voltage will then be

$$V_{T2}(t) = V_{H1}(t) + V_{H2}(t) = A_1 \left[\sin\left(\omega_0 t\right) + \alpha_2 \sin\left(2\omega_0 t\right)\right] \tag{3.5}$$

$V_{H1}(t)$, $V_{H2}(t)$ and $V_{T2}(t)$ are plotted in Fig. 3.5 (a) for α_2=0.1 and A_1=1 V. $V_{H1}(t)$ has two zero-crossings within its period: at t_1 and t_2, and their rise and fall times are symmetric with derivatives: $V'_{H1}(t_1) = -V'_{H1}(t_2)$. V_{H2}'s zero-crossings are also at t_1 and t_2; however $V'_{H2}(t_1) = V'_{H2}(t_2)$. Consequently, the opposite slope polarities of V_{H1} and V_{H2} at t_1 slow the fall time of V_{T2} while the same slope polarities at t_2 sharpen its rise time. Consequently, as can be gathered from 3.5 (a), V_{T2} features *asymmetric* rise and fall slopes.

The resulting ISF of the gm transistor is calculated based on (36) in Ref. [13] and is shown in Fig. 3.5 (b), with its mean dependent on α_2. Larger α_2 leads to more asymmetry between $V_{T2}(t)$ rise and fall slopes, hence $\Gamma_{eff,dc}$ will increase. Furthermore, repeating the same simulations to obtain g_{m1} with drain and gate voltages that contain 2^{nd} harmonic components results in asymmetric g_{m1} and consequently NMF. The slower rise/fall times increase the duration when M_1 is turned on, thus widening g_{m1}. A sharper rise/fall time decrease the amount of time when M_1 is turned on, resulting in a narrower g_{m1}. The NMF and effective ISF of such waveforms are shown in Fig. 3.5 (b). The effective ISF has a dc value which results in $M_{1,2}$'s flicker to PN up-conversion. Dependency of the dc value of the effective ISF on α_2 is shown in Fig. 3.5 (c).

This argument is valid for all even-order current harmonics, and we can conclude that the fluctuations in the even harmonics of the tank's current convert to the 1/f^3 PN noise through the modulation of the oscillating waveform.

Let us now investigate a case of the tank current containing only odd-harmonic components, with $I_{H3} = |I_{H3}|\sin(3\omega_0 t)$ as a representative. I_{H3} flows mainly into the tank capacitors and creates a 3^{rd} harmonic voltage as

$$V_{H3}(t) = \frac{1}{C \cdot 3\omega_0} \cdot |I_{H3}| \sin\left(3\omega_0 t - \pi/2\right) = \alpha_3 A_1 \sin\left(3\omega_0 t - \pi/2\right) \tag{3.6}$$

where, again, the $-\pi/2$ phase shift is due to the capacitive load. The oscillation voltage will then be

$$V_{T3}(t) = V_{H1}(t) + V_{H3}(t) = A_1 \left[\sin(\omega_0 t) + \alpha_3 \sin(3\omega_0 t - \pi/2)\right] \tag{3.7}$$

$V_{H1}(t)$, $V_{H3}(t)$ and $V_{T3}(t)$ are plotted in Fig. 3.6 (d) for α_3=0.1 and A_1=1 V. It is obvious that the oscillation waveform falling and rising slopes are symmetric, and $\Gamma_{dc} = 0$, as

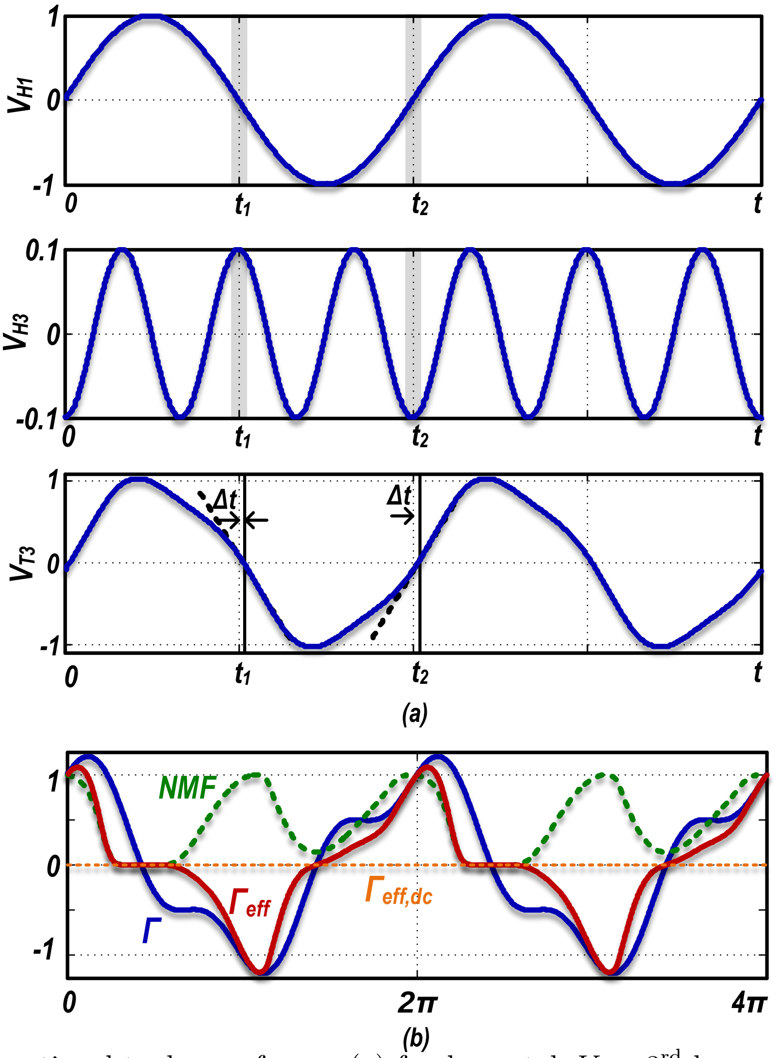


Figure 3.6: Conventional tank waveforms: (a) fundamental, V_{H1}, 3$^{\text{rd}}$ harmonic, V_{H3}, voltage component and oscillation waveform, V_{T3}; (b) its ISF, NMF and effective ISF.

easily gathered from Fig. 3.6 (e). The simulations show that g_{m1} is slightly asymmetric due to amplitude distortion of the oscillation voltage. However this asymmetry is canceled out when multiplied by ISF (see Fig. 3.6 (e)), resulting in an effective ISF with almost zero dc value and thus preventing low-frequency noise up-conversion. These arguments can be generalized for all odd-order harmonics. Consequently, the low-frequency noise of gm transistors does not upconvert to PN if the tank current only contains odd harmonics.

To further support that 1/f noise upconverts more to PN if α_2 is increased we tried to run some simulations on the voltage biased class-B oscillator of Fig. 3.7(a). Controlling the second-harmonic current is not very straightforward. It can be modified by changing the core transistors' width, W, or by changing tank's quality factor, Q. In both of these methods, the oscillation waveform amplitude would get affected. If we fix the oscillation amplitude when W or Q are swept, the second harmonic power modification

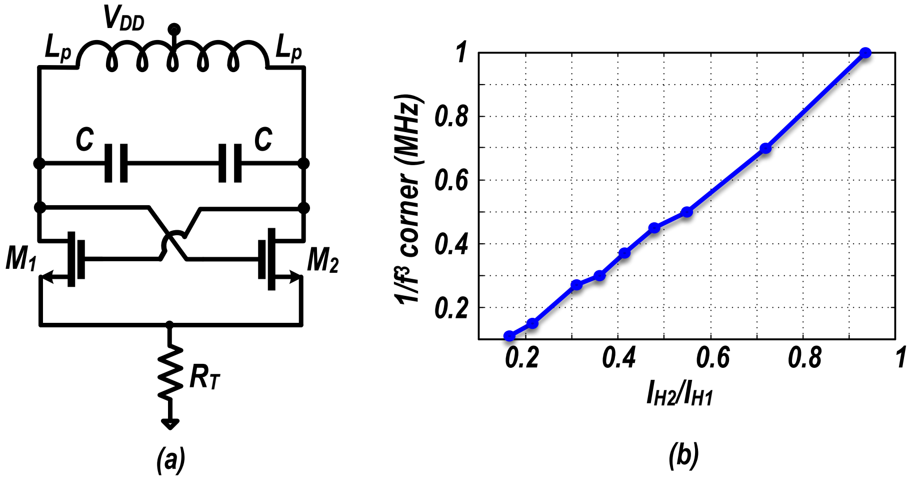


Figure 3.7: (a) Voltage biased class-B oscillator schematics (b) $1/f^3$ corner vs.I_{H2}/I_{Hn}.

range becomes very limited. On the other hand, by changing the transistors' width, the flicker noise of the device also changes and adds another parameter. Consequently, in the following simulations we swept the tank quality factor and all the other parameters, such as transistor sizes, supply voltage, etc., are kept the same. With higher Q, the oscillation voltage increases, the device spends more time in triode region and becomes more non-linear, consequently generating more current harmonics. M_1 and M_2 in the class-B oscillator are thick-oxide $56\mu/270$n devices, $V_{DD} = 1.2V$, $R_T = 9$ Ohm. The capacitors are ideal and not tunable. The simulation results are shown in Fig. Fig. 3.7(b). As we have discussed it, the flicker noise up-conversion depends on the α_2 value, which is proportional to the I_{H2}/I_{Hn} ratio. Therefore, we reported the $1/f^3$ corner vs. I_{H2}/I_{Hn} , and it is obvious from Fig. 3.7(b) that the corner increases for larger I_{H2}/I_{Hn} ratios in this class-B oscillator.

3.2.3 Resonant Frequency at $2\omega_0$

Thus far, we have shown that the even components of the tank's current are chiefly accountable for the asymmetric oscillation waveform and the 1/f noise upconversion to PN. Let us investigate what happens to the oscillation waveform and effective ISF if the tank has an auxiliary CM resonance at $2\omega_0$. Such resonance provides a resistive (i.e., via R_{p2}) path for I_{H2} to flow into it and hence the voltage 2^{nd} harmonic component is

$$V_{H2,aux}(t) = R_{p2}|I_{H2}|\sin\left(2\omega_0 t + \pi/2\right) = A_1\alpha_{2,aux}\sin\left(2\omega_0 t + \pi/2\right) \tag{3.8}$$

The composite oscillation voltage will become

$$V_{T2,aux}(t) = V_{H1}(t) + V_{H2,aux}(t) = A_1\left[\sin\left(\omega_0 t\right) + \alpha_{2,aux}\sin\left(2\omega_0 t + \pi/2\right)\right] \tag{3.9}$$

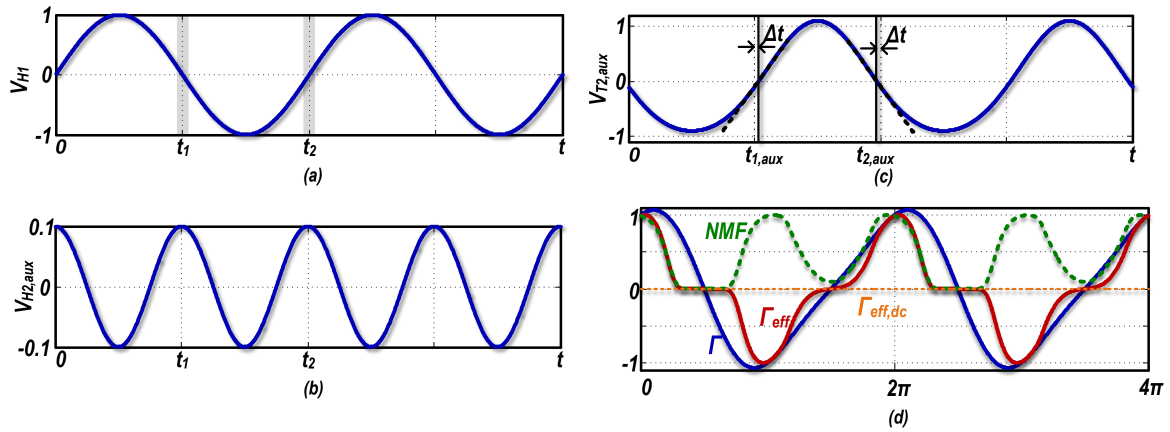


Figure 3.8: Proposed tank waveforms: (a) fundamental voltage component, V_{H1}; (b) voltage 2^{nd} harmonic in presence of auxiliary resonance, $V_{H2,aux}$; (c) oscillation waveform, $V_{T2,aux}$; (d) its ISF, NMF and effective ISF.

$V_{H1}(t)$, $V_{H2,aux}(t)$ and $V_{T2,aux}(t)$ are plotted in Fig. 3.8(a),(b),(c) for $\alpha_{2,aux}$=0.1 and A_1=1. The rise and fall times of the oscillation voltage are now symmetric (see Fig. 3.8(c)) and so the ISF is zero mean, as shown in Fig. 3.8(d). g_{m1}, and thus NMF, are also completely symmetrical; consequently the effective ISF has a zero dc value, preventing low-frequency noise from being up-converted. The oscillation waveform is still dependent on $\alpha_{2,aux}$, but the rise and fall times are always symmetric, thus keeping $\Gamma_{eff,dc}$ zero.

The second and third current harmonics are the most dominant in all classes of oscillators, so α_2 and α_3 are significantly larger than other α_n for n=4, 5, ... Meanwhile, Γ_{dc} is a growing function of α_n for $n = 2k$, where $k = 1, 2, \ldots$. We can, therefore, conclude that I_{H2} is the main contributor to the 1/f noise upconversion. Consequently, attention to only one auxiliary resonant frequency at $2\omega_0$ appears sufficient [22] [24].

3.2.4 ω_{CM} Deviation from $2\omega_0$

The balance in the rise and fall zero-crossing slopes in Fig. 3.8(c) is rooted in the $\pi/2$ phase shift between $V_{H1}(t)$ and $V_{H2}(t)$. This is a combination of the $\pi/2$ phase difference between $I_{H1}(t)$ and $I_{H2}(t)$, and zero phase of the resistive tank impedance at $2\omega_0$. When ω_{CM} deviates from $2\omega_0$

$$\begin{aligned} V_{T2,aux}(t) = V_{H1}(t) + V_{H2,aux}(t) &= R_{p1}|I_{H1}|\sin(\omega_0 t) + |Z_{CM}|\cdot|I_{H2}|sin(2\omega_0 t + \pi/2 + \phi_{CM}) \\ &= A_1\left[\sin(\omega_0 t) + \alpha_{2,aux} sin(2\omega_0 t + \pi/2 + \phi_{CM})\right] \end{aligned} \tag{3.10}$$

where, $|Z_{CM}|$ and ϕ_{CM} are the CM input impedance magnitude and phase, respectively, derived as,

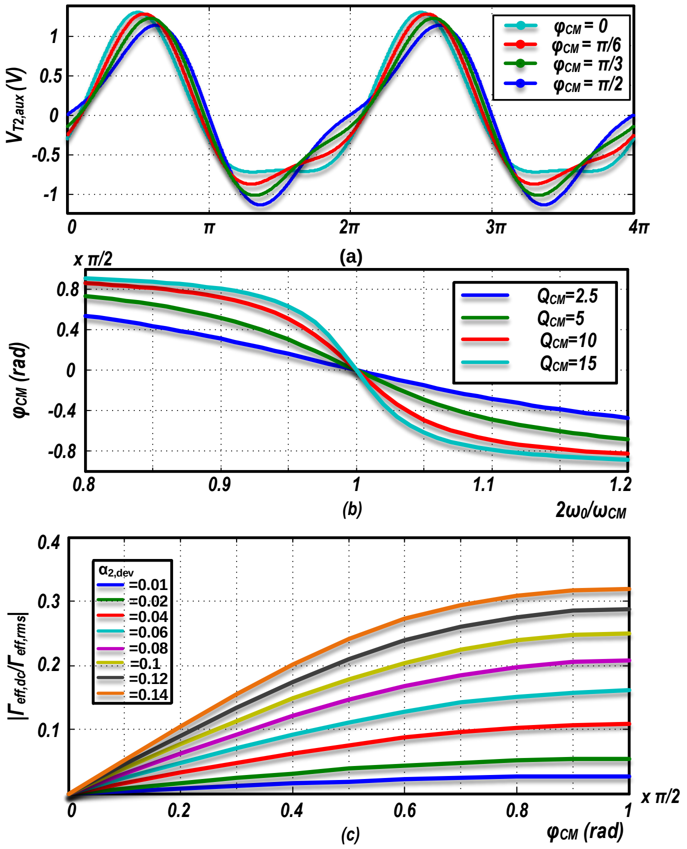


Figure 3.9: (a) $V_{T2,aux}$ for different ϕ_{CM}; (b) ϕ_{CM} for different Q$_{CM}$ when ω_{CM} deviates from $2\omega_0$; (c) $\Gamma_{eff,dc}/\Gamma_{eff,rms}$ for different $\alpha_{2,aux}$ and ϕ_{CM}.

$$\phi_{CM} = \arctan\left(\frac{1-\zeta^2}{\frac{\zeta}{Q_{CM}}}\right) \tag{3.11}$$

$$|Z_{CM}| = R_{p2}\cdot\frac{\frac{\zeta}{Q_{CM}}}{\sqrt{\left(1-\zeta^2\right)^2+\left(\frac{\zeta}{Q_{CM}}\right)^2}} \tag{3.12}$$

where $\zeta = \dfrac{2\omega_0}{\omega_{CM}}$. The ω_{CM} vs. $2\omega_0$ misalignment has two effects. The first directly translates ϕ_{CM} into the waveform asymmetry. Figure 3.9(a) shows $V_{T2,aux}(t)$ for different ϕ_{CM}; $\alpha_{2,aux}$ was chosen 0.3 to better illustrate the asymmetry. When grossly mistuned from $2\omega_0$, ϕ_{CM} could approach $\pm\pi/2$, thus making the auxiliary resonance completely ineffective. A larger Q-factor of the common-mode resonance, Q_{CM}, results in ϕ_{CM} closer to $\pm\pi/2$ for the same $2\omega_0/\omega_{CM}$ ratios, as illustrated in Fig. 3.9(b).

The second effect is due to $\alpha_{2,aux}$, which determines the amount of second harmonic in the voltage waveform. When ϕ_{CM} is not zero, $\Gamma_{eff,dc}$ becomes dependent on $\alpha_{2,aux}$: The larger $\alpha_{2,aux}$, the more asymmetric waveform and more 1/f noise upconversion. The $\alpha_{2,aux}$ value can be found from the following equation

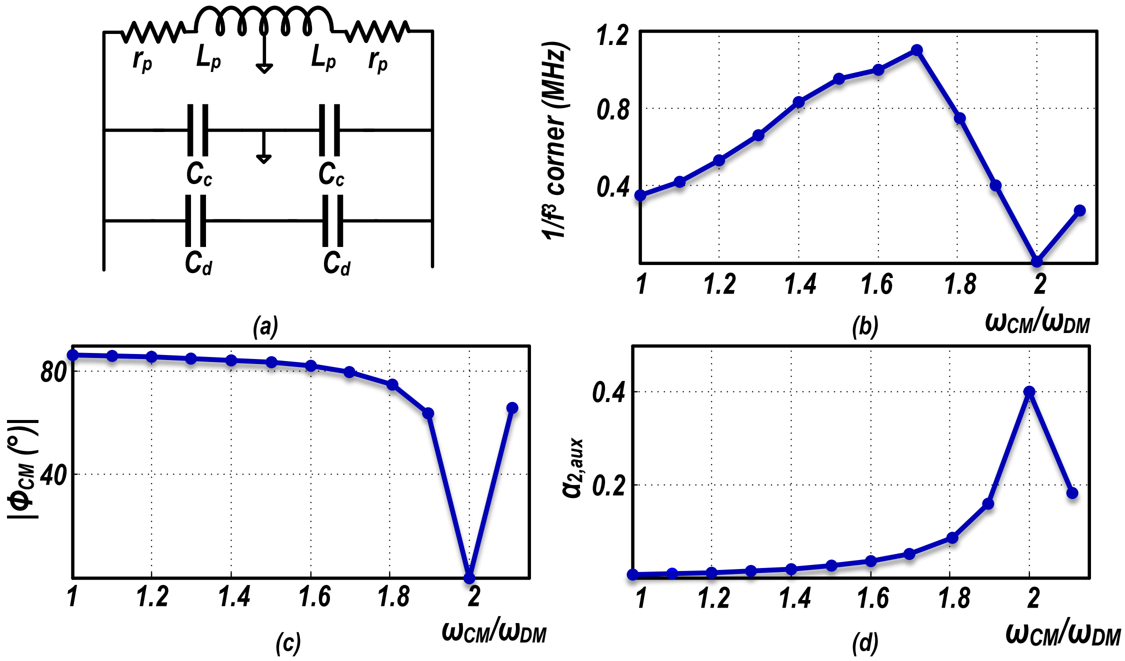


Figure 3.10: (a) A tank with DM and CM resonances ; (b) 1/f^3 corner of the oscillator employing this tank; (c) ϕ_{CM}; and (d) $\alpha_{2,aux}$ of the tank vs. ω_{CM}/ω_{DM}.

$$\alpha_{2,aux} = \left|\frac{I_{H2}}{I_{H1}}\right| \cdot \frac{|Z_{CM}|}{R_{p1}} \tag{3.13}$$

I_{H2}/I_{H1} is dependent on the oscillator's topology. Furthermore, the larger Q_{CM}, the larger R_{p2} and hence the larger $\alpha_{2,aux}$. Figure 3.9(c) shows the expected $\Gamma_{eff,dc}/\Gamma_{eff,rms}$ vs. ϕ_{CM} for different $\alpha_{2,aux}$. Both of these effects point out that Q_{CM} should be low to reduce the sensitivity of this method to the ω_{CM} deviation from $2\omega_0$.

3.3 Circuit Implementation

We have shown that if the tank demonstrates an auxiliary CM resonance at the 2$^{\text{nd}}$ harmonic of its fundamental ω_0 resonance, the oscillation waveform would be symmetric and, hence, the flicker noise upconversion would be suppressed. Since the differential capacitors are not seen by the CM signals (i.e., I_{H2}), a straightforward solution for realizing a CM peak is to design a tank as demonstrated in Fig. 3.10(a)) with a set of differential C_d and single-ended (SE) C_c capacitors [24]. r_p is the equivalent series resistance of the inductor and it is assumed all capacitors are nearly ideal. This tank shows a fundamental DM resonant frequency, $\omega_{DM} = \dfrac{1}{\sqrt{L_p(C_c + C_d)}}$ and a CM resonant frequency $\omega_{CM} = \dfrac{1}{\sqrt{L_p C_c}}$. From (3.11)–(3.13):

$$\phi_{CM} = \arctan\left(\frac{1-\frac{4C_c}{C_c+C_d}}{\frac{1}{Q_{DM}}\cdot\frac{2C_c}{C_c+C_d}}\right) \tag{3.14}$$

$$\alpha_{2,aux} = \frac{R_{p2}}{R_{p1}}\cdot\frac{\frac{2}{Q_{DM}}\cdot\left(\frac{C_c}{C_c+C_d}\right)}{\sqrt{\left(1-\frac{4C_c}{C_c+C_d}\right)^2+\left(\frac{2}{Q_{DM}}\cdot\frac{C_c}{C_c+C_d}\right)^2}}\cdot\frac{I_{H2}}{I_{H1}} \tag{3.15}$$

where, Q_{DM}, R_{p2} and R_{p1} are, respectively, the quality factor at DM resonance, and impedance peaks at CM and DM resonances. In an extreme condition of C_d=0, the tank contains only the SE capacitors and reduces to a conventional tank discussed in Section 3.2.2. Targeting ω_{CM}=2ω_{DM} results in C_d=3C_c and we can prove that Q_{CM}=2Q_{DM}. As discussed supra, the fairly large Q_{CM} exacerbates the effects of CM resonance misalignment. To investigate the effectiveness of the proposed method on the tank mistuning sensitivity, we performed an analysis of a 5 GHz voltage-biased class-B oscillator of Fig. 3.1(b) with Q_{DM}=10. The oscillator is designed in a 40-nm CMOS technology, and $M_{1,2}$ are thick-oxide (56/0.27)-μm devices. The power consumption is 10.8 mW at V_{DD}=1.2 V. As expected, the 1/f^3 corner of this oscillator is at its minimum of ∼10 kHz at C_d/C_c=3 (see Fig. 3.10(b)). When ω_{CM} deviates from 2ω_{DM}, i.e., C_d/C_c ratio deviates from the ideal value of 3, while keeping $C_c + C_d$ constant, the 1/f^3 corner starts to increase from the 10 kHz minimum, and reaches its peak at ω_{CM}=1.7ω_{DM} when the CM resonance phase, ϕ_{CM}, gets close to $\pi/2$ (about 80° as shown in Fig. 3.10(c)). After this point, the ϕ_{CM} barely changes, but $\alpha_{2,aux}$ decreases (Fig. 3.10(d)) and, consequently, the 1/f^3 corner reduces again. The maximum 1/f^3 corner of 1.1 MHz is actually much worse than the 400 kHz corner of extreme case when C_d=0 (see Fig. 3.10(b)). This means that if the tank is not designed properly, the performance would be even worse than that without applying this technique. Consequently, to ensure no performance degradation in face of the misalignment, $\alpha_{2,aux}$ at $\phi_{CM} \approx 80°$ should be less than that of the tank without the applied technique. α_2 when C_d=0 can be found from (3.15):

$$\alpha_2 \approx \frac{2}{3Q_{DM}}\cdot\frac{I_{H2}}{I_{H1}} \tag{3.16}$$

$\phi_{CM} = 80°$, (3.14) and (3.15) result in

$$\alpha_{2,aux} = \frac{R_{p2}}{R_{p1}}\cdot\frac{\tan\left(\frac{\pi}{18}\right)}{\sqrt{1+\tan^2\left(\frac{\pi}{18}\right)}}\cdot\frac{I_{H2}}{I_{H1}} \tag{3.17}$$

Hence,

$$\frac{R_{p2}}{R_{p1}} < \frac{3.84}{Q_{DM}} \tag{3.18}$$

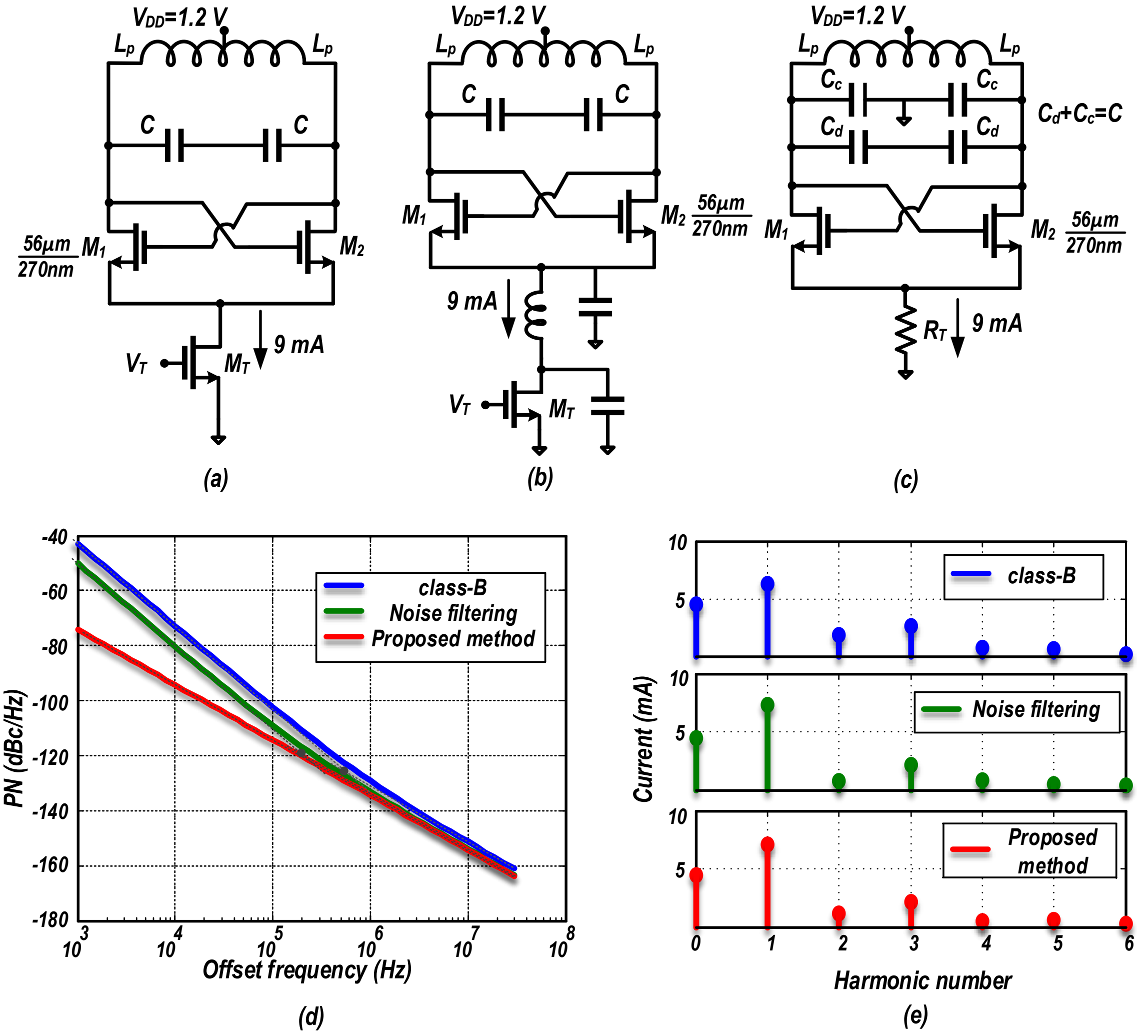


Figure 3.11: d) PN; and (e) current harmonic components of a class-B oscillator (a), and similar counterparts with noise filtering technique [29] (b), and the proposed method applied (c).

to satisfy this condition, which results in non-practical Q_{DM} values.

In the following two subsections we show how to substantially reduce the sensitivity to such misalignment by employing, at no extra area penalty, an inductor exhibiting distinct and beneficial characteristics in DM and CM excitations. The different behavior of a 1:2 turn transformer in DM and CM excitations is also exploited to design a transformer-based F_2 tank. With these new tanks, we construct class-D and a class-F oscillators to demonstrate the effectiveness of the proposed method of reducing the flicker noise upconversion. Before we do that, lets compare the $1/f^3$ corner and current harmonics of a current biased class-B (see Fig.3.11(a)), a current biased class-B with noise filtering technique [29] applied to it (see Fig.3.11(b)), and a voltage biased class-B with the proposed technique applied to it (see Fig.3.11(c)). In the current-biased configuration

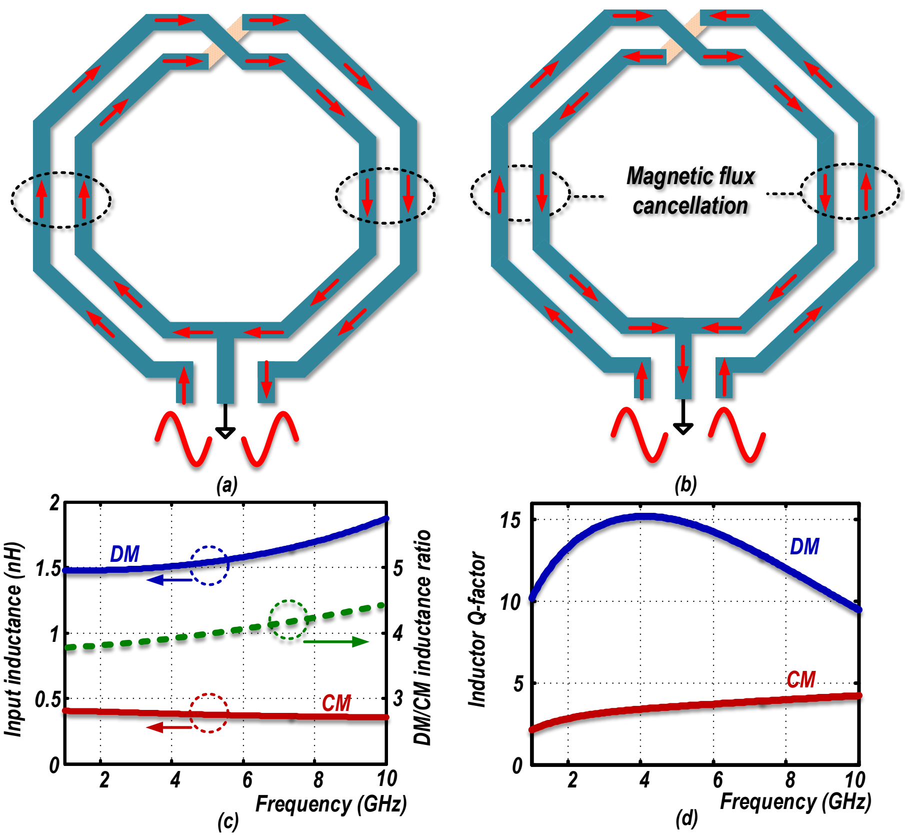


Figure 3.12: A 2-turn "F$_2$" inductor in (a) DM excitation; (b) CM excitation; (c) F_2 DM and CM inductances and their ratio; (d) Q_{DM} and Q_{CM}.

proposed in [29], a capacitor in parallel with the current source shorts noise frequencies around $2\omega_0$ to ground. An inductor is interposed between the common source of the cross-coupled transistors and the current source. That inductor resonates at $2\omega_0$ with the equivalent capacitor at the common source of the oscillator transistors, (see Fig3.11(b)). The purpose of that resonator is creating a high impedance path at $2\omega_0$ to stop the tank loading when one of the core transistors enters the triode region. That method is also partially effective in reducing low-frequency noise up-conversion of core transistors, by linearizing the core transistors and reducing current harmonics, especially the 2^{nd} harmonic component content. That resonator has to be tunable over the tuning range and it increases the die area. Figures 3.11(d-e) show the PN performance and current harmonic components of the three oscillators shown in 3.11(a-c). In the simulations, all the capacitors are ideal capacitors and non-tunable. It is obvious how much the 2^{nd} harmonic current is reduced in the noise filtering method, and consequently the $1/f^3$ corner is lower than in a conventional class-B oscillator.

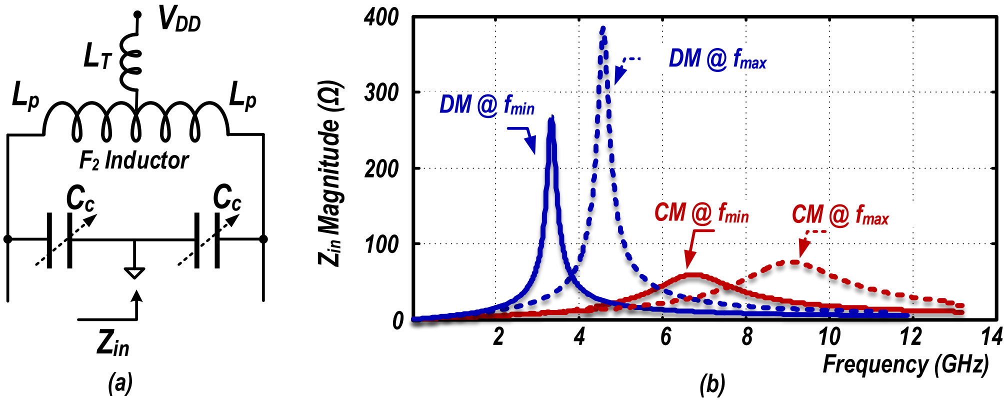


Figure 3.13: (a) Inductor-based F_2 tank; and (b) its input impedance.

3.3.1 Inductor-Based F_2 Tank

Figures 3.12(a),(b) show a 2-turn "F$_2$" inductor when it is excited by DM and CM signals. In the DM excitation, currents in both turns have the same direction, resulting in an additive magnetic flux. However, in the CM excitation, currents have opposite direction and cancel each other's flux [25]. With the proper spacing between the F_2 inductor windings, effective inductance in CM can be made 4x smaller than in DM. The L_{DM}/L_{CM} inductance ratio is controlled through lithography that *precisely* sets the physical inductor dimensions and, consequently, makes it *insensitive* to process variations. Figure 3.12(c) shows the DM and CM inductances and their ratio over frequency. L_{DM}/L_{CM} is close to 4 within a 30–40% tuning range.

Differential capacitors cannot be seen by the CM signals; hence to be able to set the CM resonance the F_2 tank capacitors should be SE, as shown in Fig. 3.13(a). The F_2 tank demonstrates two resonant frequencies: ω_{DM} and ω_{CM}. Both of these are tuned simultaneously by adjusting C_c. The precise inductor geometry maintains $L_{DM}/L_{CM} \approx 4$ and hence $\omega_{CM}/\omega_{DM} \approx 2$ over the full tuning range. The input impedance of the tank is shown in Fig. 3.13(b). Presuming the capacitance losses are negligible, the DM and CM resonance quality factors are,

$$Q_{DM} = \frac{L_p \omega_{DM}}{r_p} = Q_0 \tag{3.19}$$

$$Q_{CM} = \frac{L_p \omega_{CM}}{4 r_p} = \frac{Q_0}{2} \tag{3.20}$$

The Q-factor of the CM resonance is half that of DM, which relaxes the F$_2$ tank sensitivity to mismatch between ω_{CM} and $2\omega_{DM}$. For this inductor-based F$_2$ tank, $R_{p2}/R_{p1} = 0.25$ and the condition in (3.18) is *satisfied* for $Q_0 < 15$. Furthermore, in the CM excitation, the currents in adjacent windings have opposite direction, which results in an increased AC resistance [28] and so the Q-factor of the CM inductance is even smaller than in (3.20). The Q-factor of L_{CM} inductance of Fig. 3.12(b) is about 3–4.

Apart from the easy tuning with only one capacitor bank, the mostly SE parasitic capacitors do not play any role in defining the $\omega_{CM}/2\omega_{DM}$ ratio. Furthermore, the low Q_{CM} and, consequently, the lower sensitivity to the $\omega_{CM}/2\omega_{DM}$ ratio that the inductor-based F_2 tank offers, make it all more attractive than the tank shown in Fig. 3.10(a).

3.3.2 Class-D/F_2 Oscillator

Among the various classes of inductor-based oscillators (e.g., class-B, complementary class-B, class-D [5]) we have decided to validate the proposed method on a class-D oscillator depicted in Fig. 3.14 (a). This recently introduced oscillator shows promising PN performance in the $1/f^2$ region due its special ISF. The tail current transistor is removed there and wide and almost ideal switches $M_{1,2}$ clip the oscillation voltage to GND for half a period (see Fig 3.14 (b)) resulting in an almost zero ISF there (Fig 3.14 (c)). However, the hard clipping of the drain nodes to GND generates a huge amount of higher-order harmonic currents. Due to the large I_{H2}, in agreement with our analysis, the oscillating waveform has asymmetric fall and rise times (clearly visible in Fig 3.14 (b)) and it exhibits a strong 1/f noise upconversion and frequency pushing. A version of class-D with a tail filter technique [29] was also designed in [5] in an attempt to reduce the low frequency noise upconversion. This method is partially effective, lowering the $1/\mathrm{f}^3$ PN corner from 2 MHz to 0.6–1 MHz. Due to the above reasons, this voltage-biased oscillator seems a perfect fit for the proposed method.

Figure 3.14 (d) shows the proposed class-D/F_2 oscillator, which adopts the F_2 tank. The gm-devices, M_1 and M_2, still inject a large I_{H2} current into the tank, but this current is now flowing into the equivalent resistance of the tank at $2\omega_0$. Clearly, the rise/fall times are more symmetric in the class-D/F_2 oscillator, as demonstrated in Fig 3.14 (e). The gm-transistors' ISF, NMF and effective ISF are shown in Fig 3.14 (f). As predicted, effective Γ_{dc} is now reduced and the simulated PN performance shows the $1/\mathrm{f}^3$ corner is lowered from 1 MHz to $\sim$30 kHz, Fig 3.14 (g).

The parasitic inductance L_T has to be considered in designing the F_2 inductor. C_c controls both CM and DM resonant frequencies simultaneously, hence any deviation of ω_{CM} from $2\omega_0$ is due to L_{CM}/L_{DM} not being exactly 4 over the TR. To examine the robustness of the tank via simulations, a C_d differential capacitor is deliberately added to the tank. $C_c + C_d$ is kept constant in order to maintain the oscillation frequency. This capacitor shifts down ω_{DM} while keeping ω_{CM} intact. Fig 3.14 (h) shows how the $1/\mathrm{f}^3$

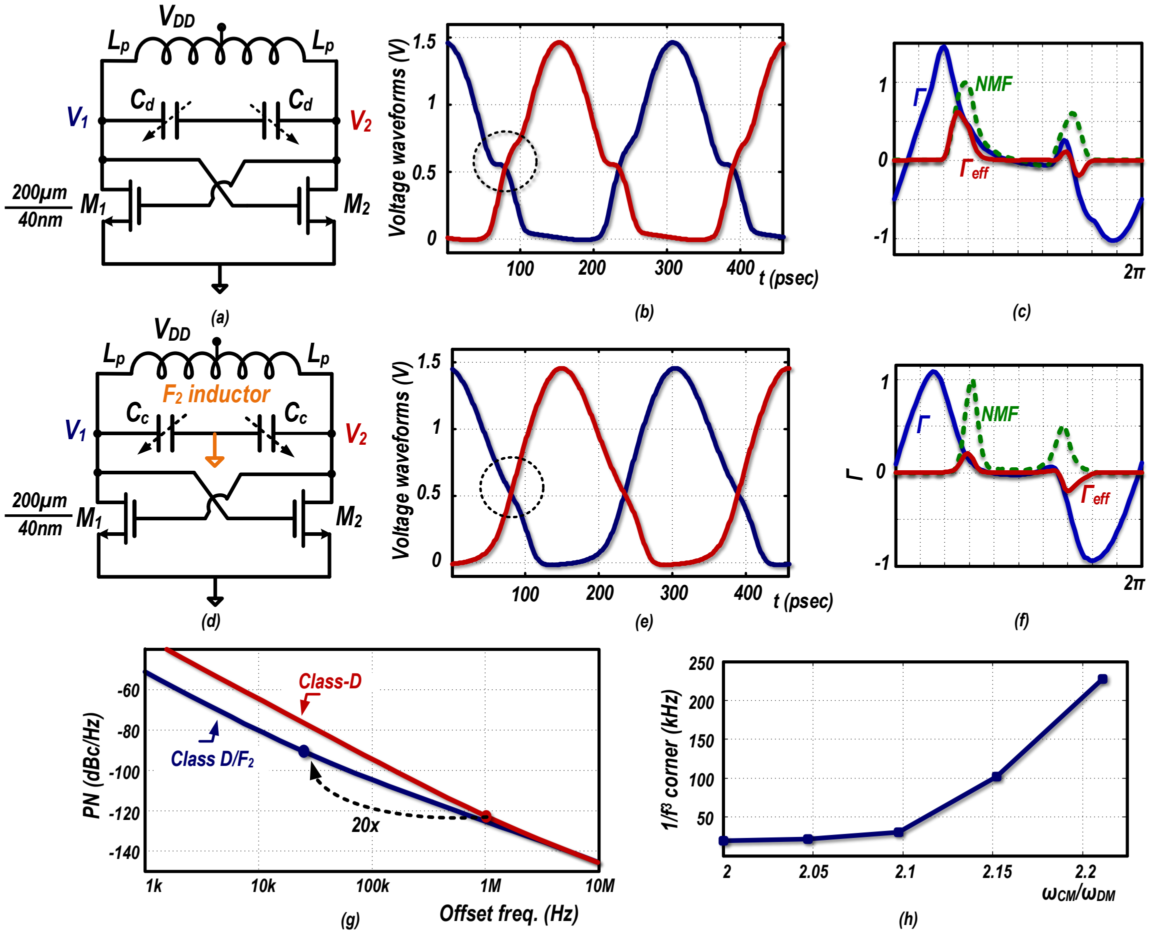


Figure 3.14: Class-D oscillator: (a) schematic; its (b) waveforms; and (c) gm-transistor ISF, NMF, and effective ISF. Class-D/F$_2$ oscillator: (d) schematic; its (e) waveforms; and (f) gm-transistor ISF, NMF, and effective ISF; (g) their PN performance; and (h) 1/f^3 corner sensitivity to ω_{CM}/ω_{DM}.

corner worsens when C_d/C_c ratio increases. The class-D/F$_2$ oscillator is quite robust to process variations. First of all, due to the low CM resonance quality factor of an F_2 inductor, this topology is less sensitive to deviations of ω_{CM} from $2\omega_0$. Furthermore, in this topology only single-ended capacitor banks are employed, hence ω_{CM}/ω_{DM} ratio is solely defined by L_{CM}/L_{DM}. The cross coupled transistors parasitic capacitors are mostly single-ended, except for C_{gd} which is less than 5% of the tanks total capacitance. Consequently, the modification of core transistors parasitic capacitance over process variations, will only change oscillation frequency and barely modify the ω_{CM}/ω_{DM} ratio. Figure 3.15(a) shows simulation results for the 1/f^3 corner of the class-D/F$_2$ oscillator in different process corners. The PN at 10 kHz offset frequency for both class-D/F$_2$ oscillator for 200 points Monte Carlo simulations on inter/intra die process variations is shown in Fig.3.15(a).

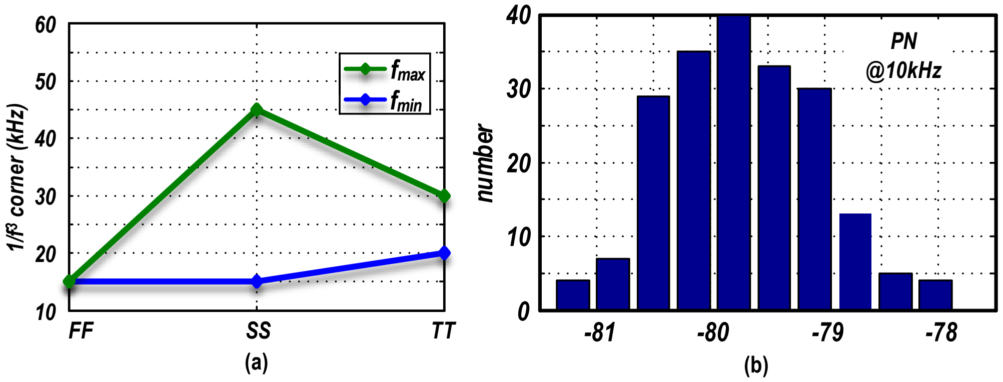


Figure 3.15: Class-D/F$_2$ oscillator: 1/f^3 corner over process variation; and (b) histogram of PN at 10kHz offset frequency.

3.3.3 Transformer-Based F$_2$ Tank

Figures 3.16 (a), (b) show a 1:2 turns transformer excited by DM and CM input signals at its primary. With a DM excitation, the induced currents at the secondary circulate in the same direction leading to a strong coupling factor, k_m. On the other hand, in CM excitation, the induced currents cancel each other, resulting in a weak k_m [27]. The latter means that the secondary winding cannot be seen by the CM signals. "F_2" transformer-based tank is shown in Fig. 3.17(a).

At the DM excitation, no current flows into the metal track inductance, L_T, that connects the center tap to the supply's AC-ground (see Fig. 3.17(a)). However, at the CM excitation, the current flowing into L_T is twice the current circulating in the inductors. Consequently, the tank inductance L_p in Fig. 3.17(a) is re-labeled as $L_{pd} = L_p$ in DM, and $L_{pc} = L_{pd} + 2L_T$ in CM excitations. This tank employs SE primary and differential secondary capacitors and demonstrates two DM and one CM resonant frequencies. $\omega_{CM} = 1/\sqrt{L_{pc}C_p}$ and if $k_{m,DM}$>0.5, $\omega_{0,DM} = 1/\sqrt{L_{pd}C_p + L_sC_s}$ [6]. F_2 tank requires $\omega_{CM} = 2\omega_{0,DM}$, hence,

$$L_sC_s = C_p(4L_{p,c} - L_{p,d}) \tag{3.21}$$

Unlike in the inductor-based tank, here the $\omega_{CM}/\omega_{0,DM}$ ratio is dependent on the secondary-to-primary capacitors ratio. Furthermore, the input impedance Z_{in}, shown in Fig. 3.17(b), reveals that Q$_{CM}$ is not low, thus making it sensitive to $\omega_{CM}/\omega_{0,DM}$. It means the C_s/C_p ratio has to be carefully designed to maintain $\omega_{CM}/\omega_{0,DM} \approx 2$ over the tuning range. In practice, the Q-factor of capacitor banks is finite and decreases at higher frequencies, so Q_{CM} will reduce, thus making the tank a bit less sensitive.

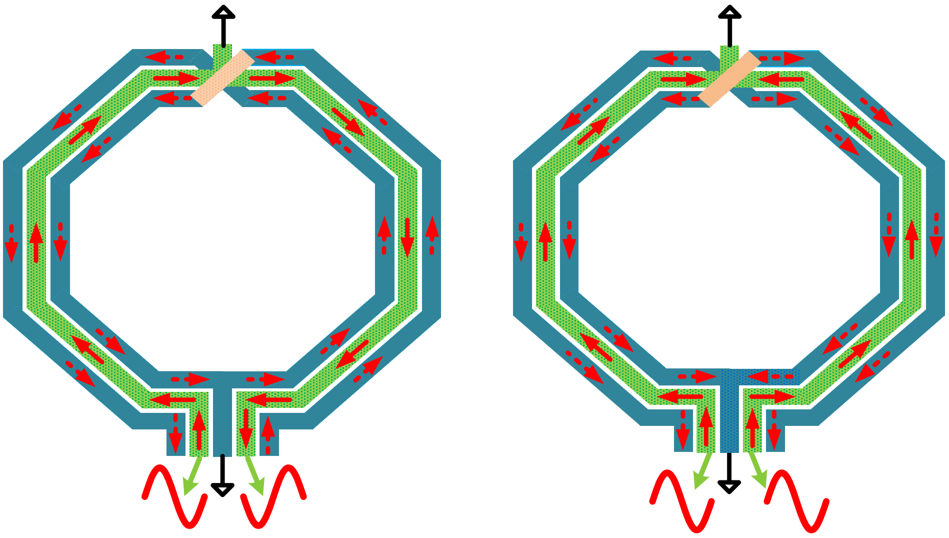


Figure 3.16: 1:2 transformer when the primary is excited with (a) DM; and (b) CM currents.

3.3.4 Class-$F_{2,3}$ Oscillator

As proven in [6], a DM auxiliary resonance at the third harmonic of the fundamental frequency is beneficial in improving the 20 dB/dec PN performance by creating a pseudo square-wave oscillation waveform (see Fig. 3.18 (b)). We can merge our transformer-based F_2 tank with the class-F_3 operation in [6] to design a class-$F_{2,3}$ oscillator, as shown in Fig. 3.18 (d)-(e). To ensure $\omega_{CM} = 2\omega_{0,DM}$ and $\omega_{1,DM} = 3\omega_{0,DM}$, we force $L_sC_s = 3.8L_{pd}C_p$ and $k_m = 0.67$. The relatively low k_m increases the impedance at $\omega_{1,DM}\equiv3\omega_{0,DM}$ [28]. However, the class-F_3 oscillator meets the oscillation criteria only at $\omega_{0,DM}$. Figure 3.18(e) demonstrates that the pseudo-square waveform of class-F_3 oscillation is preserved in the class-$F_{2,3}$ oscillator. The waveform does not appear to differ much; however, the oscillation voltage spectrum indeed confirms the class-$F_{2,3}$ operation. I_{H2} is not very large in this class of oscillators, consequently, the fall/rise-time asymmetry is not as distinct as in the class-D oscillator. However, the 1/f^3 corner improvement from 400 kHz in class-F_3 to <30 kHz in class-$F_{2,3}$, as demonstrated in Fig. 3.18(g), proves the effectiveness of the method. The ISF, NMF and effective ISF's for these oscillators are shown in Fig. 3.18 (c), (f). Class-$F_{2,3}$ oscillator performance is sensitive to the deviation of ω_{CM} from $2\omega_0\equiv2\omega_{DM}$. C_p changes both CM and DM resonant frequencies while C_s only changes the DM one. To examine the robustness of the F_2 operation, differential capacitors are added in the tank's primary. Here again $C_{p,c} + C_{p,d}$ is constant to maintain the oscillation frequency. Figure 3.18(h) shows the 1/f^3 corner vs. ω_{CM}/ω_{DM} ratio and underscores the need to control the capacitance ratio, as per (3.21). Otherwise, a small deviation increases the 1/f^3

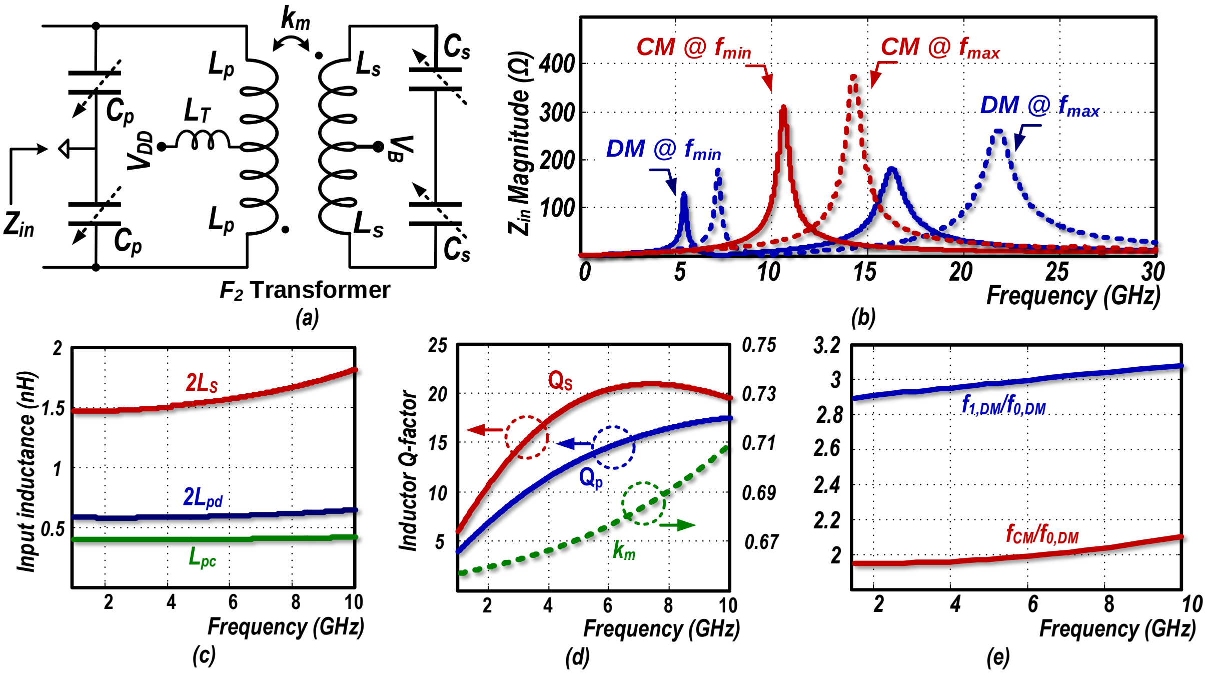


Figure 3.17: (a) Transformer-based F_2 tank; (b) its input impedance; (c) DM and CM primary and secondary inductance; (d) primary and secondary inductance quality factor and coupling factor; (e) DM and CM resonant frequencies over TR.

corner rapidly and with larger deviations the method becomes ineffective. the class-$F_{2,3}$ topology is somewhat less robust to process variations. This topology is generally more sensitive to deviations of ω_{CM} from $2\omega_0$, due to higher CM resonance quality factor. Moreover, in this topology, $\omega_{CM}/\omega_{DM} = \sqrt{((L_sC_s + L_pC_p)/(L_pC_p))}$ and is dependent on secondary and primary windings' inductance and capacitance ratio. The modification of core transistors parasitic capacitance modifies both primary and secondary capacitances and, hence, both DM and CM resonant frequencies are affected in the same direction (they are both going to increase with less parasitic capacitance and vice versa). Therefore, the ω_{CM}/ω_{DM} ratio is not affected drastically with the parasitic capacitance variations; however due to larger Q_{CM}, the small effects are also important. Figure 3.19(a) shows the simulation results for $1/\mathrm{f}^3$ corner of the class-$F_{2,3}$ oscillator in different process corners. The $1/\mathrm{f}^3$ corner is more affected compared to the class-D/F_2 oscillator, however it is still very competitive. The PN at 10 kHz offset frequency for class-$F_{2,3}$ oscillator for 200 points Monte Carlo simulations on inter/intra die process variations is shown in Fig. 3.19(b).

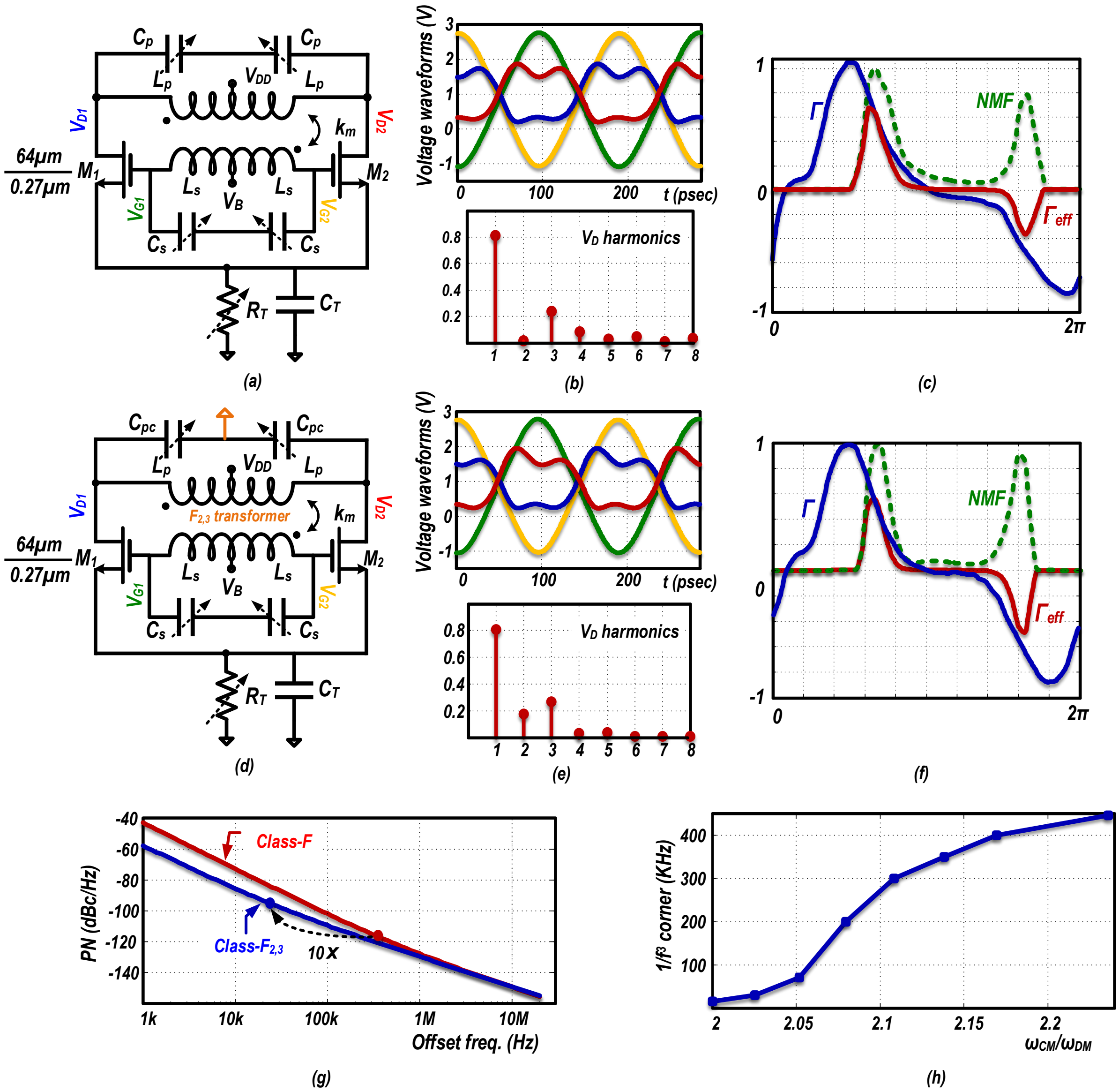
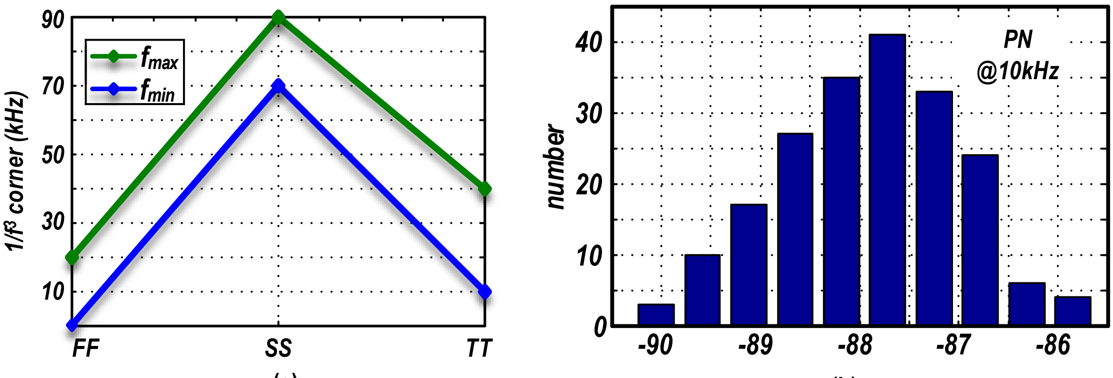


Figure 3.18: Class-F_3 oscillator: (a) schematic; its (b) waveforms; and (c) gm-transistor ISF, NMF, and effective ISF. Class-$F_{2,3}$ oscillator: (d) schematic; its (e) waveforms; and (f) gm-transistor ISF, NMF, and effective ISF; (g) their PN performance; and (h) $1/f^3$ corner sensitivity to ω_{CM}/ω_{DM}.

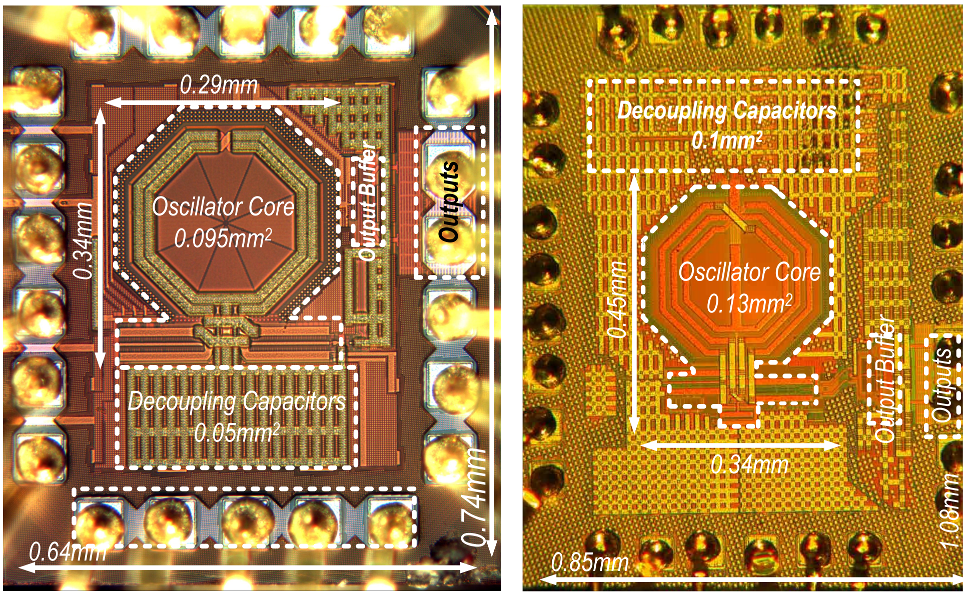
3.4 Experimental Results

The class-D/F_2 and class-$F_{2,3}$ oscillators, whose schematics were shown in Fig. 3.14(d) and Fig. 3.18(d), respectively, are designed in 40 nm CMOS to demonstrate the suppression of the 1/f noise upconversion. For fair comparison, we attempted to design the oscillators with the same specifications, such as center frequency, tuning range and supply voltage, as their original reference designs in [5] and [6].



(a) (b)

Figure 3.19: Class-$F_{2,3}$ oscillator: $1/f^3$ corner over process variation; and (b) histogram of PN at 10kHz offset frequency.


0.29mm
0.34mm
Oscillator Core
0.095mm²
Output Buffer
Outputs
Decoupling Capacitors
0.05mm²
0.74mm
0.64mm
Decoupling Capacitors
0.1mm²
0.45mm
Oscillator Core
0.13mm²
Output Buffer
Outputs
0.34mm
1.08mm
0.85mm

(a) *(b)*

Figure 3.20: Chip micrographs: (a) class-D/F_2 oscillator; (b) class-$F_{2,3}$ oscillator.

3.4.1 Class-D/F_2 Oscillator

The class-D/F_2 oscillator is realized in a 40-nm 1P8M CMOS process *without* ultra-thick metal layers. The two-turn inductor is constructed by stacking the 1.45 μm Alucap layer on top of the 0.85 μm top (M8 layer) copper metal. The DM inductance is 1.5 nH with simulated Q of 12 at 3 GHz. Combination of MOS/MOM capacitors between the supply and ground is placed on-chip to minimize the effective L_T inductance, and the remaining uncompensated inductance is modeled very carefully. The capacitor bank is realized with 6-bit switchable MOM capacitors with LSB of 30 fF. The oscillator is tunable between 3.3–4.5 GHz (31% TR) via this capacitor bank. $M_{1,2}$ transistors are

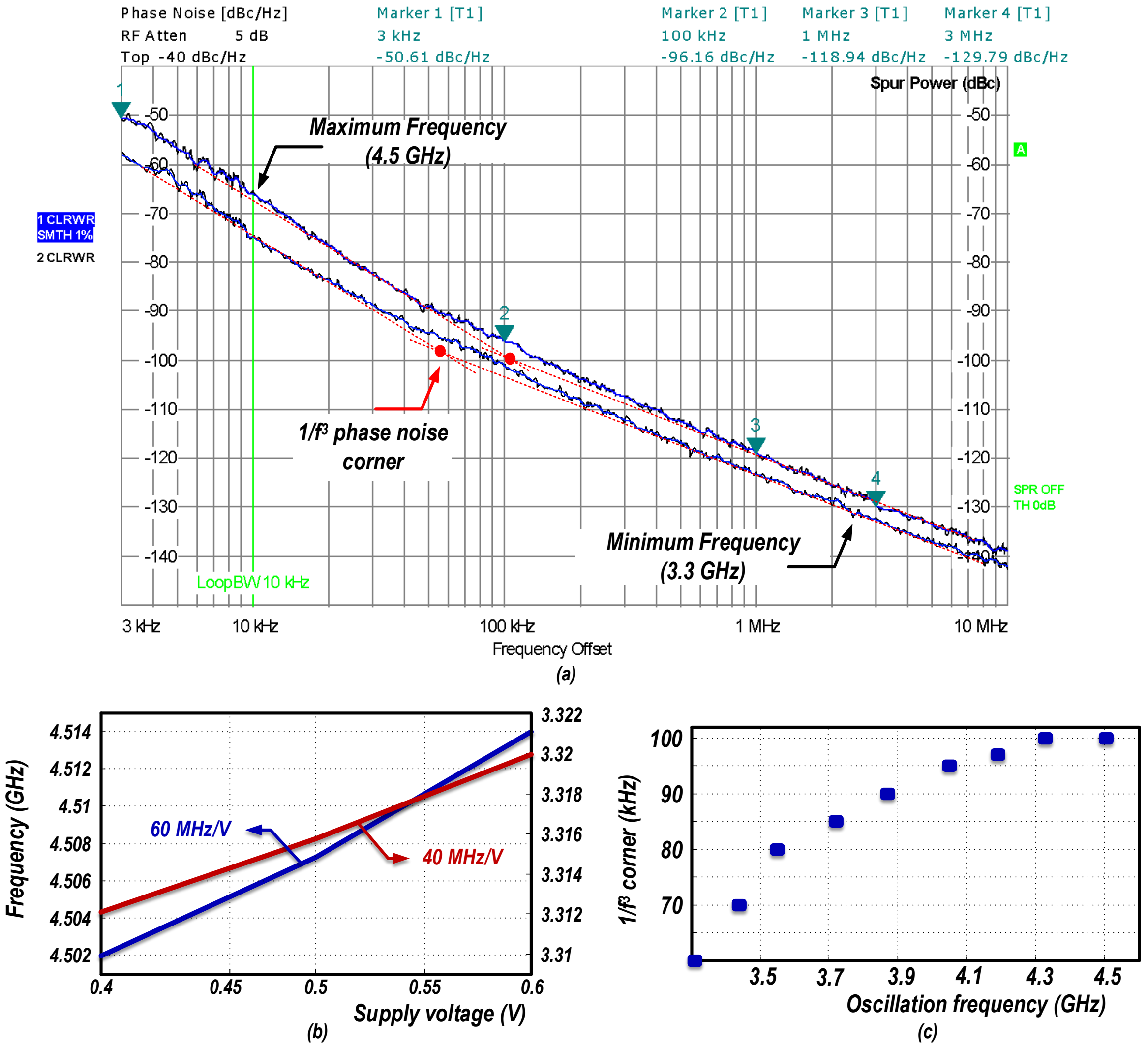


Figure 3.21: Class-D/F$_2$ oscillator: measured (a) PN at f_{max} and f_{min}; (b) frequency pushing due to supply voltage variation; and (c) 1/f^3 corner over tuning range.

(200/0.04)-μm low-V$_t$ devices to ensure start-up and class-D operation over PVT. The chip micrograph is shown in Fig. 3.20(a) with core area of 0.1 mm^2. Figure 3.21(a) shows the measured PN at f_{max} and f_{min} with V_{DD}=0.5 V. Current consumption is 6 mA and 4 mA, respectively. The 1/f^3 corner is 100 kHz at f_{max} and reduces to 60 kHz for f_{min}. The 1/f^3 corner over TR is shown in Fig. 3.21(c). The supply frequency pushing is 60 and 40 MHz/V at f_{max} and f_{min}, respectively (see Fig. 3.21(b)). Table I compares its performance with the original class-D oscillators (as well as two other state-of-the-art oscillators [21] [24] aimed at reducing the 1/f noise upconversion). Compared to the original design, the FoM at 10 MHz offset is degraded in the class-D/F$_2$ oscillator by 3 dB, mainly due to the lack of ultra-thick metal layers, which lowers the inductor's Q. However, even with this degradation, FoM at 100 kHz offset is improved at least 3 dB. 1/f^3 corner is

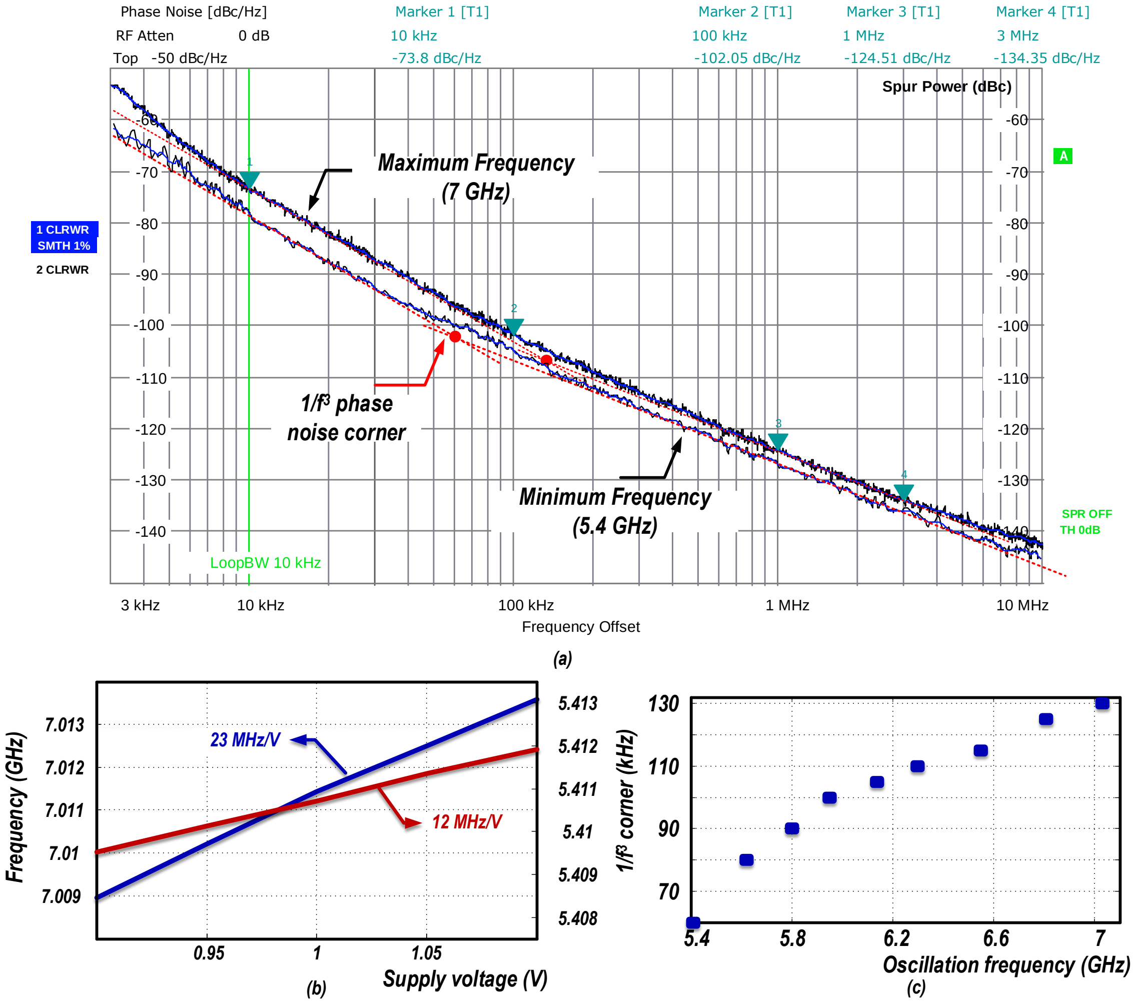


Figure 3.22: Class-$F_{2,3}$ oscillator: measured (a) PN at $f_{\max}$ and $f_{\min}$; (b) frequency pushing due to supply voltage variation; and (c) $1/f^3$ corner over tuning range.

improved at least 10 times versus both class-D and noise-filtering class-D oscillators.

3.4.2 Class-$F_{2,3}$ Oscillator

The class-$F_{2,3}$ oscillator is realized in 40-nm 1P7 CMOS process with ultra-thick metal layer. The 1:2 transformer is constructed with the 3.4 μm top ultra-thick (M7 layer) copper metal. The primary and secondary winding inductances are 0.58 nH and 1.5 nH, respectively, and k_m=0.67. The simulated Q-factors of the primary and secondary windings are 15 and 20 at 6 GHz. Like the class-D/F_2, the L_T inductance has to be compensated with enough decoupling capacitance. The unfiltered part has to be modeled precisely due to the relatively large R_{p2}. The single-ended primary and differential secondary capacitor banks are realized with two 6-bit switchable MOM capacitors, with LSB of 30 fF and 50 fF, respectively. Due to the sensitivity of this oscillator to the frequency mismatch, an 8-bit

Table 3.1: Performance summary and comparison with relevant oscillators.

		Class-D/F_2		Class-D [4]		Noise Filtering Class-D [4]		**Class-$F_{2,3}$**		Class-F_3[5]	[20]	[24]	[29]
Technology		**40 nm**		65 nm		65 nm		**40 nm**		65 nm	65 nm	28 nm	130 nm
Thick metal		**No**		Yes		Yes		**Yes**		Yes	NA	NA	NA
V_{DD} (V)		**0.5**		0.4		0.4		**1**		1.25	1.2	0.9	1.4
Tuning range (%)		**31**		45		45		**25**		25	18	27.2	1.7
Core area (mm^2)		**0.1**		0.12		0.15		**0.13**		0.12	0.08	0.19	0.09
Freq. (GHz)		**f_{min}**	**f_{max}**	f_{min}	f_{max}	f_{min}	f_{max}	**f_{min}**	**f_{max}**	f_{max}	f_{max}	f_{mid}	f_{mid}
		3.3	**4.5**	3	4.8	3	4.8	**5.4**	**7**	7.4	3.6	3.3	2.4
P_{DC} (mW)		**4.1**	**2.5**	6.8	4	6.8	3.6	**12**	**10**	15	0.72	6.8	4.2
PN (dBc /Hz)	100kHz	**-101.2**	**-96.2**	-101	-91	-102	-92.5	**105.3**	**102.1**	-98.5	-94.4	-106	88.4
	1MHz	**-123.4**	**-119**	-127	-119	-128	-121	**126.7**	**124.5**	-125	-114.4	-130	128.4
	10MHz	**-143.4**	**-139**	-149.5	-143.5	-150	-144.5	**146.7**	**144.5**	-147	-134.4	-150	148.4
FoM† (dB)	100kHz	**185.4**	**185.3**	182.2	178.6	183.2	180.6	**189.1**	**188.9**	184.1	187	188.2	189.8
	1MHz	**187.6**	**188**	188.2	186.6	189.2	189.1	**190.5**	**191.4**	190.6	187	192.2	189.8
	10MHz	**187.6**	**188**	190.7	191.1	191.2	192.6	**190.5**	**191.4**	192.6	187	192.2	189.8
$1/f^3$ corner (kHz)		**60**	**100**	800	2100	650	1500	**60**	**130**	700	10	200	<10
Freq. pushing (MHz/V)		**40 @0.5 V**	**60 @0.5 V**	140 @0.5 V	480 @0.5 V	90 @0.5 V	390 @0.5 V	**12 @1V**	**23 @1V**	50 @1.25 V	15 @1.2 V	NA	NA

†$FOM = |PN| + 20\,log_{10}(\omega_0/\Delta\omega) - 10\,log_{10}(P_{DC}/1mW)$

unit-weighted capacitor bank with LSB of 4 fF is also placed at the primary to tune the DM and CM resonance frequencies. The oscillator is tunable between 5.4–7 GHz and the primary and secondary capacitors are changed simultaneously to preserve the class-$F_{2,3}$ operation. The $M_{1,2}$ transistors are (64/0.27) μm thick-oxide devices to tolerate large voltage swings. The tail resistor R_T bank is realized with a fixed 40 Ω resistor in parallel with 7-bit binary-weighted switchable resistors with LSB size of 5 Ω. This bank can tune the oscillation current from 5 to 20 mA. The chip micrograph is shown in Fig. 3.20(b); the core die area is 0.12 mm^2.

Figure 3.22(a) shows the measured PN of the class-$F_{2,3}$ oscillator at f_{max} and f_{min} with V_{DD}=1 V. Current consumption is 10 and 12 mA, respectively. The $1/f^3$ corner is 130 kHz at f_{max} and reduces to ~60 kHz at f_{min}. The $1/f^3$ corner over TR is plotted in Fig. 3.22(c). The supply frequency pushing is 23 and 12 MHz/V at f_{max} and f_{min}, respectively, see Fig. 3.22(b). Table I compares its performance with the original class-F oscillator. Compared to the original design, FoM is degraded about 1–2 dB at the 10 MHz offset, which is due to the tail resistor loading the tank more than the tail transistor originally, thus degrading PN slightly. Despite this degradation, FoM at 100 kHz is enhanced by at least 4 dB, and the $1/f^3$ corner is improved 5 times.

3.5 Conclusion

This chapter presented a technique to reduce a 1/f noise upconversion in a harmonically rich tank current. We showed that when even-order harmonics of the tank current flow into the capacitive part of the tank, they distort the oscillation waveform by making its rise and fall times asymmetric and hence causing the 1/f noise upconversion. Odd-order harmonics also distort the oscillation waveform; however, the waveform in that case is still symmetric and will not result in the 1/f noise upconversion. We proposed to design a ω_0-tank that shows an auxiliary common-mode (CM) resonant peak at $2\omega_0$, which is the main contributor to the 1/f noise upconversion, and showed how oscillation waveform becomes symmetric by the auxiliary resonance. We described how to realize the F_2-tank without the die area penalty, by taking advantage of different properties of inductors and transformers in differential-mode (DM) and CM excitations. Class-D/F_2 and class-$\mathrm{F}_{2,3}$ oscillators employing, respectively, inductor and transformer-based F_2 tanks are designed in 40 nm CMOS to show the effectiveness of our proposed method. The 1/f^3 corner improves 10x in class-D/F_2 and 5x in class-$\mathrm{F}_{2,3}$ versus their original counterparts.

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Chapter 4

A Wide-Tuning-Range DTC-Assisted Fractional-N All-digital PLL

This chapter presents a digital-to-time converter (DTC)-assisted fractional-N all-digital PLL (ADPLL) that utilizes a new wide-tuning-range (WTR) oscillator covering almost an octave[1]. The ADPLL employs a MASH $\Delta\Sigma$ time-to-digital converter (TDC) to achieve low in-band phase noise, and a mode switching wide tuning-range digitally-controlled oscillator (DCO). Fabricated in 40-nm CMOS, the ADPLL consumes 10.7 mW while outputting 1.73 to 3.38 GHz (after a $\div 2$ division) and achieves better than -109 dBc/Hz in-band phase noise and 420 fs_{rms} integrated jitter. A stand-alone WTR oscillator with the same structure is also implemented. It features a 65% tuning range with average FoM of 188 dB.

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[1] Material of this chapter was published at 2016 European Solid-State Circuit Conference (ESSCIRC) [1]. The leader of this project is Ying Wu from TU Delft. The author is *fully* and *solely* responsible for the oscillator and divider and their interfacing with the ADPLL. The rest of the ADPLL was designed by Ying Wu and Yue Chen, both PhD students at TU Delft.

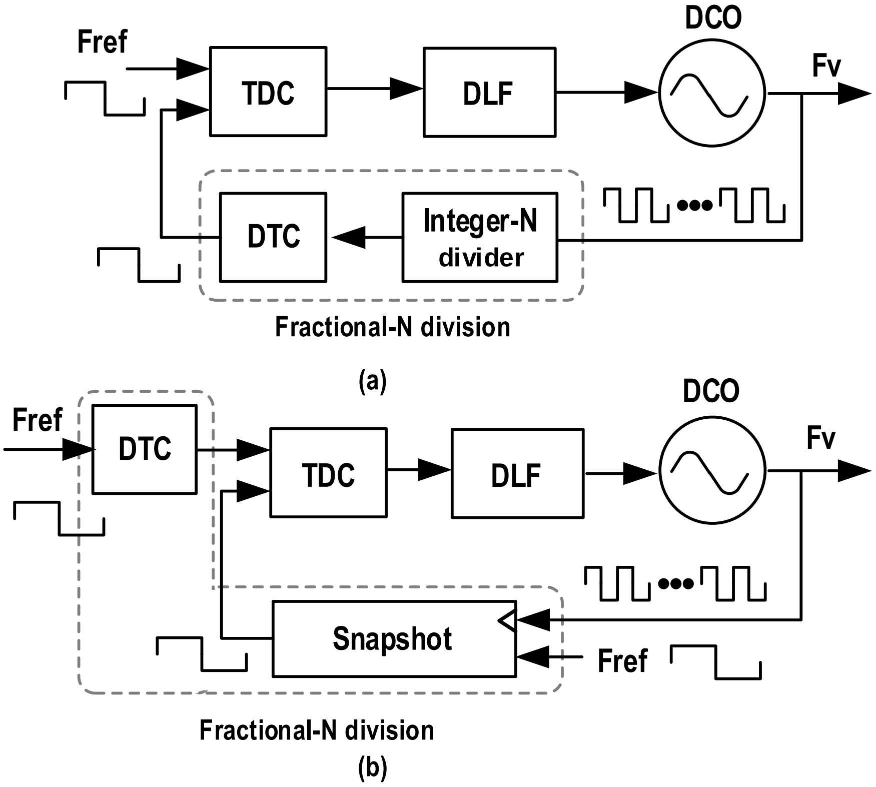


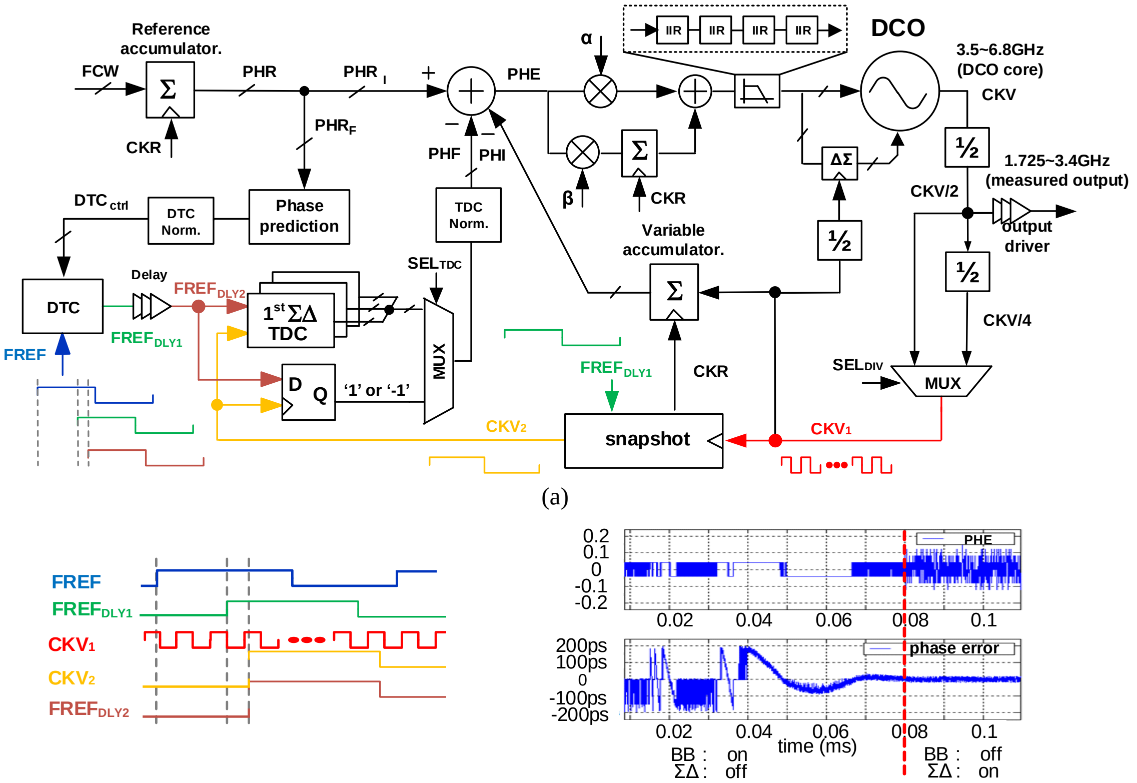
Figure 4.1: DTC assisted ADPLLs with (a) divider; and (b) snapshot.

4.1 Introduction

Fractional-N PLLs are key building blocks in wireless transceivers and many system-on-chips (SoCs). Wide tuning-range offers flexibility in frequency planning and such PLLs are thus well-suited for realizing single-chip multi-standard solutions in wireline/wireless applications. A wide PLL bandwidth is further desirable since it can often improve both system and circuit-level performance.

Analog charge-pump PLLs have been preferred in the past. Nowadays, however, their area and power consumption do not scale well with CMOS technology. By contrast, ADPLLs eliminate the charge pump and use a digital loop filter whose area and power scale down with technology. Furthermore, the loop parameters, as well as other calibration algorithms, are easily implemented with less complexity and more robustness in a digital manner.

Recently, extensive efforts have been spent on digital-to-time converter (DTC)-assisted ADPLLs. Compared to the original ADPLL with a TDC [2], the DTC can be designed more power efficiently and with less hardware complexity. Furthermore, the DTC alleviates the TDC's wide range requirement. Consequently, a simple 1-bit TDC or bang-bang phase


Reference accumulator.
FCW
Σ
CKR
PHR
PHR_I
PHR_F
+
−
PHF
PHI
PHE
α
β
IIR
IIR
IIR
IIR
DCO
3.5~6.8GHz (DCO core)
CKV
½
1.725~3.4GHz (measured output)
output driver
CKV/2
½
CKV/4
ΔΣ
½
Σ
CKR
Variable accumulator.
Σ
DTC ctrl
DTC Norm.
Phase prediction
TDC Norm.
SEL_TDC
DTC
Delay
FREF_DLY2
1st ΣΔ TDC
FREF_DLY1
FREF
D
Q
'1' or '-1'
MUX
FREF_DLY1
CKR
CKV2
snapshot
CKV1
SEL_DIV
MUX
FREF
FREF_DLY1
CKV1
CKV2
FREF_DLY2
0.2
0.1
0
-0.1
-0.2
PHE
0.02
0.04
0.06
0.08
0.1
200ps
100ps
0
-100ps
-200ps
phase error
time (ms)
BB : on
ΣΔ : off
BB : off
ΣΔ : on

(a)

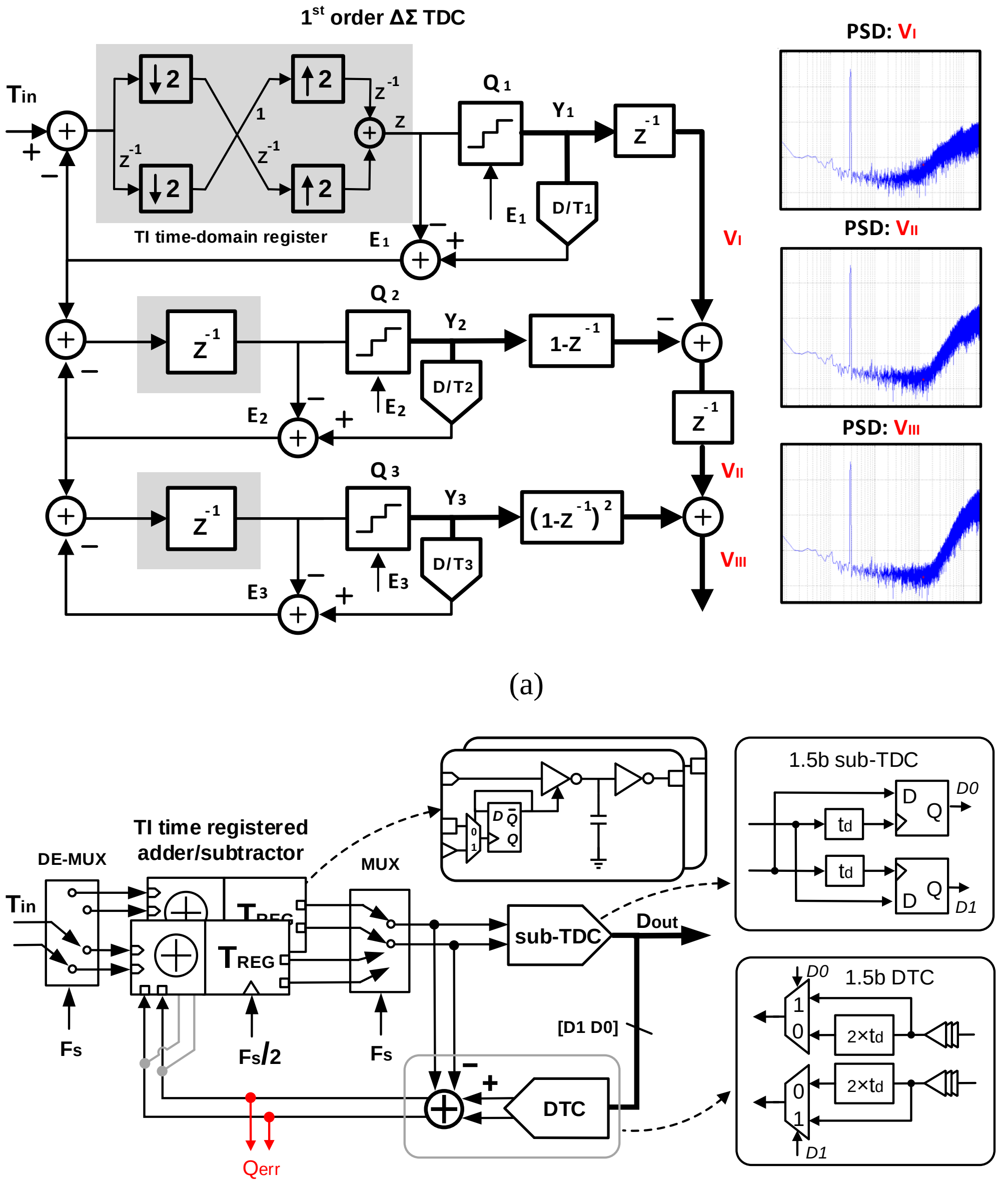
(b)

(c)

Figure 4.2: (a) Block diagram of the proposed ADPLL; (b) the timing of snapshot; and (c) the locking process: from BBPD to ΔΣ TDC.

detector (BB-PD) [3] and a narrow input range time amplifier (TA)-based TDC [4] could be adequate. However, the DTC-BB DPLLs are slower to acquire lock and might easier lose the lock. Also, their in-band phase noise is determined by the resolution of DTC. To achieve such fine resolution will not only increase complexity of the analog-intensive circuits (sensitive to PVT variations) but also consume large power. The DTC-TA ADPLL replaces the BB-PD with a high-resolution TA. It can obtain a very low in-band phase noise but the integrated jitter will be degraded by the poor linearity of TA. Two of the above ADPLLs are implemented as in Fig. 4.1(a). The fractional-N division is realized by combining a DTC with an integer-N divider, but that dissipates more power.

In this chapter, a method which allows snapshot TDC and DTC to be used for fractional-N operation, as shown in Fig. 4.1(b) is presented . The snapshot circuit converts the high RF frequency down to the reference clock rate with simple D-flip-flops and a combinatorial logic [5]. At the same time, the ADPLL achieves low in-band phase noise by using a digital-intensive high-resolution MASH ΔΣ TDC and wide range tuning with a transformer-based tank DCO.


1st order ΔΣ TDC
Tin
↓2
↑2
z-1
1
z
TI time-domain register
Q1
Y1
E1
D/T1
VI
PSD: VI
Q2
Y2
E2
D/T2
1-Z-1
VII
PSD: VII
Q3
Y3
E3
D/T3
(1-z-1)2
VIII
PSD: VIII
DE-MUX
TI time registered adder/subtractor
TREG
MUX
sub-TDC
Dout
[D1 D0]
DTC
Fs
Fs/2
Qerr
1.5b sub-TDC
td
D
Q
D0
D1
1.5b DTC
2×td

(a)

(b)

Figure 4.3: (a) MASH 1-1-1 structure of TDC; (b) architecture of the 1st order ΔΣ TDC.

4.2 Structure of the ADPLL

The system diagram of the proposed ADPLL is shown in Fig. 4.2(a). The key components are the delay-line based DTC, a multi-stage noise-shaping (MASH) ΔΣ TDC, a snapshot circuitry which reduces the input frequency of the TDC to match the reference rate, a digital loop filter (DLF) and a wide tuning-range LC-DCO with low-power ÷2 dividers.

The DTC-assisted ADPLL realizes the fractional-N multiplication by introducing the DTC that dynamically delays the rising edge of FREF to align the delayed reference signal FREFDLY1 with the next rising edge of CKV2. Thus, the TDC only needs to cover one delay unit of DTC's delay cell (16ps here). In practice, some margin is left in case of gain estimation error of the DTC delay line. This dramatically relaxes the dynamic requirement of TDC and makes the TDC with small dynamic range but high absolute resolution feasible. The timing of snapshot is shown in Fig. 4.2(b). The snapshot circuit in the feedback loop works like a D-flip-flop, which samples the FREFDLY1 by high frequency clock CKV1 and it always delays the sampled signal CKV2 behind FREFDLY1. This could cause a problem when the loop is configured in type-II since the averaged phase error between FREFDLY1 and CKV2 (as seen by the TDC) must be equal to zero. Therefore, a delay-line is added between DTC and TDC to compensate for that offset. The extra delay in the loop will not affect the loop stability since it is much smaller than one reference period.

The phase error between FREFDLY2 and CKV2 is limited to tens of pico-seconds when the loop is locked. However, the phase error changes dramatically during the locking process. It certainly exceeds the narrow TDC input range and it could lead to the ADPLL not getting properly locked. To avoid this issue, a BB-PD is used during the locking. The TDC can be switched into the loop after the ADPLL is locked in the type-II configuration. The Fig. 4.2(c) shows the simulated phase error during the BB-PD operation and then when the TDC gets switched in. It is noted that the switching process from BB-PD to TDC is smooth.

The TDC samples the phase error and sends the quantized output into the digital loop filter. The structure of the TDC was adapted from [6]. Three 1st order $\Delta\Sigma$ TDCs can be cascaded in a MASH configuration to realize 1st to 3rd order noise-shaping. When the $\Delta\Sigma$ TDC is applied to the ADPLL, the $\Delta\Sigma$ shaped quantization noise will not degrade in-band phase noise because the ADPLL bandwidth is narrower than that of $\Delta\Sigma$ TDC. Furthermore, the 4th order IIR filter can also effectively eliminate the far-out $\Delta\Sigma$ quantization noise.

The DCO with nearly 2:1 tuning range allows the ADPLL to have an almost continuous frequency coverage. The multiplexer on the feedback path selects either $\div 2$ or $\div 4$ divided DCO clock fed as CKV1 to the high speed variable accumulator. The reference and high speed variable accumulators can be turned off after the ADPLL is locked since the phase error then varies only within a few degrees of the RF cycle.

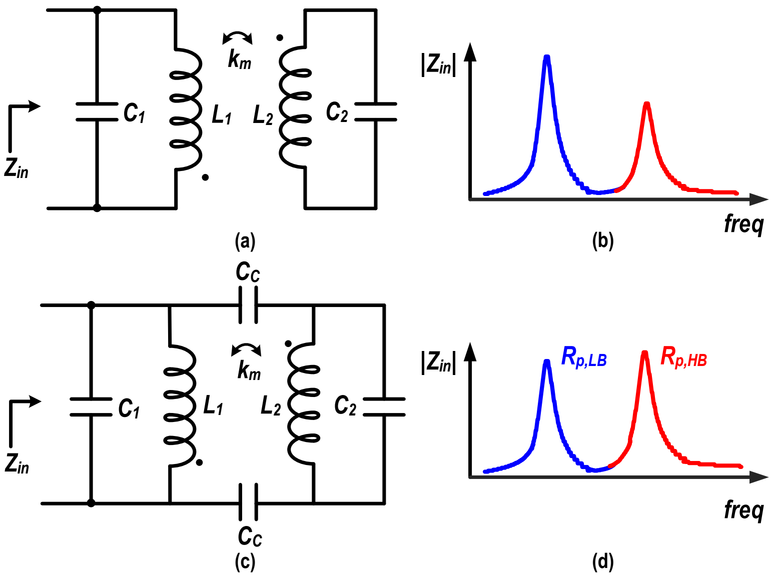


Figure 4.4: (a) Transformer based tank; and (b) its input impedance; (c) capacitively coupled transformer based tank; and (d) its input impedance.

4.3 Circuit Implementation

4.3.1 Implementation of MASH ΔΣ TDC

As the loop bandwidth of ADPLLs has been steadily increasing, the in-band phase noise now becomes the key performance limitation. In this work, the ΔΣ oversampling technique is applied to push the territory of TDC resolution to the device noise, such as flicker/thermal noise, which is generally much lower than the quantization noise.

The block diagram of the MASH ΔΣ TDC is shown in Fig. 4.3(a). The ΔΣ TDC, realized as a 1st order error-feedback topology can be cascaded in a MASH 1-1-1 configuration to realize a 3rd order noise-shaping without any stability concerns. A time-interleaved (TI) time-domain register, which is equal to the unit delay z^{-1}, is implemented in the ΔΣ loop to provide the trade-off between speed and accuracy.

Fig. 4.3(b) shows further details of the 1st order ΔΣ TDC in the error-feedback configuration. It consists of a TI time registered adder/subtractor, a 1.5-bit sub-TDC and a 1.5-bit DTC. The TI time registered adder/subtractor is implemented using two parallel identical units. Each of them consists of 2-parallel tristate inverters, capacitors and controlling circuitry. The tristate inverters convert the input time difference to voltages on capacitors when the tristate inverters are switched to a high impedance state. The delayed addition/subtraction is realized when the tristate inverters are changed to an active state. The ΔΣ TDC runs at its full speed FS, which is equal to the reference clock of ADPLL, while the de-multiplexer delivers the input samples to the 2-parallel time

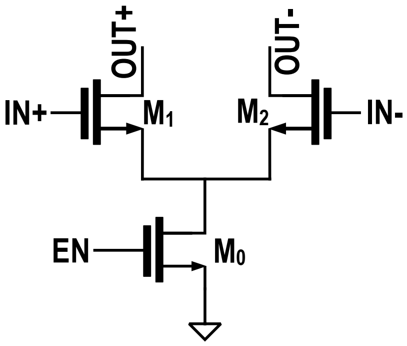


Figure 4.5: Differential trans-conductance schematic.

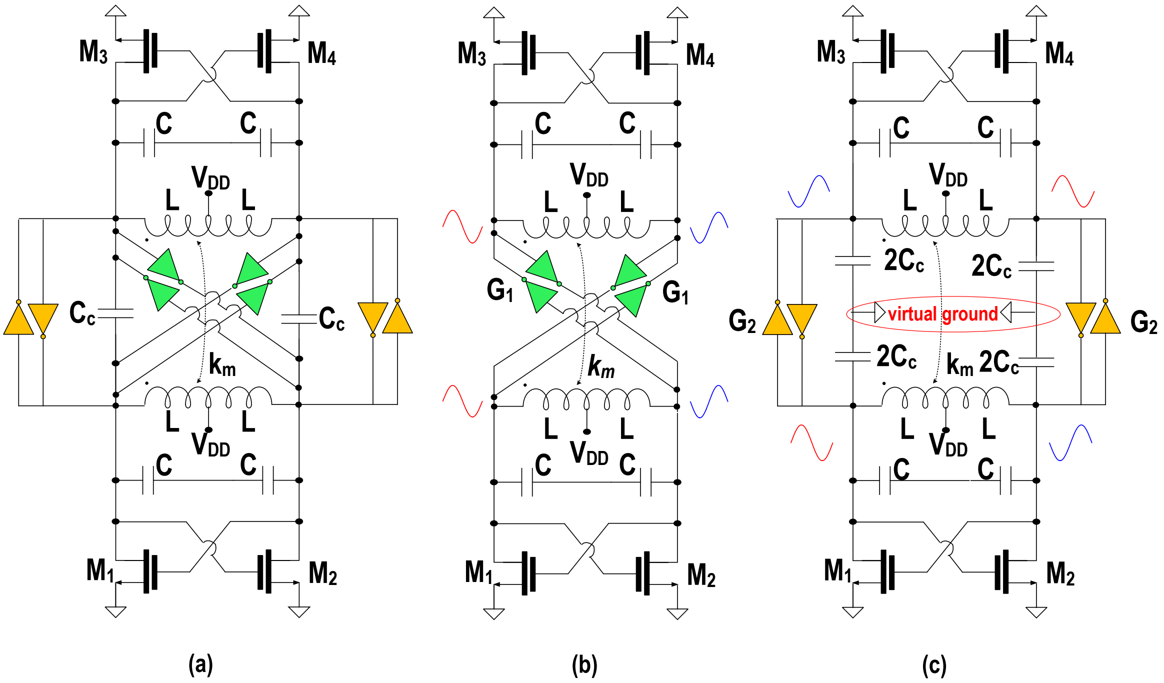


Figure 4.6: (a) Simplified schematic of DCO; (b) DCO operates in HB; and (c) LB.

registered adders/sub-tractors whose operation frequency is reduced to FS/2. Then, the multiplexer sequentially selects the output of each channel to obtain FS, that is, the full rate output. A 1.5-bit sub-TDC with resolution of 2xtd (64 ps) is used to ease the possible stability issues caused by the out-of-range residues from the preceding stage DTC.

4.3.2 Implementation of Wide Tuning-Range DCO

Nowadays, the oscillator design for multi-mode multi-band cellular applications demands wide tuning range (TR) while ensuring low phase noise (PN) for a range of bands and channels. Poor Q-factor of the switched-capacitor networks for the wide TR limits the oscillator's PN. LC-tank oscillators are preferred, if not outright necessary, over

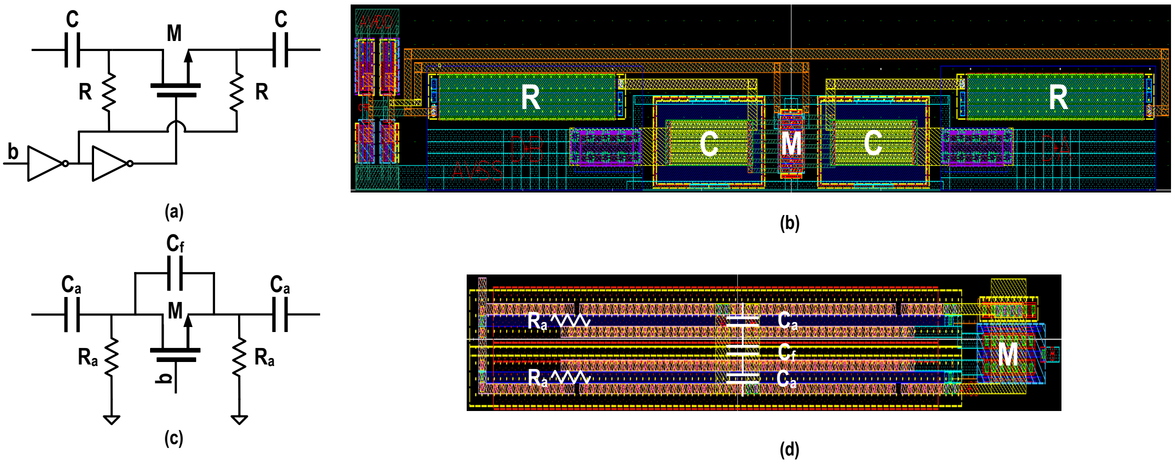


Figure 4.7: (a) Schematic; and (b) layout of the LSB of the PVT capacitor bank. (c) Schematic; and (d) layout of the unit cell of acquisition and tracking capacitor bank.

inverter-based ring oscillators (which are naturally wide TR) for cellular applications because of their superior PN.

One technique to widen the oscillator TR is to replace the tank's inductor with a transformer. The input impedance of the transformer-based tank, shown in Fig. 4.4(a), has a fourth-order polynomial denominator and exhibits two resonant frequencies [7],

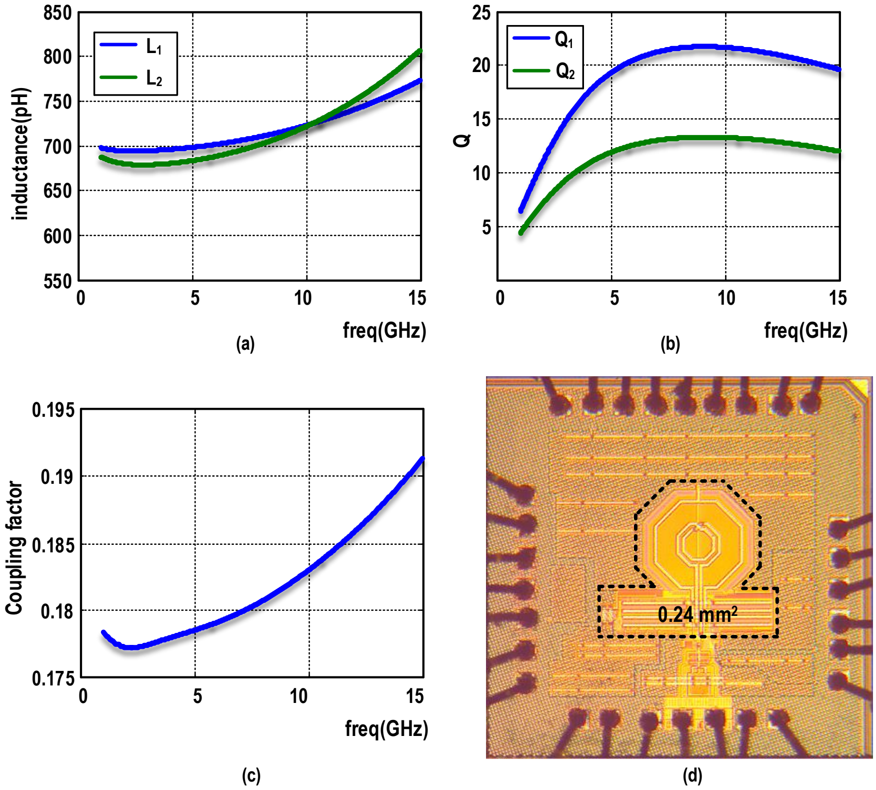
$$\omega_{L,H}^2 = \frac{1 + X \pm \sqrt{(1+X)^2 - 4X\left(1-k_m^2\right)}}{2\left(1-k_m^2\right)}\omega_2^2 \tag{4.1}$$

where $\omega_1^2 = \dfrac{1}{L_1C_1}$, $\omega_2^2 = \dfrac{1}{L_2C_2}$ and $X = \dfrac{L_2C_2}{L_1C_1}$. The oscillator built around the transformer tank can be chosen to excite at either ω_L or ω_H at a time in order to expand its tuning range. However, the difference in impedances of these two resonances, see Fig. 4.4(b), is likely to result in a large PN performance gap between these two modes.

The transformer tank can also be capacitively coupled, as shown in Fig 4.4(c). Two sides of the transformer can be forced to oscillate either in-phase or 180° out-of-phase with the help of four switches (see Fig. 4.6(a)) [8]. In a high-frequency band (HB), the oscillation is in-phase and so the coupling capacitors C_C cannot be seen. Assuming $L_1 = L_2 = L$ and $C_1 = C_2 = C$ [8],

$$\omega_{HB} = \frac{1}{\sqrt{(1-k_m)LC}} \tag{4.2}$$

However, if the two sides of the transformer are forced to oscillate out-of-phase, there



(a) (b) (c) (d)

Figure 4.8: (a) Inductance; and (b) quality factor of the transformer's primary and secondary winding. (c) The coupling factor. (d) Chip micrograph.

will be a virtual ac ground at the middle of C_C, as shown in Fig. 4.6(c). Therefore, the oscillator is switched to the low-frequency band (LB). The output frequency is obtained as follows [8]:

$$\omega_{LB} = \frac{1}{\sqrt{(1+k_m)L(C+C_C)}} \tag{4.3}$$

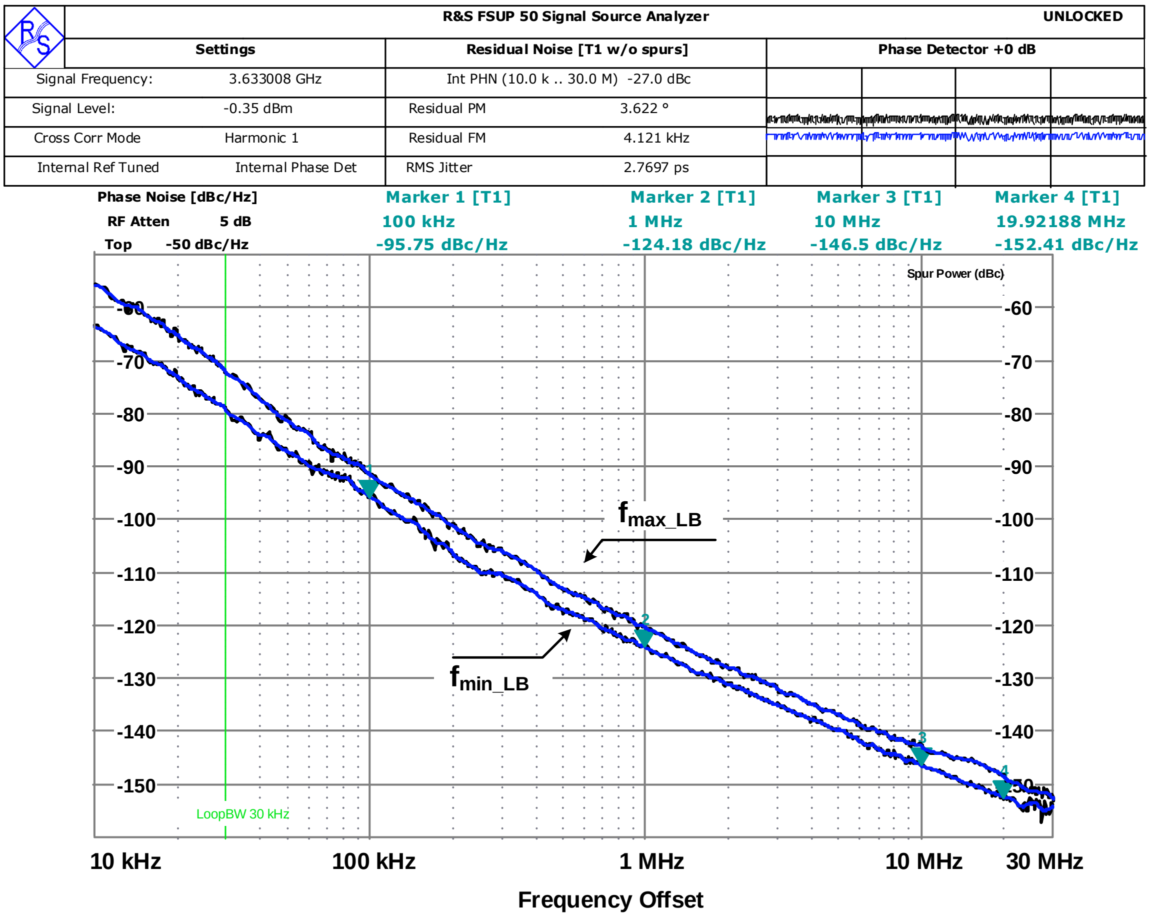
where C_C is the coupling capacitance between the two windings. Both C_C and a low coupling factor k_m of the transformer ensure that the separation between the high-band and low-band has no gaps but is as narrow as practically possible.

The equivalent parallel resistance of the two modes of the resonators can be found as [8],

$$R_{p,HB} \approx \frac{(1-k_m)\,L}{C \cdot r_s} \tag{4.4}$$

$$R_{p,LB} \approx \frac{(1+k_m)\,L}{(C+C_c) \cdot r_s} \tag{4.5}$$

in which r_s is the equivalent series resistance of the primary and secondary inductances (they are assumed to be the same in order to simplify the analysis). These four design parameters, k_m, C_C, C and L, are used to design an oscillator with a continuous tuning



R&S FSUP 50 Signal Source Analyzer				UNLOCKED
Settings		Residual Noise [T1 w/o spurs]		Phase Detector +0 dB
Signal Frequency:	3.633008 GHz	Int PHN (10.0 k .. 30.0 M)	-27.0 dBc	
Signal Level:	-0.35 dBm	Residual PM	3.622 °	
Cross Corr Mode	Harmonic 1	Residual FM	4.121 kHz	
Internal Ref Tuned	Internal Phase Det	RMS Jitter	2.7697 ps	

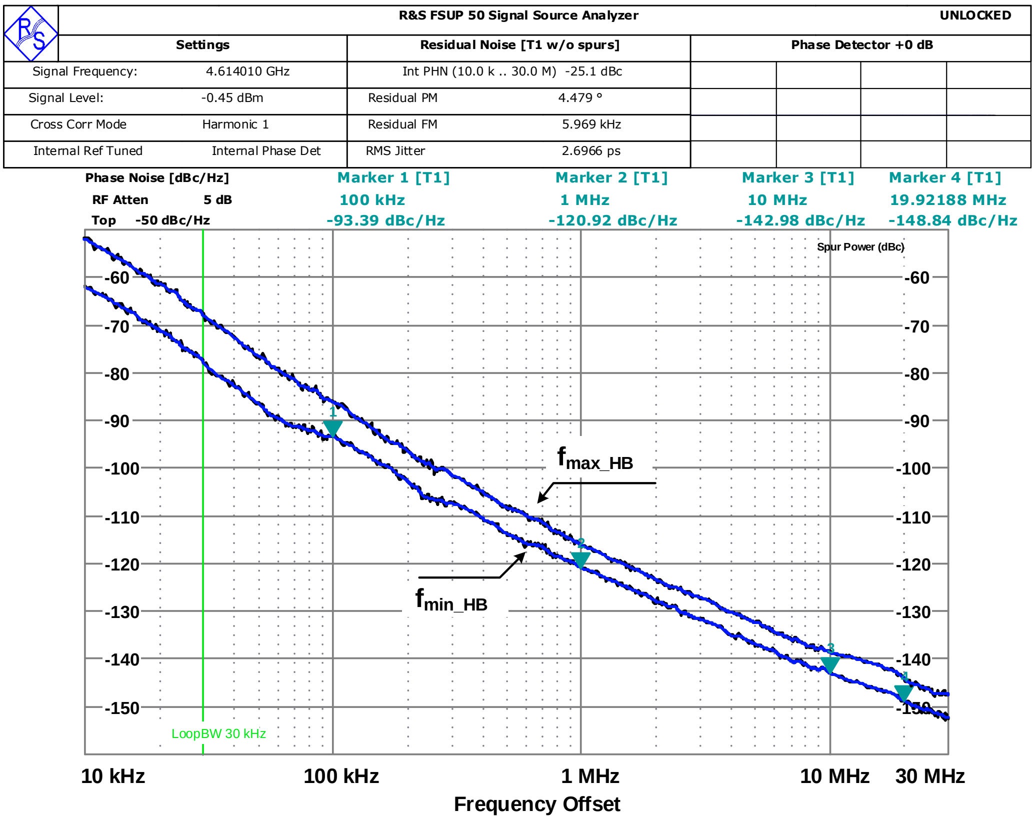
Phase Noise [dBc/Hz]		Marker 1 [T1]	Marker 2 [T1]	Marker 3 [T1]	Marker 4 [T1]
RF Atten	5 dB	100 kHz	1 MHz	10 MHz	19.92188 MHz
Top	-50 dBc/Hz	-95.75 dBc/Hz	-124.18 dBc/Hz	-146.5 dBc/Hz	-152.41 dBc/Hz

Figure 4.9: PN of the odcillator in the LB.

range that also ensures some frequency overlap between the oscillation modes, while making possible $R_{p,HB} \approx R_{p,LB}$ [see Fig. 4.4(d)] to ensure the balanced performance throughout the entire tuning range.

The coupled tank resonates at one of these modes (bands) depending on the state of G_1 and G_2 trans-conductances [see Fig. 4.6(a)]. When G_1's are on and G_2's are off, two sides of the tank oscillate at the same phase. In the opposite state, G_1's are off and G_2's are on, so the two sides of the resonator oscillate out-of-phase. In order to avoid the HB/LB frequency gap in face of component tolerances and mismatches, C_C and k_m are chosen to provide a certain level of the frequency overlap and also to assure the consistent phase noise performance [8]. The trans-conductances are designed as differential cells, as shown in Fig. 4.5.

Since this oscillator is designed to be incorporated in an ADPLL, it should contain various switched-capacitor banks. The same 7-bit binary PVT capacitor banks are employed at both windings of the transformer to coarse tune the output frequency.



R&S FSUP 50 Signal Source Analyzer				UNLOCKED			
Settings		Residual Noise [T1 w/o spurs]		Phase Detector +0 dB			
Signal Frequency:	4.614010 GHz	Int PHN (10.0 k .. 30.0 M)	-25.1 dBc				
Signal Level:	-0.45 dBm	Residual PM	4.479 °				
Cross Corr Mode	Harmonic 1	Residual FM	5.969 kHz				
Internal Ref Tuned	Internal Phase Det	RMS Jitter	2.6966 ps				

Phase Noise [dBc/Hz]	Marker 1 [T1]	Marker 2 [T1]	Marker 3 [T1]	Marker 4 [T1]
RF Atten 5 dB	100 kHz	1 MHz	10 MHz	19.92188 MHz
Top -50 dBc/Hz	-93.39 dBc/Hz	-120.92 dBc/Hz	-142.98 dBc/Hz	-148.84 dBc/Hz

Figure 4.10: PN of the odcillator in the HB.

However, for fine tuning, the unit weighted acquisition and tracking capacitor banks are incorporated only on the primary winding for area considerations. This is at the expense of unbalanced oscillation amplitude and PN degradation. However, the total capacitance of the acquisition and tracking banks, $C_a + C_t$, is about $4C_{LSB,PVT}$ (in the ADPLL version of the oscillator) and so the drop in PN is not more than 1dB. The oscillator employs 64 unit-weighted cells for both the acquisition and tracking banks. The schematic and layout of the unit cells of these capacitor banks are shown in Fig. 4.7. The tracking bank resolution is desired to be very fine; consequently a fixed capacitor C_f is paralleled with the switch to substantially decrease C_{on}/C_{off} [5] (see Fig. 4.7(c)). However the smallest available MOM capacitor is still much coarser than the value required for the finest resolution. Hence, a custom made capacitor is designed to satisfy the required resolution of this fine bank.

A stand-alone oscillator is also designed to measure the oscillator without the loop to verify the resolution, tuning range and phase noise performance of the oscillator. In this stand-alone oscillator, 9-bit unit-weighted acquisition and tracking banks are designed to validate the tank resolution. The DCO tank employs a transformer with L=700 pH and

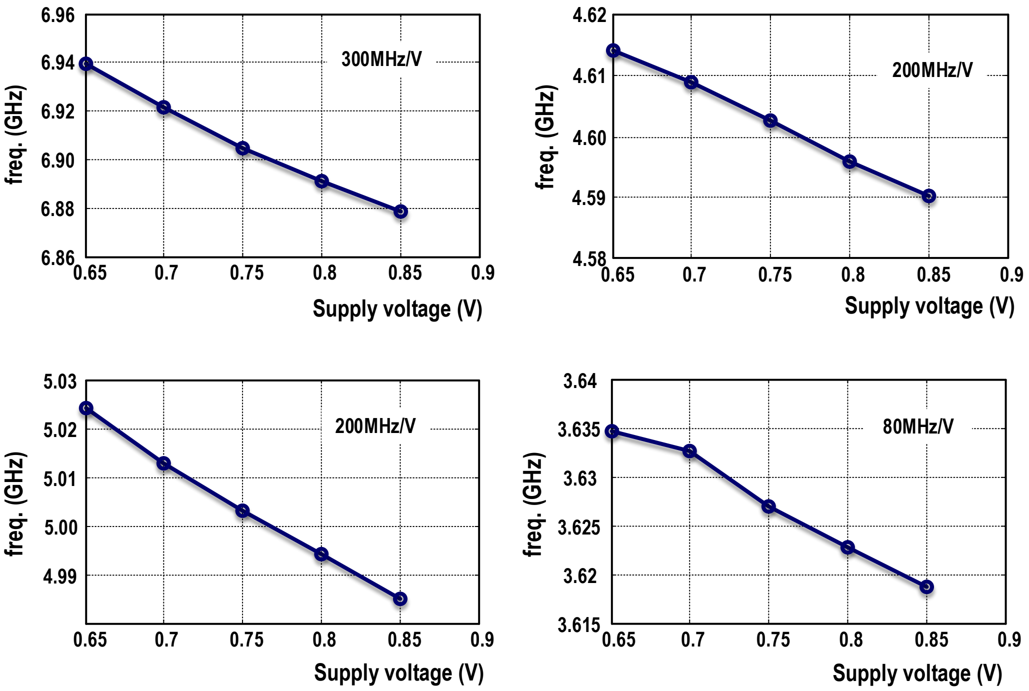


Figure 4.11: Oscillation frequency dependency on supply voltage for different frequency bands.

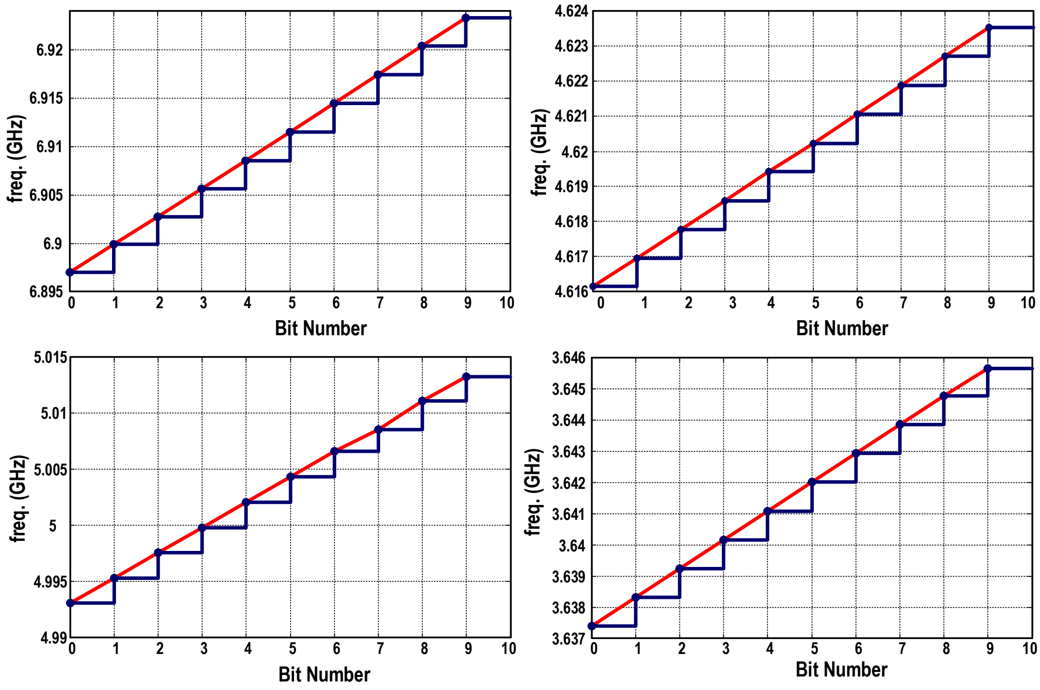


Figure 4.12: Acquisition bank linearity for different frequencies.

k_m=0.18. The transformer characteristics and chip micrograph are shown in Fig. 4.8.

The stand-alone oscillator is designed in a 40-nm 1P7M CMOS process technology. V_{DD} is chosen to be 0.65 V. The oscillation frequency was measured 3.6–5.02 GHz (32% tuning range) in LB an 4.6–6.94 GHz (40% tuning range) in HB, resulting in total of 65% tuning range. The PN performance at f_{max}, f_{mid}, and f_{min} in LB and HB modes is

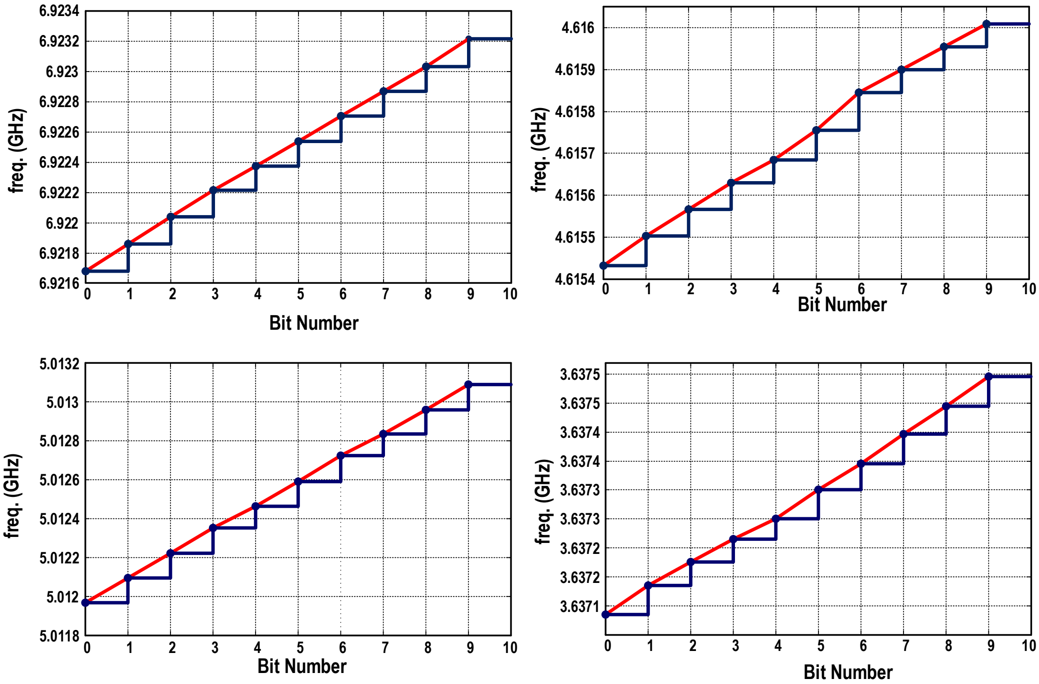


Figure 4.13: Tracking bank linearity for different frequencies.

shown in Fig. 4.9 and Fig. 4.10, respectively.

Sources of the M_1–M_4 transistors are connected to ground. Consequently, the tank's higher current harmonics are relatively powerful. In agreement with our discussion in Chapter 3, the 1/f^3 corner is therefore relatively large. For the same reason, the measured frequency pushing is also relatively high, as shown in Fig. 4.11.

The custom-designed acquisition and tracking banks are proven to be quite linear. The oscillation frequency vs. the acquisition and tracking tuning codes are shown in Fig. 4.12 and Fig. 4.13, respectively.

4.4 ADPLL Measurements Results

The ADPLL is realized in 40-nm CMOS and occupies an active area of 0.5 mm^2. It is powered by 0.65 V, 0.8 V and 1.1 V supplies. The 0.65 V supply is used for the DCO core. The digital logic supply is reduced to 0.8 V to save the power. The DTC, TDC and other blocks are supplied at 1.1 V. At a 50 MHz reference and 4 GHz DCO, the power consumption is 10.7 mW, where the DTC and TDC consume 0.5 mW and 1.2 mW (all 3-stage $\Delta\Sigma$ TDCs are enabled), respectively. The power consumption of DCO is 8 mW. All other blocks and digital parts consume 1 mW. The chip micrograph is shown in Fig. 4.14 As shown in Fig. 4.15(b), the ADPLL output frequency tuning spans from 1.73 GHz to 3.38 GHz, which is 64.6% fractional vs. 66.7% needed for the continuous

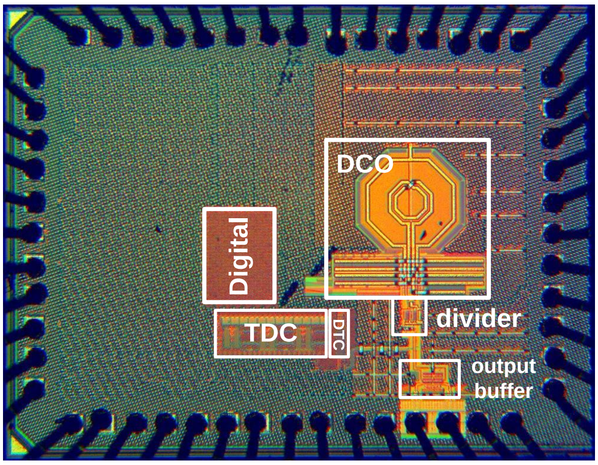


Figure 4.14: Chip micrograph of the proposed ADPLL.

Table 4.1: Performance summary and comparison with state-of-the-art.

	This work	JSSC'11 [2]	JSSC'15 [3]	ISSCC'12 [4]
Scheme	DTC-ΔΣ	DTC-BB	DTC-TA	DTC-FH
Technology	40nm	65nm	65nm	40nm
F_{ref} [MHz]	50	40	50	32
F_{RF} [GHz]	3.5 - 6.8	2.9 - 4	4.4 - 5.2	2.1 – 2.7
Tuning range	64.6%	31.9%	17%	25%
Bandwidth [MHz]	0.8	0.31	0.75	0.2
Inband PN [dBc/Hz] *	-109	-106	-109	-92
$Jitter_{rms}$ [ps]	0.42	0.56	0.49	1.71
Power [mW]	10.7	4.5	3.7	0.86
Area [mm^2]	0.5	0.22	0.22	0.2
FoM_J [dB] **	-237	-238	-240	-236
FoM_{IBPN} [dB] ***	-285	-285	-287	-280

* *Normalized to* 2*GHz*

** $FoM_J = 10\log[(\sigma_{rms}/1s)^2 \times Power/1mW]$.

*** $FOM_{IBPN} = IBPN + 10\log[(1Hz/f_{out})^2 \times Power/1mW]$.

frequency coverage. Note that, as mentioned in section 4.3.2, in order to avoid the DCO's tuning discrepancy between HB and LB the frequency overlap should be guaranteed. As shown in spectrum, the maximum frequency of LB is 2.35 GHz, which is 70 MHz higher than HB's minimum frequency of 2.28 GHz.

The phase noise was measured with Rohde&Schwartz FSUP50 spectrum analyzer. It is shown in Fig. 4.15(a) for the output carrier of 2 GHz. For comparison, both the fractional-N and integer-N frequencies are superimposed. There is just a little degradation in the fractional-N mode. The in-band phase noise reaches -109 dBc/Hz and -111 dBc/Hz in fractional-N and integer-N mode, respectively. The integrated jitter from 1 kHz to 30 MHz is 420 fs and 350 fs, respectively. The measured spur level and integrated jitter are

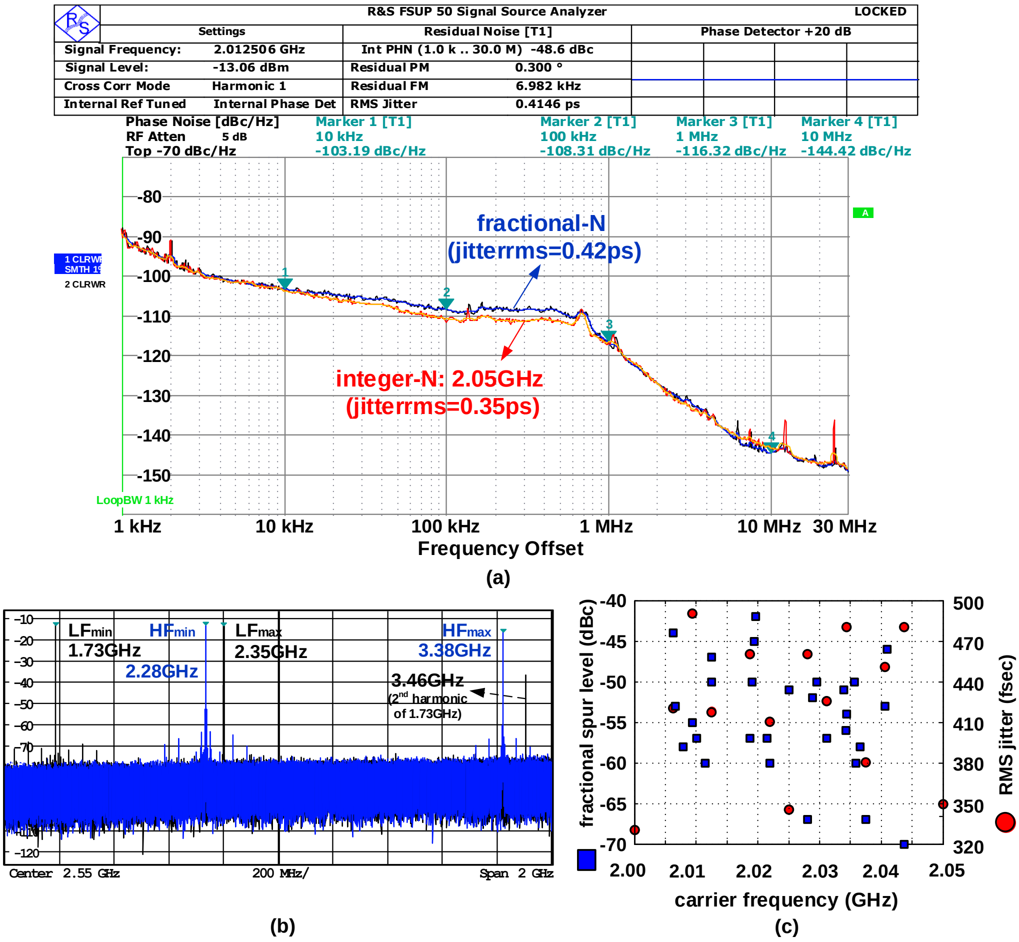


Figure 4.15: (a) Measured phase noise; (b) spectrum of output frequency; and (c) spur level and integrated jitter across channels away from integer-N at 2.00 GHz.

shown in Fig. 4.15(c). The worst case in-band fractional spur is -42 dBc. The integrated jitter spans between 330 fs and 490 fs depending on the FCW.

The performance summary of the proposed ADPLL and comparison with state-of-the-art DTC-based DPLLs are shown in Table I. It is worth noting that the FoM of this ADPLL is almost the same as [3] and [4] but it has much wider tuning range.

4.5 Conclusion

This chapter presents a wide tuning-range DTC-assisted fractional-N ADPLL with MASH $\Delta\Sigma$ TDC that is suitable for modern wireless and wireline standards. The proposed ADPLL, implemented in 40-nm CMOS, achieves -109 dBc/Hz in-band phase noise and 420 fs$_{rms}$ integrated jitter. The ADPLL consumes 10.7 mW while generating 1.73 GHz to 3.38 GHz output (after ÷2 division) using 50 MHz reference with a loop bandwidth of

800 kHz. The wide tuning-range oscillator is also implemented as a standalone chip in 40-nm CMOS and achieves 65% tuning range and average FoM of 188 dB with an active area of 0.25 mm^2.

This chapter is unique in the sense that it covers the application of oscillators and the realization of our WTR oscillator within an ADPLL. To be effective at the system level, the oscillator needs to support fine frequency steps thus acting as a digitally controlled oscillator (DCO).

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Chapter 5

Tuning range extension of an oscillator through CM resonance

In this chapter, we introduce a method to broaden a tuning range of a CMOS LC-tank oscillator without sacrificing its area[1]. The extra tuning range is achieved by forcing a strongly coupled transformer-based tank into a common-mode resonance at a much higher frequency than in its main differential-mode oscillation. The oscillator employs separate active circuits to excite each mode but it shares the same tank, which largely dominates the core area but is on par with similar single-core designs. The tank is forced in common-mode oscillation by two injection locked Colpitts oscillators at the transformer's primary winding, while a two-port structure provides differential mode oscillation. An analysis is also presented to compare the phase noise performance of the dual core oscillator in common-mode and differential-mode excitations. A prototype implemented in digital 40-nm CMOS verifies the dual mode oscillation and occupies only 0.12 mm^2 and measures 56% tuning range.

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[1] Material of this chapter has been accepted on October 19, 2016 for publication at IEEE Transaction of Circuits and Systems I (TCAS-I).

5.1 Introduction

Oscillator design for multi-mode multi-band (e.g., Fourth Generation (4G) cellular) applications demands wide tuning range (TR) while ensuring sufficiently low phase noise (PN) for a range of targeted frequency bands. The maximum achievable TR of a traditional single-core LC-tank oscillator is limited at 35–40% by a $C_{\mathrm{on}}/C_{\mathrm{off}}$ capacitance tuning ratio of its switched-capacitor network, further constrained by large size of its switches needed to prevent deterioration of the LC-tank's quality (Q)-factor. For example, the Q-factor of a switched-capacitor network in a 40-nm technology is about 80 at 4 GHz resonant frequency when $C_{\mathrm{on}}/C_{\mathrm{off}} = 2$. For an inductor's Q-factor of 15 at this frequency, the tank's equivalent Q-factor reduces to 12.6.

The most straightforward solution seems to be designing two *separate* oscillators [1] [2] at the expense of large area, and the need for high-frequency source-selecting multiplexers, which increase power consumption and noise floor. A system-level local oscillator (LO) solution in [3] uses a single 40 GHz oscillator followed by a ÷2 divider and an LC-tank mixer to generate 20 and 30 GHz LO signals. However, the extra mixer costs significant power and area as well as it produces spurs. Another attempt is to decrease the area of a *two-core* oscillator by placing one inductor underneath the other [4] [5]. However, the top inductor has to be very large so the other one can be placed at its center without degrading the top inductor's quality factor. Therefore, the oscillator area is still considerably larger than that of a single-tank oscillator.

Employing switched resonator tanks, in which the tank's inductance is controlled by turning on/off interconnecting switches, is another TR expanding technique [6]– [11]. However, the switches' resistance limits the tank's Q-factor, thus degrading the oscillator PN [12]. Transformer based dual-band oscillators [13] [14] offer wide but not continuous tuning range. A switched-shielded transformer [15] is another method to increase the oscillator's tuning range but it appears effective only at mm-wave frequencies. A shielded inductor [16] with a shorting switch is inserted between two windings of a transformer [15]. The coupling factor between the windings changes as to whether the current is flowing in the shielded inductor or not. This transformer is not large, however, its inductors' quality factor gets compromised. Consequently, this range-increasing technique is interesting for mm-wave applications where the tank's quality factor is rather limited by the capacitive part; however for the single-GHz RF frequencies the degradation of the tank's Q-factor would seem to be excessive.

Recent works on mode-switching oscillators significantly improve the PN vs. TR

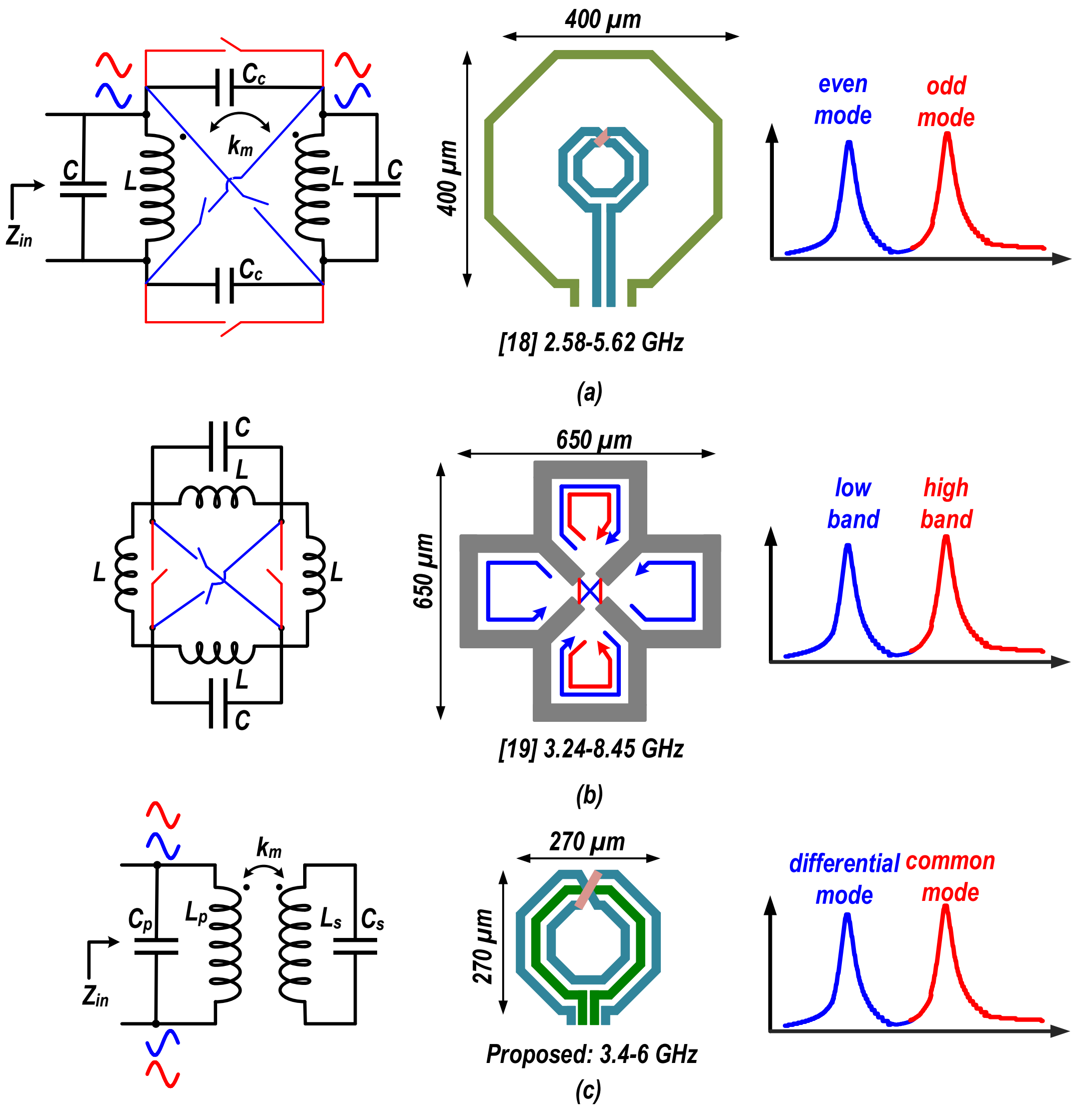

C_c
k_m
C
L
Z_{in}
C_c
400 μm
400 μm
even mode
odd mode
[18] 2.58-5.62 GHz
(a)
C
L
650 μm
650 μm
low band
high band
[19] 3.24-8.45 GHz
(b)
k_m
C_p
L_p
L_s
C_s
Z_{in}
270 μm
270 μm
differential mode
common mode
Proposed: 3.4-6 GHz
(c)

Figure 5.1: LC-tanks for wide tuning range: (a) resonant mode switching technique [18]; (b) band switching technique [19]; (c) proposed technique.

trade-off [17] [18] [19], however, they *do not* improve the TR vs. die area trade-off. For example, Li et al. [18] switches between resonant modes (even/odd) of two capacitively and magnetically coupled LC resonators, as shown in Fig. 5.1(a). Strong magnetic coupling enhances the difference between the two resonant frequencies; hence, a continuous TR extension calls for a low coupling factor, such that the transformer ends up to be quite large. Unfortunately, the recent CMOS technology nodes (28 nm and, to a lesser extent, 40 nm) have brought about very tough minimum metal-density requirements, therefore, the inductors and transformers should be filled with a lot of dummy metal pieces [20]. This has negative consequences on inductors as resistive losses due to eddy currents in the dummy fills degrade the Q-factor. And, that is in addition to increasing the parasitic capacitance, thus narrowing the TR. The losses are even more severe in the weakly coupled transformers. The spacing between their primary and secondary windings is larger [see Fig. 5.1(a)] and must be filled with dummy metal pieces, but it is precisely where the magnetic flux is concentrated the most.

In Taghivand et al. [19], as shown in Fig. 5.1(b), four identical inductors are coupled through four mode-switching transistors, providing two oscillation bands. In a *low-band* oscillation mode, there is no AC current flow possibility in two of these inductors [see Fig. 5.1(b)], however in a *high-band* mode, the AC current can flow in all the inductors. Thus, the effective inductance value in each band could be controlled. Obviously, the four inductors significantly increase the area.

Considering that not all applications require as stringent PN performance as does cellular wireless, we concentrate in this chapter on maintaining the die area similar to that of a single LC-tank oscillator, while significantly improving the TR and keeping a reasonable PN performance. The proposed single-tank oscillator employs a strongly coupled transformer-based tank and forces the tank to oscillate either in a differential mode (DM) or common mode (CM), see Fig. 5.1(c). The DM oscillation provides the TR equivalent of a single-tank oscillator. The TR is then *extended* by the CM oscillation. The oscillator has two separate active circuits to excite each mode. However, since the passive part is shared in both modes, the die area is comparable to that of a typical narrow TR oscillator.

Section 5.2 describes how the transformer-based tank can exhibit both DM and CM resonances. Section 5.3 describes a circuit implementation of the two-core oscillator that excites one of these resonances at a time. Section 5.4 shows measurement results.

5.2 Common Mode Resonances

A transformer-based tank, depicted in Fig. 5.2(a), exhibits two DM resonant frequencies. If this transformer possesses a strong magnetic coupling factor, k_m, its leakage inductance would be small and so the second DM resonant frequency would be much higher than the main one. Consequently, we would not get a continuous extension of the TR by forcing the oscillation at the second DM resonant frequency. On the other hand, in order for the transformer size to be not much larger than that of an inductor, $k_m > 0.6$ appears a necessary condition. With this constraint, the first resonance can be estimated as [22]:

$$\omega_{0,DM} \approx \frac{1}{\sqrt{L_p C_p + L_s C_s}}, \tag{5.1}$$

where, L_p and C_p are primary, and L_s and C_s are secondary windings' inductances and capacitances. The approximation error of (5.1) from the exact resonant frequency (Eq. (5) in [22]) is less than +6% for $k_m \geq 0.7$.

Abandoning the hope of exploiting the second DM resonance, suppose now this tank is excited by CM signals, and, for now, we assume primary and secondary winding inductances and k_m are similar in DM and CM excitations. CM signals cannot see the differential capacitors, thus the tank can only exhibit CM resonances when these capacitors are single-ended. If this tank were to employ only single-ended primary and *differential* secondary capacitors, the secondary winding inductances and capacitances would not affect the CM characteristics of the tank, e.g., resonant frequency. This tank will show a single CM resonance at

$$\omega_{0,CM} \approx \frac{1}{\sqrt{L_p C_p}}. \tag{5.2}$$

The difference between the CM and DM resonance frequencies, i.e., Eqs. (5.2) and (5.1), suggests a new possibility for extending the tuning range toward higher frequencies, provided we can build an oscillator around this transformer-based tank that can excite it with either DM or CM signals, without adding any bulky passive components. To investigate how much tuning range we can expect from a single tank, we assume the tank employs a switched capacitor bank with a 2:1 capacitance switching ratio:

$$C_{p,max}/C_{p,min} = C_{s,max}/C_{s,min} = 2, \tag{5.3}$$

This ratio should guarantee a sufficiently high Q-factor of switched-capacitors in recent CMOS technologies. With this assumption, $f_{max}/f_{min} = \sqrt{2}$ in both modes, and thus, both DM and CM resonant frequencies (Eqs. (5.1) and (5.2)) will tune by $2(\sqrt{2}-1)/(\sqrt{2}+1)$ = 34.3%. To avoid any gaps between the DM and CM tuning ranges, at least $\omega_{CM,low} = \omega_{DM,high}$. Hence,

$$L_p C_{p,max} = L_s C_{s,max} \tag{5.4}$$

With these conditions, the resonant frequency could theoretically cover an octave while going from DM to CM oscillations. Practically, C_{max}/C_{min} has to be >2 due to parasitics and difficulty with controlling the precise overlap between the DM and CM resonances.

One limiting factor in the tuning range of such an oscillator is the single-ended parasitic capacitance throughout the secondary winding side. If the CM coupling factor, $k_{m,c}$, were hypothetically similar to the DM one, $k_{m,d}$; and $k_{m,c} = k_{m,d} > 0.6$, then the CM resonance would shift down to $\omega_{0,CM} = 1/\sqrt{L_p C_p + L_s C_{s,c}}$, where $C_{s,c}$ is the total of single ended

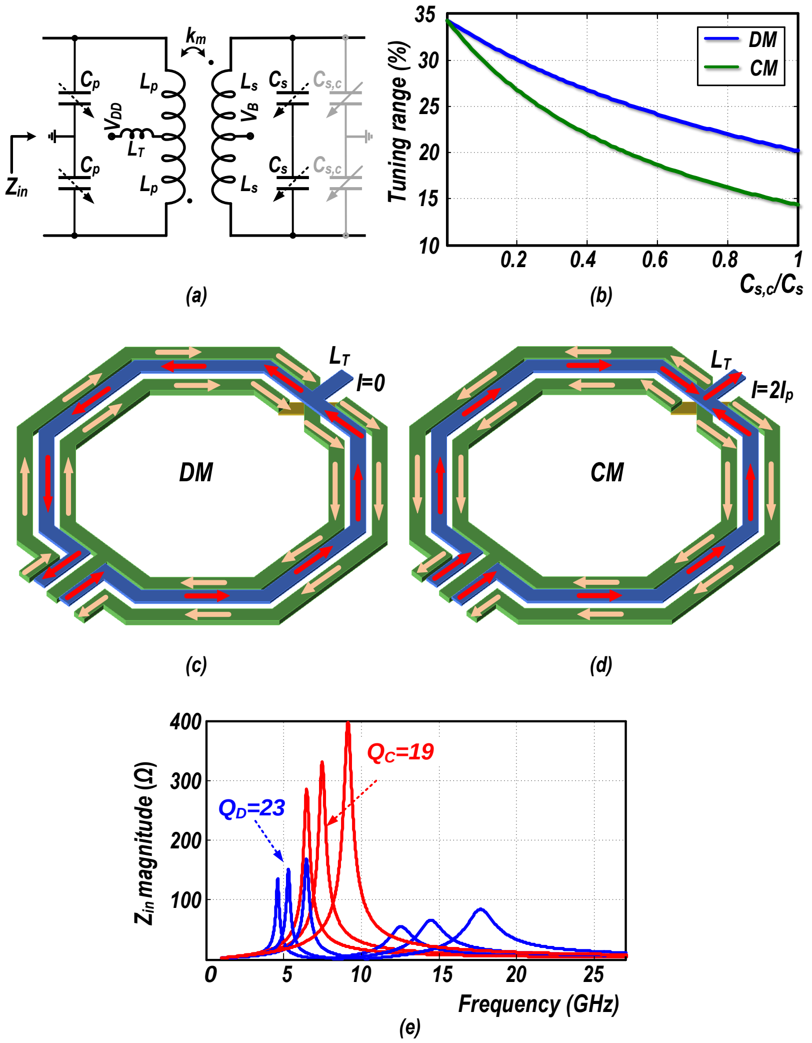

k_m
C_p
L_p
V_{DD}
L_T
Z_{in}
L_s
V_B
C_s
$C_{s,c}$
(a)
Tuning range (%)
35
30
25
20
15
10
0.2
0.4
0.6
0.8
1
$C_{s,c}/C_s$
DM
CM
(b)
L_T
I=0
DM
(c)
L_T
I=2I_p
CM
(d)
Z_{in} magnitude (Ω)
400
300
200
100
0
5
10
15
20
25
Frequency (GHz)
Q_C=19
Q_D=23
(e)

Figure 5.2: (a) a transformer-based tank; (b) limited DM and CM TR due C_s, c; 1:2 turn transformer: (c) DM excitation; (d) CM excitation; and (e) tank's input impedance.

capacitances on the secondary side, Fig. 5.2(a). At the same time, the DM resonance would also shift down to $\omega_{DM} = 1/\sqrt{L_pC_p + L_sC_s + L_sC_{s,c}}$. Interestingly, satisfying the overlap between CM and DM oscillations with the condition in (5.3) results in the same constraint as (5.4). However, the fixed parasitic capacitance, $C_{s,c}$, degrades the CM oscillation tuning range more than it degrades the DM oscillation tuning range, see Fig. 5.2(b).

A 1:2 turns-ratio transformer, which has distinctly different characteristics in DM and CM excitations, relieves such a degradation. Figures 5.2 (c) (d) show this transformer when its primary is excited, respectively, with DM or CM signals. In the DM excitation, the induced currents at the two sides of the secondary winding circulate constructively in the same direction, thus creating a strong coupling factor between the transformer windings, while in the CM excitation these induced currents cancel each other within each full turn of the secondary winding (i.e., from the secondary's terminal to the secondary's

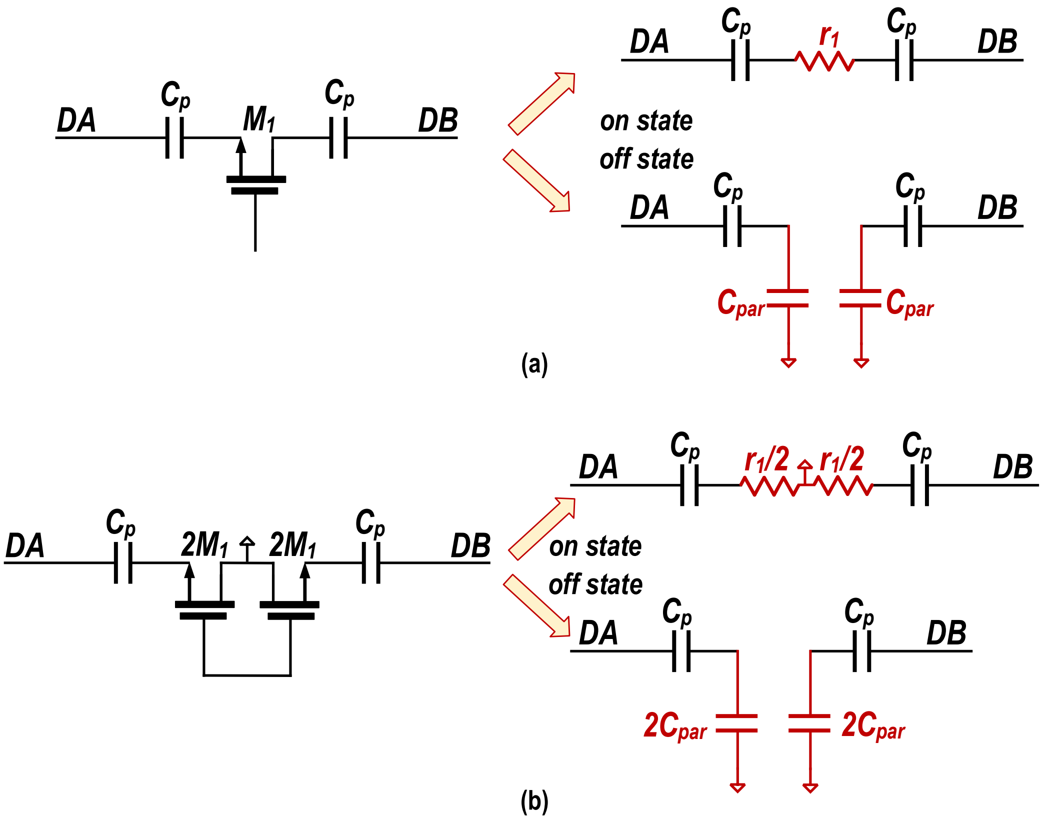


Figure 5.3: (a) Differential and (b) single ended capacitor banks.

center-tap), leading to a weak coupling factor [21]. This weak $k_{m,c}$ can be interpreted as the secondary winding not being seen from the primary and, therefore, the secondary's single-ended capacitors have an insignificant effect on the tank's CM resonant frequency.

Assuming the capacitor bank is almost ideal, at least compared to the lossy inductors represented by the r_p and r_s equivalent series resistances of the primary/secondary windings, CM resonance has the quality factor of $Q_{CM}{=}Q_p{=}L_p\omega/r_p$, which is similar to that of an inductor-based tank. The high Q-factor of this resonance indicates that with an appropriate active circuitry, the CM oscillation of a reasonable quality would be possible. The DM and CM input impedances of this tank are shown in Fig. 5.2 (e). The single-ended switched capacitors require two switches to provide a ground connection in the middle, which results in a 50% lower Q-factor as compared to a differential switched capacitor with the same switch size. This would appear as a disadvantage of our proposed technique; however, that is not the case. Let us compare the tuning range of a typical inductor-based tank oscillator employing the differential capacitor bank with our transformer-based tank oscillator employing the single-ended primary and the differential secondary capacitor banks. The equivalent capacitance of this bank varies from

$C_{\mathrm{on,D}} = C_p$ to $C_{\mathrm{off,D}} = \dfrac{C_p C_{par}}{C_p + C_{par}}$, where C_{par} is the parasitic capacitance of the switch (see Fig. 5.3(a)). For a typical $C_{\mathrm{off,D}}/C_{\mathrm{on,D}}$ value of 0.5 ($C_{par} = C_p$), the inductor-based oscillator employing this tank would exhibit $f_{max}/f_{min} = \sqrt{2}$.

The width of each switch in the single-ended switched-capacitor bank should be twice the width of each differential counterpart for the same Q-factor. Consequently, $C_{\mathrm{off,C}} = \dfrac{2C_p C_{par}}{C_p + 2C_{par}} = \dfrac{2}{3}C_p$, (see Fig. 5.3(b)). Employing this capacitor bank in a transformer-based tank at the primary winding and employing the differential bank at the secondary winding, and benefiting from the impedance transformation of the 1:2 turns-ratio transformer ($L_s/L_p \approx 3$), results in $\dfrac{f_{max}}{f_{min}} = \sqrt{1.9}$, which is very close to the inductor-based tank tuning range.

5.3 Proposed Wide Tuning Range Oscillator

5.3.1 Dual-Core Oscillator

Forcing the transformer-based tank to resonate in DM is quite straightforward. The oscillator can be realized as a one-port or a two-port structure [23] [24]. However, only the two-port structure will guarantee a reliable start-up at the first DM resonance [22], thus preventing the mixed DM oscillation. A separate active circuit is now needed to force the tank into the CM resonance. Colpitts and Hartely topologies are two well known examples of single-ended oscillators. Invoking our ground principle of sharing the *same* tank by the active CM and DM circuits, the Coplitts structure is consequently chosen. To improve the PN, two mutually injection-locked Colpitts oscillators share the primary inductor. The schematic of the proposed dual core oscillator is shown in Fig. 5.4(a). To avoid the dual oscillation, only one active circuit core is turned on at a time.

The left side of Fig. 5.4(a) is the two-port DM oscillator. In this mode, $V_{B2} = V_{B3} = 0V$, M_7 switch is on biasing $M_{1,2}$, while M_8 switch is off. The waveforms are shown in Fig. 5.5 (a) (b). The transformer has the 1:2 turns ratio and its gain reduces the $M_{1,2}$ noise up-conversion to PN, and also results in a larger gate voltage compared to drain voltages, which facilitates oscillation start up.

The right-hand side of the oscillator schematic are two locked single-ended Colpitts oscillators. M_8 switch is now turned on to ensure the in-phase operation of the two Colpitts oscillators, without which the two cores might exhibit an arbitrary phase shift. In this mode, $V_{B1} = 0V$ to turn off the differential oscillation. M_7 switch is also off to minimize the CM inductive loading on the primary winding by the secondary one. Both

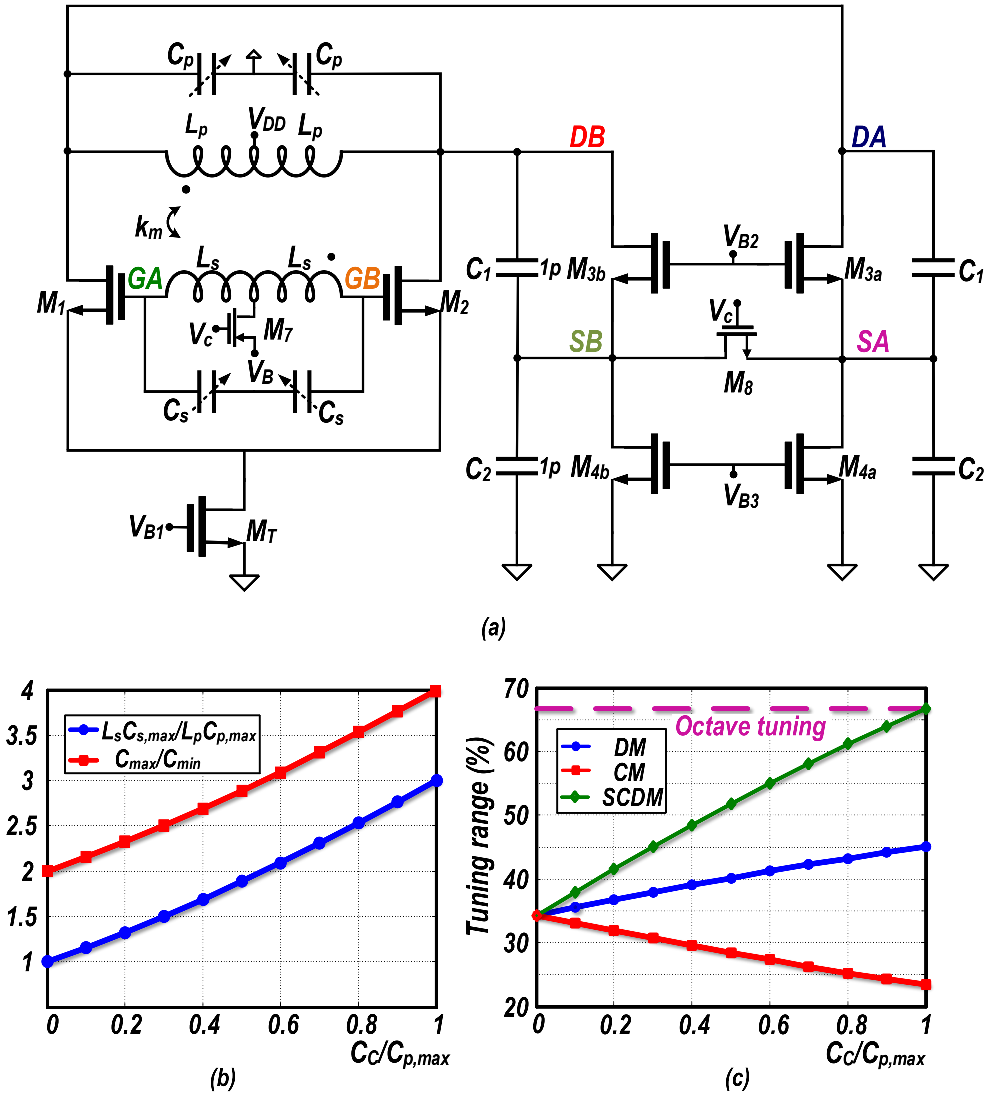

Cp
Cp
Lp
VDD
Lp
km
Ls
Ls
GA
GB
M1
M2
Vc
M7
VB
Cs
Cs
VB1
MT
DB
DA
C1
1p
M3b
VB2
M3a
C1
Vc
SB
SA
M8
C2
1p
M4b
VB3
M4a
C2
(a)
4
3.5
3
2.5
2
1.5
1
0
0.2
0.4
0.6
0.8
1
LsCs,max/LpCp,max
Cmax/Cmin
Cc/Cp,max
(b)
70
60
50
40
30
20
Tuning range (%)
Octave tuning
DM
CM
SCDM
0
0.2
0.4
0.6
0.8
1
Cc/Cp,max
(c)

Figure 5.4: Dual core oscillator: (a) schematic; (b) overlap and octave oscillation conditions; and (c) tuning range.

single-ended oscillators start at the same frequency but could be slightly out of phase; subsequently, they lock to each other and there is no phase shift between them. The locking of the two oscillators gives an additional 3 dB PN improvement. Waveforms are shown in Fig. 5.5 (c) (d).

Note that an attempt of simplifying the CM structure by removing M_8 and permanently shorting the sources of M_3 transistors would be detrimental to the DM tuning range. While obviously the DM oscillation would still work – M_3 transistors are off in this mode – the extra capacitance C_{fix} due to the CM circuitry seen by C_p would be larger. With M_8 off, DA/DB node sees $C_{fix} = C_1C_2/(C_1 + C_2)$, but when M_3 sources are shorted, that capacitance raises to $C_{fix} = C_1 > C_1C_2/(C_1 + C_2)$. Furthermore, an attempt of moving M_8 from the SA/SB source nodes of M_3 to the DA/DB drain nodes would likewise increase the effective parasitic capacitance of M_8.

The C_1 and C_2 capacitors are necessary to create a negative resistance for the Colpitts oscillators; however, they are limiting the tuning range in both modes. In their presence, (5.3) and (5.4) are not valid anymore for the overlap and octave tuning. Assuming the same capacitance variation range on the primary and secondary sides, $C_{p,max}/C_{p,min} = C_{s,max}/C_{s,min}$, the octave tuning requirement is now

$$\frac{L_s C_{s,max}}{L_p C_{p,max}} = 3\frac{C_C}{C_{p,max}} + 4\frac{C_{p,min}}{C_{p,max}} - 1, \tag{5.5}$$

where, $C_C = C_1C_2/(C_1 + C_2)$. The minimum overlap condition, $f_{DM,max} = f_{CM,min}$, dictates

$$\frac{C_{p,max}}{C_{p,min}} = 1 + \frac{L_s C_{s,max}}{L_p C_{p,max}}. \tag{5.6}$$

Figure 5.4(b) shows how the required C_{max}/C_{min} increases with C_C/C_p ratio. Satisfying (5.6) and (5.5) in the presence of C_C also unbalances the DM and CM tuning range, as shown in Fig. 5.4 (c). For a certain value of C_C, the required $C_{p,max}/C_{p,min}$ ratio can become prohibitively large, likely leading to the Q-factor degradation. In practice, $C_{s,max}/C_{s,min}$ and $C_{p,max}/C_{p,min}$ should not be necessarily equal. The secondary-winding capacitor ratio in this design is chosen to be larger than at the primary side, due to the tougher Coplitts oscillator start-up conditions.

5.3.2 Phase Noise Analysis

Ideally, a wide TR oscillator would have a comparable PN performance in both oscillation modes. In this section, we investigate the PN of the dual core oscillator and then compare the two modes.

The linear time-variant model [26] suggests,

$$\mathcal{L}\left(\Delta\omega\right) = 10\log_{10}\left(\frac{kT}{R_t N q_{max}^2 (\Delta\omega)^2}\cdot F\right), \tag{5.7}$$

where, k is Boltzmann's constant, T is temperature, R_t is the equivalent parallel resistance of the tank, and q_{max} is the maximum charge displacement across the equivalent capacitance in parallel to R_t. N is the number of resonators, which is 2 here in both DM and CM oscillators. F, the oscillator's effective noise factor, is

$$F = \sum_i \frac{N\cdot R_t}{2kT}\cdot\frac{1}{2\pi}\int_0^{2\pi}\Gamma_i^2\left(\phi\right)\overline{i_{n,i}^2(\phi)}\,d\phi, \tag{5.8}$$

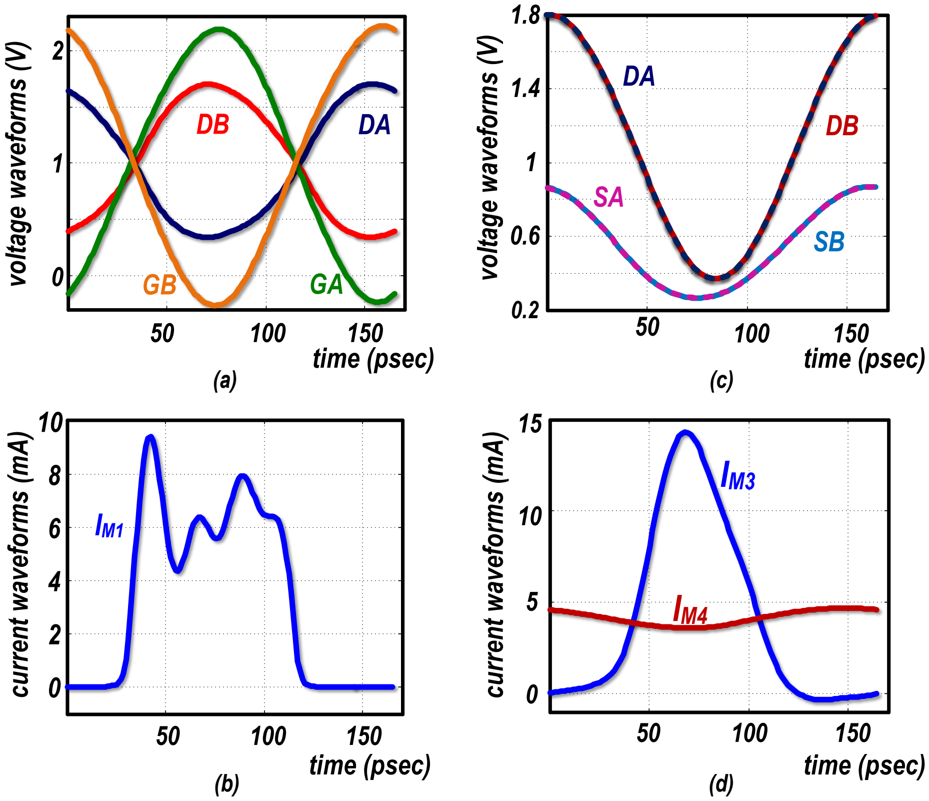


Figure 5.5: Dual core oscillator waveforms: (a)(b) DM; and (c)(d) CM.

in which Γ_i is the ISF of the i^{th} noise source. The relevant ISF of noise sources associated with a sinusoidal waveform oscillator can be estimated by a $\pi/2$ phase shifted sinusoidal function, $\Gamma = \dfrac{sin(\phi)}{N}$, where $\phi = \omega_0 t$ [25]. In this work, we try to find the noise factors of different noise sources in the dual core oscillator.

The noise sources of the Colpitts oscillator are R_t, M_3 and M_4. R_t in the CM oscillation is the parallel resistance of the primary winding, R_p. It is insightful to refer every noise source and nonlinearity back to the tank, as it is demonstrated step-by-step in Fig. 5.6. The negative conductance between DA and SA nodes is

$$g_n = \frac{i_{d3}}{v_{DA} - v_{SA}} = \frac{-g_{m3} v_{SA}}{v_{DA} - v_{SA}} = -g_{m3}\frac{C_1}{C_2} \tag{5.9}$$

where, i_{d3} is the small-signal drain current of M_3. The equivalent negative conductance in parallel with the tank is found as

$$G_n = \left(\frac{C_2}{C_1 + C_2}\right)^2 \cdot g_n = -g_{m3}\frac{C_1 C_2}{(C_1 + C_2)^2} \tag{5.10}$$

With a similar derivation, M_3 channel resistance is referred to the tank as

$$R_{ds3} = r_{ds3}\left(\frac{C_1+C_2}{C_2}\right)^2 \tag{5.11}$$

To sustain the oscillation, the average dissipated power in the tank loss and R_{ds3} should be equal to the average power delivered by the negative resistance, which leads to the condition:

$$G_{mEF3} = \frac{1}{n(1-n)}\cdot\frac{1}{R_p} + \frac{1-n}{n}\cdot G_{dsEF3}, \tag{5.12}$$

where, $n = C_1/(C_1+C_2)$, $G_{mEF} = G_m[0] - G_m[2]$, and $G_{dsEF} = G_{ds}[0] - G_{ds}[2]$, in which $G_m[k]$ and $G_{ds}[k]$ are the k^{th} Fourier coefficients of $g_m(t)$ and $g_{ds}(t)$, respectively [27]. The required G_{mEF3} is minimized for $n = 0.5$, which is chosen in this design to facilitate start-up.

To refer the current noise sources to the tank, they are first converted to their Thevenin voltage source equivalents and then converted back to Norton current source equivalents, as demonstrated in Fig. 5.6(b) and (c). The equivalent noise of M_3 and M_4's transconductance then becomes

$$\overline{i_{n3}^2} = 4kT\gamma g_{m3}\left(\frac{C_2}{C_1+C_2}\right)^2, \tag{5.13}$$

$$\overline{i_{n4}^2} = 4kT\gamma g_{m4}\left(\frac{C_1}{C_1+C_2}\right)^2, \tag{5.14}$$

where γ is the transistor excess noise coefficient. Assuming a sinusoidal oscillation, the tank noise factor is found as

$$F_t = \frac{2N}{2kTR_p}\cdot\frac{1}{2\pi}\int_0^{2\pi}\frac{4kT}{R_p}\frac{\sin^2(\phi)}{N^2}\,d\phi = 1. \tag{5.15}$$

M_3 and M_4 noise factors are found as

$$F_{gm3} = \frac{2NR_p}{4kT\pi}\int_0^{2\pi}\frac{\sin^2(\phi)}{N^2}4kT\gamma g_{m3}(\phi)\cdot\left(\frac{C_2}{C_1+C_2}\right)^2 d\phi = (1-n)^2\gamma G_{mEF3}R_P \tag{5.16}$$

$$F_{gds3} = \frac{2NR_p}{4kT\pi}\int_0^{2\pi}\frac{\sin^2(\phi)}{N^2}4kT\gamma g_{ds3}(\phi)\cdot\left(\frac{C_2}{C_1+C_2}\right)^2 d\phi = (1-n)^2 G_{dsEF3}R_p \tag{5.17}$$

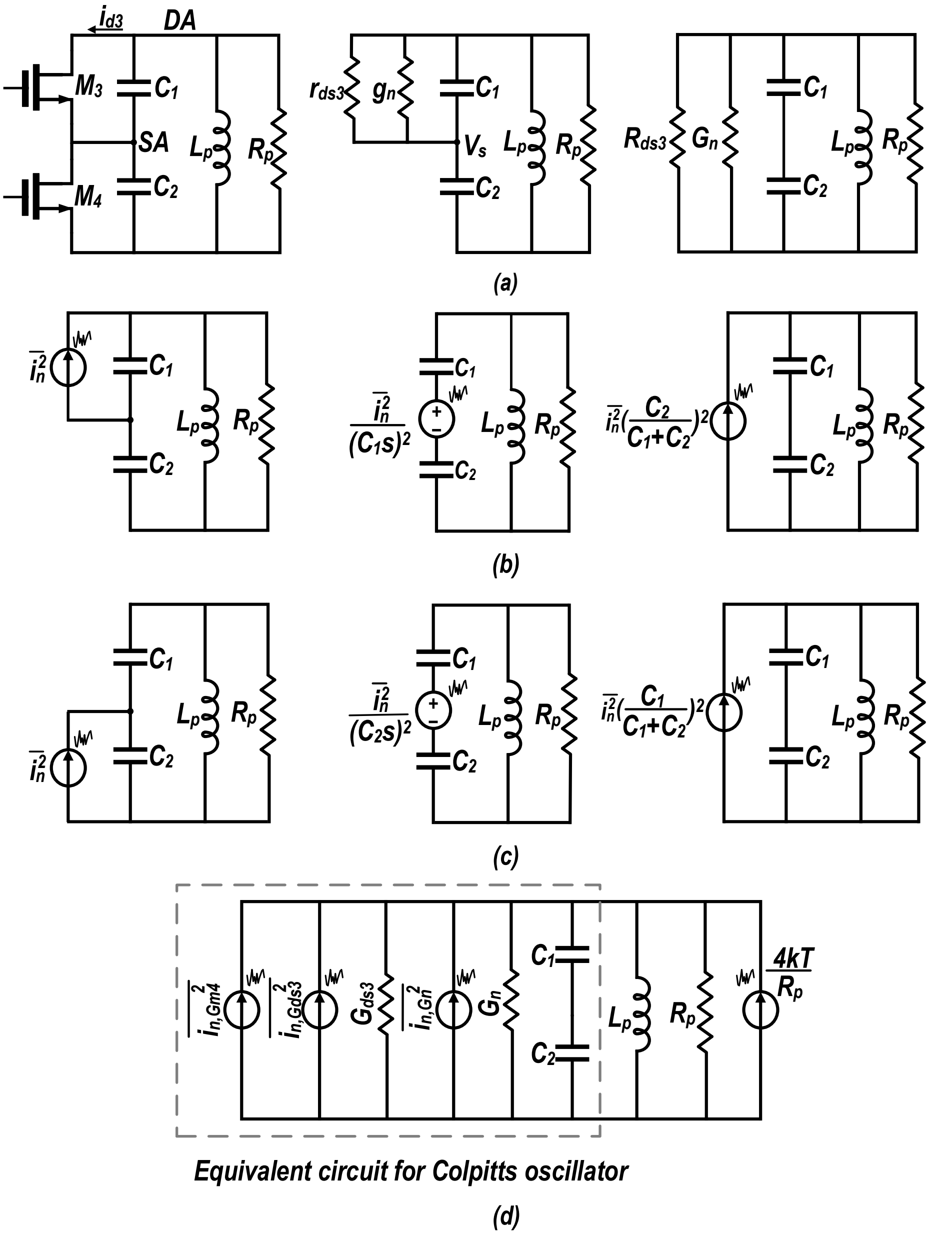

i_{d3}
DA
M_3
M_4
C_1
C_2
SA
L_p
R_p
r_{ds3}
g_n
V_s
R_{ds3}
G_n
(a)
$\overline{i_n^2}$
$\frac{\overline{i_n^2}}{(C_1s)^2}$
$\overline{i_n^2}(\frac{C_2}{C_1+C_2})^2$
(b)
$\frac{\overline{i_n^2}}{(C_2s)^2}$
$\overline{i_n^2}(\frac{C_1}{C_1+C_2})^2$
(c)
$\overline{i_{n,Gm4}^2}$
$\overline{i_{n,Gds3}^2}$
G_{ds3}
$\overline{i_{n,Gn}^2}$
G_n
$\frac{4kT}{R_p}$
Equivalent circuit for Colpitts oscillator
(d)

Figure 5.6: Procedures of referring the noise back to the tank from: (a) r_{ds3} and negative conductance; (b) g_m of M_3; and (c) g_m of M_4. (d) The equivalent circuit of the Colpitts oscillator.

$$F_{gm4} = \frac{2NR_p}{4kT\pi}\int_0^{2\pi}\frac{\sin^2(\phi)}{N^2}4kT\gamma g_{m4}\cdot\left(\frac{C_1}{C_1+C_2}\right)^2 d\phi = n^2\gamma G_{mEF4}R_P \tag{5.18}$$

g_{ds4} noise is very small due to M_4 operating in a saturation region and, consequently, is disregarded in our calculations. Since g_{m4} is fairly constant throughout the period, $G_{mEF4} = g_{m4}$. To estimate the contribution of M_4 to PN, we can calculate g_{m4} as

$$g_{m4} = \frac{2I_0}{V_{gs4} - V_{th}} \approx \frac{2I_0}{V_{ds,min}}, \tag{5.19}$$

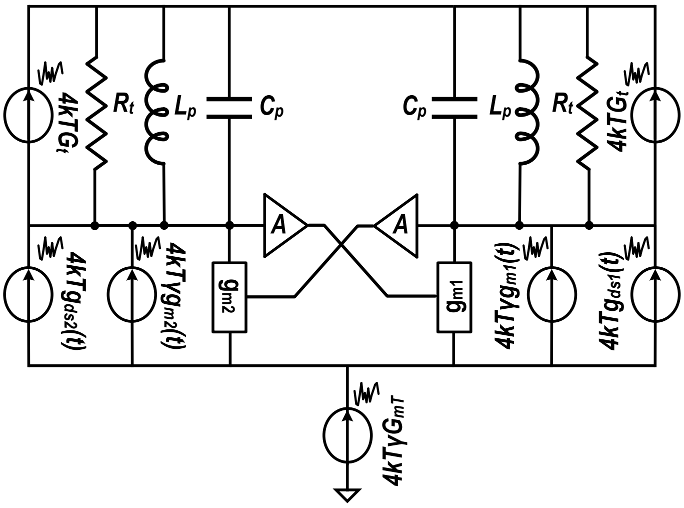

4kTGt
Rt
Lp
Cp
Cp
Lp
Rt
4kTGt
A
A
4kTgds2(t)
4kTγgm2(t)
gm2
gm1
4kTγgm1(t)
4kTgds1(t)
4kTγGmT

Figure 5.7: Noise sources of the DM oscillator [22].

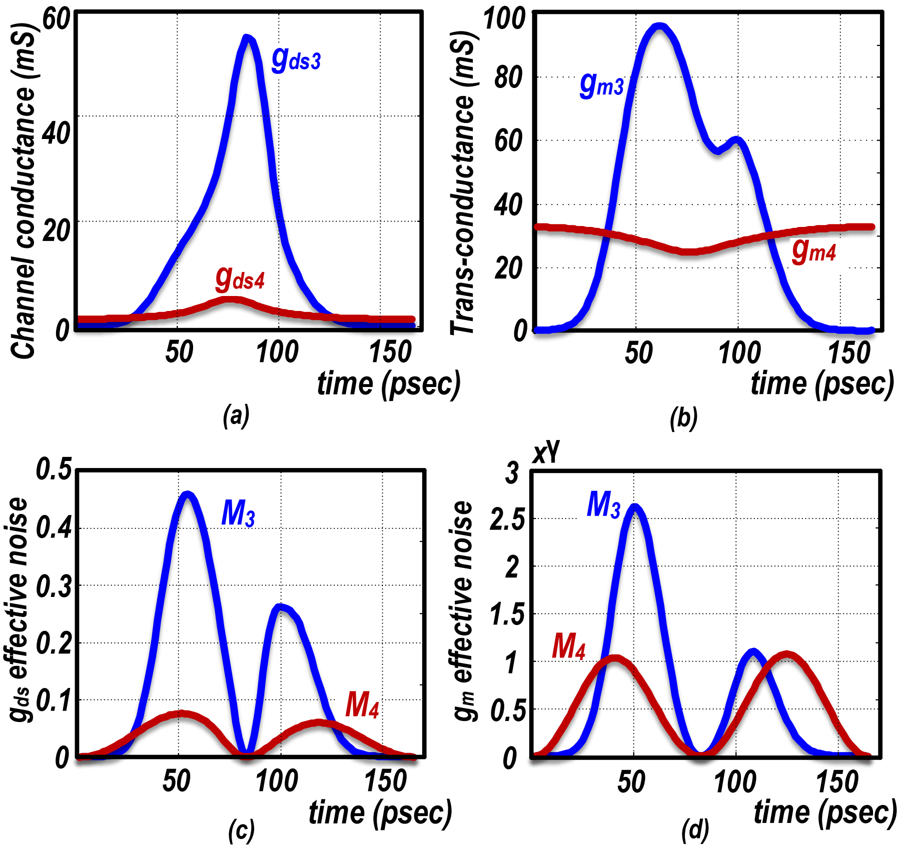


Figure 5.8: Circuit to phase noise conversion in CM oscillator.

where, V_{th} is the transistor's threshold voltage. Let us assign $V_{DD}/2$ to the SA (SB) node, and $V_{DA} \approx 2I_0R_p(1-n)$ [25],

$$g_{m4} \approx \frac{4I_0}{V_{DD} - 4n(1-n)I_0R_p} \tag{5.20}$$

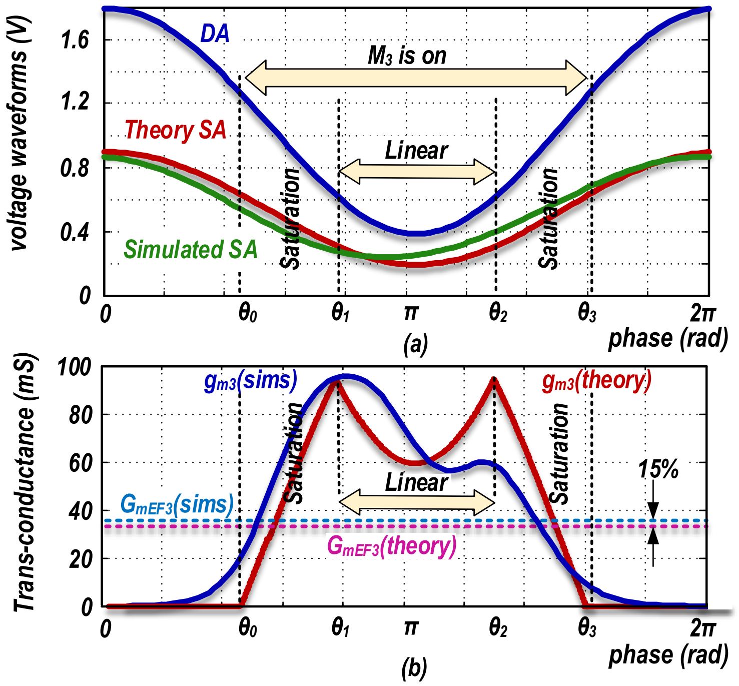


Figure 5.9: (a) Drain and source voltage waveforms. (b) g_{m3}: theory and simulations.

Disregarding g_{ds4} noise contribution,

$$F_{M4} \approx F_{gm4} = \frac{4n^2\gamma R_p I_0}{V_{DD} - 4n(1-n)I_0 R_p} \approx \gamma. \tag{5.21}$$

By substituting (5.12) in (5.16), with G_{mEF3} and G_{dsEF3} numerically obtained from simulations, the total oscillator effective noise factor then will be,

$$\begin{aligned} F_{CM} = R_P[(1-n)^2 G_{mEF3}(\gamma + \frac{n}{1-n}) + \\ \frac{4n^2\gamma I_0}{V_{DD} - 4n(1-n)I_0 R_p}] - 1 \approx 2.2\gamma + 0.2 \end{aligned} \tag{5.22}$$

The circuit-to-phase noise conversion of the CM oscillator is shown in Fig. 5.8 (a)-(d).

The noise contribution of M_3 transistor can be numerically calculated based on design parameters. For M_3, $V_d(\phi) = V_{DD} + A_C\cos(\phi)$, $V_s(\phi) \approx V_{DD}/2 + nA_C\cos(\phi)$ and $V_g = V_{B2}$. Figure 5.9 shows the M_3 operating regions during one oscillating period. At θ_0, V_s gets low enough for M_3 to turn on and enter the saturation region. When the drain voltage gets lower, M_3 enters the triode region at θ_1 and remains there till $\theta_2 = 2\pi - \theta_1$. M_3 finally turns off again at $\theta_3 = 2\pi - \theta_0$. θ_0 and θ_1 can be found from boundary conditions as

$$\theta_0 = \cos^{-1}\left(\frac{V_1}{nA_C}\right) \tag{5.23}$$

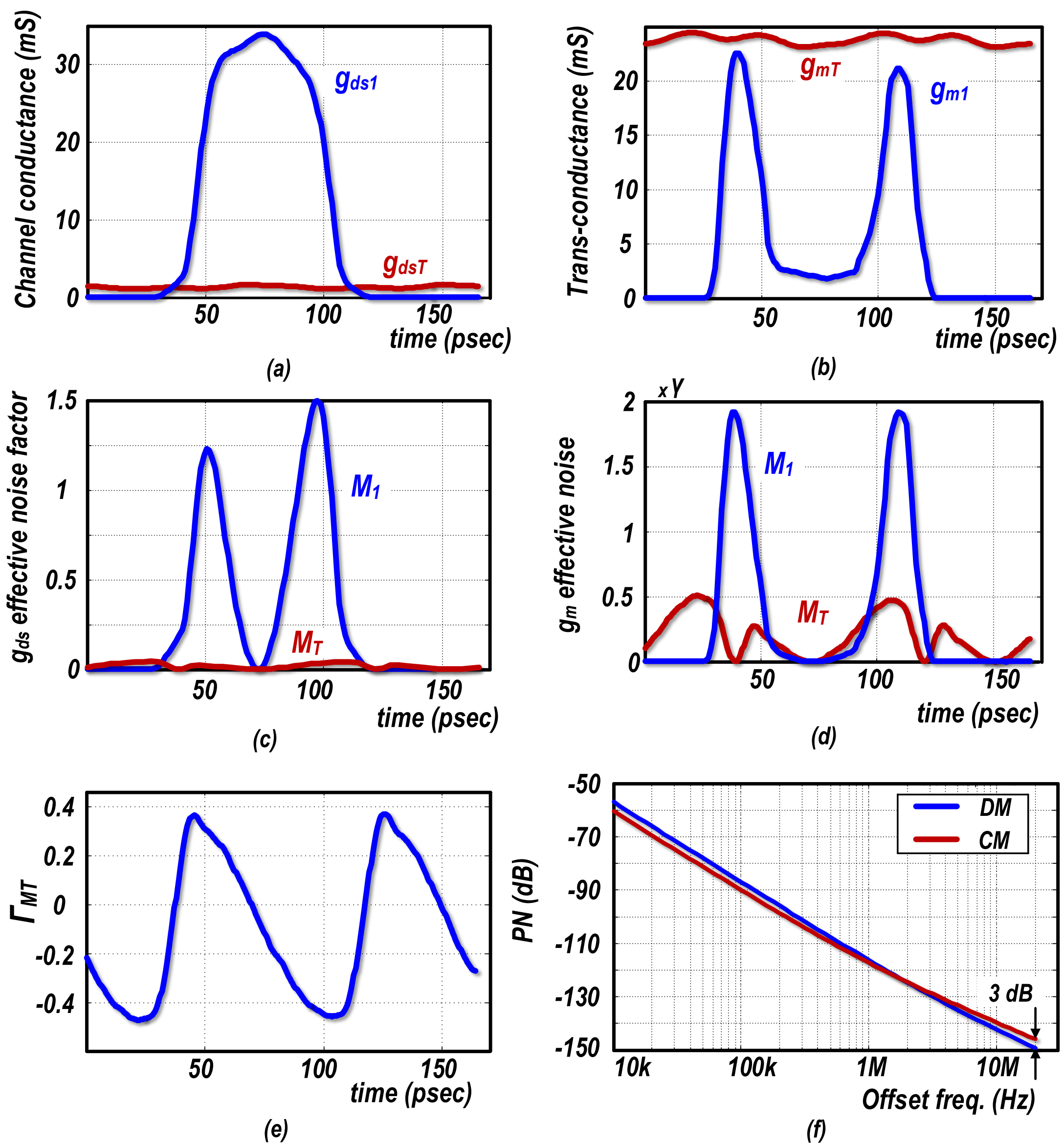


Figure 5.10: (a)-(d) Circuit to phase noise conversion in DM oscillator; (e) tail transistor ISF; and (f) PN of CM and DM oscillators at the overlap frequency.

and

$$\theta_1 = \cos^{-1}\left(\frac{V_2}{A_C}\right) \tag{5.24}$$

where, $V_1 = V_{B2} - V_{DD}/2 - V_{th}$ and $V_2 = V_{B2} - V_{DD} - V_{th}$.

Assuming square law,

$$g_{m3}(\phi) = \begin{cases} K(V_1 - nA_C\cos(\phi)) & \text{saturation,} \\ K(\frac{V_{DD}}{2} + (1-n)A_C\cos(\phi)) & \text{linear,} \\ 0 & \text{cut off,} \end{cases} \tag{5.25}$$

where $K = \mu C_{ox}\left(\dfrac{W}{L}\right)$ is the customary designation of MOS transistor strength. G_{mEF3} now can be determined by calculating the Fourier coefficients of $g_{m3}(\phi)$. Solving the lengthy integrations results in

$$\begin{aligned} G_{mEF3} = \frac{K}{2\pi}[&2V_1(\theta_1-\theta_0)+V_{DD}(\pi-\theta_1)+nA_c\sin(\theta_0)-A_c\sin(\theta_1) \\ &+V_1\sin(2\theta_0)+(\frac{V_{DD}}{2}-V_1)\sin(2\theta_1)-\frac{nA_c}{3}\sin(3\theta_0)+\frac{A_c}{3}\sin(3\theta_1) \end{aligned} \tag{5.26}$$

G_{mEF3} in (5.26) can be calculated by substituting θ_0 and θ_1 from (5.23) and (5.24), together with other design parameters: V_{DD}=1.1 V, V_{B2}=1 V, $V_{th}\approx$ 0.37 V. Fig. 5.9 (b) shows a very good agreement (within 15%) with the simulation results.

Major noise sources of the DM oscillator are shown in Fig. 5.7. A general result of the effective noise factor, assuming that the M_T thermal noise is completely filtered out, is derived in [22] as

$$2\Gamma^2_{t,rms}\cdot\left(1+\frac{\gamma}{A}\right)\cdot(1+R_tG_{dsEF1})\approx 1.6+0.9\gamma. \tag{5.27}$$

However, the M_T thermal noise is not completely filtered out here. To calculate the M_T's noise contribution, the tail node ISF is obtained through simulations and plotted in Fig. 5.10(e). From that

$$F_{M_T}=\frac{1}{2\pi}\int_0^{2\pi}4kT\gamma g_{mT}\cdot\Gamma^2_{M_T}(t)\,\frac{R_t}{4kT}\,dt\approx 0.5\gamma \tag{5.28}$$

Hence, the DM oscillator noise factor is,

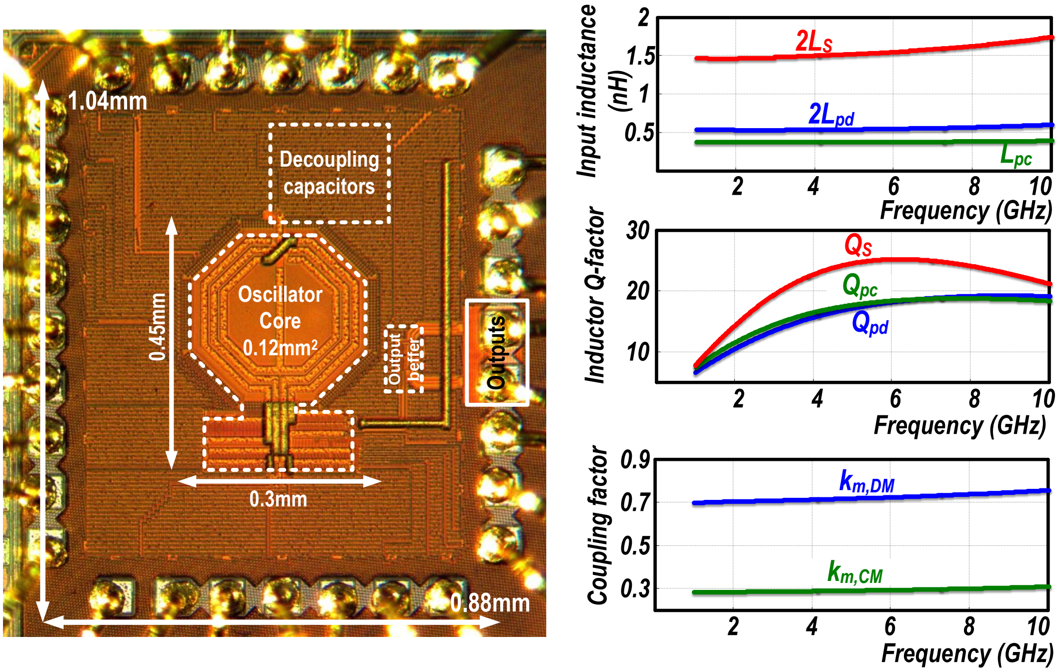
$$\begin{aligned} F_{DM} = 2\Gamma^2_{t,rms}&\cdot\left(1+\frac{\gamma}{A}\right)\cdot(1+R_tG_{dsEF1}) \\ &+\Gamma_{M_T,rms}R_pG_{MTEF}\approx 1.6+1.4\gamma \end{aligned} \tag{5.29}$$

The DM oscillator circuit-to-phase noise conversion is shown in Fig. 5.10 (a)-(d).

Substituting (5.22) and (5.29) in (5.7) at the *overlap* frequency results in

$$\mathcal{L}_{DM}-\mathcal{L}_{CM}=10\log_{10}\left(\frac{R_tQ_pA_C^2}{R_pQ_tA_D^2}\cdot\frac{F_{DM}}{F_{CM}}\right)\approx -2.5\,dB, \tag{5.30}$$

Due to its single-ended structure and the CM resonance, the Colpitts oscillator would appear to be more sensitive to supply noise. However, that is not the case. Supply pushing is the parameter that indicates the supply noise effect on the phase noise. Figure 5.12(e)(f) demonstrates this parameter for the DM and CM oscillators, which is quite comparable,



(a) (b)

Figure 5.11: Transformer characteristics.

indicating the CM oscillation does not result in higher phase noise up-conversion sensitivity to the supply noise. To explain that, let us look at the actual mechanism: The oscillation frequency can be modulated by the supply noise by modulating the nonlinear voltage-dependent parasitic capacitors of the core transistors, C_{gs}. In the Colpitts oscillator, the supply voltage is connected to the core transistors' drains, which cannot modulate their C_{gs} directly. Consequently, the oscillation frequency modulation due to the supply noise is considerably reduced.

5.3.3 Center Tap Inductance

The single-ended nature of the Colpitts oscillator makes its characteristics especially sensitive to single-ended parasitics. A key parasitic that must be properly modeled and accounted for is the metal track inductance, L_T, which connects the center tap of the transformer's primary to the supply's AC-ground [see Figs 5.2(a)]. At the DM excitation, the AC current will not flow into L_T, thus the DM inductance and DM resonant frequency are independent of its value. However, at the CM excitation, the current flowing into L_T is twice the current circulating in the inductors. Consequently, the tank inductance L_p in Fig. 5.2(a) is re-labeled as $L_{pd} = L_p$ in DM, and $L_{pc} = L_{pd} + 2L_T$ in CM excitations. The CM oscillation frequency will be reduced to $\omega_{CM} = 1/\sqrt{(L_p + 2L_T)C_P}$. This implies that L_T must be carefully modeled and included in simulations, otherwise the increased overlap between CM and DM oscillations would severely limit the total tuning range.

Another important parasitic that is only influential in the CM oscillation is the supply loop resistance between the $\mathrm{V_{DD}}$ feed to the center-tap of the primary winding and the sources of M_4 transistors (see Fig. 5.4), assuming sufficient decoupling capacitance on $\mathrm{V_{DD}}$. This resistance is added directly to the equivalent negative resistance of the Colpitts structure and increases it from $-g_{m3}/C_1C_2\omega^2$ to $-g_{m3}/C_1C_2\omega^2 + r_b$. In our design, the average of that negative resistance at 6 GHz with $C_1 = C_2 =$1 pF is about -25Ω, which means the r_b parasitic resistance should be kept much smaller as to not endanger the start-up.

5.4 Experimental results

The proposed oscillator is prototyped in TSMC 40-nm 1P7M CMOS process with top ultra-thick metal. $M_{1,2}$ are (60/0.27)μm and $M_{3,4}$ are (128/0.04) μm low-V_{th} devices for safe start-up of the Colpitts oscillator. The tank employs a 1.4 nH secondary inductor with Q of 25 at 5 GHz and 0.54 nH primary inductor with Q of 17 at 5 GHz. $k_{m,DM}$= 0.72 and $k_{m,CM}$=0.29. The transformer size is 250x250μm^2 and the primary-to-secondary winding spacing is 5 μm. The chip micrograph and transformer characteristics are shown in Fig. 5.11 and Fig. 5.11 respectively. The oscillator's core area is 0.12 mm^2, which is similar in size to typical narrow tuning-range oscillators. The tank is shared in the two modes of oscillation and so the output is common; hence no further multiplexing is necessary. A comparison with other relevant wide tuning-range oscillators is summarized in Table I. This work is smaller than state-of-the-art by at least a factor of 2. The oscillators are tuned via 4-bit switched MOM capacitor banks at the primary and secondary. According to post-layout circuit-level simulations, the tuning range is 46% in DM and 20% in CM, with a 100 MHz overlap, giving the total TR of 63%. However, measurements show that DM oscillator is tunable between 3.37–5.32 GHz (45% TR) and the CM oscillator is tunable between 5.02–5.96 GHz (17% TR) and the overlap between the DM and CM oscillations is wider than expected, resulting in a tuning range of 55.5%.

Figure 5.12 shows PN at f_{max} and f_{min} frequencies of the DM and CM oscillations. In both modes, V_{DD} is 1.1V. Figure 5.12 also reports the PN and FoM of this oscillator over the tuning range. The FoM increases from 188.2 dB to 189.4 dB in the DM and from 181.3 dB to 182.3 dB in the CM tuning ranges. The PN in the CM mode is worse than in the DM mode, but it is worth mentioning that not all applications demand ultra-low phase noise in all bands and channels uniformly.

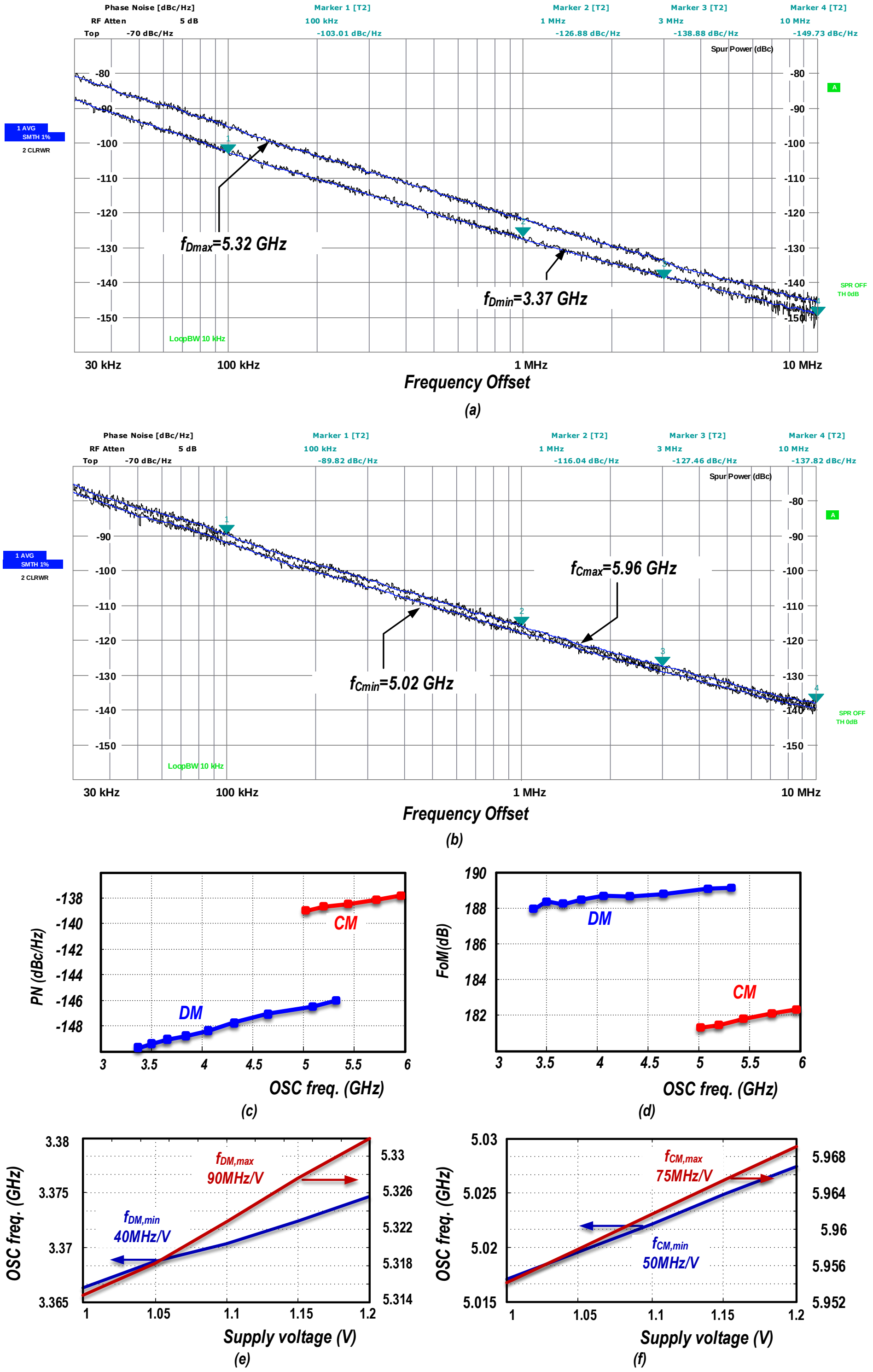


Figure 5.12: (a) Measured PN at $f_{DM,max}$, $f_{DM,min}$; (b) $f_{CM,max}$ and $f_{CM,min}$. Measured (c) PN; and (d) FoM at 10MHz offset across TR. Frequency pushing due to supply voltage variation in (e) DM; and (f) CM oscillators.

Table I also compares FoMA, introduced in [29], of the proposed oscillator with other relevant oscillators. The DM oscillator shows the best FoMA and the CM oscillator's FoMA is comparable with the other state-of-the-art oscillators.

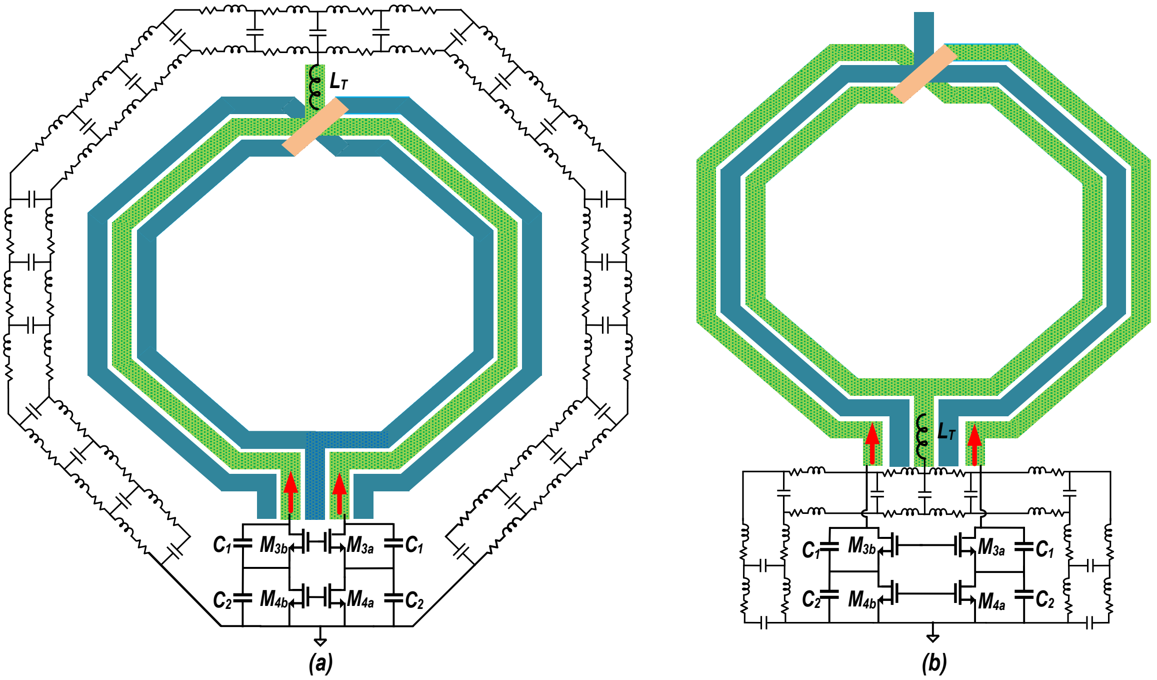


Figure 5.13: Return current path in the 1:2 transformer.

5.4.1 Supply and Ground Routing Inductances and Losses

The measurement results deviate from the simulations and theory in two ways. The first is the wider overlap between the DM and CM oscillation frequencies. The second is the degraded PN in the CM Colpitts oscillator. To explain the performance degradation, we first take a closer look at a layout of the transformer-based tank. As revealed in Fig. 5.13, the CM inductance should also include the impedance of the current return route, from the center-tap of the primary winding to the sources of M_{4a} (M_{4b}). The de-coupling capacitors together with the RLC routing network present an equivalent impedance that is inductive but its real part adds to the circuit losses. Therefore, unless the return current path happens to resonate at the same oscillation frequency (through the equivalent inductances and decoupling capacitors along it), the CM oscillation shifts down from the expected value, which is precisely what we observe in our measurements. The DM oscillation frequency is not affected, therefore, the expected TR is decreased. Furthermore, the losses in the return path are added to the losses of the primary inductor, thus degrading the quality factor of the tank. The long return path causes the losses to be comparable to the inductor's loss and this jeopardies the CM start up. Furthermore, this path also partially cancels the magnetic field of the inductor, thus degrading its Q-factor. The severe PN degradation compared to the simulation results gives thus credence to the Q degradation of the tank. Our EM simulations predict a $0.25\,\Omega$ resistance in this

Table 5.1: Performance summary and comparison with state-of-the-art.

		This Work		[18]		[19]		[4]		[5]		[11]		[12]
Frequency (GHz)		**3.37-5.96**		2.5-5.6		3.24-8.45		2.4-5.3		1.3-6		3.28-8.35		3.14-6.44^2
Tuning range (%)		**55.5**		76		89		75.3		128		87.2		69^2
V_{DD} (V)		**1**		0.6		0.8		0.4		1.5		1.6		1.2
Technology		**40 nm**		65 nm		40 nm		65 nm		130 nm		130 nm		180 nm
OSC core area		**0.12 mm^2**		0.29 mm^2		0.43 mm^2		0.25 mm^2		0.295mm^2		0.1mm^2		0.35mm^2
		f_{min}	**f_{max}**	f_{min}	f_{max}	f_{min}	f_{max}	f_{min}	f_{max}	f_{min}	f_{max}	f_{min}	f_{max}	f_{mid}
P_{DC} (mW)		**16**	**12.5**	14.1	9.9	16.5	14	6	4.4	4.35^1	9.15^1	15.4	6.5	8.8
PN (dBc/Hz)	100kHz	**-103**	**-90**	-101.1	-89	-109	-91	-98	-86	NA	NA	-96	NA	-92
	10MHz	**-149.7**	**-137.8**	-151.9	-145.8	-150	-142	-149	-139	-135	-132	-142	-137.2	-140
FoM† (dB)	100kHz	**181.8**	**174.5**	177.6	174	187	178.1	177.8	174.1	NA	NA	174.4	NA	175.4
	10MHz	**188.2**	**182.3**	188.4	190.8	188	189.1	188.8	187	171	178	180.4	187.5	183.4
FoMA†† (dB)	100kHz	**191**	**183.7**	182.9	179.4	190.7	181.7	183.8	180.1	NA	NA	184.4	NA	180
	10MHz	**197.4**	**191.5**	193.7	196.2	191.7	192.7	194.8	193	176.2	183.2	190.4	197.5	188
FoMAT††† (dB)	100kHz	**205.6**	**198.6**	200.5	197	209.7	200.7	201.3	197.6	NA	NA	203.3	NA	196.8
	10MHz	**212.3**	**206.4**	211.3	213.8	210.7	219.7	212.3	210.5	198.3	205.4	209.3	216.3	204.8

†FoM= $|PN|+20\log_{10}(\omega_0/\Delta\omega)-10\log_{10}(P_{DC}/1mW)$ ††FoMA= $|PN|+20\log_{10}(\omega_0/\Delta\omega)+10\log(1mm^2/A)-10\log_{10}(P_{DC}/1mW)$

†††FoMAT= $|PN|+20\log_{10}(\omega_0/\Delta\omega)+20\log_{10}(TR/10)+10\log(1mm^2/A)-10\log_{10}(P_{DC}/1mW)$

^{1} *Including bias circuitry.* ^{2} *Before frequency division.*

path and circuit simulations show that such resistance in series with the primary inductor would degrade the CM oscillator phase noise by 4 dB. This appears to agree with our measurements.

One possible solution would be employing a 2:1 transformer. A 2-turn primary inductor will have its supply connection node very close to the transistors; therefore the current return path would not be very long, thus minimizing the path inductance. However, in that transformer, the CM current in the two windings of the primary inductor has opposite direction, thus cancelling each other's flux [28]. Consequently, the CM primary inductance would be smaller than the DM one. The spacing between the transformer windings should be chosen properly to satisfy the overlap condition for the reasonable capacitor bank $C_{\mathrm{on}}/C_{\mathrm{off}}$ ratios.

5.5 Conclusion

In this chapter, we introduced a technique to extend a tuning range (TR) of an LC-tank oscillator without significantly increasing its die area. A strongly coupled 1:2 turns-ratio transformer-based tank is normally excited in a differential mode (DM), where it achieves the TR of 45% with a good FoM of 188.2–189.4 dB. The TR is extended by exciting the tank in common mode (CM) with two locked Colpitts oscillators. The proposed oscillator is implemented in 40-nm CMOS and delivers the total TR of 55.5% while constraining the core die area to only 0.12 mm^2. Although the measured tuning range extension and phase noise (PN) in the CM mode were worse than theoretically predicted, we have identified the common cause as a current return route inductance that not only lowers the CM frequencies but also adds losses that result in a reduced Q-factor.

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Chapter 6

Conclusion

This dissertation presents analysis, design considerations and implementation of RF CMOS oscillators for mostly high-performance cellular applications. In Section 6.1 we summarize the outcome of this thesis and Section 6.2 proposes suggestions for future work.

6.1 Thesis Outcome

As explained in Chapter 3, the oscillator's low-frequency noise may not be filtered in a PLL loop and so it may affect the synthesizer and, consequently, performance of the communication system. The unfiltered low-frequency noise portion is due to the relatively lower loop bandwidth of the PLL (few hundred kHz) compared to the oscillator's $1/f^3$ corner frequency (around 1 MHz or higher).

On the other hand, contemporary cell phones have to support multi-standard communications with ever increasing data rates. The challenge in designing a transceiver that supports such standards leans on an oscillator with a very wide tuning-range that can satisfy performance requirements of the most stringent standards.

In Chapter 3, various flicker noise upconversion mechanisms in an oscillator are studied together with available solutions. We investigate the importance of core transistors' flicker noise on the oscillator's low-frequency phase noise and show that the phase and amplitude of even-order tank's current harmonics affects this upconversion. We also introduce a method to minimize it. The method involves a tank that contains an extra common-mode resonant frequency at twice the oscillation frequency. An implementation method for both inductor- and transformer-based tanks is proposed that satisfies this condition without any die area penalty. As a proof of concept, we chose two oscillators, class-D and class-F, and applied the proposed method to them. We could prove on silicon that the 1/f^3 corner of these oscillators can reduce 5–10×. The solutions available in literature to reduce the flicker noise upconversion are either very area consuming or sacrifice phase noise in the thermal region. In the proposed solution, spacing between the windings of a 2-turn inductor (F_2 inductor) and a 1:2 turn step up transformer (F_2 transformer) is designed properly to satisfy the $\omega_{CM} = 2\omega_0$ condition. The F_2 inductor and transformer are not much larger than an ordinary inductor or transformer and, consequently, the proposed method does not suffer from any area penalty. The extra CM resonance adds another resistance in the tank's input impedance and, consequently, increases the tank's thermal noise contribution compared to the ordinary tank. However as the simulations show, the thermal-region phase noise performance of the class-D/F_2 and class-$\mathrm{F}_{2,3}$ oscillators is quite close to their class-D and class-F counterparts.

The second part of the dissertation, Chapters 4 and 5, is devoted to wide tuning-range oscillators for multi-band and multi-standard applications. Chapter 4 is dedicated to designing a dual-mode oscillator with nearly an octave of tuning. The oscillator is then incorporated inside an all-digital PLL (ADPLL). The very fine frequency resolution is achieved by manually designing capacitor cells and capacitor banks and its linearity is proved in measurements. The ADPLL, in which the oscillator is incorporated in, shows only 420 fs_{rms} integrated jitter. Although this oscillator exhibits very promising tuning-range and phase noise, it is at least twice as large in area as a corresponding narrow tuning-range oscillator. This was the motivation for the wide tuning-range oscillator that is proposed in Chapter 5. The strongly-coupled 1:2 turns-ratio transformer-based tank shows separate differential- and common-mode resonant frequencies and, consequently, can offer wide tuning-range oscillation if the tank can be excited with differential and common mode signals. The investigation of common-mode resonance proved an encouraging quality factor that would assure the possibility of the oscillation start up in this mode. Two coupled Colpitts oscillators could force the tank to start common-mode oscillation and extend its tuning-range, all with an active area of $0.12\,\mathrm{mm}^2$, which is similar to the conventional narrow tuning-range oscillators in the same technology (40-nm CMOS).

6.2 Suggestion for Future Works

This dissertation presents several oscillators for different applications. The results reveal some further research possibilities:

- A detailed analysis on the thermal noise upconversion of the oscillators that employ F_2 tank is very beneficial. The proposed oscillators (or a "class-D/F_2" oscillator) can be incorporated inside a PLL to investigate the improvement of employing such an oscillator on the phase jitter of a PLL.

- As discussed in Chapter 5, the incorrect estimation of inductance and resistance components of the return-current path has resulted in a reduced common-mode resonant frequency compared to the simulations. It also resulted in the Q-degradation of the common-mode resonance and, consequently, the phase noise of the common-mode oscillator is worse than expected. Designing a wide tuning-range oscillator with accurate estimation will increase its tuning range to beyond 60%. Further, we could connect the center tap in the current solution from the top to the supply pad, and to provide a short return-current path by a metal track from this node within the transformer and with a series capacitor connect it to the ground. This capacitor value cancels out the metal track inductance, and since the CM oscillator tuning range is not very large, a fixed capacitor would be enough to cancel out the inductance throughout the whole CM tuning range. That short return would be less lossy and would not degrade the CM inductance's Q-factor. In the DM oscillation, since the center tap is a virtual ground, this metal track and the series capacitor will not affect the oscillation characteristics.

- Another interesting research topic could explore the possibility of forcing the common-mode oscillation by a circuitry different from the Colpitts structure. The fixed capacitors of the Colpitts oscillator limit tuning range in both common-mode and differential-mode oscillations. The Colpitts structure suffers also from difficulties of start-up, since its start-up condition is much tougher than in a cross-coupled structure. Designing a new structure that can avoid these limitations is the key to designing a wide tuning-range oscillator with a very good phase noise performance while occupying the area of a narrow tuning-range oscillator.

List of Publications

Journal Papers

- **M. Shahmohammadi** and R. B. Staszewski, "Tuning range extension of a transformer-based oscillator through common-mode Colpitts resonance," *IEEE Trans. on Circuits and Systems I (TCAS-I)*, vol. 63, iss. x, pp. xx–xx, xxx. 2016. (In print)
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- M. Babaie, F.-W. Kuo, R. Chen, L.-C. Cho, C.-P. Jou, F.-L. Hsueh, **M. Shahmohammadi**, and R. B. Staszewski, "A Fully Integrated Bluetooth Low-Energy Transmitter in 28-nm CMOS with 36% System Efficiency at 3 dBm," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 51, no. 7, pp. 1547–1565, Jul. 2016. DOI: 10.1109/JSSC.2016.2551738. [IEEE Xplore link (Open Access)] (Special ESSCIRC issue)

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- E. Charbon, F. Sebastiano, M. Babaie, A. Vladimirescu, **M. Shahmohammadi**, R. B. Staszewski, H. A.R. Homulle, B. Patra, J. P.G. van Dijk, R. M. Incandela, L. Song, and B. Valizadehpasha, "Cryo-CMOS circuits and systems for scalable quantum computing", *Proc. of IEEE Solid-State Circuits Conf. (ISSCC)*, sec. x.x, pp. xx–xx, xx Feb. 2017, San Francisco, CA, USA. (accepted)
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- **M. Shahmohammadi**, M. Babaie, and R. B. Staszewski, "A 1/f noise upconversion reduction technique applied to class-D and class-F oscillators," *Proc. of IEEE Solid-State Circuits Conf. (ISSCC)*, sec. 25.4, pp. 444–445, 25 Feb. 2015, San Francisco, CA, USA. DOI: 10.1109/ISSCC.2015.7063117. [IEEE Xplore link]
- **M. Shahmohammadi**, K. Souri and K. A. A. Makinwa, "A resistor-based temperature sensor for MEMS frequency references," *ESSCIRC*, Sept. 2013, pp. 225–228.

Seminars

- **M. Shahmohammadi**, "A 1/f noise upconversion reduction technique applied to class-D and class-F oscillators," Seminar (1-hr) presented at Qualcomm Inc, San Diego, CA, USA, 17 Feb. 2015.

Patent Applications

- **M. Shahmohammadi**, M. Babaie, R. B. Staszewski, "Flicker noise up-conversion reduction technique applied to a class-F oscillator," International Application No. PCT/EP2015/051573, Filed Jan. 2015.
- **M. Shahmohammadi**, M. Babaie, R. B. Staszewski, "A single tank dual mode oscillator," International Application No. PCT/EP2015/051574, Filed Jan. 2015.

Summary

A radio-frequency (RF) oscillator is one of the key building blocks of a wireless transmitter/receiver (a.k.a., transceiver). As such, its spectral purity and power efficiency substantially affect operation and performance of wireless communication systems. Applications which demand high spectral purity employ inductor/capacitor (LC)-tank CMOS oscillators, where their close-in spectra are limited by flicker (i.e., 1/f) noise. Although low-frequency noise of the oscillator is filtered out partially when it is incorporated in a frequency synthesizer's phase-locked loop (PLL), the unfiltered noise can still be considerable since the loop bandwidth is typically lower than the $1/f^3$ corner frequency of the oscillator (i.e., boundary between the upconverted flicker and thermal noise). This issue is becoming nowadays more important due to higher flicker noise of deep-submicron CMOS technologies.

On the other hand, the massive interest in multi-standard wireless communications requires RF oscillators that cover a very broad frequency span. One strategy is employing multiple oscillators where each one covers part of that frequency span. However, that strategy is area-inefficient and consequently costly. The other strategy is to design a wide tuning-range oscillator that can cover the required wide frequency span at the expense of increased phase noise. Interestingly, most wide tuning-range oscillators that have managed to tackle the phase noise degradation are at least twice as large in area as a corresponding narrow tuning-range oscillator.

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[1] Mr. Frerik Witte and Mr. Hans Stoffels have translated the summary as well as the propositions of this dissertation into Dutch.

This dissertation is composed of two parts. The first part (Chapter 3) is dedicated to reducing core transistor's flicker noise upconversion to phase noise in voltage-biased CMOS LC-tank oscillators. That chapter elaborates on how the 2^{nd} harmonic component of the tank current, which flows into the capacitive part of the tank, results in asymmetric rise/fall times of the oscillating voltage waveform and, consequently, the 1/f to phase-noise upconversion. It is also shown how an auxiliary resonance at the 2× resonant frequency, $2\omega_0$, makes the oscillation waveform more symmetric by providing a resistive path for the 2^{nd} harmonic current, thus significantly reducing the 1/f to phase-noise upconversion. We also explore realizations of both inductor- and transformer-based tanks with a main ω_0 and an auxiliary $2\omega_0$ resonance peaks without any die area penalty. Such tanks are created by exploiting a different behavior of 2-turn inductors and step-up 1:2-turn transformers in differential- and common-mode excitations. Class-D/F_2 and class-$F_{2,3}$ oscillators are implemented as a proof-of-concept for, respectively, inductor- and transformer-based tank oscillators.

The objective of the second part of the dissertation (Chapters 4–5) is designing wide tuning-range CMOS LC oscillators. Implementation of a mode-switching oscillator and its incorporation inside an all-digital PLL (ADPLL) are elaborated in Chapter 4. State-of-the-art wide tuning-range oscillators have adequate phase noise over the tuning span but at the expense of large silicon area. To tackle this common disadvantage, a tuning range extension through a common-mode oscillation of a transformer-based tank is proposed in Chapter 5. This new oscillator employs a strongly coupled transformer-based tank and excites it with either differential- or common-mode signals. The tank's common-mode resonant frequency is sufficiently larger than that of the differential mode in order to ensure continuous tuning over an octave. The oscillator employs separate active circuits to excite each mode. Forcing the tank to resonate in the differential mode is quite straightforward and is realized by a two-port structure and two mutually injection-locked Colpitts oscillators force the tank to resonate in the common mode. However, these two active circuits share the same passive tank; therefore, the area of this oscillator is comparable to that of a typical narrow tuning-range oscillator. Due to the single-ended nature of the common-mode excitation, the oscillator makes its characteristics sensitive to single-ended parasitics. The important parasitics and their role are also investigated in this chapter.

Samenvatting

Een radiofrequentie (RF) oscillator is een van de belangrijkste bouwblokken van een draadloze zender/ontvanger (ook gekend als transceiver). De spectrale zuiverheid en het vermogensverbruik van de oscillator beïnvloeden de werking en prestatie van draadloze communicatie systemen. Toepassingen die een hoge spectrale zuiverheid vereisen, gebruiken spoel en capaciteit (LC)-tank CMOS oscillatoren. Daarbij bepaalt flicker (met andere woorden 1/f) ruis de close-in spectra. Laagfrequente ruis van een oscillator wordt deels uitgefilterd als de oscillator opgenomen wordt in een fasegeregelde lus (PLL) van een frequentie synthesizer. Toch kan dan de ongefilterde ruis nog steeds aanzienlijk zijn omdat de lus bandbreedte doorgaans lager is dan de $1/f^3$ hoek frequentie van de oscillator (met andere woorden de grens tussen de opgeconverteerde flicker ruis en thermische ruis). Deze kwestie wordt tegenwoordig steeds belangrijker vanwege het hogere flicker ruis niveau van diepe-submicrometer CMOS technologieën.

Aan de andere kant vereist de massale belangstelling voor meervoudige standaarden van draadloze communicatie RF oscillatoren die een erg brede frequentiebereik dekken. Een strategie is om meerdere oscillatoren te gebruiken die ieder een deel van dat bereik dekken. Deze strategie gaat inefficiënt met het chip-oppervlak om en is daardoor kostbaar. Een andere strategie is om een oscillator te ontwerpen met een wijd afstembaar bereik, die het vereiste grote frequentiebereik dekt ten koste van een toegenomen fase ruis. Interessant genoeg zijn de meeste breed afstembare bereik oscillatoren, die de ruis degradatie succesvol hebben aangepakt, minstens twee keer zo groot in oppervlak als de corresponderende smal

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[1] De samenvatting als de proposities zijn beide vertaald door Mr. Frerik Witte en Mr. Hans Stoffels.

afstembare bereik oscillator.

Dit proefschrift is opgebouwd uit twee delen. Het eerste deel (Hoofdstuk 3) behandelt het verminderen van de flicker ruis opconversie tot fase ruis in spanning gebiasde CMOS LC-tank oscillatoren. Deze ruis ontstaat in de transistoren van de oscillator kern. Dit hoofdstuk werkt uit hoe de 2^{de} harmonische component van de tank stroom, die in het capacitieve deel van de tank stroomt, leidt tot ongelijke stijg- en daaltijden van de oscillerende spanningsgolfvorm. Daardoor ontstaat opconversie van 1/f tot fase ruis. Ook wordt aangetoond hoe een toegevoegde resonantie van 2x de resonantie frequentie -$2\omega_0$- de oscillatie golfvorm meer symmetrisch maakt. Dit wordt bereikt door een resistief pad te voorzien voor de 2^{de} harmonische stroom. Dit reduceert de opconversie van 1/f tot fase ruis beduidend. We verkennen ook realisaties van zowel spoel als transformator gebaseerde tanks met een voornaamste ω_0 en een toegevoegde $2\omega_0$ resonantie piek zonder enig oppervlakte nadeel. Zulke tanks worden gemaakt door een verschillend gedrag van common-mode en differentiële-mode excitaties uit te buiten in 2-turn spoelen en step-u 1:2-turn transformatoren. Klasse-D/F_2 en klasse-F_{23} oscillatoren zijn geïmplementeerd als haalbaarheidsstudie voor respectievelijk spoel en transformator gebaseerde tank oscillatoren.

Het doel van het tweede deel van het proefschrift (hoofdstuk 4–5) is het ontwerpen van CMOS LC oscillatoren met een breed afstembereik. De implementatie van een mode schakelende oscillator en zijn opname in een geheel digitale PLL (ADPLL) zijn uitgewerkt in hoofdstuk 4. De modernste oscillatoren met breed afstembereik hebben adequate fase ruis over het hele afstembare bereik maar ze kosten veel silicium oppervlak. Om dit gemeenschappelijke nadeel op te lossen wordt een uitbreiding van het afstembereik voorgesteld in hoofdstuk 5. Dit geschiedt door een common-mode oscillatie van een transformator gebaseerde tank te gebruiken. Deze nieuwe oscillator gebruikt een gebaseerde tank met sterk gekoppelde transformator en exciteert de tank met ofwel differentieel ofwel common-mode signalen. De common-mode resonantiefrequentie van de tank is voldoende groter dan de differentiële-mode om een continu afstembaar bereik te verzekeren over een octaaf. De oscillator gebruikt gescheiden actieve circuits om iedere mode te exciteren. Het is relatief eenvoudig om de tank te laten resoneren in de differentiële-mode en dit wordt gedaan met een tweepoort structuur. Twee gemeenschappelijk injectiegeregelde Colpitts oscillators laten de tank resoneren in de common-mode. Deze twee actieve circuits delen echter dezelfde passieve tank. Daarom is het oppervlak van deze oscillator vergelijkbaar met die van een gangbare oscillator met smal afstembereik. Door de single-ended aard van de common-mode excitatie is deze oscillator gevoelig voor single-ended parasieten. De belangrijke parasieten en hun rol worden ook onderzocht in dit hoofdstuk.

List of Figures

1.1 (a) Analog and; (b) digital phase locked loops [9]. 2

1.2 Oscillator's open loop and output frequency phase noise. 4

2.1 A generic RF transceiver [1]. 10

2.2 Phase response to an impulse current [9]. 11

2.3 A class-B oscillator (a) schematic; (b) oscillation amplitude vs. tail current; (c) ideal and real drain current waveforms; (d) oscillation voltages waveforms. 13

2.4 The switched-capacitor tuning circuit in on and off states. 14

2.5 (a) A class-C oscillator schematic; and (b) its voltages waveforms. 15

2.6 (a) A class-C with dynamic generation of V_{bias} [22]; (b) a hybrid class-B/class-C oscillator [26]. 16

2.7 (a) A class-D oscillator schematic; and (b) its voltages waveforms. 17

2.8 (a) Fundamental, V_{H1}; (b) 3^{rd} harmonic, V_{H3}, voltage components; (c) oscillation waveform; and (d) expected ISF. (e) Fundamental, V_{H1}; (f) 2^{nd} harmonic, V_{H2}, voltage components; (g) oscillation waveform; and (h) expected ISF. 18

2.9 (a) A transformer based tank class-F oscillator schematic; and (b) its voltages waveforms. 19

2.10 (a) A transformer based tank class-F oscillator schematic; and (b) its voltages waveforms [38]. 20

3.1 Class-B oscillator: (a) with tail transistor $\mathrm{M_T}$; (b) with tail resistor $\mathrm{R_T}$; and their PN when (c) $\mathrm{M_T}$ is always in saturation; (d) $\mathrm{M_T}$ enters partially into triode. 28

3.2 (a) Current harmonics paths; (b) drain current in time and frequency domains; (c) frequency drift due to Groszkowski effect. 30

3.3 (a) Auxiliary resonances at higher harmonics; (b) current harmonic paths; (c) frequency drift; (d) input impedance of the tank. 32

3.4 Oscillator example: (a) schematic; (b) V_{DS}, V_{GS}, and g_m of M_1 transistor when oscillation voltage contains only fundamental component; (c) its ISF, NMF, and effective ISF. 33

3.5 Conventional tank waveforms: (a) fundamental, V_{H1}, 2$^{\text{nd}}$ harmonic, V_{H2}, voltage components and oscillation waveform, V_{T2}; (b) its ISF, NMF and effective ISF; (c) $\Gamma_{eff,dc}/\Gamma_{eff,rms}$ for different α_2 values. 34

3.6 Conventional tank waveforms: (a) fundamental, V_{H1}, 3$^{\text{rd}}$ harmonic, V_{H3}, voltage component and oscillation waveform, V_{T3}; (b) its ISF, NMF and effective ISF. 36

3.7 (a) Voltage biased class-B oscillator schematics (b) $1/f^3$ corner vs.I_{H2}/I_{Hn}. 37

3.8 Proposed tank waveforms: (a) fundamental voltage component, V_{H1}; (b) voltage 2$^{\text{nd}}$ harmonic in presence of auxiliary resonance, $V_{H2,aux}$; (c) oscillation waveform, $V_{T2,aux}$; (d) its ISF, NMF and effective ISF. 38

3.9 (a) $V_{T2,aux}$ for different ϕ_{CM}; (b) ϕ_{CM} for different Q$_{CM}$ when ω_{CM} deviates from $2\omega_0$; (c) $\Gamma_{eff,dc}/\Gamma_{eff,rms}$ for different $\alpha_{2,aux}$ and ϕ_{CM}. 39

3.10 (a) A tank with DM and CM resonances ; (b) 1/f^3 corner of the oscillator employing this tank; (c) ϕ_{CM}; and (d) $\alpha_{2,aux}$ of the tank vs. ω_{CM}/ω_{DM}. . 40

3.11 d) PN; and (e) current harmonic components of a class-B oscillator (a), and similar counterparts with noise filtering technique [29] (b), and the proposed method applied (c). 42

3.12 A 2-turn "F$_2$" inductor in (a) DM excitation; (b) CM excitation; (c) F_2 DM and CM inductances and their ratio; (d) Q_{DM} and Q_{CM}. 43

3.13 (a) Inductor-based F_2 tank; and (b) its input impedance. 44

3.14 Class-D oscillator: (a) schematic; its (b) waveforms; and (c) gm-transistor ISF, NMF, and effective ISF. Class-D/F$_2$ oscillator: (d) schematic; its (e) waveforms; and (f) gm-transistor ISF, NMF, and effective ISF; (g) their PN performance; and (h) 1/f^3 corner sensitivity to ω_{CM}/ω_{DM}. 46

3.15 Class-D/F$_2$ oscillator: 1/f^3 corner over process variation; and (b) histogram of PN at 10kHz offset frequency. 47

3.16 1:2 transformer when the primary is excited with (a) DM; and (b) CM currents. 48

3.17 (a) Transformer-based F_2 tank; (b) its input impedance; (c) DM and CM primary and secondary inductance; (d) primary and secondary inductance quality factor and coupling factor; (e) DM and CM resonant frequencies over TR. 49

3.18 Class-F_3 oscillator: (a) schematic; its (b) waveforms; and (c) gm-transistor ISF, NMF, and effective ISF. Class-$F_{2,3}$ oscillator: (d) schematic; its (e) waveforms; and (f) gm-transistor ISF, NMF, and effective ISF; (g) their PN performance; and (h) $1/f^3$ corner sensitivity to ω_{CM}/ω_{DM}. 50

3.19 Class-$F_{2,3}$ oscillator: $1/f^3$ corner over process variation; and (b) histogram of PN at 10kHz offset frequency. 51

3.20 Chip micrographs: (a) class-D/F_2 oscillator; (b) class-$F_{2,3}$ oscillator. . . . 51

3.21 Class-D/F_2 oscillator: measured (a) PN at $f_{\max}$ and $f_{\min}$; (b) frequency pushing due to supply voltage variation; and (c) $1/f^3$ corner over tuning range. 52

3.22 Class-$F_{2,3}$ oscillator: measured (a) PN at $f_{\max}$ and $f_{\min}$; (b) frequency pushing due to supply voltage variation; and (c) $1/f^3$ corner over tuning range. 53

4.1 DTC assisted ADPLLs with (a) divider; and (b) snapshot. 62

4.2 (a) Block diagram of the proposed ADPLL; (b) the timing of snapshot; and (c) the locking process: from BBPD to $\Delta\Sigma$ TDC. 63

4.3 (a) MASH 1-1-1 structure of TDC; (b) architecture of the 1st order $\Delta\Sigma$ TDC. 64

4.4 (a) Transformer based tank; and (b) its input impedance; (c) capacitively coupled transformer based tank; and (d) its input impedance. 66

4.5 Differential trans-conductance schematic. 67

4.6 (a) Simplified schematic of DCO; (b) DCO operates in HB; and (c) LB. . 67

4.7 (a) Schematic; and (b) layout of the LSB of the PVT capacitor bank. (c) Schematic; and (d) layout of the unit cell of acquisition and tracking capacitor bank. 68

4.8 (a) Inductance; and (b) quality factor of the transformer's primary and secondary winding. (c) The coupling factor. (d) Chip micrograph. 69

4.9 PN of the odcillator in the LB. 70

4.10 PN of the odcillator in the HB. 71

4.11 Oscillation frequency dependency on supply voltage for different frequency bands. 72
4.12 Acquisition bank linearity for different frequencies. 72
4.13 Tracking bank linearity for different frequencies. 73
4.14 Chip micrograph of the proposed ADPLL. 74
4.15 (a) Measured phase noise; (b) spectrum of output frequency; and (c) spur level and integrated jitter across channels away from integer-N at 2.00 GHz. 75

5.1 LC-tanks for wide tuning range: (a) resonant mode switching technique [18]; (b) band switching technique [19]; (c) proposed technique. 81
5.2 (a) a transformer-based tank; (b) limited DM and CM TR due C_s, c; 1:2 turn transformer: (c) DM excitation; (d) CM excitation; and (e) tank's input impedance. 84
5.3 (a) Differential and (b) single ended capacitor banks. 85
5.4 Dual core oscillator: (a) schematic; (b) overlap and octave oscillation conditions; and (c) tuning range. 87
5.5 Dual core oscillator waveforms: (a)(b) DM; and (c)(d) CM. 89
5.6 Procedures of referring the noise back to the tank from: (a) r_{ds3} and negative conductance; (b) g_m of M_3; and (c) g_m of M_4. (d) The equivalent circuit of the Colpitts oscillator. 91
5.7 Noise sources of the DM oscillator [22]. 92
5.8 Circuit to phase noise conversion in CM oscillator. 92
5.9 (a) Drain and source voltage waveforms. (b) g_{m3}: theory and simulations. 93
5.10 (a)-(d) Circuit to phase noise conversion in DM oscillator; (e) tail transistor ISF; and (f) PN of CM and DM oscillators at the overlap frequency. . . . 94
5.11 Transformer characteristics. 96
5.12 (a) Measured PN at $f_{DM,max}$, $f_{DM,min}$; (b) $f_{CM,max}$ and $f_{CM,min}$. Measured (c) PN; and (d) FoM at 10MHz offset across TR. Frequency pushing due to supply voltage variation in (e) DM; and (f) CM oscillators. 98
5.13 Return current path in the 1:2 transformer. 99

List of Tables

1.1 Communication standards requirements [10]. 3

3.1 Performance summary and comparison with relevant oscillators. 54

4.1 Performance summary and comparison with state-of-the-art. 74

5.1 Performance summary and comparison with state-of-the-art. 100

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About the Author

Mina Shahmohammadi received the B.Sc. degree in communication systems from Amirkabir University of Technology, Tehran, Iran, in 2005, and the M.Sc. degree in electronics from the University of Tehran, Tehran, Iran, in 2007. From 2007 to 2011, she was with Rezvan Engineering Co. as an analog designer. She was a research assistant with the Electronic Instrumentation Lab at Delft University of Technology from 2011 to 2013, working on resistor based temperature sensors. She joined the Electronics Research Laboratory at Delft University of Technology in 2013, where she is currently pursuing the Ph.D. degree. Her research interests are in analog and RF integrated circuits design.