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Ge, X.

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Temporal Noise Reduction in CMOS Image Sensors

Temporal Noise Reduction in CMOS Image Sensors

Proefschrift

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Xiaoliang GE

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Technische Universiteit Delft, Nederland
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Prof.dr.ir. A.J.P. Theuwissen

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Rector Magnificus,	voorzitter
Prof.dr.ir. A.J.P. Theuwissen,	Technische Universiteit Delft, promoter

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1

Introduction

1

1.1. Background of Low-Noise CMOS Image Sensors

Image sensors are the heart of a digital imaging system. They act as the interface between the optical field and the electric field, converting light information into electrical signals. After half a century of evolution, CMOS image sensors (CISs) have been established as a family of indispensable solid-state imaging devices, by virtue of their massive commercialization and consistent technical innovation. The development of image sensors has never stopped in revolutionizing the technology and expanding the application scopes. In the early days, thanks to the growing demand for portable electronic devices, the low-cost and low-power consumption features of CISs helped them gradually overtake charge-coupled-devices (CCDs) in the commercial market. Nevertheless, the performance of conventional CIS were not on-par with CCD sensors, especially in sensitivity and noise. With a series of remarkable technology breakthroughs, in particular the development of pinned-photodiodes (PPDs) [1], CISs have overcome the performance barrier and began to seize niche market that used to belong CCDs. To date, the applications of CISs have gone beyond photography. The demand for photon-efficient imaging systems keeps growing in many emerging applications, such as space and medical imaging, night vision and diverse scientific imaging, calling for the development of CIS with higher sensitivity and lower noise.

Among these niche applications, single-photon imaging is the holy grail of photon sensing. It is an extension of photon-starved imaging where the systematical sensitivity of photon-detection is enhanced to the level that the arrival of individual photons can be spatially resolved. This ultimate precision photon detection can be utilized in a wide range of applications, from biological imaging to remote sensing. For example, in nuclear medical imaging, single-photon imaging is one of the key technologies that enable human positron emission tomography (PET) and single photon emission computed tomography (SPECT) scan equipment. This equipment is of great significance for the diagonsis and therapy of a variety of challenging diseases, such as cancer, Alzheimer and Parkinson [2]-[3].

One of the most crucial evaluation parameter of the single photon detection confidence level is the CIS pixel's input-referred noise [5]. Given that the electronic charge detection is a statistical process, the sensor may

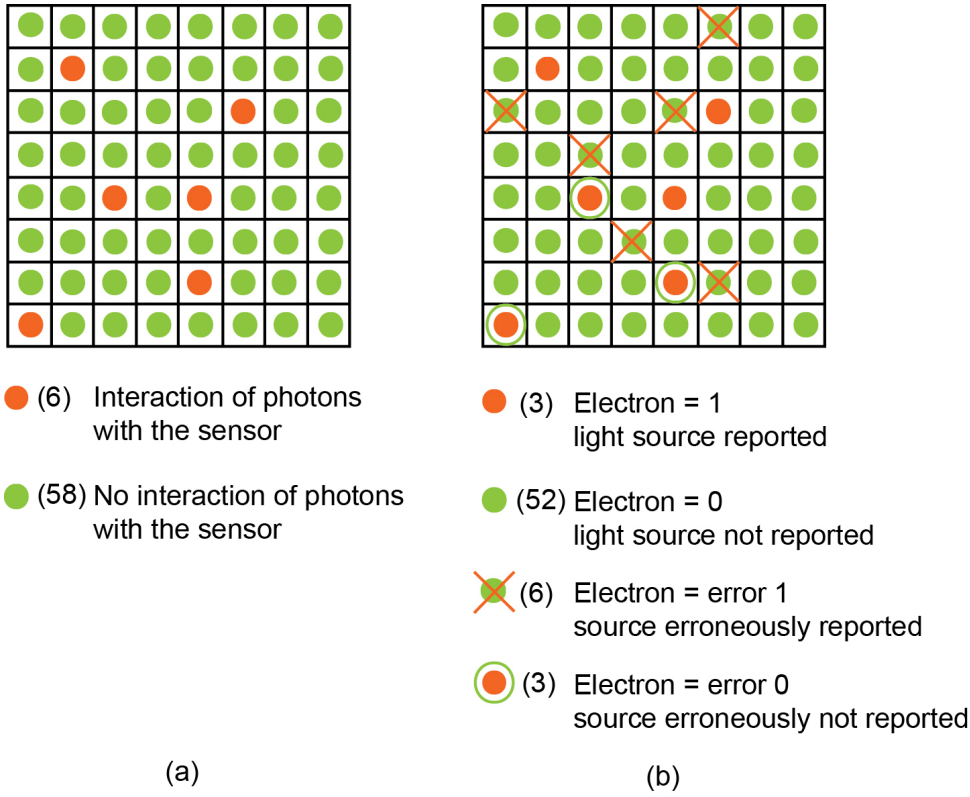


Figure 1.1: Illustration of the consequences of the noisy electronic charge conversion process taking place in the image sensor (redraw from [4])

not be able to identify photons correctly under a low-intensity light condition if the electronic noise of the charge detection process is too large. Figure 1.1 is a graphical illustration of a noisy photon detection process, where (a) represents the distribution of photons interacting with the image sensor and (b) illustrates results of the electronic photon-charge detection within the image sensor [4].

In order to calculate the maximum noise level that can be tolerated in the electronic photon-charge detection process, a Gaussian distribution of detection noise is assumed. The noise probability density function $p_D(x)$ normalized by LSB is then given by [4]:

$$p_D(x) = \frac{1}{\sqrt{(2\pi)} \cdot \sigma_D} e^{-\frac{(x-\mu)^2}{2\sigma_D^2}} \tag{1.1}$$

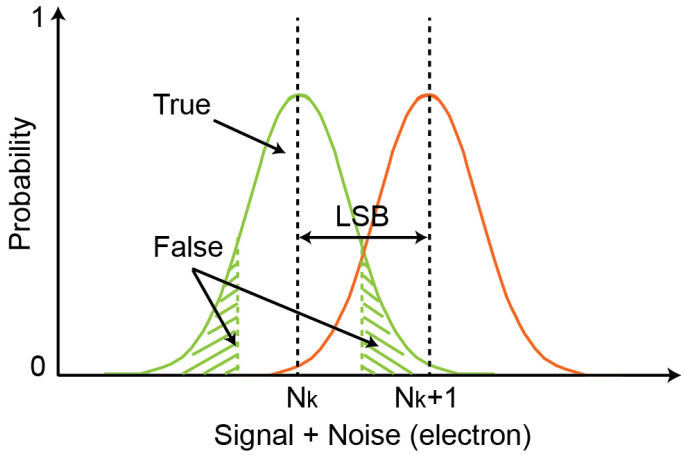


Figure 1.2: Quantization error by noise (redraw based on [5])

where μ = 0 is the mean of the distribution and σ_D is the standard deviation and LSB is the quantization step. Figure 1.2 illustrates the noise distribution at two different quantization levels, where N_k and $N_k + 1$ stands for the k-th and $k + 1$-th quantized level. When the signal is located between $N_k - LSB/2$ and $N_k + LSB/2$, miscounting will not happen and the event will be labeled as "True". When the signal is out of the "True" interval, then the miscounting will occur and therefore the event is labeled as "False". To quantitatively estimate this probability, an expression which describes the probability p of incorrect counting in a pixel can be derived as:

$$p = 2\int_{\frac{1}{2}LSB}^{\infty} p_D(x)dx = erfc(\frac{LSB}{\sqrt{8}\sigma_D}) \tag{1.2}$$

where $erfc$ is the complementary error function. Figure 1.3 presents the probability p dependence over the noise standard deviation normalized by LSB, i.e. σ_D/LSB. The probability is increased when σ_D/LSB is decreased. For a handy calculation, Winitzki's approximation of the error function $erf(x)$ is adopted to assist estimating which σ_D is required to reach a given probability p. As a results, if the case of single-electron detection is assumed, σ_D/LSB should be 0.304 when the true probability is 0.95, which is equivalent to a noise level of 0.304 e^- (LSB = 1 electron).

Currently, single-photon detection is also being pursued by other solid-state imaging techniques, such as single-photon avalanche photodiodes (SPADs) and electron multiplication CCDs (EMCCDs). The

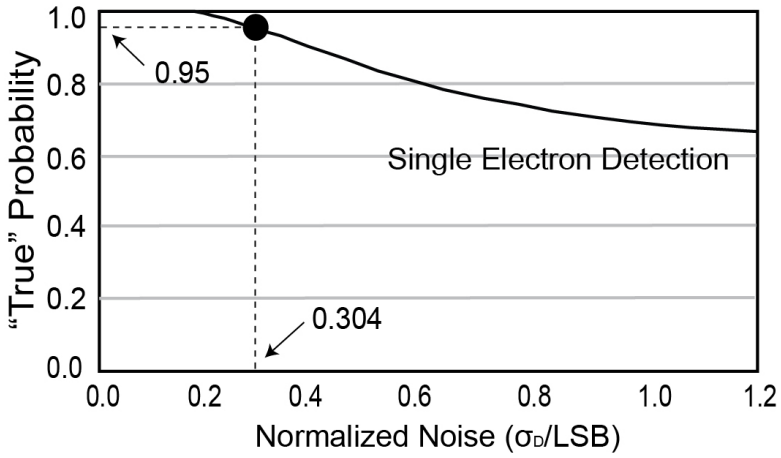


Figure 1.3: Target noise level for photon single electron detection (redraw from [5])

former intensifies the photo-generated signals through impact ionization [10], while the latter does this by triggering an avalanche process [6]. In this way, they show excellent performance with respect to signal-to-noise ratio (SNR) and input-referred noise under photon-starved conditions. However, the limitations of each method are as follows:

- SPADs are not able to integrate the photo-electrons, thus require a counter in each SPAD element to record the output of each readout cycle. This approach enables a high operating speed and temporal resolution, however, also increases the complication of the readout structure in SPAD pixels. What's worse, due to the existence of dead time, the cycle time for these devices is less than 100%. Dark counting also introduces count errors and limits the performance. Furthermore, the light sensitivity is restricted by a low fill-factor and low quantum-efficiency (QE), especially in the range of long wavelength. Finally, the fabrication of high-resolution SPAD in a CMOS process suffers from a relatively low yield [7]-[9].

- EMCCDs usually need extra cooling to avoid the impact of dark current. In addition, they are sensitive to temperature variation and voltage variation of the clock pulses. Furthermore, an aging effect also constrain their on-the-shelf storage period and causes reliability issues. Lastly, their very high operating voltages (up to 50V) makes

it difficult to fabricate EMCCDs in a conventional CMOS process [11]-[12].

In contrast to SPADs and EMCCDs, standard CISs doesn't have the above mentioned drawbacks. Furthermore, since the CIS process is based on well-established CMOS technology, process scaling provides much more potential for the development of CIS. Over the last two decades, the pixel pitch has shrunk significantly, from 8 μm in 2000 to 0.61 μm [13] in 2020. Nowadays, the pixel pitch shrinking race is still on-going and it is difficult to predict its end. On the other hand, the CMOS technology also enables the integration of image sensors with on-chip application-specific integrated circuits (ASICs), which include signal conversion circuits, memories, digital signal processors (DSP), etc.. Such high-level integration not only improves the image quality but also satisfies the growing demands for intelligent sensing functions. Therefore, a low-noise CIS will be an attractive candidate for single-photon imaging and the associated niche applications.

1.2. Challenges and Motivations

As mentioned above, the interest in single-photon imaging has stimulated the research of low-noise CISs. However, the challenge of reducing the noise in a CIS has been around for a long time. The amount of noise from the imager's output signal depends on a number of different noise sources, the origins of which are complicated and often process dependent. All these factors impose a great challenge to realize a low noise CIS.

Table 1.1 gives an overview of different categories of CIS noise sources. In general, the noise generated in the imager can be categorized as temporal noise and fixed pattern noise (FPN), which represent the signal variation in the time domain and the spatial domain respectively. In terms of FPN, this consists of the dark signal non-uniformity (DSNU) and the dark current non-uniformity (DCNU) under dark condition, and the photo-response non-uniformity (PRNU) under illumination. As FPN is fixed in spatial position, it is relatively easy to correct by means of double sampling, calibration or digital signal processing procedures.

Temporal noise is typically recognized as the fundamental limit of the imager performance in terms of noise. It is composed of several major noise components, such as the photon shot noise under illumination, the

Table 1.1: Noise summary

	Fixed pattern noise (FPN)	Temporal noise
Dark	Dark signal non-uniformity (DSNU) Dark current non-uniformity (DCNU)	Dark current shot noise Read-out noise (reset noise, thermal noise, random telegraph signal (RTS) noise, $1/f$ noise)
Illumination	Photo-response non-uniformity (PRNU)	Photon shot noise

dark current shot noise and the read-out noise. The latter generally includes reset noise, thermal noise. random telegraph signal (RTS) noise and $1/f$ noise. Although a number of circuit techniques can be employed to minimize the above noise components, they never come without a cost, as any addition to pixel-level devices, signal readout circuits and signal processing functions may have an impact on the input-referred noise of an imager. Furthermore, temporal noise reduction always comes with tradeoffs between chip area, frame-rate, design complexity, power consumption and cost or risk.

To address these challenges, the pursuit of system-level and circuit-level innovations and optimizations for CIS noise never ends. The motivation of this thesis is to tackle the dominant noise sources in CISs and improve the sensor performance by reducing the sensor's dark temporal noise level with both novel techniques and optimizations.

1.3. Context of the Research

The first high-performance photodiode-type active pixel sensor (APS) for solid-state imaging was successfully demonstrated in 1995 [14]. Fabricated in a 1.2 μm process, this pioneering CIS design adopted a three-transistor (3T) pixel structure with CMOS fabrication facilities. As the reset noise was uncorrelated in this work, designers spent a lot of efforts in investigating and compressing it. Although the later proposed soft reset [15], active reset [16]-[17] and in-pixel capacitive-coupled noise canceller (CCNC) scheme [19] are capable of reducing the reset noise, the remaining noise still constrains the image performance.

Fortunately, it didn't take long time for designers to realize the necessity of migrating pinned-photodiode (PPD) process from CCD to CMOS imagers [1]. In 1997, the first PPD-type CIS with four-transistor (4T) pixel structure was implemented. This work achieved a low dark current level, good spectral response (with shorter wavelength), and most importantly, a low temporal noise level (at the rolling shutter mode). Until now, the 4T pixel scheme is still widely used and quite a lot of innovative pixel architectures are based on this revolutionary design. In contrast with 3T pixels, the reset noise for 4T pixels can be removed completely by correlated double sampling (CDS). Combined with a lower floating diffusion (FD) capacitance and a higher conversion gain (CG), the dark temporal noise level is dramatically reduced. This leaves the $1/f$ and RTS noise from the in-pixel source follower (SF) transistors and thermal noise generated by readout circuits as major noise sources for CMOS imagers. In the following, a brief overview of recently developed CIS noise reduction methodologies will be discussed.

Source Follower Process and Operation Optimization

Beginning from the early 2000s, substantial efforts from a number of research groups have been made to analyze, characterize and model the $1/f$ and RTS noise with various SF transistor sizes [21]-[22], shapes [25], CDS periods [23], extracted time constants [24]-[25] and biasing voltages and currents [27]. The resulting findings are of great importance for understanding the mechanisms of noise and giving insights on the noise reduction for SFs thereafter.

Besides the above-mentioned research efforts, the continuous improvement of CIS process provides the possibility of reducing the process-dependent noise contribution in SFs. Buried channel and its variants with optimized junction profile were reported to be used in a pixel-level SF transistor [28]-[29]. In order to suppress the interface traps-induced noise, the focus of this approach is to move the conducting carriers away from the Si-SiO_2 interface for nMOS transistors. For the same purpose, the pMOS-based pixel was reported, coming along with the development of hole-based PPDs [30]-[31]. Fluorine implantation is another optimization process for SF transistors [32]. By passivating the dangling bonds in the Si-SiO_2 interface with fluorine atoms, the SiO_2 imperfection is mitigated and hence leads to a reduced 1/f noise. Beyond

that, an ultraviolet (UV) annealing process [33] and the hydrogen-assisted low pressure radical oxidation (LPRO) process [34], which are typically applied in CMOS logic and flash process, were also introduced to CIS process form improving the CIS noise performance. Compared to the above mentioned methodologies, the implementation of a thin gate oxide device as SF has been considered as a more economical solution [35]. Such devices have a gate oxide (G_{ox}) capacitance per unit area (C_{ox}) that is higher than the counterparts with a thick G_{ox}. From the well-known flicker noise model [36], $\overline{v_n^2} = K/C_{ox}^2 WLf$, where K is a process-dependent constant, W and L are the width and length of a transistor, f is the frequency, we can see that a higher C_{ox} is advantageous for suppression of the $1/f$ noise portion.

Floating Diffusion Capacitance Reduction

Concurrent with the above advances in process developments for in-pixel transistors, several research groups have been working on the reduction of the floating diffusion (FD) node capacitance, with the motivation of boosting the signal before the occurance of readout noise. To minimize the parasitic coupling capacitance between the transfer gate (TG) and the FD node, an effective technique was proposed in [37]. In this work, the PPD p+ pinning layer is extended to the edge of the FD, forming a fully-depleted-diode between the TG and the FD, which helps to minimize the TG-FD coupling capacitance. Similarly, inspired by a pinned-photodiode pump-gate (PPD-PG) device [38], a vertical transfer pump-gate with a distal FD was demonstrated in a prototype CIS [39]. Furthermore, in order to eliminate the parasitic capacitance between the FD and the reset gate (RST), a tapered reset transistor and a gate-less reset method [40] were proposed. The former one employs a tapered channel on the FD side to reduce the overlap width, and the latter one adopts the punch-through operation to completely remove the RST transistor and its associated parasitic capacitance. In addition, instead of minimizing the TG-FD and RST-FD parasitic capacitance individually, a general solution was proposed in [41] and [42]. In this work, a self-aligned source-drain offset structure is implemented by omitting the lightly doped drain (LDD) implantation and the channel stop under FD, which leads to the decrease of the p-n junction capacitance and the gate overlap capacitance.

Circuit-level Technique for Noise Reduction

Besides process-level explorations, innovative circuit-level solutions and good design practices for noise reduction in a CIS keep emerging.

To achieve a single-photon detection performance, an effective way is to apply high gain at the front stage of the signal path. [43] and [44] attempted to realize a pixel-level open-loop amplification with nMOS and pMOS transistors respectively. Such a pixel architecture could provide a flicker noise limited noise performance, but it is not compatible with a small pixel pitch. As an alternative, in-pixel differential common-source amplifiers were proposed, which are capable of fitting into a pixel size as small as 1.45 μm, while outperforming in terms of noise [45]-[46].

Compared to the pixel-level circuit, integrating a read-out path at the column level further relaxes power and area constraints, therefore provides higher flexibility for noise canceling while maintaining a good trade-off with other key specs. For example, low noise and high dynamic range (DR) are essential specifications for a CIS operating in both dark and bright conditions. Employing an adaptive gain is a very effective approach to achieve both features simultaneously [47]. With the assistance of look-ahead circuits, the readout circuit is switched to a higher gain to reduce the random noise when a pixel signal is lower than a certain threshold level. To avoid exceeding the amplifier output range, the gain is reduced when the pixel signal goes beyond the threshold [48]. Such an approach suppresses the noise while keeping the pixel signal range, leading to a DR that is wider than an ADC-only readout circuit.

Digital correlated multiple sampling (CMS) has been recognized as an effective technique for the suppression of both thermal noise and $1/f$ noise, but at the cost of low frame-rate [49]. To achieve low-noise in high frame-rate applications, several techniques based on the most widely used single-slope (SS) analog-to-digital converters (ADCs) have been proposed. Example include the conditional CMS SS-ADC [50], the gain-adaptive SS-ADC [51], the differential slope with accelerated counter ADC [52], the pseudo-multiple sampling [53], the time-stretched SS-ADC [54], and so on. Besides, quite a few different ADC architectures have been successfully demonstrated to leverage the CMS function while keeping a good frame-rate. Such contributions include the inverter-based $\Delta\Sigma$ ADCs [55], the phase-delay-counting dual-slope ADCs [56] and the folding-integration/cyclic ADCs [57].

State-of-the-art

With the incorporation of continuously developed CIS process and innovative solutions, the past decade has witnessed the realization of several CISs with sub-electron noise performance. These results are summarized in Table 1.2.

1.4. Thesis Organization

This thesis consists of six chapters. The rest of this thesis is arranged as follows.

Exploiting the advantage of a pMOS transistor over its nMOS counterpart in minimizing low frequency noise, a body-effect free pMOS-based SF pixel with standard n-type PPD scheme is proposed in **Chapter 2**. It has been demonstrated in a prototype with a power-supply rejection ratio (PSRR) enhanced single-ended amplifier as the column-parallel readout circuit. The noise performance has been characterized, demonstrating the effectiveness of this technique.

Chapter 3 presents the calculation, the measurement and a comparative analysis of the temporal noise in n-type and p-type pixels. In this chapter, the noise power spectral density (PSD) of in-pixel source followers has been evaluated. Then, the CMS noise transfer function for both cases has been investigated in the frequency domain. Afterwards, a temporal readout noise measurement based on the histogram variance of the output signal for both pixels involving CMS has been performed. The measured results show that the input-referred temporal noise level of n-type and p-type pixels reach 1.1 e^-_{rms} and 0.88 h^+_{rms} respectively.

Based on the analysis and measurement results from Chapter 3, a prototype equipped with a high-gain stage and a digital CMS technique is presented in **Chapter 4**. Implemented in a 65 nm CIS back-side-illumination (BSI) technology, the proposed architecture incorporates a column-parallel inverter-based analog-front-end (AFE) circuit and a digital CMS reference-adaptive $\Delta\Sigma$ ADC along the readout path. This prototype design reaches an input-referred noise of 0.55 e^-_{rms} within a row time of 5 µs.

As mentioned in Section 1.3, an efficient approach to reduce the noise floor is to place a high gain stage as close as possible to the photo-detector as possible. This is demonstrated in **Chapter 5**, where a Gm-cell-based pixel targeting a deep sub-electron temporal noise CIS is presented. To

Table 1.2: Sub-one electron noise results summary

Reference	Noise reduction approach	Read-noise [e^-_{rms}]	Pixel pitch [µm]	Process node [nm]
ISSCC2011 [44]	in-pixel amplifier	0.86	11	180
ISSCC2012 [49]	buried channel SF + CMS + high-gain column amplifier	0.7	10	180
VLSI2015 [58]	high CG (self-aligned S/D offset)	0.5	5.5	180
VLSI2015 [50]	conditional CMS + high-gain column amplifier	0.66	1.1	-
EDL 2015 [59]	high CG (pump-gate with distal FD + tapered reset gate	0.28	1.4	65
IISW2015 [60]	thin oxide layer SF + high-gain column amplifier	0.5	10	180
IISW2015 [61]	inversion-accumulation cycling	0.34	25	180
ISSCC2017 [62]	high CG (reset-gate-less FD)	0.44	11.2	110
IISW2017 [63]	high CG (JFET SF)	0.34	1.4	45/65
IEDM2018 [64]	high CG	0.8	1.5	-
IEDM2018 [65]	high CG	0.68	3	90
IISW2019 [66]	high CG	0.83	2.8	-
ISSCC2020 [46]	in-pixel differential amplifier + CMS	0.5	1.45	90/55
ISSCC2020 [67]	high CG	0.6	3	90/65/40

overcome the trade-off between high DR and low input-referred noise, a pixel-level variable-gain has been realized in a period-controlled manner. As such, the read-out path CG can be programmed according to the specific application of the CIS without any reconstruction of the hardware. This prototype achieves an input-referred noise of 0.5 e^-_{rms} within a correlated double sampling (CDS) period of 5 μs and a row read-out time of 10 μs.

Chapter 6 summarizes this thesis with discussions and a conclusion. Recommendations for future research are also presented.

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2

Temporal Noise Reduction Using pMOS Unity-Gain Source Follower and Optimized Column Amplifier

This chapter is an extended version of the following published article:

- X.Ge and A. Theuwissen, ”A CMOS Image Sensor with Nearly Unity-Gain Source Follower and Optimized Column Amplifier” in *Proc. IEEE SENSORS*, Oct. 2016, pp. 1–3, doi: 10.1109/ICSENS.2016.7808589.

2.1. Introduction

The conceptual diagram of a typical architecture for a CMOS image sensor (CIS) is depicted in Figure 2.1. It consists of several electrical function modules: pixel array, analog signal processor, A-to-D converter (ADC), and digital signal processor, which are the main building blocks that directly process the received optical signal. The digital system controller and the biasing/reference/supply generator are the auxiliary blocks that support and control the signal processing flow of the CIS. In most CIS applications, the imaging quality at low light levels is highly susceptible to noise originating from these blocks, especially from a variety of sources along the signal processing chain[1], both in temporal and spatial domain.

Among these noise sources, the low frequency noise, i.e. random telegraph signal (RTS) noise and flicker noise (1/f), are generated by the in-pixel source follower (SF), and the latter one has been recognized as one of the most significant noise contributors [2, 3]. Despite the fact that the exact physical mechanism for both 1/f and RTS noise is still under debate, it is widely agreed that these low frequency type noises are caused by lattice defects at the interface of the Si-SiO_2 channel of the CMOS transistor [4, 5]. Given the fact that holes have lower mobility than electrons, the rate of trapping/re-emission events for a pMOS transistor is reduced compared to nMOS.

Therefore, implementing a SF with a pMOS transistor can provide a substantial low frequency noise reduction, and so has been investigated in a few recent works [2–5]. However, this approach also suffers from a voltage gain degradation due to the higher body effect trans-conductance of pMOS transistors, which increases the noise contribution of succeeding circuits when referred to the input of the source follower. Thus, a body-effect free design strategy for pixel-level circuit is called for.

Another dominant noise source in the CIS is located at the analog signal processor. In CIS systems with a column-level readout scheme, such an analog processor is usually embodied as a column-parallel amplifier with correlated double sampling (CDS) function. By linearly amplifying the signals from pixel elements, this amplifier provides a proper gain to boost the signal and reduces the noise contribution from the succeeding circuits. In terms of the noise sources of the amplifier, intrinsic noise generated by MOS transistors (inside the amplifier) is certainly one of the main sources.

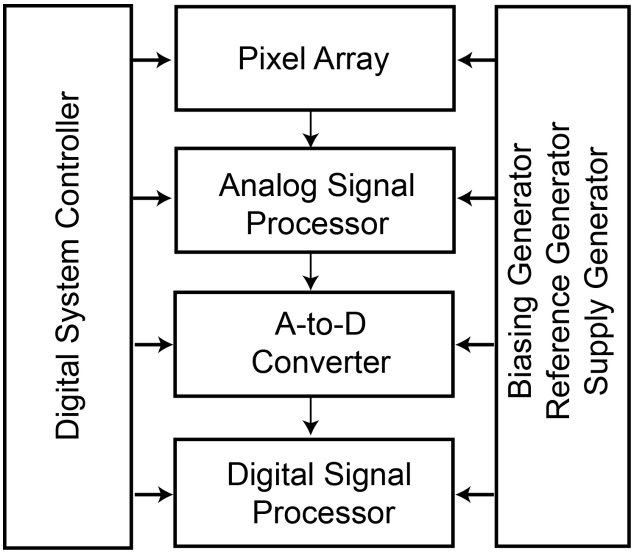


Figure 2.1: Conceptual diagram of a typical CIS architecture

Apart from that, the interference on the supply and ground lines caused by the switching activity of co-integrated digital processing circuits also plays a role, impacting the noise performance of the CIS. Hence, developing and optimizing a low-noise amplifier with improved power-supply rejection ratio (PSRR) and small silicon area becomes the main challenge for a column-parallel analog-front-end circuit of CIS.

In this work, considering the advantage of the pMOS transistor over its nMOS counterpart in minimizing the low frequency noise, we propose to investigate how a pMOS SF without body effect can further reduce the input-referred noise in the CIS. Moreover, in order to improve the PSRR of the column-level analog readout circuits and hence their noise performance, a single-ended cascode common source amplifier with local ground line regulation has been adopted as the operational trans-conductance amplifier (OTA) at the column level [6]. A prototype CIS has been built and fabricated in a 0.18 µm CIS process to prove the concept. Its noise performance has been characterized to further demonstrate the effectiveness of the proposed techniques.

2.2. Sensor Architecture

2.2.1. Pixel Structure

Figure 2.2 and Figure 2.3 show the pixel-level structures of a CIS, which employ nMOS and pMOS as the source follower, respectively. As discussed above, one of the pixel structures dedicated for low-noise CMOS image sensors uses a pMOS transistor as the SF in combination with a standard n-type PPD. In order to maintain the source-body junction reverse biased, the bulk terminal of the pMOS-based SF is conventionally connected to the supply voltage, sharing a common n-well with other pMOS transistors (*RST, RS*) in the same pixel, which results in the body effect.

The MOS body effect trans-conductance g_{mb} refers to the change in the drain current by a change in body-source voltage V_{BS} with all other terminals held at a constant voltage [7]. To account for the fact that this g_{mb} is acting like a second gate, a V_{BS} controlled current source connected between the source and drain terminals can be used to model this dependence in the MOS small-signal model. Also in small-signal analysis, the body effect trans-conductance g_{mb} is often expressed as a fraction of the gate trans-conductance g_m. In an ideal case, the output resistance of both the current source and the SF are infinite, then the voltage gain (A_v) of the source follower approaches $g_m/(g_m+g_{mb}) = 1/(1+\eta)$. According to [7], the ratio $\eta = g_{mb}/g_m$ increases with a higher substrate doping concentration and a lower body-source voltage.

Assume *VPIX* ($VRST_N$ and $VRST_P$ as shown in Figure 2.2 and Figure 2.3) is the reset level of pixel, the V_{BS} for nMOS SF and pMOS SF cases are given as:

nMOS SF:

$$V_{SBn} = (VPIX - V_{GS}) - VSS \tag{2.1}$$

pMOS SF:

$$V_{SBp} = (VPIX + V_{GS}) - VDD \tag{2.2}$$

where V_{GS} is the gate-source potential, VDD and VSS are the supply and ground of the pixel. Then we see that the body-source potential V_{BS} for pMOS SF is typically much lower than that of the nMOS SF. Therefore, the in-pixel pMOS SF suffers from a more pronounced body effect and hence results a much lower voltage gain (Figure 2.4), whose value depends on the input level.

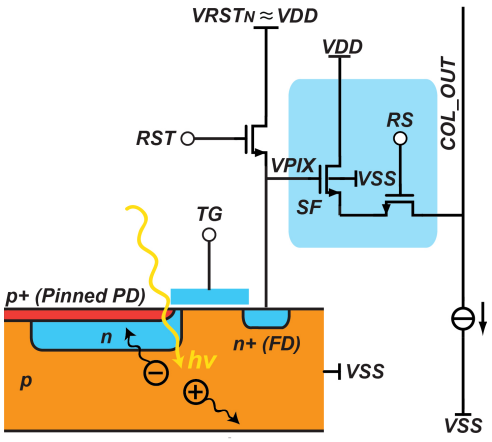


Figure 2.2: Schematic of a nMOS-based SF pixel structure with body effect

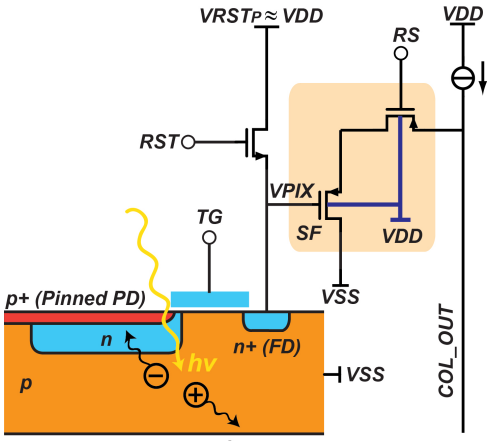


Figure 2.3: Schematic of a pMOS-based SF pixel structure with body effect

As shown in Figure 2.5, an effective approach to eliminate this undesirable body effect of an in-pixel SF is to employ a separated n-well for the SF transistor instead of sharing the common n-well with other in-pixel transistors [8]. Benefiting from this separation, the bulk terminal of the SF can be directly tied to the source terminal. Thus, the contribution of g_{mb} to the overall output trans-conductance of the SF could be ignored. As such, the voltage gain of a pMOS SF without body effect approaches unity. The simulation results show that the proposed SF structure achieves a -95mdB (0.988) voltage gain, which is nearly unity.

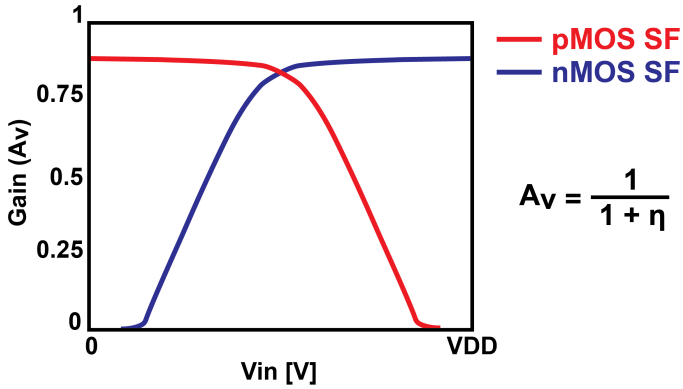
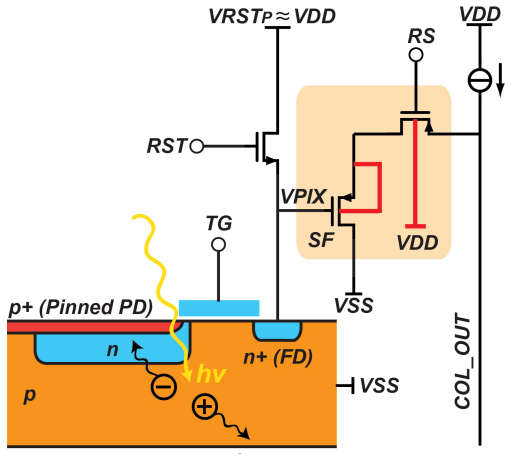
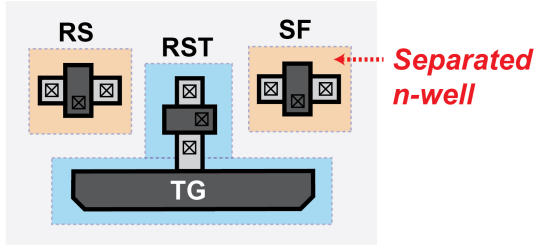


Figure 2.4: nMOS and pMOS SF cases: voltage gain of SF vs. input voltage



(a)



(b)

Figure 2.5: (a) Schematic of a pMOS-based SF pixel structure without body effect and (b) the corresponding in-pixel transistors layout

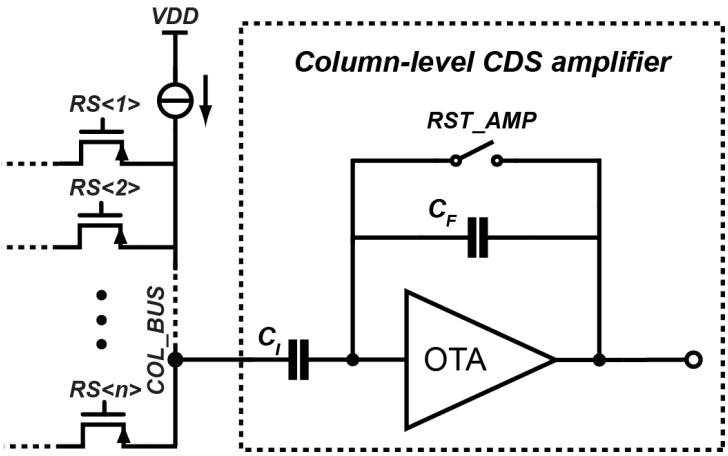


Figure 2.6: The column-parallel amplifier with CDS function

2.2.2. Column Amplifier Structure

Following the pixel-level SF readout structure, the CIS front-end signal conditioning in each column is performed by a switched-capacitor CDS amplifier, as shown in Figure 2.6. In order to achieve an input-referred noise level that is small enough compared to the pixel's output noise, an improved common-source cascode amplifier has been used as the OTA for the column amplifier.

A conventional common-source cascode stage is inherently single-ended and senses the voltage difference between the input node and the ground rail. Accordingly, any noise that appears on the ground rail will also be manifest at the output node. To address this problem, we propose to locally generate a ground rail with a column-level low-dropout (LDO) regulator for each column amplifier, so as to reject interference from the common ground. Due to the fact that the loading currents for this column-level LDO regulator are known and approximately constant, the scheme implementation of this regulator can be kept simple to fit to the column pitch. A single-transistor-controlled (STC) LDO based on a flipped voltage follower [9] is adopted as the topology for the regulator as shown in Figure 2.7. When V_{OUT_REG} varies, M_C provides an error voltage at its drain, so as to control the drain current delivered by M_P and to regulate . With this control, the STC LDO is capable of providing sufficient loop gain and hence provides a PSRR to ground better than -38 dB within the frequency range of interest according to the simulation results.

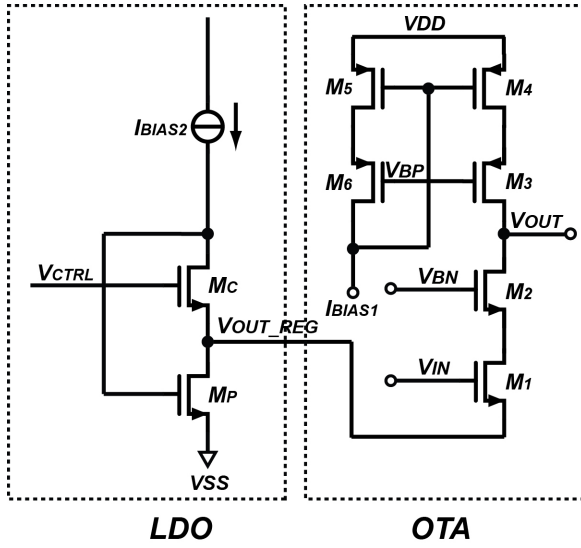


Figure 2.7: Common source cascode amplifier with local ground-rail regulator

2.2.3. Implementation Details

To evaluate the proposed noise reduction techniques, a CIS pixel array has been divided into two sub-arrays, one of which is implemented with the conventional pMOS-based SF structure with body effect as the reference pixel, and the other with the proposed SF structure without body effect. Each sub-array contains 32(H) × 64(V) pixels and features the same pixel pitch of 11 μm. Moreover, the size of the floating diffusion (FD) node and the studied SF transistors for both pixel sub arrays are identical in the layout.

The column-level switched-capacitor amplifiers are placed at the bottom of the pixel array with 11 μm pitch. To enhance the dynamic range of the column amplifier, a programmable gain function is implemented by including switchable input and feedback capacitors. Five gain levels (×1, ×2, ×4, ×8, ×16) are provided, among which the ×16 gain step is designed to achieve the highest sensitivity and the best noise performance.

2.3. Experiment Results

The test sensor with the proposed readout architecture has been fabricated in a 0.18 μm CIS process technology. Figure 2.8 presents a microphotograph of the prototype chip.

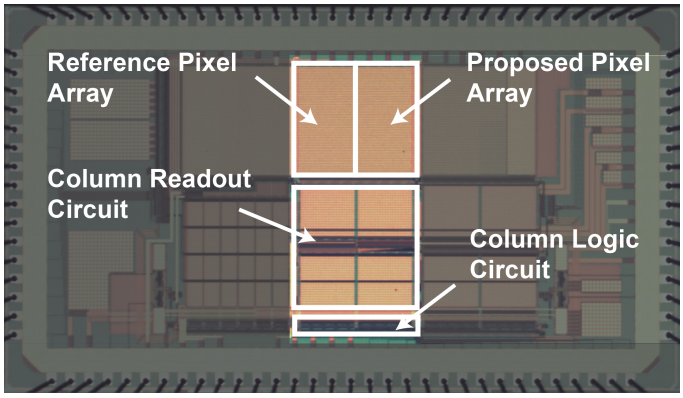


Figure 2.8: Photograph of the prototype sensor

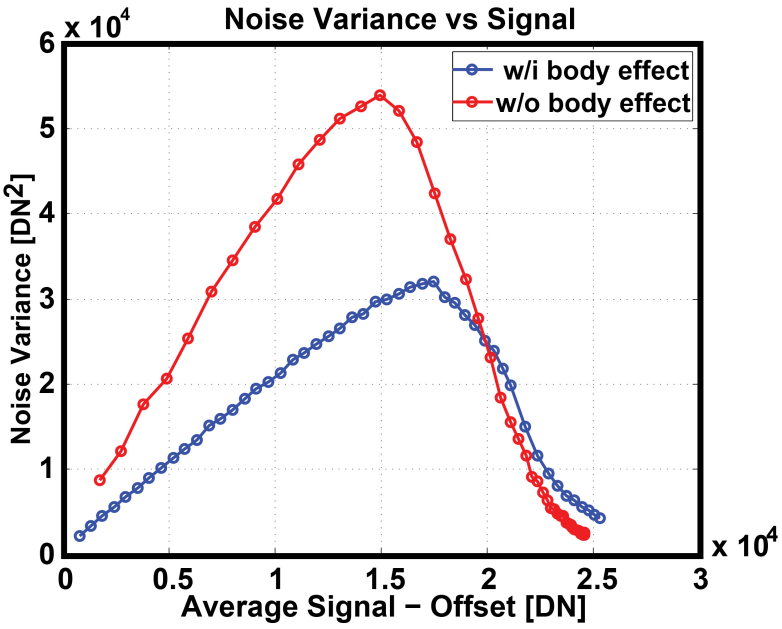


Figure 2.9: Conversion gain for pMOS source follower w/i and w/o body effect.

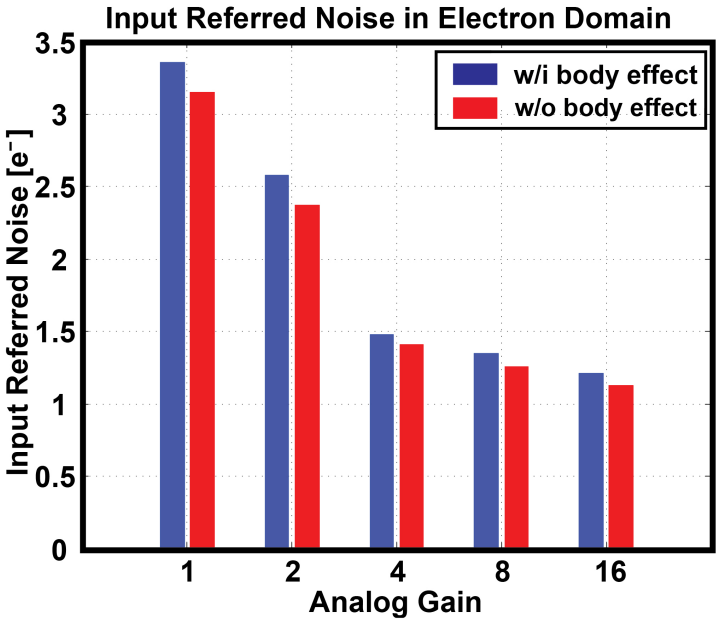


Figure 2.10: Input-referred noise vs. column amplifier gain.

Figure 2.9 shows the measured plot of the noise variance as a function of the average output signal voltage value for both pixels. The conversion gain (CG) after the source follower for the reference pixel with body effect is 71 $\mu V/e^-$, while for the proposed pixel without body effect it is 122 $\mu V/e^-$. As the measured resultant CG is not only determined by the FD capacitance but also is associated to the voltage gain of the source follower. The proposed SF structure improves the conversion gain after the in-pixel SF by 42% compared to the reference pixel.

Temporal noise characterization has been done in dark and implemented by using the reset voltage as an input for the SF and keeping the transfer gate TG and the reset gate RST on during the measurement period. During the measurement, only correlated double sampling (CDS) was implemented. The RMS temporal noise is first measured by a board-level 16bit ADC and then referred to the electron domain by dividing it with the measured conversion gain. Figure 2.10 shows the input-referred noise for proposed pixels as a function of the column-parallel amplifier gain. For the gain steps of 1 and 2, the proposed pixel structure improves the input-referred noise by 10%. As the gain of the column amplifier

increases, the difference of the noise levels between the two types of pixels becomes smaller, which indicates that the effectiveness of succeeding noise reduction by the high gain of the column amplifier becomes dominant. By adopting the proposed pixel structure and amplifier configuration, the prototype CIS features an input-referred noise of 1.1 e^- with a column-level ×16 analog gain.

2.4. Conclusions

A CMOS image sensor targeted for low noise applications has been presented in this chapter. It adopts various techniques both at pixel level and column level, including in-pixel nearly unity gain pMOS-based source followers and improved column-parallel amplifiers. By connecting the body terminal to the source, the loss of voltage gain from unity has been avoided for the in-pixel source follower. A single-ended cascode amplifier with ground-rail regulation is employed to achieve a better PSRR to ground. The prototype sensor with proposed readout architecture reaches a 1.1 e^- input-referred temporal noise with a column-level ×16 analog gain.

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3

Temporal Noise Analysis and Measurement of n-Type and p-Type Pixels with CMS Technique

This chapter is an extended version of the following published article:

- X.Ge, B. Mamdy and A. Theuwissen, ”A comparative noise analysis and measurement for n-type and p-type pixels with CMS technique” in *IS&T International Symposium on Electronic Imaging*, Feb., 2016.

3.1. Introduction

The increasing requirement for better visualizations under low light conditions, especially in medical and diverse scientific fields, calls for the development of low noise CMOS image sensors. Such image sensor will be capable of operating under photon starved conditions and capturing visually distinguishable images, while being more cost efficient, power efficient [1] and providing higher spatial resolution than alternative imaging techniques [2]. Among different noise performance improving techniques and structures, a p-type pixel has been considered as one of the promising candidates for a low-noise CMOS image sensor. Thanks to the combination of a hole-based photo detector coupled with dedicated pMOS transistors, p-type pixels feature several advantages over their n-type counterparts, including lower dark current and better low frequency noise characters [3], [4], as well as more radiation hardness for the p-type pixel. However, compared with nMOS transistors, the use of pMOS as a source follower in p-type pixels suffers from a larger thermal noise due to its lower trans-conductance. Consequently, the doubled thermal noise power after correlated double sampling (CDS), together with the residual 1/f noise power, becomes one of the most significant factors that prevents the temporal noise of p-type pixels from achieving sub-carrier (electron or hole) temporal noise level. Different from doubling the thermal noise caused by CDS, as a circuit level noise reduction technique, correlated multiple sampling (CMS) has proved very effective not only for $1/f$ noise reduction, but also for thermal noise reduction [5]. However, its application to p-type pixels has not yet been analyzed or characterized in the open literature. Hence, an analysis and measurement of the CMS noise reduction effect for p-type pixels in comparison with n-type ones is meaningful for further temporal noise minimization.

In this work, a temporal noise calculation and measurement, as well as a comparative analysis for both n-type and p-type pixels targeted for low noise image sensor application is presented. First, the noise power spectral density (PSD) of in-pixel source followers is evaluated, followed by an analysis of the sources of different noise components, such as thermal noise and 1/f noise. Then, the CMS noise transfer function for both n- and p-type pixels has been investigated in the frequency domain. Afterwards, a measurement of the temporal readout noise measurement based on the histogram variance value of the output signal for both pixels involving

CMS has been performed. The measured results show that the input-referred temporal noise level of n-type and p-type pixels reach $1.1e^-$ and $0.88h^+$ respectively.

3.2. Noise Analysis with CMS Technique

3.2.1. Noise Sources of Pixel

In the following noise calculation, we consider the flicker noise and thermal noise originated from the pixel part as the dominant noise source. Figure 3.1 shows the schematic of source followers used in n-type and p-type pixels as well as the circuit including noise sources. The nMOS MN_1 and pMOS MP_1 are the pixel-level input transistors, while MN_2 and MP_2 serve as the bias current source transistors which are implemented at the column-level, V_{bn} and V_{bp} are the equivalent biasing voltage for the current sources, V_{in} is the input voltage, V_{outn} and V_{outp} are the output voltages. In the noise model, g_{mn1}, g_{mn2}, g_{mp1} and g_{mp2} are the trans-conductances, $V^2_{n,np}$, $V^2_{n,pp}$, $I^2_{n,nc}$, and $I^2_{n,pc}$ are the noise sources, the output noise is expressed as $V^2_{n,n}$ and $V^2_{n,p}$.

An established fact for in-pixel source followers is that the driving source impedance is moderate while the input impedance is quite high. Therefore, in this noise model, the input-referred noise current source can be neglected, and only the noise voltage source needs to be taken care of [6]. Assuming that all transistors operate in saturation, the noise PSD for n-type [7] and p-type source followers can be represented as:

$$S_{n,n}(f) = \overline{v^2_{n,n}} = \frac{3}{8}kT\frac{1}{g_{mn1}}(1+\frac{g_{mn2}}{g_{mn1}}) + [N_{fmn1} + N_{fmn2}(\frac{g_{mn2}}{g_{mn1}})^2]\frac{1}{f} \quad (3.1)$$

$$S_{p,n}(f) = \overline{v^2_{n,p}} = \frac{3}{8}kT\frac{1}{g_{mp1}}(1+\frac{g_{mp2}}{g_{mp1}}) + [N_{fmp1} + N_{fmp2}(\frac{g_{mp2}}{g_{mp1}})^2]\frac{1}{f} \quad (3.2)$$

where $k = 1.3807 \times 10^{-23}$J/K is the Boltzmann constant, T is the absolute temperature, f is the frequency, and N_{fmn1}, N_{fmn2}, N_{fmp1} and N_{fmp2} are the flicker noise parameter of MN_1, MN_2, MP_1 and MP_2, respectively.

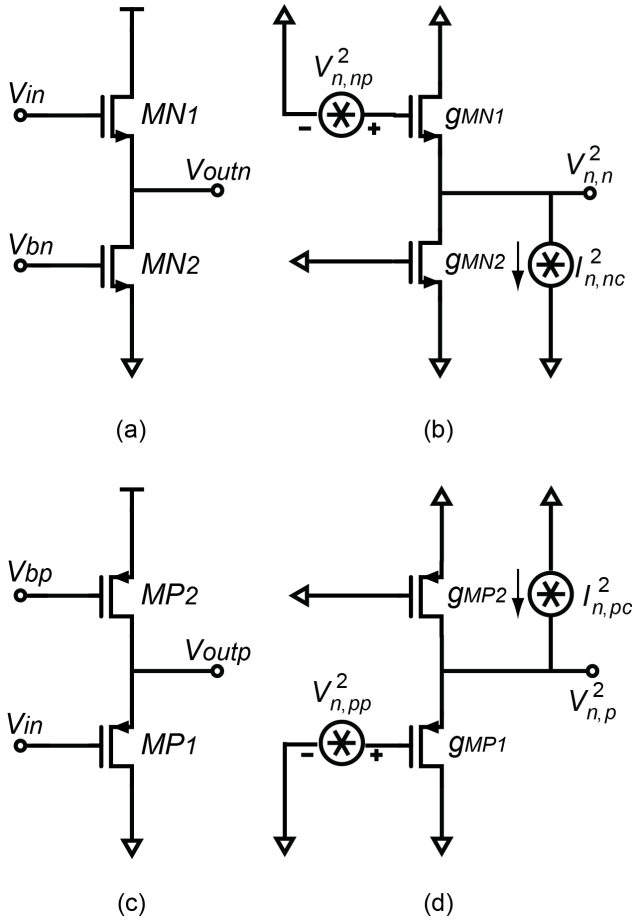


Figure 3.1: Source follower schematic and equivalent circuit for noise analysis. (a) n-type source follower; (b) n-type source follower including noise sources; (c) p-type source follower; (d) p-type source follower including noise sources.

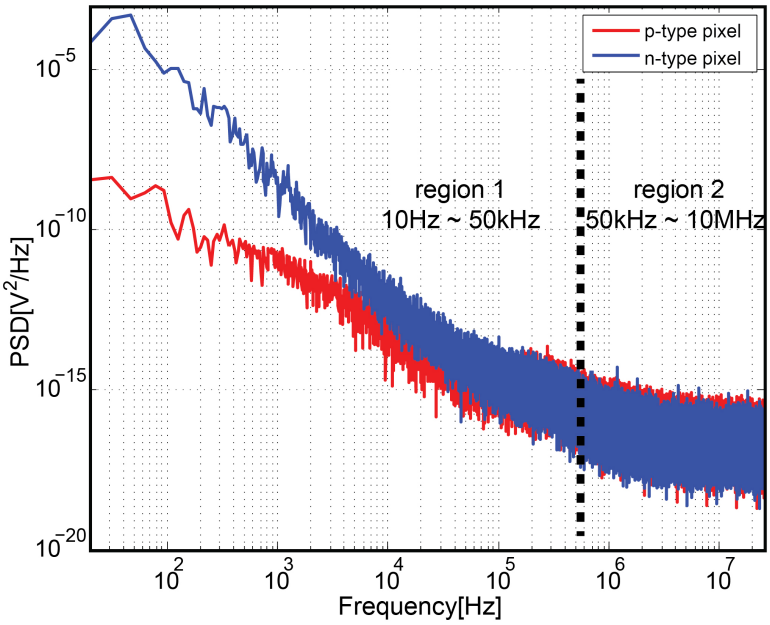


Figure 3.2: The noise PSD for the n-type and p-type pixel.

The noise PSD of the p-type and n-type pixels have been first extracted from the measurement. The measurement details will be mentioned in Section 3.4. As shown in Figure 3.2, the p-type pixel exhibits less 1/f noise power density in the low frequency region than the n-type one, due to a naturally formed "buried channel" inside the pMOS transistor, which could carry the holes in the channel at some distance from the "dirty" silicon oxide-silicon interface.

Moreover, the thermal noise or the noise floor is also obtained from the extracted data, which are 1.68×10^{-15} V^2/Hz for the n-type source follower and 2.76×10^{-15} V^2/Hz for the p-type one respectively. The thermal noise PSD in this feature is due to the fact that the thermal noise of source followers is determined by the trans-conductance g_{mn1} and g_{mp1}. If the input transistors in the n-type and p-type pixels have the same width/length ratio and are biased with the same current, g_{mp1} for the pMOS transistor will be smaller than g_{mn1} as a result of a lower carrier mobility of the holes.

3.2.2. CMS Operation and Noise Reduction Effect

The CMS operation has been considered as an alternative to the CDS operation for CIS system [8]. The sampling diagram of CMS operation for CIS is depicted in Figure 3.3. In Figure 3.3, T_0 is the sampling period; $T_g = M_g T_0$ is the interval period between two groups of multiple sampling, where M_g is an integer. Firstly, reset levels ($V_{rst,1}, V_{rst,2}...V_{rst,M}$) and signal levels ($V_{sig,1}, V_{sig,2}...V_{sig,M}$) are sampled for M times sequentially. The delay between each correlated sampling levels (e.g. $V_{rst,1}$ and $V_{sig,1}$, $V_{rst,2}$ and $V_{sig,2}$) is $(M + M_g)T_0$. Then, the sum of reset levels and signal levels, which are obtained from M-times sampling, are subtracted from each other. Finally, the output signal can be derived by dividing the differential result by the factor of M. As such, the correlated noise and the low frequency noise can be eliminated and reduced by the subtraction or differentiation in a way similar to standard CDS. In addition, the input-referred thermal noise amplitude also gets a reduction with a factor that is inversely proportional to $\sqrt{M}$ thanks to the averaging effect [8]-[10].

Due to the differentiation and averaging procedures in the CMS configuration, the effectiveness of the CMS noise canceller can be characterized as a pass-band narrowing operation, or a noise power density reduction operation by oversampling [11]-[12].

Let's first consider that the noise reduction effect of CMS as the result of the bandwidth-narrowing operation. As interpreted by Figure 3.4, in the initial sampling phase, the signal is first sampled by the sampling circuits with a cut-off frequency f_c. Next, the operation of subtracting two correlated levels can be interpreted as a discrete time high-pass filter with an equivalent cut-off frequency f_l, which corresponds to the time interval between two group sampling operations. Finally, the output noise power are low-pass filtered for the second time with another equivalent cut-off frequency $f_h \gg f_c$ by virtue of the bandwidth limitation effect. Therefore, the entire CMS operation is equivalent to a continuous time band-pass filter whose first zero f_l and first pole f_h are respectively located at:

$$f_l = \frac{1}{2\pi(M + M_g)T_0} \tag{3.3}$$

$$f_h = \frac{\sqrt{2}}{\pi(M + M_g)T_0} \tag{3.4}$$

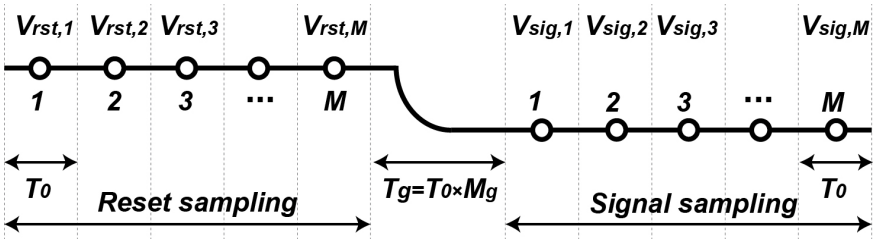


Figure 3.3: The sampling diagram of CMS operation

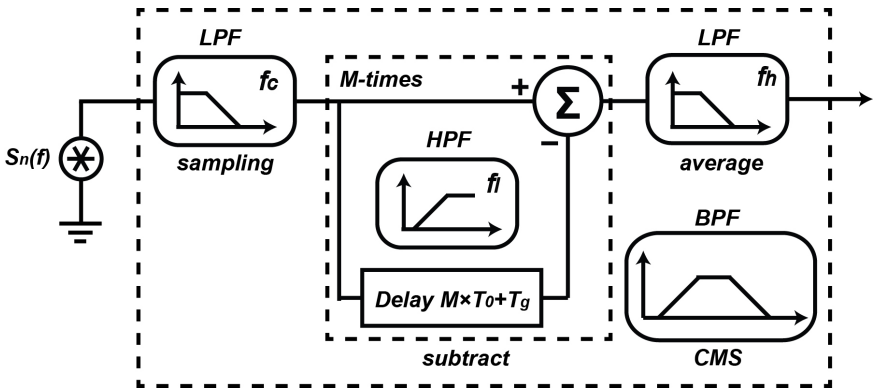


Figure 3.4: The simplified model of a CMS circuit

As such, the bandwidth of the band-pass filter can be defined as:

$$f_h = \frac{2\sqrt{2}-1}{2\pi(M+M_g)T_0} \tag{3.5}$$

Figure 3.5 shows the equivalent transfer function of the CMS band-pass filter as a function of $(M + M_g)T_0$. With a fixed sampling period T_0, and a decreasing M, the pass-band shifts to a higher frequency band with a widened bandwidth. Consequently, more low frequency noise could be attenuated, while more thermal noise in the high band will be integrated due to the wider bandwidth. On the other hand, if M is a constant value and T_0 increases, both the resonant frequency and the pass-band will be shifted along with the sampling period. Thus, the effectiveness of noise reduction for both 1/f noise and thermal noise is greatly depending on M or T_0.

Instead of considering the CMS thermal noise reduction effect as a bandwidth narrowing operation, it can also be characterized as an oversampling operation, i.e. applying a sampling frequency higher than the

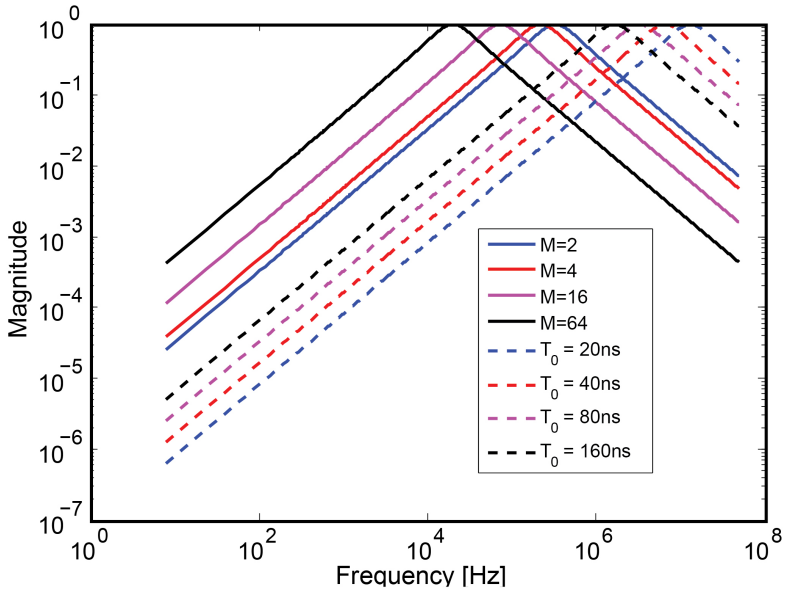


Figure 3.5: Equivalent CMS band-pass transfer function

Nyquist rate. If the sampling rate of CMS is increased from the Nyquist criterion $f_{s,ny} = 1/(M + M_g)T_0$ to a new frequency $f_s = 1/T_0$, the noise power density of the white band thermal noise is reduced with the ratio of the sample rates, N, where

$$N = \frac{f_s}{f_{s,ny}} = M + M_g \tag{3.6}$$

Therefore, with a fixed sampling interval $(M + M_g)T_0$, as M increases, the thermal noise is reduced by a factor of $\sqrt{M}$ while the reduction of the 1/f noise in the low frequency region keeps the same for different M. Accordingly, for a given sampling interval, with a larger value of M and a shorter sampling period T_0, a relatively smaller thermal noise can be obtained without sacrificing the reduction of the 1/f noise.

3.3. Noise Calculation with CMS Technique

Based on the above analysis, the post-CMS noise behavior for both n-type and p-type pixels can be modeled in MATLAB by calculating their output noise power spectrum density $S_n(f)$ as well as the noise transfer function,

and their final integrated noise power can be estimated. The input noise PSD $S_n(f)$ used in this calculation is extracted from the test chips as presented in Section 3.2.1. Furthermore, the output noise power spectrum after CMS process can be expressed in frequency domain as:

$$\overline{v_{n,CMS}^2} = \frac{1}{M^2}\int_0^\infty S_n(f)\frac{1}{1+(f/f_c)^2}|H_{CMS}(f)|^2 df \qquad (3.7)$$

where $H_{CMS}(f)$ equals to:

$$|H_{CMS}(f)| = |\frac{2sin(\pi f \cdot MT_0)sin(\pi f \cdot (M+M_g-1)T_0))}{sin(\pi f \cdot T_0)}| \qquad (3.8)$$

Figure 3.6 to Figure 3.8present the calculated results. In Figure 3.6 (a) and (b), the noise PSD for both type pixels are calculated by using the constant sampling period T_0= 100 ns and a variety of values for the number of sampling times M = 2, 4, 16 and 64. Note that as M increases, the noise PSD decreases at higher frequency region and increases at lower frequency region. This indicates that as a result of a longer interval period $(M+M_g)T_0$,with M increasing, the 1/f noise suppression effect by CMS operation declines while the thermal noise reduction tendency remains.

Figure 3.7 (a) and (b) shows the noise PSD as a function of sampling period T_0= 200 ns, 400 ns, 1600 ns and 6400 ns with a constant sampling number M = 4. The noise PSD reduction for both 1/f noise and thermal noise are primarily consistent with the results in (a) and (b), This indicates that, for a constant sampling number M, increasing T_0 also leads to a lower resonant frequency for the pass-band bandwidth, thus reducing the effectiveness of CMS for 1/f noise reduction.

As shown in Figure 3.8 (a) and (b), the noise PSD is obtained as a function of M_g = 2, and M = 2, 4, 16 and 64 within a fixed sampling interval $(M+M_g)T_0$ = 6.4 µs. Significant noise reduction in the high frequency region can be observed, while the noise PSD in low frequency region keeps almost the same with variant M. Thus, thanks to the oversampling operation, the wide-band thermal noise can be effectively compressed with an increased M, while the effectiveness of low frequency noise reduction stays the same.

In order to clarify and estimate the residual value of different noise components after CMS operation; the noise PSD in different frequency regions (e.g. region 1 and 2, as shown in Figure 3.2) has been integrated

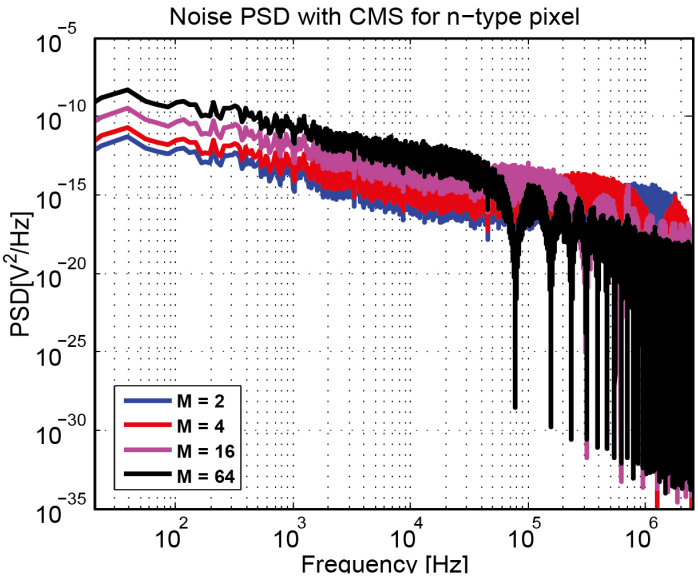


Figure 3.6: Noise PSD for (a) n-type pixel with a sampling number M = 2, 4, 16, 64 and sampling period T_0 = 100 ns; (b) p-type pixel with a sampling number M = 2, 4, 16, 64 and sampling period T_0 = 100 ns.

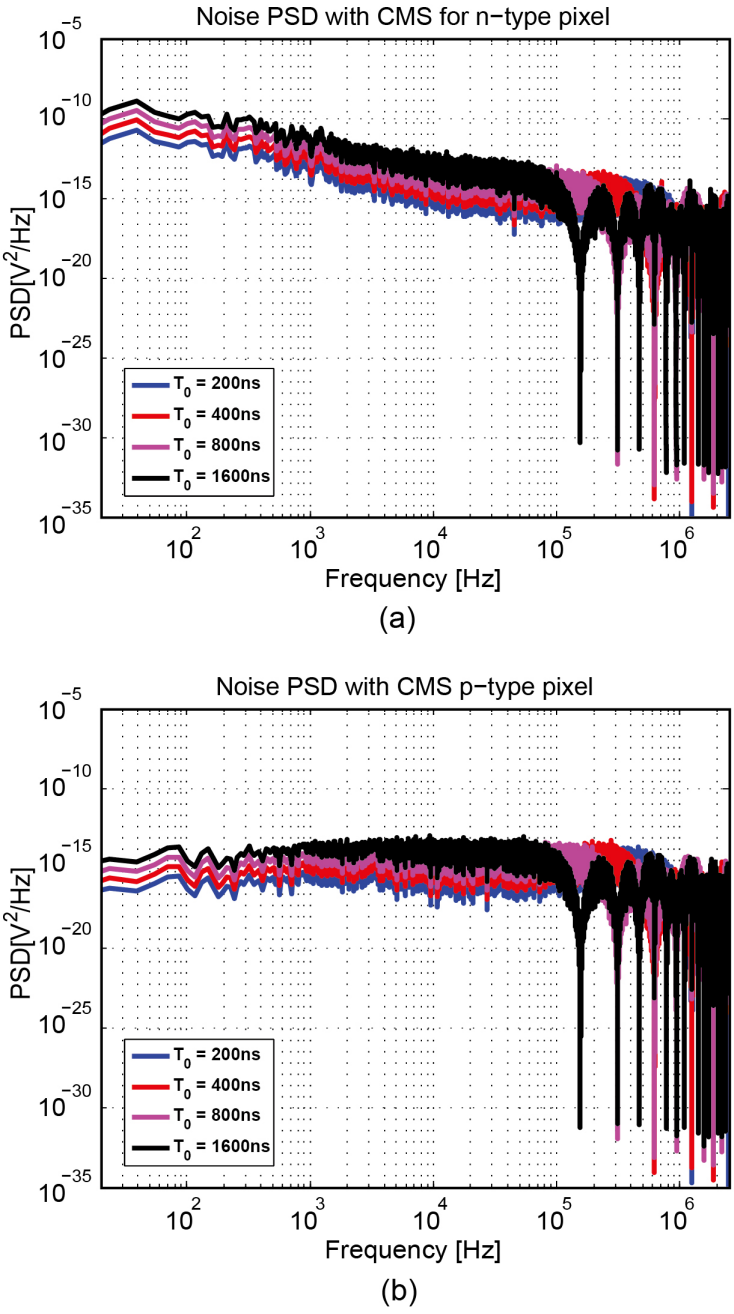


Figure 3.7: Noise PSD for (a) n-type pixel with a sampling period T_0 = 200 ns, 400 ns, 800 ns, 1600 ns and sampling number M = 4; (b) p-type pixel with a sampling period T_0 = 200 ns, 400 ns, 800 ns, 1600 ns and sampling number M=4.

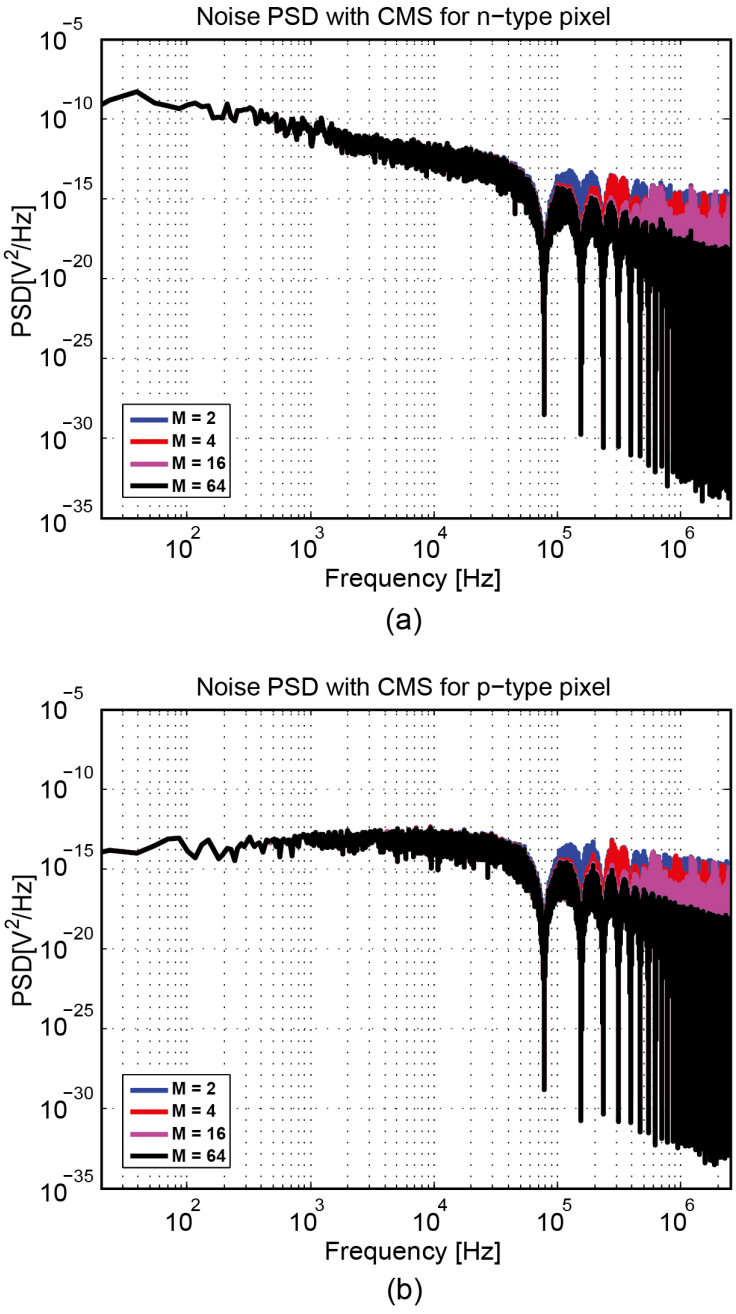


Figure 3.8: Noise PSD for (a) n-type pixel with a sampling number M = 2, 4, 16, 64 and $(M + M_g)T_0$ equals to a constant 6.4 µs; (b) p-type pixel with a sampling number M = 2, 4, 16, 64 and $(M + M_g)T_0$ equals to a constant 6.4 µs.

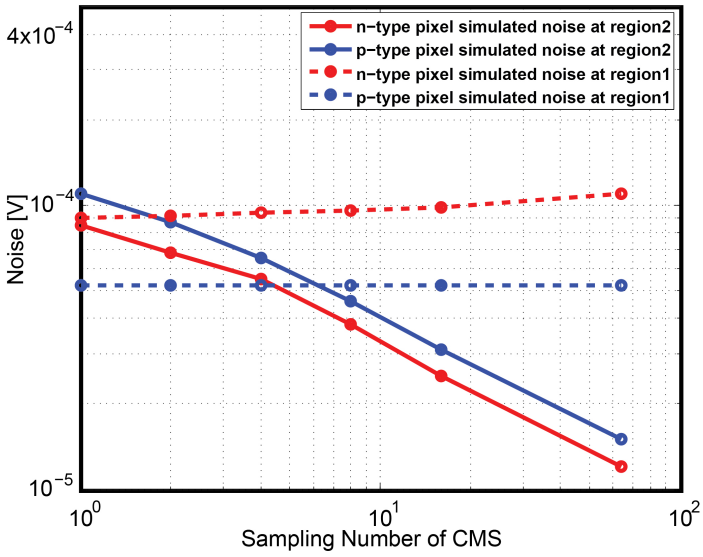


Figure 3.9: Integrated simulated noise for n-type and p-type pixel at region1 and region2

separately. Figure 3.9 compares the n-type and p-type noise in each region after CMS operation as a function of M, where M = 1, 2, 4, 8, 16, 64 and T_0= 100 ns. At M = 1, the integrated noise in region 1 for the n-type transistor is higher than that of the p-type noise, and lower in region 2, which indicates that a n-type pixel has a larger 1/f noise while a p-type pixel suffers from a higher thermal noise, as has been analyzed in Section 3.2.1. As M increases, on one hand, the integrated noise level in the high frequency region (region 2) for both types of pixels is suppressed until M = 64, with a factor of 72% for the n-type pixel and 80% for the p-type pixel respectively. On the other hand, the integrated noise amplitude in the low-frequency region (region 1) is slightly increased in proportion to M. These results suggest that it is the low frequency noise that limits the total noise reduction effect of the pixel source follower.

In summary, based on the above calculation, by means of the CMS operation, the final noise reduction factor is 31% for the n-type pixel and 50% for the p-type.

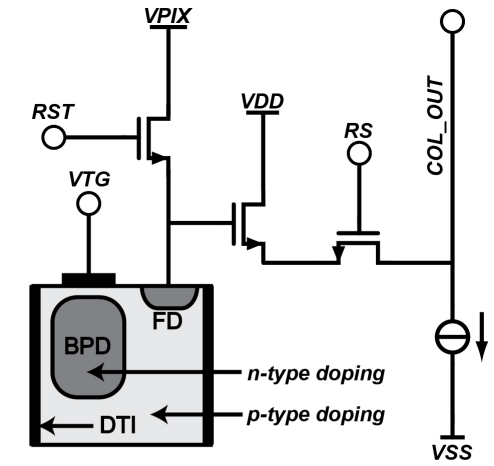
3.4. Noise Measurement with CMS Technique

To evaluate the CMS noise reduction effect for p-type pixels in comparison with n-type ones, 2 sub-groups of pixels have been implemented in the test chip. One of which is fabricated with n-type pixels process and the other one with p-type pixel process. The front-end-of-line (FEOL) and back-end-of-line (BEOL) of both pixel types were designed and processed respectively in 90 nm and 65 nm technology, respectively. Both sub-groups feature the same pixel pitch of 2.5 µm. As shown in Figure 4.2 (a) and (b), the 3D pixel structure isolated by deep trench isolation (DTI) technology integrates a back-side-illuminated buried vertically pinned-photodiode (BPD) as well as a planar transfer gate (TG) in each pixel [13, 14]. Unlike the arrayed image sensor, the test chip includes only one effective pixel for each test structure owing to the area limitation. For both pixels, the gate width and length of the studied SF transistors are 0.2 µm/0.7 µm. The current sources for both SFs are set to 2 µA.

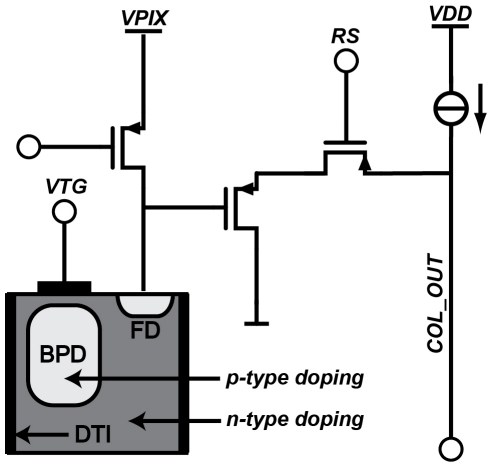
In comparison with standard n-type pixels, all doping species type used to form the BPD and TG are inverted in the p-type pixel and the in-pixel MOS transistors are also switched from nMOS to pMOS. Hence, as can be seen from Figure 3.11, the transistor gate in the p-type pixel has to be driven low to switch on and high to switch off, while the other timing details remains the same.

Temporal noise characterization has been performed in dark by employing the reset voltage (VPIX) as the SF input, while keeping TG off and RST on during the entire measurement period. In order to reduce the impact of the PCB noise, an off-chip PGA with a gain of 6 has been implemented in the readout chain. The rms temporal noise is first measured by a board-level 16bit ADC and then referred to the carrier domain by dividing it with the measured conversion gain (CG). A sampling period T_0 = 100 ns, which is the same as the value used in the calculation, is applied for both test chips. Instead of running a statistical analysis of spatial dispersion, the noise value given here is the histogram-based (fit to a Gaussian-like distribution) variance value of the output signal.

Figure 3.12 shows the measured plot of the noise variance as a function of the average output signal voltage value for both pixels. The conversion gain for the n-type and p-type pixel are measured as 153 µV/e^- and 110



(a)



(b)

Figure 3.10: Schematic with cross-section of BPD and TG region as well as readout architecture (a) n-type pixel; (b) p-type pixel.

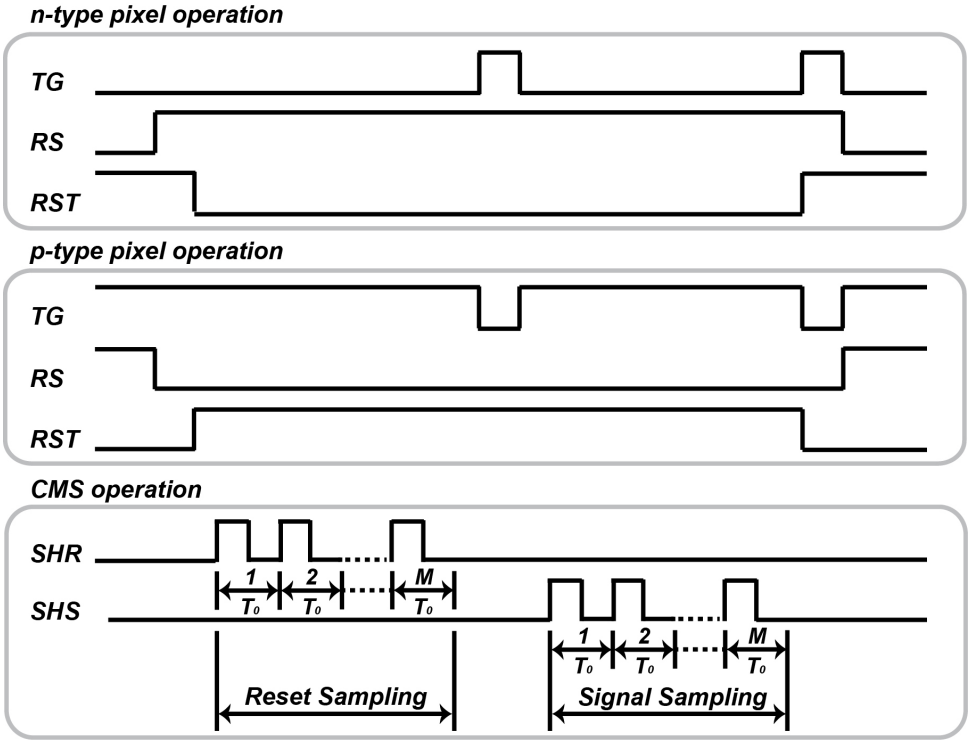


Figure 3.11: Timing diagram of the readout sequence for n-type pixel, p-type pixel and CMS operation.

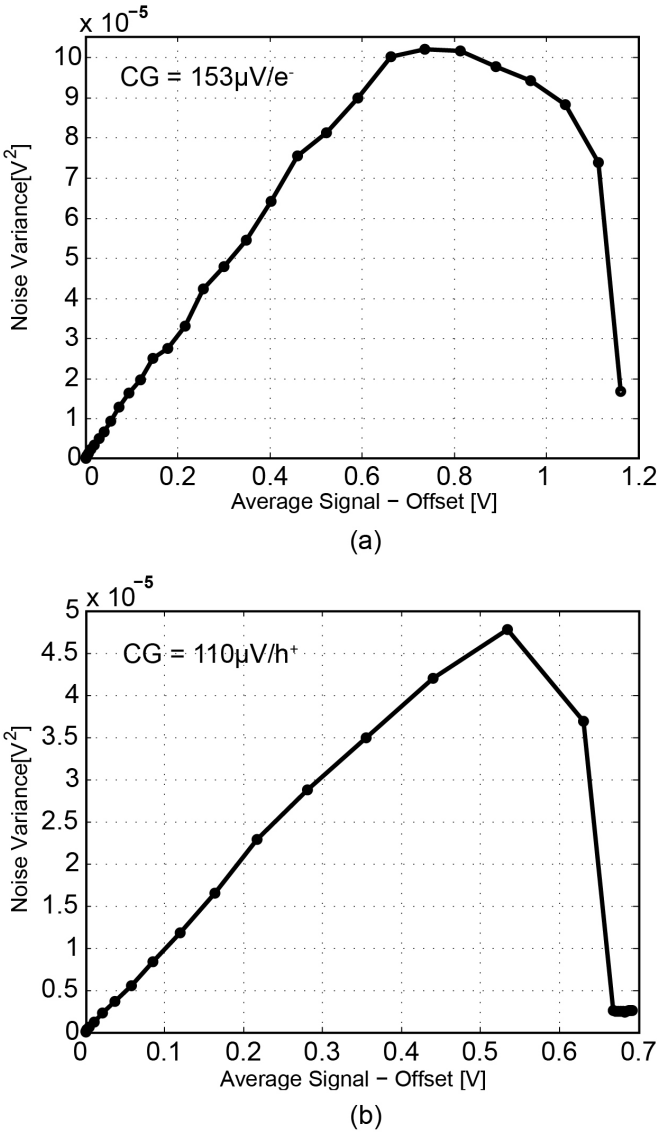


Figure 3.12: Conversion gain for (a) n-type pixel; (b) p-type pixel

$\mu V/h^+$ respectively.

Figure 3.13 shows the measured input-referred noise for both the n-type and p-type pixels with a comparison to the simulation results in both the voltage and the carrier domain. In the calculation results described above, noise due to the sample and hold process is ignored. Owing to omission of the aliasing effect in the calculation, there exists a deviation between the simulated and measured values, which is around 20% for the n-type pixel and 22% for the p-type pixel. However, the measured and calculated results show a good agreement in the noise reduction factor by CMS for both types of pixels, demonstrating the validity of the presented noise methodology.

As predicted by the noise calculation, the measurement result shows a noise reduction tendency as the sampling number of CMS increases. Moreover, it also indicates that the low-frequency random noise of the pixel source follower limits the noise reduction effect as the number of sampling times increases. As shown in Figure 3.13 (a), compared to the p-type pixel, the n-type pixel shows a saturation of the noise improvement tendency from 8-times CMS. However, the p-type pixel elevates this saturation level up to 64-times thanks to a lower 1/f noise coefficient. Comparing the input-referred noise with digital-only CDS, the CMS noise reduction factor is around 24% for n-type pixels and 45% for p-type pixels with 64-times CMS applied. For M = 1, 2, 4 and 8, the noise level in the charge domain for an n-type pixel is lower than that for a p-type pixel thanks to a larger CG. However, for M = 16 and 64, the residual 1/f noise in nMOS SF constraints further noise reduction and the noise level of the p-type pixel becomes lower than that of the n-type one. As indicated in Figure 3.13 (b), for M = 64, the n-type pixel features an input-referred noise of 1.1e^-_{rms} and the p-type pixel shows a lower noise level at 0.88 h^+_{rms}.

In conclusion, both simulated and measured results reveal that the incorporation of a CMS operation and a p-type pixel is capable of realizing better noise reduction as compared to the n-type one.

3.5. Conclusions

In this chapter, we first explored the noise reduction effect of CMS on the noise PSD of n-type and p-type pixels. Based on the noise PSD and the transfer function of CMS, the residual noise of both types of pixels has been calculated. Subsequently, we measured the temporal noise of the n- and p-type pixels with a CMS technique. A good agreement between calculated

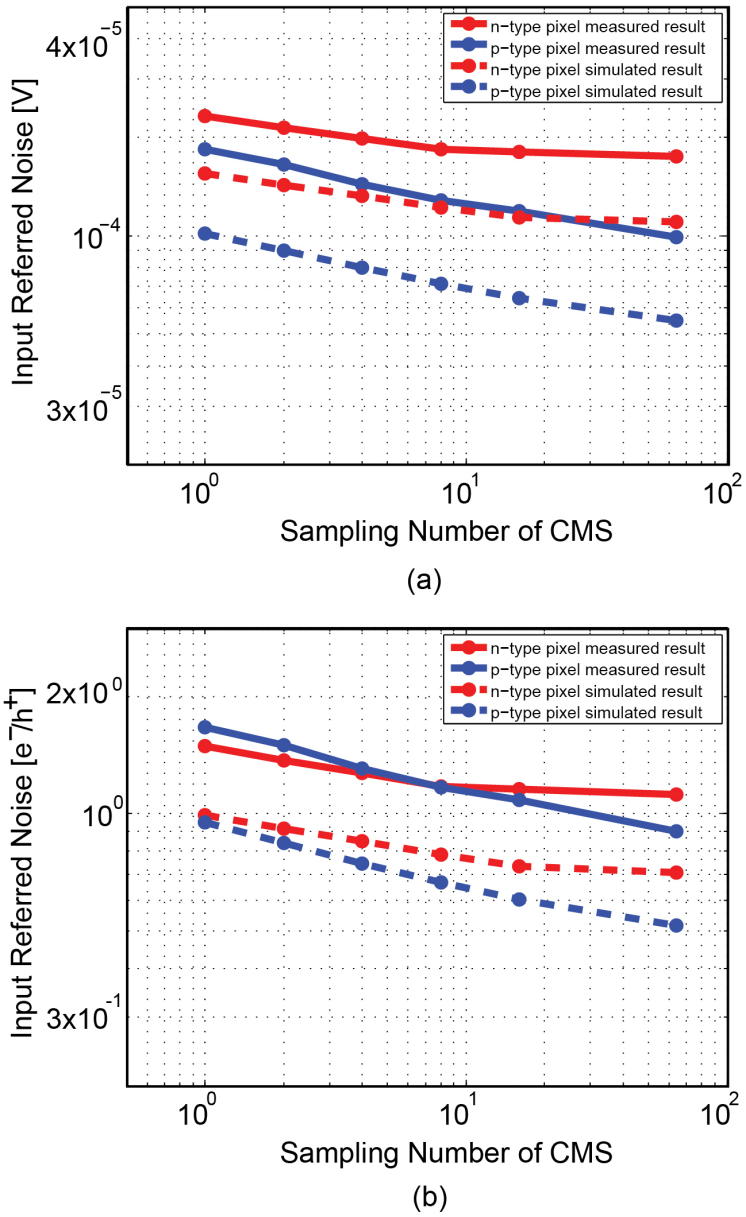


Figure 3.13: Input-referred noise for measured and simulated results (a) in voltage domain; (b) in charge domain.

and measurement results shows that the noise performance improvement brought by CMS has been demonstrated theoretically and experimentally. With a board-level ×6 analog gain, the noise reduction factor for the n-type pixels is 24% and for the p-type pixels is 45%, and as a result of that, the n-type and p-type pixel achieve a temporal noise level of 1.1 e^-_{rms} and 0.88 h^+_{rms}respectively after 64 times digital CMS during the readout phase.

3.6. Discussion

In general, the flicker noise PSD falls off at 10 dB/decade of frequency. Based on the post-review of the flicker noise measurement results for both n-type and p-type pixels, however, the nominal slopes of the PSD shown in Figure 3.2 do not comply with this trend. Instead, the p-type pixel noise PSD follows the slope of $1/f^2$, while the one of n-type pixel follows $1/f^4$. In addition, as described in equation (3.8), the CMS transfer function should has a zero when f = 0 Hz, thus, the remaining flicker noise after CMS would be zero in theory. On the contrary, the trace of the residue flicker noise PSD (shown in Figure 3.6 to Figure 3.8) is horizontal for p-type pixel and upward inclined for n-type pixel at low frequency region. These kinds of trace can only be seen when the PSD of the noise is $1/f^2$ or $1/f^4$[15].

There are a few of hypothesis that could explain this measurement artifact. One possible reason is the RST transistor might contribute an extremely high noise and impact the flicker noise PSD extraction. However, in order to employ the reset supply voltage as the source follower input, the RST transistor was kept constantly on during the noise measurement. The impedance of either nMOS or pMOS transistor (switch-on state) would not be able to generate a so high thermal noise.

Another suspected root cause is the board-level devices might introduce high noise, leading to an interference on the flicker noise PSD measurement. As mentioned in section 3.4, due to the area limitation, all the peripheral and auxiliary circuits can only be outside the chip and be on a PCB board. Any noise come from the board-level devices, routings or interfaces may couple to the test-chip or directly impact the noise results.

A low PSRR design of this test-chip may also be one of the reason cause this measurement artifact. Since the in-pixel source follower is single-ended, when we collect the flicker noise data without CDS function, the output of the pixel is relatively vulnerable to any variations on the supply.

Based on the above discussion, in order to get an accurate flicker noise measurement, a higher-level integrated image sensor with well PSRR design, instead of a single pixel test-chip, is strongly recommended.

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4

Temporal Noise Reduction Using Programmable-Gain Amplifier and Digital CMS Reference-adaptive ADC

4.1. Introduction

Advanced imaging systems for high-end applications, such as scientific and medical imaging, demand high-sensitivity CMOS image sensors (CIS). The noise performance of such CISs usually determines the ultimate detection sensitivity of the entire imaging system. However, CISs generally suffer from high temporal noise, which is typically measured by the minimum number of detectable electrons (e^-_{rms}) at the input of the pixel.

As discussed in Chapter 2 and Chapter 3, an effective approach to improve the temporal noise performance of the CIS is to implement a high-gain stage and apply a digital correlated multiple sampling (CMS) technique along the signal path [1]. By virtue of the high-gain, such an approach is capable of effectively reducing the input-referred thermal noise of the pixel source follower and subsequent circuits [2]. In view of the CMS technique, it can effectively reduce the thermal noise by a factor of $\sqrt{M}$ (M = sampling times) due to averaging. However, the effectiveness of a low frequency noise reduction by CMS is dependent on the signal level processing period, owing to its inherent band-pass filtering feature [3]. In other words, the shorter the sampling period, the less low frequency noise remains throughout CMS operations.

Typically, the CMS technique can be realized in either analog domain or digital domain. Analog CMS integrates the pixel output in the analog domain without sacrificing the operating frame-rate, but with the cost of additional noise added during analog integration. Digital CMS eliminates this excess noise by accumulating the conversion data in the digital domain, but requires a long signal sampling period. In pursuit of taking fully advantages of a CMS technique on noise reduction both in thermal noise and low frequency noise, namely flicker noise and RTS noise, dedicated low-noise signal process solutions with an effective CMS feature for CIS is called for. These solutions are supposed to be realized by optimizing the trade-off between noise, speed and power consumption of the entire readout circuit, as well as combining with a highly-compact layout.

To demonstrate and assess circuit techniques that will be applied in a CIS, a prototype with VGA format (640(H)×480(V)) is presented in this chapter. Implemented in a 65/90 nm CIS back-side-illumination (BSI) technology, the proposed architecture integrates a column-parallel inverter-based analog-front-end (AFE) circuit and a digital CMS reference-adaptive $\Delta\Sigma$ ADC along the readout path. The proposed circuits

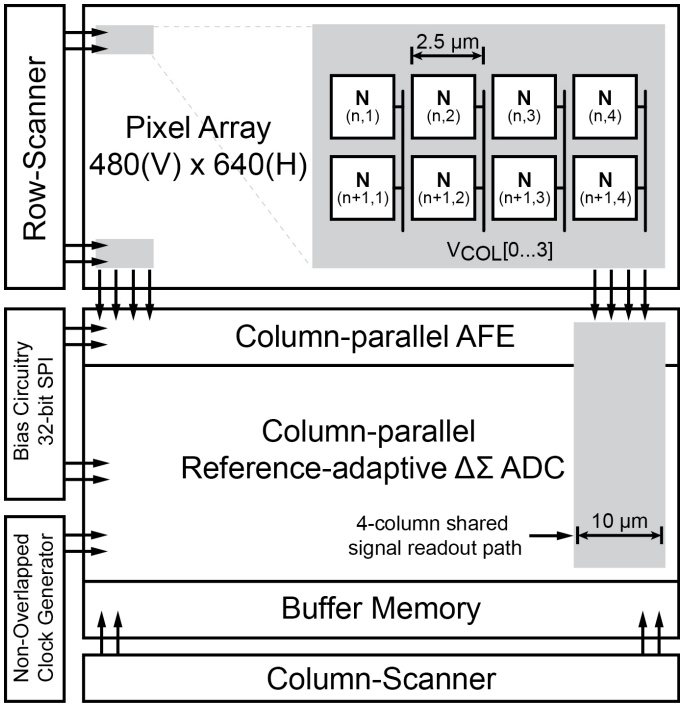


Figure 4.1: Block diagram of the proposed CMOS image sensor.

are implemented with thin oxide layer MOS devices powered by a supply voltage of 1.2 V. Measurement results show that the prototype design reaches an input-referred noise of 0.55 e^-_{rms} within a row time of 5 µs.

The rest of this chapter is organized as follows. Section 4.2 provides an overview of the proposed CIS architecture. Section 4.3 presents the implementation details of the AFE circuit. Section 4.4 describes the digital CMS circuits. The characterization results of the fabricated image sensor are presented in Section 4.5. Finally, a conclusion is given in Section 4.6.

4.2. Sensor Architecture

Figure 4.1 shows an architecture overview of the proposed CMOS image sensor. The main building blocks of the prototype sensor consists of the pixel array, column-parallel AFEs and ADCs, as well as peripheral auxiliary circuits, including row and column scanners, buffer memory, bias circuits, a clock generator and a serial peripheral interface (SPI).

As illustrated in Figure 4.2, the pixel architecture, which is isolated by

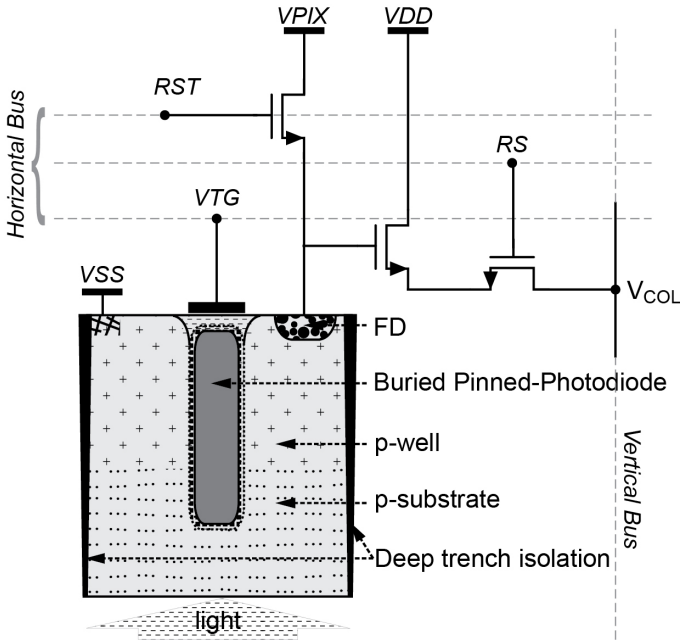


Figure 4.2: Schematic with cross-section of BPD and TG region as well as readout architecture.

deep trench isolation (DTI) technology, integrates a back-side-illuminated (BSI) buried vertically pinned photodiode (BPD) as well as a planer transfer gate (TG) in each pixel. The reset (RST), transfer (TG) and selection (RS) signals generated from the row scanner block control the integration time and operate as a rolling shutter for each line of pixels. The overall 640 (H) $\times$ 480 (V) pixel array features a pixel pitch of 2.5 μm.

The front-end signal processing in each column is performed by an AFE circuit and a digital CMS structure. The AFE circuit, which is implemented by a programmable-gain amplifier (PGA) with embedded correlated double sampling (CDS) function, first acquires and amplifies the photon signal from the pixels and conveys them to a reference-adaptive $\Delta\Sigma$ ADC. A dedicated ADC architecture is proposed for realizing the CMS function and addresses the conversion time and power consumption issue for the low-noise CMOS image sensor. In each row-time, the A-to-D conversion is operated twice for each row of pixel: one for the signal level and the other for the reset level. The digital CMS function is realized within an on-chip decimation filter, which carries out second-order

low-pass filtering, corresponding to the averaging effect. After the A/D conversion and CMS, the digitized data is then transferred into a 16-bit column latch which acts as a buffer memory. During the A/D conversion of the next line, the digital output from the buffer memory is read out through 8-channel digital output buffers. With the proposed readout approach, the single-pixel conversion time is 5 µs at a frame-rate of 410 frame/s with 480 rows. As a proof-of-concept, we adopt a shared 4-to-1 column signal readout path layout approach, that is, each readout path is multiplexed with 4 columns pixels. In this way, the layout requirement is relaxed for this prototype design. As a result, the frame-rate is 4 times slower when reading out the full frame of the sensor, but the column and pixel readout time remain the same.

4.3. Analog-Front-End Design

4.3.1. Noise Analysis of thin oxide vs. thick oxide layer MOS devices

In general, a given CIS process design kit usually provides transistors with two different oxide thickness. To achieve a better trade-off between area, speed and power consumption, thin oxide layer transistors are widely chosen to be used for digital circuits in a CIS design. In contrast, since the thicker oxide layer MOSFETs is more robust with higher supply voltages, transistors implemented both in the pixel array and analog blocks always feature thick oxide layer with a consideration of exploiting a high dynamic range in a conventional CIS.

However, in respect of the noise performance, a thinner oxide layer MOSFETs typically shows a better low frequency noise, e.g. 1/f noise, than the thicker one [4]. In a SPICE model, we can find that the thin oxide layer transistor model generally shows a lower value than the thicker one in terms of the noise parameter NOIA, which represents the oxide trap density in BSIM (Berkeley Short-channel IGFET Model) [5]. This can be understood that a thin oxide layer gate benefits from a better control of the gate terminal over the channel, thus, showing less mobility fluctuations [6]. In addition, it can be also understood based on the simplified $1/f$ noise expression (4.1). A suppression of $1/f$ noise can be obtained with a higher

C_{ox} (gate oxide (G_{ox}) capacitance per unit area).

$$\overline{v_{1/f,n}^2} = \frac{K}{C_{ox}^2 WLf} \tag{4.1}$$

where K is a process-dependent constant, W and L are the width and length of a transistor, f is the frequency [7]. As explained in Chapter 2, the low frequency noise is recognized as one of the most crucial noise contributor in a CIS system. Hence, theoretically, using thin oxide devices for analog signal processing circuit would offer a fundamental advantage for noise reduction in a CIS.

To verify the effectiveness of this design choice, a noise comparison simulation has been performed with a given process and design kit. As shown in Figure 4.3, a common-source (CS) amplifier with a resistive load has been chosen as the topology in this simulation, where $R1$ and $R2$ are resistive loading; $M1$, a thick oxide layer transistor, and $M2$, a thin oxide layer transistor, operate as the input transistor with supply voltages of $VDD25$ = 2.5V and $VDD12$ = 1.2V, respectively. In order to make a fair comparison, we adopt the same resistance value for the loads, and the same transistor sizes in both implementations. The simulated noise power spectral density (PSD) at the output of the amplifier is shown in Figure 4.4. A notable noise PSD difference is found in the spectrum at low frequency regime. In respect of quantitative values, the total simulated noise voltage for the case with a thin oxide MOSFET is 43 μV_{rms} when integrated from 1Hz to 200kHz, while it is 145 μV_{rms} in the same bandwidth in the other case. This result demonstrates that thin oxide layer MOS devices have a better noise performance at the frequency of interest, confirming our theoretical study and design choice.

4.3.2. Analog-front-end Circuit Implementation

To facilitate the noise reduction of the succeeding digital CMS ADC, an AFE circuit in each column is realized by a capacitive-feedback PGA, as shown in Figure 4.5(a). To adapt the sensor input-output, the PGA provides four closed-loop gain steps ($\times$0.25, $\times$1, $\times$5, $\times$20) according to the register code map as shown in Figure 4.5(b). Under low light condition, the highest gain step $\times$20 can be applied to achieve the best noise performance and the highest sensitivity. On the other hand, under high light condition, the lowest gain step $\times$0.25 is dictated to attenuate the signal and avoid output saturation

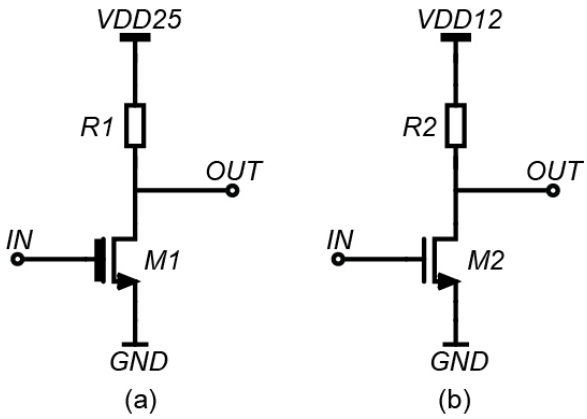


Figure 4.3: Schematic with common-source amplifier (a) thick oxide layer MOSFETs; (b) thin oxide layer MOSFETs.

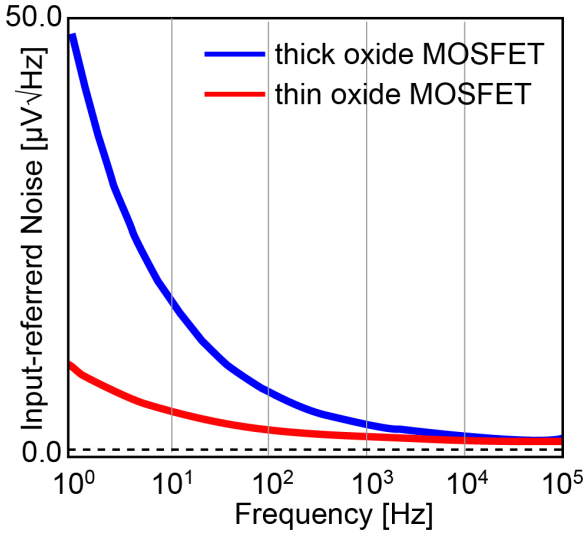


Figure 4.4: Noise spectrum comparison between two types of transistors.

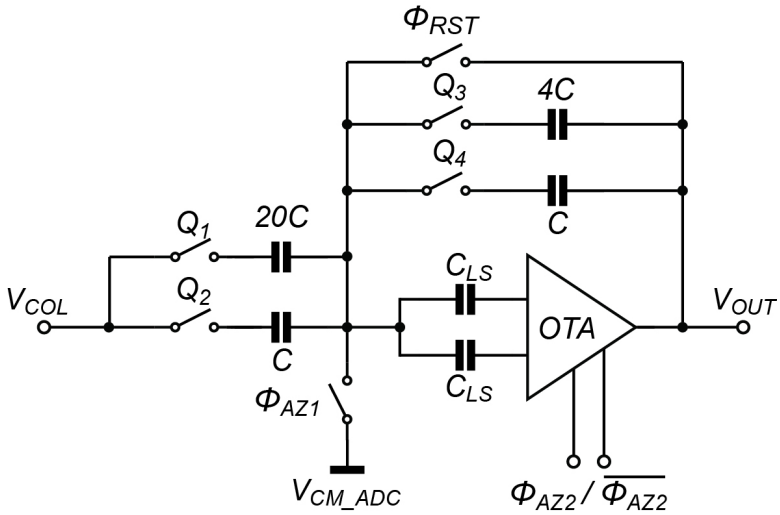
at high light signal levels, on account of the fact that the largest voltage swing at the output of the pixel is around 1.5 V. This is the differential result of the the reset level and the pinning voltage of the BPD.

Typically, differential amplifiers are widely used in CIS readout circuits because they are capable of providing a higher rejection to interference noise. However, compared to the single-ended structure, the differential structure requires duplication of the circuit branch, leading to twice area and power, as well as twice thermal noise excess factor for achieving the same transconductance. Therefore, in order to minimize the noise, area, and power consumption, a single-ended topology has been chosen for the proposed operational transconductance amplifier (OTA) in this work.

As shown in Figure 4.6, a current-reuse OTA based on a gain-boosted cascoded inverter is employed in this prototype design with the concern of maximizing the current-efficiency and minimizing the noise. In the schematic, AMP_N and AMP_P are two common source amplifiers, operating as a gain-boosting stage to regulate cascoded transistors M_{CASN} and M_{CASP} respectively. This gain-boost circuitry enhances the output impedance of the OTA, and hence, ensures a high linearity and an accurate closed-loop gain in PGA. As a result, an open-loop gain of 80 dB is obtained with this OTA scheme in this work.

A well-known down-side of an inverter structure is its quiescent current being strongly rely on its input voltage, making it prone to process, supply voltage, and temperature (PVT) variations. To address this issue, a dynamic biasing scheme has been proposed in [8]. Its operating timing diagram is shown in Figure 4.5(c). During the sampling phase, diode connections are established for input transistors M_1 and M_2 by switching on $\overline{\phi_{AZ2}}$. Meanwhile, the floating current source, comprising M_{BIASN} and M_{BIASP}, forces a bias current of 20 µA through M_1 and M_2. This bias approach ensures that both inputs are biased with exactly the same bias currents. At the same time, the bias voltages V_{ON} and V_{OP} associated with this operating condition are stored on the offset-storage capacitors C_{LS}. During the amplification phase, the diode connections are released and the floating current source is bypassed by opening the switches $\overline{\phi_{AZ2}}$. This operation disconnects the inverter from the floating current source and re-configures it back to the high gain push-pull common-source amplifier with a bias current well-defined during the sampling phase.

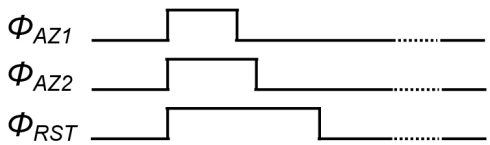
The above mentioned dynamic biasing technique not only provides a



(a)

	Q_1	Q_2	Q_3	Q_4
× 0.25	0	1	1	0
× 1	0	1	0	1
× 5	1	0	1	0
× 20	1	0	0	1

(b)



(c)

Figure 4.5: Column-parallel PGA (a) schematic; (b) gain control code map; (c) timing diagram.

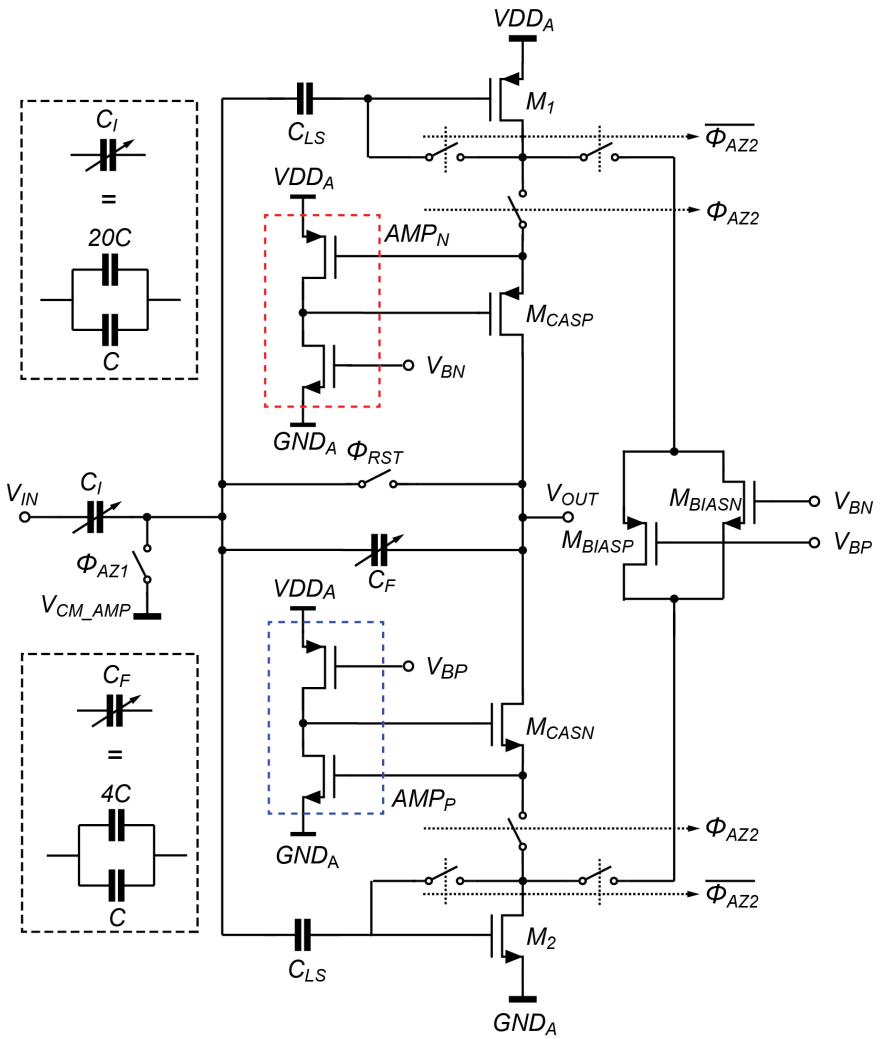


Figure 4.6: Gain-boosted cascode inverter with floating current source.

robust PVT immunity, but also inherently includes an auto-zero process. This process, however, reduces $1/f$ noise at the cost of increased thermal noise due to noise-folding [9]. In order to overcome this noise penalty, the effective noise bandwidth is lowered by increasing the value of the offset-storage capacitor C_{LS} during the auto-zero phase. Hence, the amount of noise-folding is reduced. This approach has no impact on the amplifier's settling time during the amplification phase, as C_{LS} is then connected in series with amplifier's input instead of added to the load of the amplifier. In this work, in order to suppress the effect of noise folding, C_{LS} is chosen as 400 fF. The simulated settling time of PGA at $\times$20 gain set is 80 ns.

The voltage gain of the PGA is defined by the ratio of the input capacitor C_I and the feedback capacitor C_F, where C_I and C_F are implemented as a switchable capacitor array with value of C_I = 1 pF and 50fF, and C_F = 200fF and 50fF. Even the 1 pF and 200 fF MoM capacitance bring extra parasitic capacitances that impact the feedback ratio, but because the absolute gain value of the PGA is not crucial for CIS applications, these layout-induced parasitic capacitances can be ignored. To minimize the impact of additional noise brought by the AFE stage, the PGA is designed to have an integrated input referred noise below 40 μV with gain step $\times$20. To maximize the DR, the bias voltage of this inverter-based OTA has been properly defined, leading to an output swing ranging from 0.3 V to 0.9 V. As such, combined with the programmable gain function, an overall 80 dB DR is achieved with a 1.2 V-supply PGA, which is sufficient for pixel readout and the prototype sensor.

4.4. Digital CMS ADC Design

4.4.1. Concept of Proposed ADC

As described in Section 4.1, digital CMS has been proved as an effective solution of scaling down wide-band noise in a CIS. However, since the multiple sampling extends the conversion time in proportion to the number of samplings, embedding digital CMS to a CIS comes at the expense of a longer signal sampling period, resulting in a slower frame-rate and a less noise reduction effectiveness.

The fact that a ΔΣ ADC performs digital CMS by its nature makes this ADC architecture an attractive candidate. A straightforward

implementations has been heavily investigated in literature [10]. However, it still requires more than 100 clock cycles to complete one data conversion. To further improve the conversion speed, we proposed a column-wise reference-adaptive incremental $\Delta\Sigma$ ADC. The ADC block diagram is shown in Figure 4.7 and its conceptual diagram and output waveform illustration is presented in Figure 4.8. Adaptive reference-control method [11] splits the $\Delta\Sigma$ data conversion into two sub-phases: the coarse pre-determined phase and the fine conversion phase. In the coarse phase, a comparator is first operated as a look ahead circuit to determine the DAC reference that will be later used for fine conversion. In the following fine phase, the pre-determined corresponding reference is adopted by the $\Delta\Sigma$ ADC to complete the fine conversion.

In our proposal, three sets of references ($V_{REFN}[0,1,2]/V_{REFP}[0,1,2]$) are adaptively switched to serve fine $\Delta\Sigma$ data conversions, corresponding to reset-level/low light, moderate light and high light conditions, as shown in Figure 4.8. During readout, a pixel reset level is processed in both coarse and fine conversion phases with the reference of $V_{REFN}[0]$ and $V_{REFP}[0]$. After the reset level is converted, the signal level is sequentially compared with the threshold voltage V_{TH0} and V_{TH1}, then one of the references is selected for conversion of the signal level. As such, in this work, a 11-bit resolution $\Delta\Sigma$ ADC offers a 12.5-bit equivalent resolution for the pixel output. By using this adaptive reference adjustment mechanism, less clock cycles are required to achieve a given quantization errors. As a consequence, the proposed operation efficiently reduces the conversion time, as well as simplifying the design for both analog integrators and digital decimation filters.

4.4.2. Coarse Phase Conversion

Figure 4.9 shows the schematic of the coarse phase data conversion circuit. It consists of a zero-crossing detector (ZCD), a shift-register and a reference bank selector. Each ZCD is constructed with an inverter-based preamplifier and a level shifting capacitor (C_{LS}), followed by a chain of two inverters that amplifies the output of the preamplifier to logic levels [12].

When the coarse conversion starts, the preamplifier is auto-zeroed during $ADC1_{\phi 1D}$, while the ZCD input is switched to the input terminal V_{IN} via $ADC1_{\phi 1}$. In this way, the voltage difference between V_{IN} and the inverter threshold voltage V_{TH} are sampled on the capacitor C_{LS}. After that, the

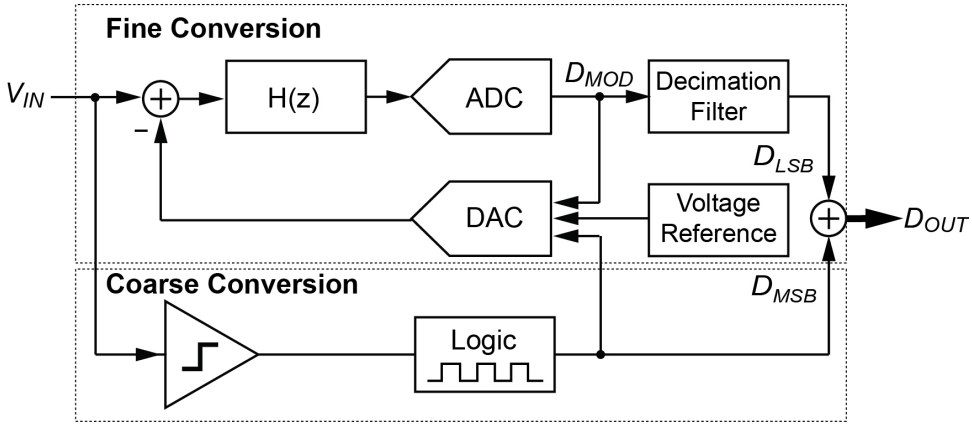


Figure 4.7: Block diagram of the proposed ADC.

ZCD input is successively compared with threshold voltages V_{TH0} and V_{TH1} by switching on $ADC1_{\phi 2}$ and $ADC1_{\phi 3}$ respectively. The ZCD output is first latched in the buffer memory and then transferred to the shift-register, forming the MSB output bits. During the succeeding fine conversion, they are fed into the reference bank selector to control the references in the $\Delta\Sigma$ modulator.

4.4.3. Fine Phase Conversion

System-Level Design

The fine phase conversion is realized with an incremental $\Delta\Sigma$ ADC. It is composed of an analog second-order $\Delta\Sigma$ modulator followed by a digital second-order decimation filter, as shown in Figure 4.10. The modulator employs a Boser-Wooley structure with two half-delay discrete-time integrators [13], a single-bit quantizer, and a feedback DAC. In addition, an input-feedforward path is added across the first integrator to help improving the stability [14].

Given that the modulator input signal V_{IN} from the PGA stage is constant within the conversion time, the outputs of the first and second integrators (w_1 and w_2) can be derived from the iterative expressions:

$$w_1[i] = w_1[i-1] + a_1 \cdot V_{IN} - a_1 y[i] \cdot V_{REF} \tag{4.2}$$

$$w_2[i] = w_2[i-1] + a_2 w_1[i] + a_2 b \cdot V_{IN} - a_2 b y[i] \cdot V_{REF} \tag{4.3}$$

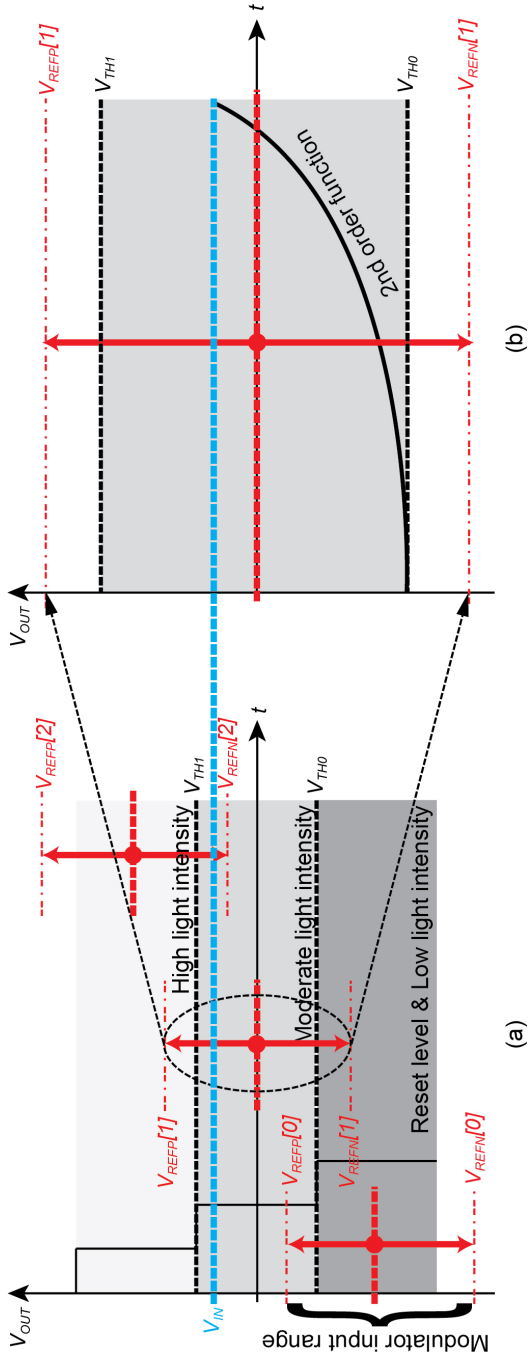


Figure 4.8: Conceptual diagram and output waveform of the proposed ADC (a) coarse phase; (b) fine phase.

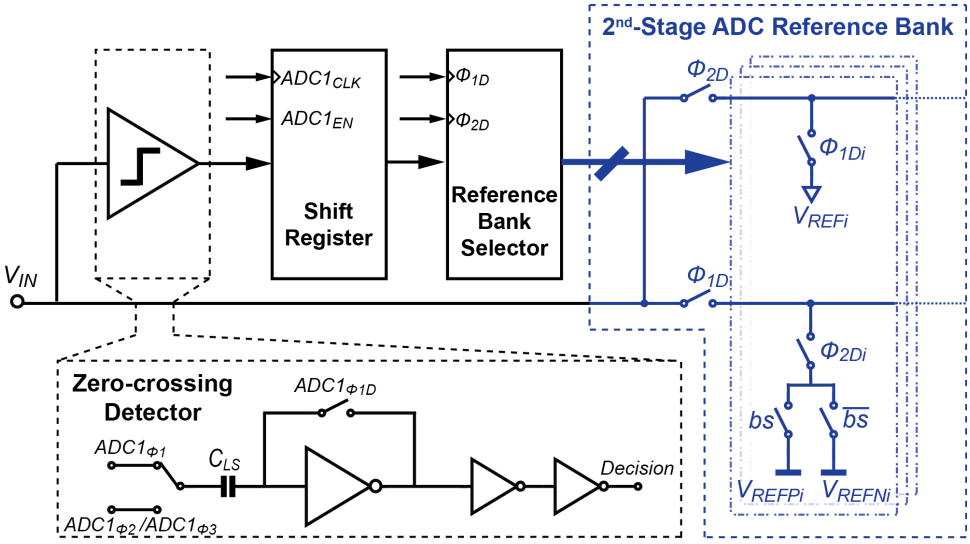


Figure 4.9: Schematic of the first-stage ADC.

where V_{REF} is the feedback DAC reference voltage, bounded within the range of $[-V_{REF}, +V_{REF}]$, i is the sample time index, $y[i]$ is the 1-bit quantizer output at i-th sample, a_1, a_2 are two modulator coefficients and b is the feedback coefficient.

By summing each item from $i = 1$ to $i = n$, the non-iterative equations at the n-th sample can be expressed as:

$$w_1[n] = a_1 n \cdot V_{IN} - a_1 \sum_{i=1}^{n} y[i] \cdot V_{REF} \tag{4.4}$$

$$w_2[n] = (a_1 a_2 \sum_{i=1}^{n} i + a_2 bn) \cdot V_{IN} - (a_1 a_2 \sum_{i=1}^{n} \sum_{j=1}^{i} y[j] + a_2 b \sum_{i=1}^{n} y[i]) \cdot V_{REF} \tag{4.5}$$

After M cycles, the residual error $w_2[M]$ at the output of the second

integrator is given as:

$$w_2[M] = (a_1 a_2 \frac{M(M+1)}{2} + a_2 bM) \cdot V_{IN} - (a_1 a_2 \sum_{i=1}^{M} \sum_{j=1}^{i} y[j] + a_2 b \sum_{i=1}^{M} y[i]) \cdot V_{REF} \quad (4.6)$$

On the basis of equation (4.6), the estimation of the ratio between the input signal and the reference V_{IN}/V_{REF} and the quantization error E_Q can be derived as:

$$\frac{V_{IN}}{V_{REF}} = \frac{2a_1}{a_1 M(M+1) + 2bM} (\sum_{i=1}^{M} \sum_{j=1}^{i} y[j] + a_2 b \sum_{i=1}^{M} y[i]) \quad (4.7)$$

$$E_Q = \frac{2a_1}{a_1 M(M+1) + 2bM} \cdot w_2[M] \quad (4.8)$$

Based on equations (4.5) to (4.8), the modulator coefficients are chosen as $a_1 = 0.25$, $a_2 = 0.5$, $b = 0.5$ [15]. It enables a maximum input range of 0.6V, comprising a 10% variation of the reset level and a 0.55 V signal level swing.

ΔΣ Modulator Design

In this prototype design, both integrators employ the same OTA structure, which employs a logic cascode inverter with a floating current source. Here we use the first integrator as an example (Figure 4.12). During the sampling phase Φ_1, the input signal is sampled on sampling capacitor the C_{S1} with respect to the signal ground. The inverter is configured at unity gain to auto-zero and its input offset is stored on the holding capacitor C_{LS1}. Inside the OTA, a pair of input transistors M_1 and M_2 are configured as diodes, and biased via cascode transistors (M_{CASN-1}, M_{CASP-1}) and floating current source (M_{BIASN} and M_{BIASP}). Simultaneously, M_{CASP-2} and M_{CASN-2} are turned off. As such, both M_1 and M_2 are biased exactly with the same current while the associated operating voltages V_{OP} and V_{ON} are stored on C_{LS1}.

During the subsequent integration phase Φ_2, a negative feedback path is formed across the inverter, pushing the sampled charge into the integration capacitor C_{I1}. At OTA level, the bias voltages of cascode transistors

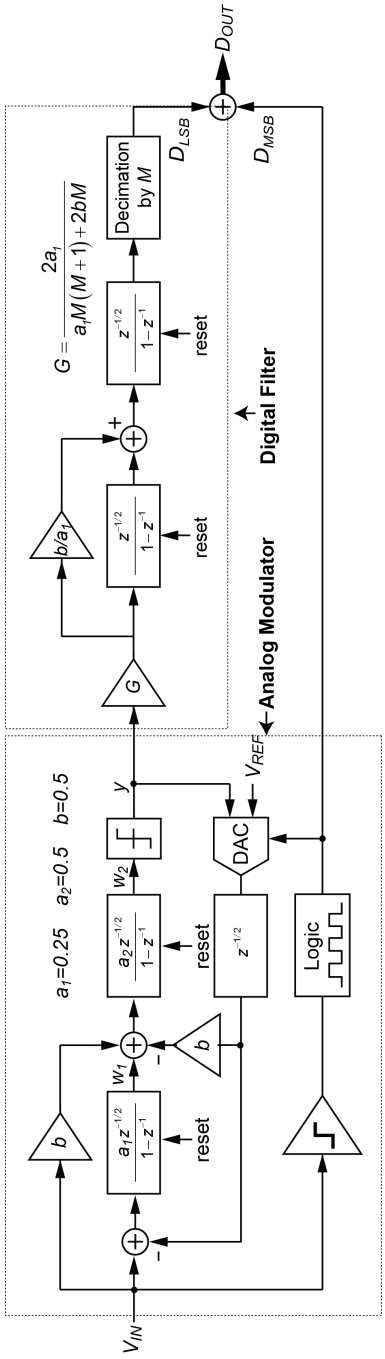


Figure 4.10: Block diagram of second-order $\Delta\Sigma$ ADC.

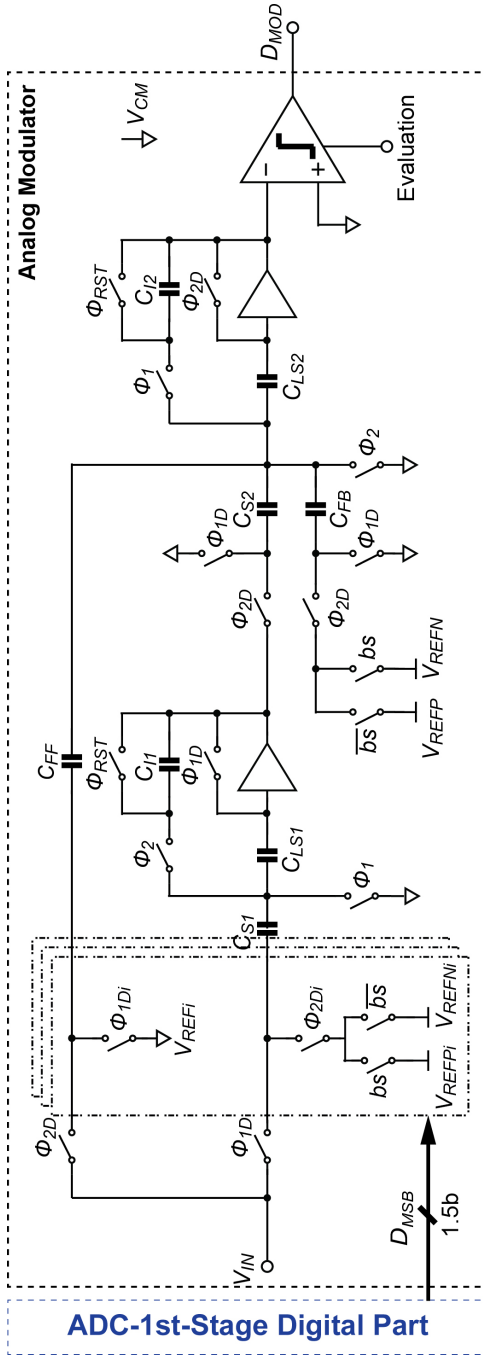


Figure 4.11: Schematic of second-order $\Delta\Sigma$ modulator.

M_{CASN-1} and M_{CASP-1} are swapped with those of M_{CASP-2} and M_{CASN-2}. Then, the inverter is disconnected from the floating current source and acts as a common-source amplifier with pre-defined bias current.

Note that when a push-pull inverter operates as an OTA, it behaves as a class-AB amplifier. At the start of the integration phase, the input node of the inverter is instantly pushed up or down, which increases the dynamic current to the load capacitor. After that, when the charge is transferred from the sampling capacitor to the integration capacitor, the inverter input gradually returns to the offset voltage. This operation provides a high dynamic current only during the transition, while keeps a low static current in other period [16]. In this work, the inverters in the first and second integrator draw 20 μA and 10 μA, while achieving DC gains of 60 dB and 40 dB, respectively.

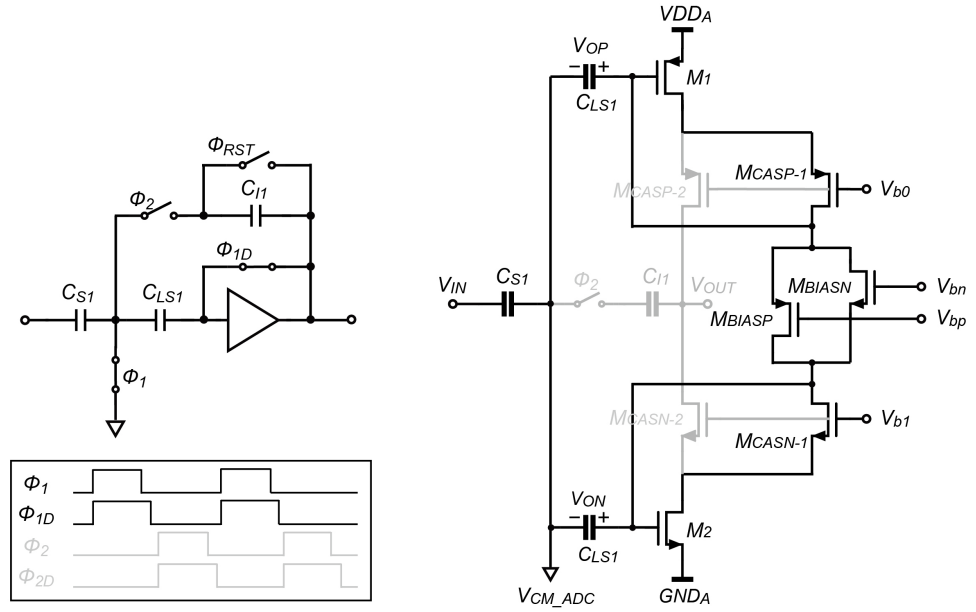
Decimation Filter Design

To re-construct the signal and attenuate the out-of-band components, such as, the quantization error, interference and circuit noise, a digital decimation filter following the analog modulator is called for. For the sake of hardware simplicity, a second-order cascade integrators with a feedforward path has been adopted as the column-parallel digital decimation filter. The decimation filter operates in the transient mode and keeps pace with their analog counterparts to minimize the potential conversion latency [14]. Figure 4.10 shows the block diagram of the decimation filter and its detailed circuit-level implementations are presented in Figure 4.13. Based on equation (4.7), the decimation filter is composed of a ripple counter combined with an accumulator as the first integrator and a stand-alone accumulator as the second integrator. To take into account of 1 bit over-flow, a 12-bit accumulator is used for 11-bit dynamic range.

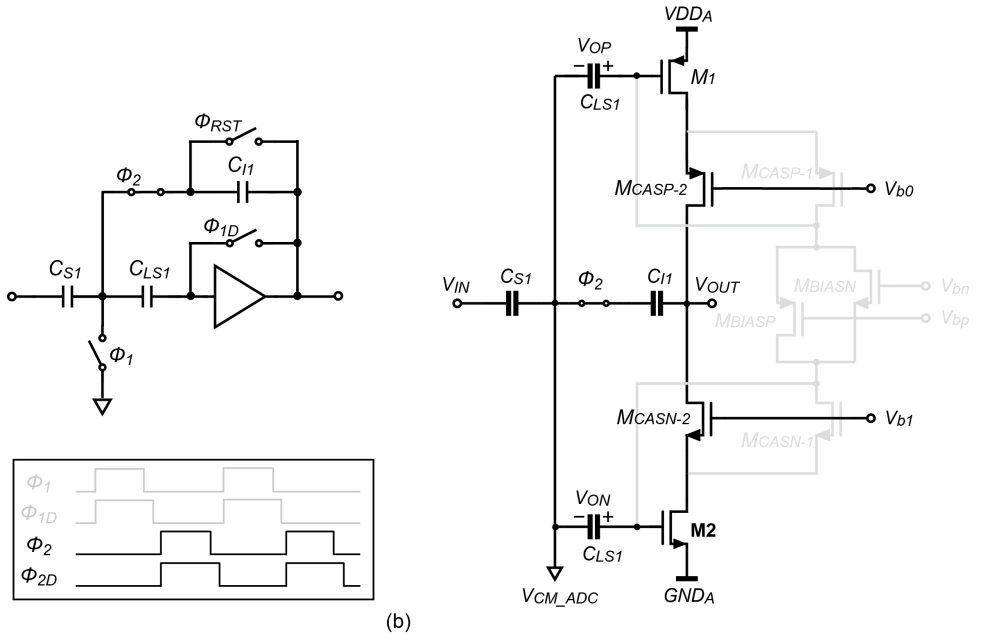
When only the quantization error is considered, a second-order $\Delta\Sigma$ ADC can be calculated by the number of clock cycles M, as revealed by:

$$N = log_2[M(M+1)] - 1 \tag{4.9}$$

hence, to achieve a 11-bit resolution, equivalent to 12.5-bit, 65 clock cycles are needed. Due to the concern that the cascade-of-integrators type decimation filter has limited capability in rejecting periodical noise, the number of clock cycles is increased to 80 cycles in this work.

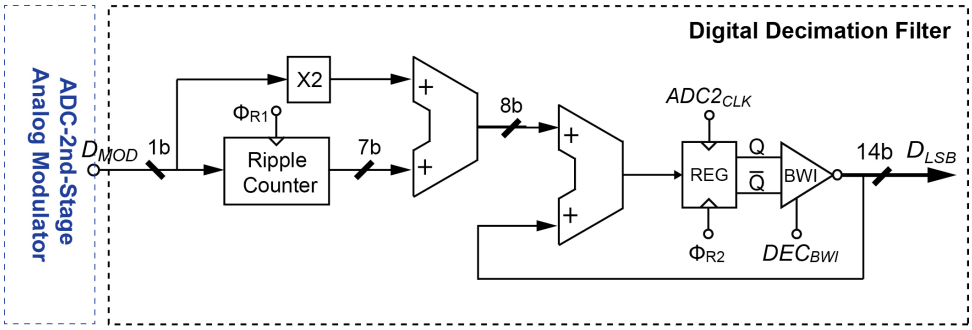


(a)

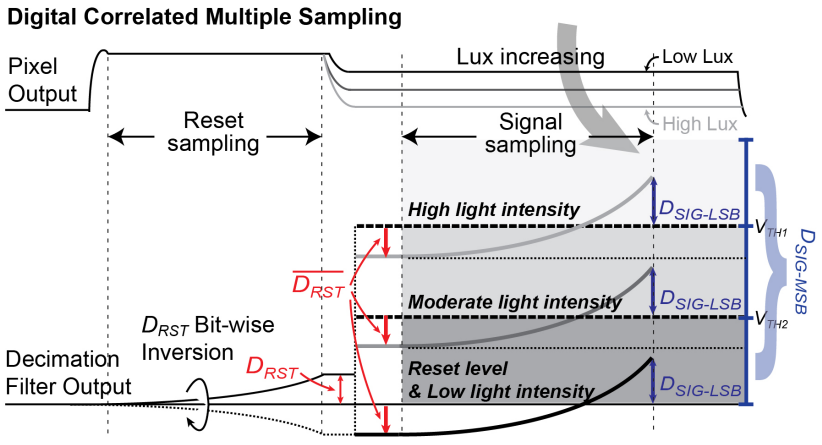


(b)

Figure 4.12: Schematic of the OTA (a) sampling phase; (b) integration phase.



(a)



(b)

Figure 4.13: (a) Schematic of second-order $\Delta\Sigma$ decimation filter; (b) Output waveform of decimation filter with BWI operation.

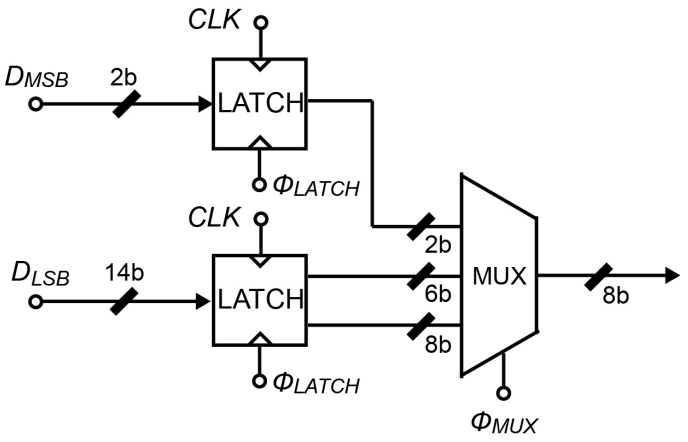


Figure 4.14: Schematic of multiplexer.

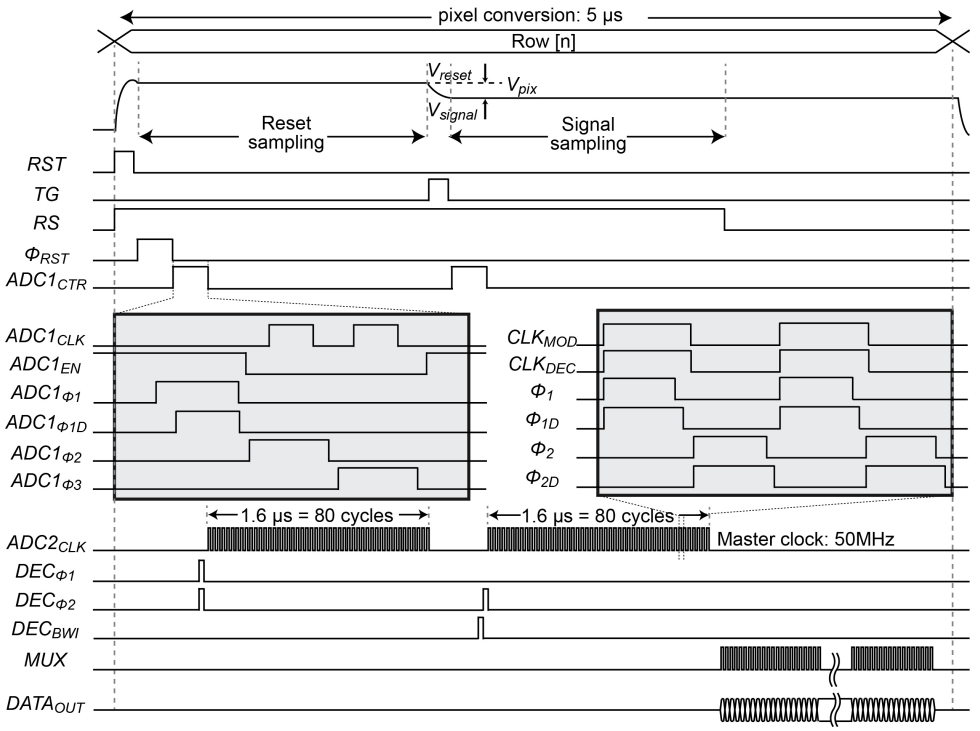


Figure 4.15: Timing diagram of row conversion.

After the ADC conversion, the digitized data is transferred into 16-bit column latches and then multiplexed and streamed out through 8-channel digital output buffers. Figure 4.14 provides a simplified circuit diagram of multiplexer.

Digital CMS Operating and Timing Diagram

A complete digital CMS operation timing diagram of reference-adaptive $\Delta\Sigma$ ADC is illustrated in Figure 4.15. At the beginning of each row time, all internal nodes of the ADC are reset via Φ_{RST}. After the FD node is reset, the pixel reset level is first sampled for analog CDS at the AFE, and then converted into digital codes after a coarse pre-determined phase and a fine conversion phase. Upon the completion of the reset level conversion, the modulator clock $ADC2_{CLK}$ is gated off and an inversion of logic level for each bit is performed inside the decimation filter with the control signal DEC_{BWI}. This operation is generally referred to as bit-wise inversion (BWI). Since BWI leads to a decimal complement digital value for the reset level, a negative value of reset level is obtained. After the photon charge is transferred from the BPD to the FD node, the pixel signal level is amplified by the PGA, and then digitized in the same manner as the case of the reset level with the same clock cycle. Inside the decimation filter, the temporarily stored negative reset value is hold as the initial value for the signal level integration. As such, the integrators digitally subtract the 80-times-sampled reset level from the 80-times-sampled signal level, resulting in a differential value $D_{RST} - D_{SIG}$, where D_{RST}, D_{SIG} are digital codes representing the reset level and the signal level respectively. Since this signal conversion and re-construction procedure integrates a differential and averaging operation, the digital CMS is realized inherently in the proposed reference-adaptive $\Delta\Sigma$ ADC.

4.4.4. Silicon realization

The prototype CMOS image sensor has been fabricated in a 1P4M CIS technology with metal-oxide-metal (MOM) capacitors. The front-end-of-line (FEOL) and back-end-of-line (BEOL) are designed and processed in 90nm and 65nm process. Figure 4.16 shows the die microphotograph along with the layout of the block diagram, which is not visible in the micrograph due to the BSI process. The area of the chip including bond pads is 3×3 mm^2. The proposed readout circuit occupies

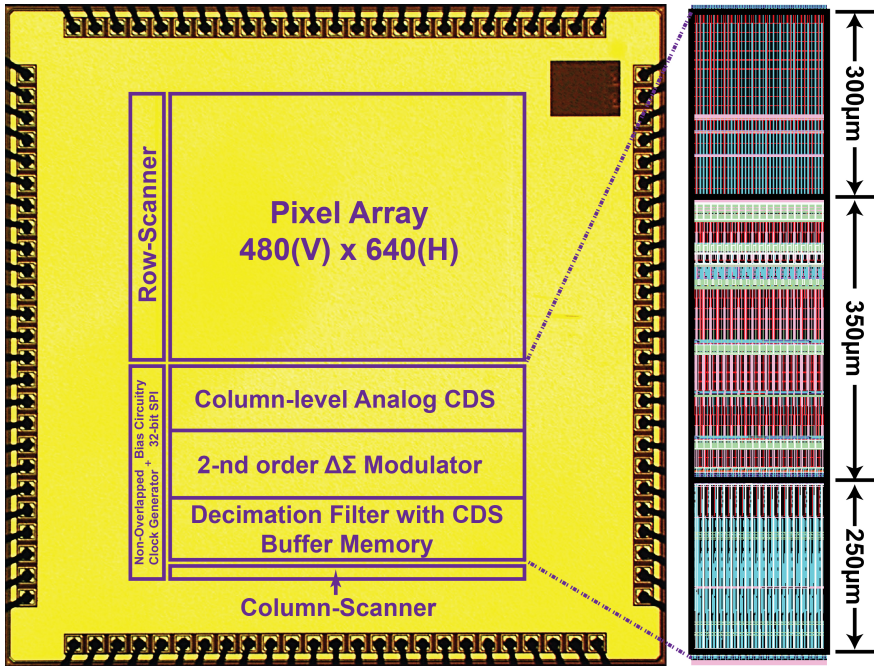


Figure 4.16: Chip microphotograph (with 16 columns highlight).

$10 \times 900\ \mu m^2$ per single column, which is comparable to the area of a PGA and a single-slope ADC. Running at a clock frequency of 50 MHz, each row of pixels requires a readout time of 5 µs, 3.2 µs of which is utilized by the $\Delta\Sigma$ Modulator to achieve a quantization noise limited resolution. For flexibility, the digital logic and the ADC reference voltages are all generated from on-board potentiometers, low-noise regulators and low-noise analog buffers.

4.5. Measurement Results

4.5.1. AFE and ADC Measurement Results

The electrical performance of the proposed AFE and ADC architecture has been characterized and evaluated with a separate design-for-testability (DFT) implementation.

Figure 4.17 shows the measured output digital code of the column readout path at 4 AFE gain settings. To prevent saturation or distortion at the output of the amplifier, a short exposure time with limited amount of

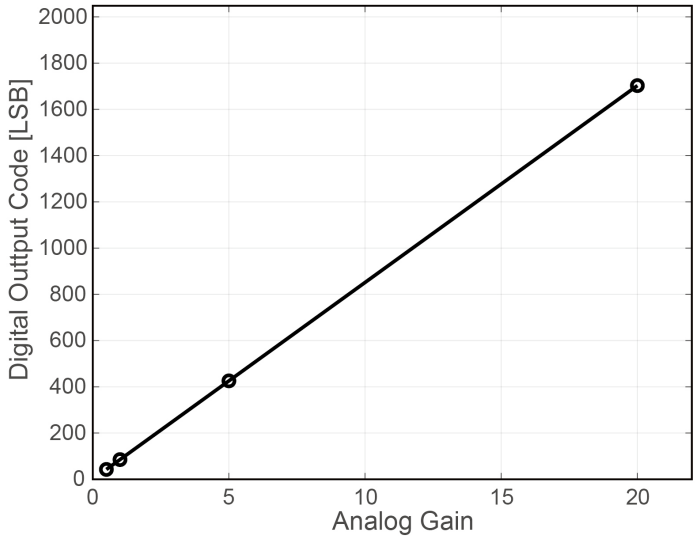


Figure 4.17: Output characterization of the column path gain.

light was applied in the measurement. In order to evaluate the PGA gain settings independently, the reference-adaptive function of the ADC is bypassed. The maximum column gain error is about 3.5%, which is determined by the ratio of the measured amplified output codes over the ideal ones. The deviation from the ideal gain step is mainly caused by the attenuation introduced by the auto-zero capacitance at the input of the PGA core amplifier, which has insufficient open-loop gain.

Figure 4.18 shows the measured power spectral density of the proposed $\Delta\Sigma$ modulator. It is obtained by applying a Kaiser window to the fast fourier transform (FFT) of the measured bitsream. The second-order noise shaping is clearly shown in the plot. The measured peak SNR is 84dB for a 800kHz bandwidth with a 50MHz clock frequency.

Figure 4.19 (a) and (b) show the measured input-referred noise and resolution of the reference-adaptive $\Delta\Sigma$ ADC as a function of the number of clock cycles (M). The input-referred noise has been measured by performing 1000 conversions with a DC input voltage and calculating the standard deviation of the decimated output. As indicated by equation (4.8), the quantization noise of a second-order $\Delta\Sigma$ ADC is inversely proportional to M^2.

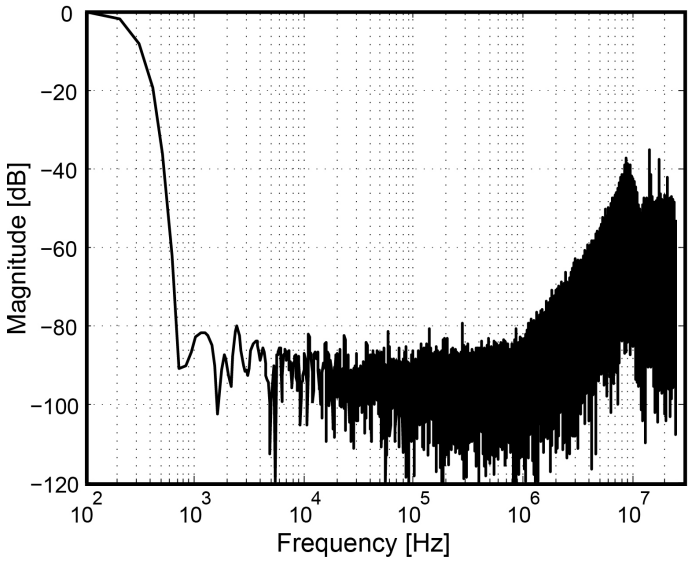
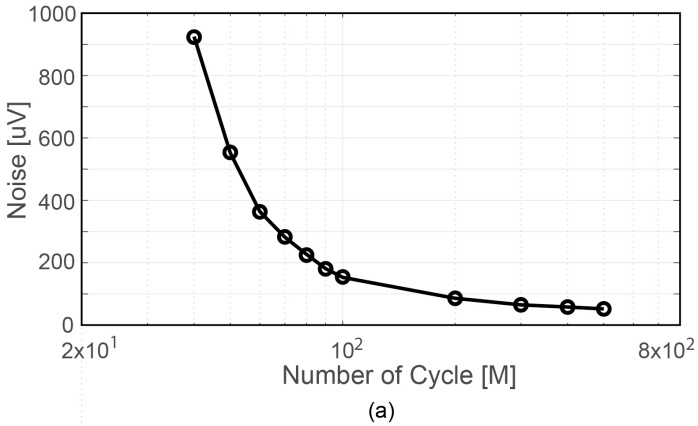


Figure 4.18: Measured power spectral density of $\Delta\Sigma$ modulator.

In both figures, it can be observed, for fewer conversions cycles (M<100), the temporal noise of the ADC is quantization noise limited, while the kTC noise and thermal noise starts to dominate the ADC noise performance when M>100. Generally, the ADC resolution is derived from the input-referred noise. With respect to an overall input range of 0.6V, the ADC achieves a resolution of 11 bits at M = 80, corresponding to an input-referred noise of 230 μV_{rms}.

The ADC's integral nonlinearity (INL) is obtained by calculating the point-to-point deviation between the first-order polynomial fitting curve and the decimated outputs. Figure 4.20(a) shows the measured INL for the proposed ADC without the reference-adaptive function. The achieved INL is within -1/+1 LSB of the 11-bit resolution, which corresponds to a nonlinearity of 0.1%. Figure 4.20 (b) presents the measured peak-to-peak INL of the proposed ADC with the reference-adaptive function enabled. In this case, the INL is within -4.5 LSB to 4 LSB with respect to 12.5-bit output codes, which is equivalent to a nonlinearity of 0.15%. It can be observed that the maximum values of INL occur around the reference transition points, where the offset and quantization errors contribute to the excess non-linearity. Given the intrinsic non-linearity of the pixel,



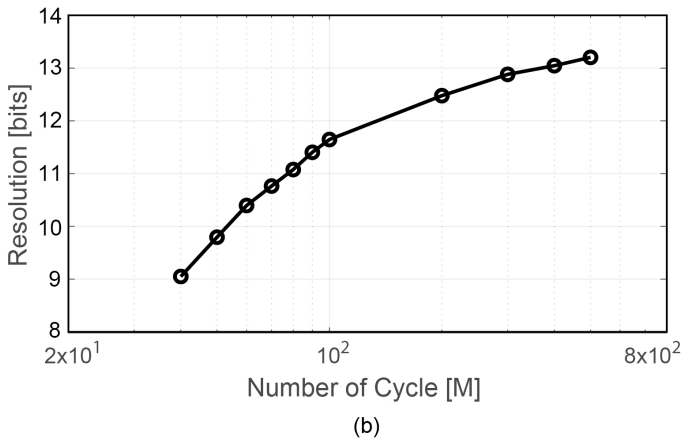


Figure 4.19: (a) Measured ADC input-referred noise as a function of the number of cycle M; (b)Measured ADC resolution as a function of the number of cycle M.

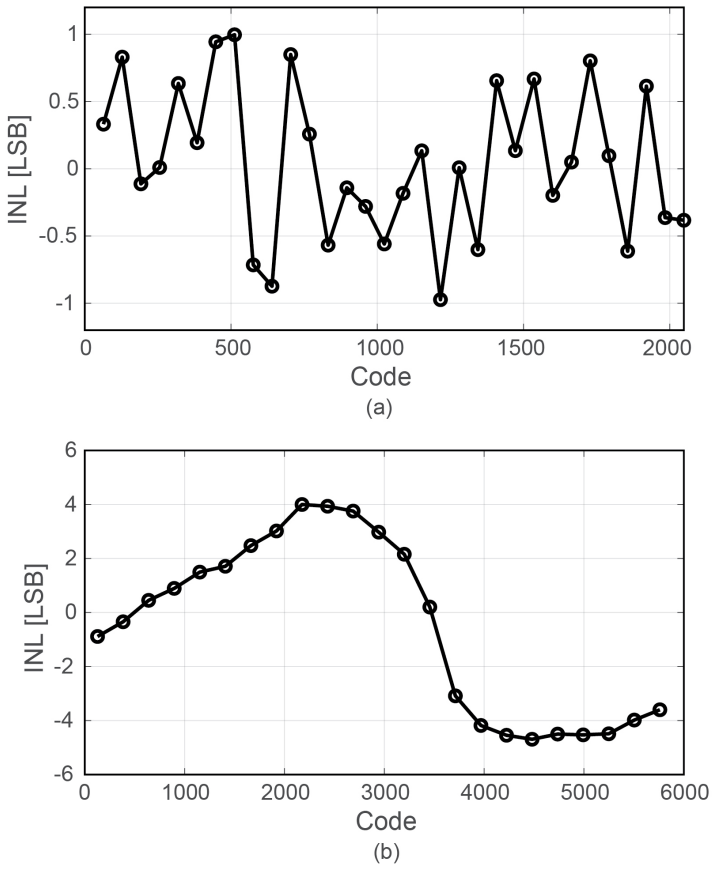


Figure 4.20: Measured INL (a) fine input range (without adaptive-reference function); (b) overall input range (with adaptive-reference function).

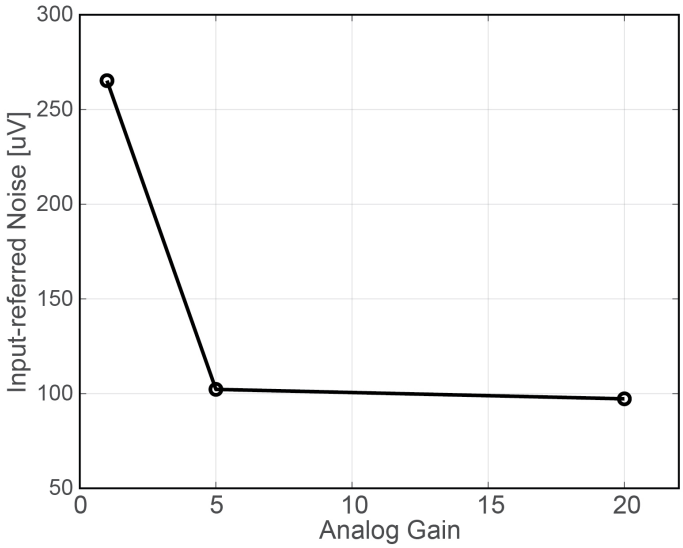


Figure 4.21: Measured input referred noise as a function of PGA gain settings.

including PPD and source follower, is at least 1%, the non-linearity of the ADC that is well below its front-end, thus can be ignored.

4.5.2. Sensor Temporal Noise Measurement Results

The noise characterization has been done with the main active array of the prototype chip. The chip is operated at a 3.3V supply for the pixel array, and a 1.2V/2.5V for analog and digital circuits. The electrical and PTC measurement show that the measured conversion gain along the readout path is 230 μV/DN and 0.74 DN/e^- when PGA gain = 1 and CMS cycle number = 80, which is equivalent to 170 μV/e^-. To exclude the impact of charge transfer noise and dark current, the pixel transfer gate is grounded during the noise measurement. All the temporal noise data has been calculated over 100 continuous frames.

Figure 4.21 shows the measured input-referred noise in the voltage domain as a function of the PGA gain (G). The pixel with a 20× PGA gain features an average input-referred noise around 98 μV, compared to 265 μV with a unity PGA gain. The temporal noise decreases at a rate of $2/G$ ($1/G < 2/G < 1/\sqrt{G}$) initially, which later becomes much smaller. This tendency indicates that the AFE circuit reduces the noise originating from

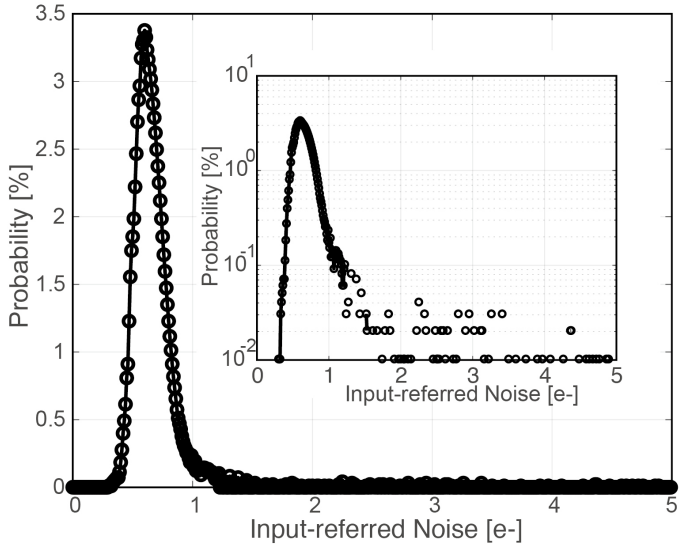


Figure 4.22: Input-referred noise histogram @ Gain = 20.

the succeeding circuits and systems at the beginning, and then suppresses the thermal noise generated by the pixel and AFE as a result of noise-bandwidth reduction.

Figure 4.22 shows the input-referred noise histogram at G = 20. The result is obtained from 480×160 pixels after performing 100 times readouts with a CMS period of 2.6 µs and a row read-out time of 5 µs. It can be found that, at G = 20, the prototype sensor achieves an input-referred noise as low as 0.55 e^-_{rms}. Although the average noise is well below a sub-electron noise level, it could be observed that some noise spread remain in the histogram, which suggests that the noise reduction effect of the proposed architecture is not perfect enough. The residual $1/f$ noise or RTS contributed by the pixel source follower or the column readout circuit can be one of the dominant noise sources that limit the effectiveness of noise reduction.

4.5.3. Performance Discussion

Table 4.1 summarizes the performance of the prototype sensor. With the measured full-well capacity of 4200 e^- and input-referred noise of 0.55 e^-_{rms}, the sensor achieves a 78 dB DR. The frame-rate showing in this table is 410 fps. However, as the prototype chip adopts a 4(pixel)-to-1(column

read-out circuit) layout approach, it will be reduced by 4 times to 102 fps if the full frame image is captured. The column FPN is 0.035 % at PGA gain $\times$20, which is equivalent to 1.5 e^-_{rms} and 255 μV_{rms}. It mainly originated from column mismatches in the pixel array and the column read-out circuit. Based on the calculation method provided in [10] and [17], the calculated FoM for this design is 0.47 e^-·nJ and 1.18 e^-·pJ respectively. For the scenario that a full image is taken, then the FoM will be four times higher. Table 4.2 summarize the performance of the prototype in comparison with prior work on ADC designs for CIS. In this design, since the proposed ADC stage employs a reference-adaptive method, we reserve a redundancy for the reference voltage of the $\Delta\Sigma$ ADC by setting the fine conversion range equal to 1.2 LSB instead of 1 LSB of the coarse conversion. In this way, the input will safely stay within the input range of the fine $\Delta\Sigma$ modulator. However, it requires an extra calibration and correction algorithm for the reference voltage, leading to digital process overhead in the FPGA at the system level.

4.6. Conclusions

In this chapter, an inverter-based programmable-gain amplifier and a digital CMS reference-adaptive ADC has been presented and verified with a VGA format prototype CIS fabricated in a 65/90 nm CIS process. The proposed column-parallel read-out circuits suppress the readout noise with a gain stage and a band-pass (CDS & CMS) filtering characteristic, achieving a 107 μV_{rms} input-referred noise, which is equivalent to 0.55 e^-_{rms}. In contrast to conventional digital CMS architectures, the proposed ADC architecture operates with a reference-adaptive mechanism, which shortens the conversion time and speeds up the frame-rate. By optimizing the trade-off between noise, power consumption and frame-rate, the figure-of-merit (FoM) is comparable to the state-of-the-art low-noise CIS. Note that the proposed adaptive-reference mechanism introduces the need for extra calibration at the system-level. This shortcoming could be tackled by adopting on-chip digital functions to automatically correct the reference error. Detailed discussions regarding potential future improvements are given in Chapter 6.

Table 4.1: Sensor performance summary

Parameter	Value
Process	65/90nm BSI DTI technology
Supply voltage	Pixel: 3.3V Analog: 1.2V/2.5V Digital: 1.2V
Area	Chip: 3×3 mm^2 Pixel: 2.5 ×2.5 μm^2 Column-parallel circuits: 10×900 μm^2
Power Consumption	Pixel: 4 mW Analog: 9 mW Digital: 9 mW IO: 5 mW
Pixel array	640 (H) × 480 (V)
Pixel size	2.5 µm (H) × 2.5 µm (V)
Conversion gain	170 µV/e^-
Pixel conversion period	5 µs
PGA gain setting	×0.25, ×1, ×5, ×20
ADC resolution	12.5 bit
Frame-rate	[1]410 fps; [2]102.5 fps
Input-referred noise	0.55 e^-_{rms}
Full-well capacity	4200 e^-
Dynamic range	78 dB
column FPN	0.035%
FoM[3]	[1]0.47 e-· nJ; [2]1.88e-·nJ
FoM[4]	[1]1.18 e-·pJ; [2]4.72e-·pJ

[1]single readout mode (160-col)

[2]multiplex readout mode (640-col)

$$^{3}\text{FoM} = \frac{\text{Power} \times \text{Noise}}{\text{Number of pixels} \times \text{Frame rate}} \times 10^{9}[\text{e-·nJ}] \tag{4.10}$$

$$^{4}\text{FoM} = \frac{\text{Power} \times \text{Noise} \times \text{Gain}}{\text{Number of pixels} \times \text{Frame rate} \times \text{dynamic range}} \times 10^{9}[\text{e}^{-}\cdot\text{pJ}] \tag{4.11}$$

Table 4.2: Comparison to Previous Works

	This work	**ISSCC'15 [18]**	**ISSCC'16 [19]**	**ISSCC'16 [20]**	**TED'16 [21]**	**JSSC'17 [22]**
Process [nm]	90/65	90/65	130	65/65	130/65	180
ADC type	$\Delta\Sigma$	SS	Dual Gain & SS	3-stage cyclic	PWM-SD	DS integrating
CG [µV/e$^-$]	170	76.6	91	92	54	96
Resolution [bit]	12.5	12	12	12	12	12
Noise [e^-_{rms}]	0.55	1.3	3.5	3.6	1.2	1
Row time [µs]	5	-	16	-	2.7	3.8
[3]FoM [e$^-$·nJ]	1.88	1.1	5.5	1.36	3.84	1.4/1.7

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5

Temporal Noise Reduction Using Gm-Cell-Based Pixel and Period-Controlled Variable Conversion Gain

This chapter is written based on the following published articles:

- X. Ge and A. Theuwissen, "A 0.5 e^-_{rms} Temporal Noise CMOS Image Sensor With Gm-Cell-Based Pixel and Period-Controlled Variable Conversion Gain" in *IEEE Trans. Electron Devices*, vol.64, no. 12, pp. 5019-5026, Dec. 2017.
- X. Ge and A. Theuwissen, "Temporal Noise Analysis of Charge-Domain Sampling Readout Circuits for CMOS Image Sensors" in *Sensors 2018,* 18(3), 707, Special Issue on the 2017 International Image Sensor Workshop (IISW).

5.1. Introduction

THE increasing demand in photon-starved imaging systems, especially in the application of medical and diverse scientific imaging, requires the development of high-sensitivity CMOS image sensors (CIS). The advantages of such a CIS solution over alternative imaging techniques include its power-efficient, cost-effectiveness, and capability of supporting higher spatial resolution. However, the read-out noise originating from the signal path of a CIS plays a significant role in the total imaging systematic error budget, and thus often limits their ultimate detection performance.

To address this shortcoming, along with recent advances in the CIS process, a variety of approaches [1]-[14] have been proposed to reduce the input-referred noise of CIS. One solution based on implementing a high-gain column-level amplifier [2], [3] has widely been used in low-light level CISs attributing to its effectiveness in temporal noise reduction. Another trend in recent works [6]–[11] is to minimize the capacitance of the floating diffusion node in the pixel. In view of the high conversion gain (CG), these image sensors exhibit a very impressive photon-counting capability in respect of the noise performance. Nevertheless, the use of a fixed high-gain amplification, either in the voltage domain or the charge domain, inevitably leads to degradation of the dynamic range (DR). Given the fact that the signal-to-noise ratio at high light levels is adequate without high-gain amplification, an efficient technique to embed a tunable CG along the read-out path is essential for the implementation of low-noise CMOS image sensor with high DR.

In this chapter, a Gm-cell-based pixel target for a deep sub-electron temporal noise CIS is presented [15]. Implemented in a standard 0.18 μm CIS technology, the proposed pixel structure adopts in-pixel amplification method [1] to reduce its input-referred noise. To overcome the trade-off between high DR, which benefits from low gain, and low input-referred noise, which benefits from high gain, a pixel-level variable-gain has been realized in a period-controlled manner. As such, the read-out path CG can be programmed according to the specific application of the CIS without any reconstruction of the hardware. In addition, the proposed pixel architecture allows the realization of pixel-level amplification without any in-pixel capacitors or resistors, enabling a relatively pixel compact layout with a pitch of 11 μm. Different from conventional low-noise CIS architectures, the Gm-cell-based pixel leverages the use of a column-level

high-gain amplifier and correlated multiple sampling (CMS). This simplifies the system and decreases the row read-out time. Measurement results show that the Gm-cell-based pixel effectively realizes a period-controlled CG, which can be tunable from 50 μV/e^- to 1.6 mV/e^- with a charging period from 100 ns to 4 μs. In addition, an input-referred noise of 0.5 e^-_{rms} is achieved in the measurement within a correlated double sampling (CDS) period of 5 μs and a row read-out time of 10 μs.

The rest of this chapter is organized as follows. Section 5.2 describes the operating principle of the Gm-cell-based pixel and the periodic filtering model of the charge domain sampling. Section 5.3 introduces the theoretical fundamentals used for the noise analysis and discusses the noise analysis model. Section 5.4 describes the circuits and sensor implementation details. The characterization results of the fabricated image sensor are presented in Section 5.5. Finally, a conclusions is given in Section 5.6.

5.2. Operating Principle

In a conventional CIS, a source follower (SF) (Figure 5.1) is used in every pixel for buffering the floating diffusion (FD) node voltage onto the sample and hold (S/H) capacitors or column-parallel switched-capacitor amplifiers. Owing to its unity-gain nature, the SF topology inherently restricts the signal amplification at pixel-level. As a consequence, the combination of the pixel-level SF and column-level amplifier has been recognized as the most significant noise contributor along the read-out path. To address this problem, in this paper, we use a trans-conductance (Gm) -cell-based pixel (Figure 5.2). In contrast to prior work [26], which employed a trans-conductance cell to convey the pixel voltage to a current-mode output, the proposed pixel integrates the output current of the trans-conductance cell on a column-level S/H capacitor, thus producing a voltage output. This topology, on the one hand, offers a pixel-level voltage gain to reduce the input-referred noise, and enables a period-controlled variable gain to achieve an optimal noise/DR tradeoff on the other hand. A dedicated charge-domain CDS technique has been applied to a CIS to realize this period-controlled method as well as to act as a *sinc*-type low-pass filter to reduce the input-referred noise, which will be discussed in this section.

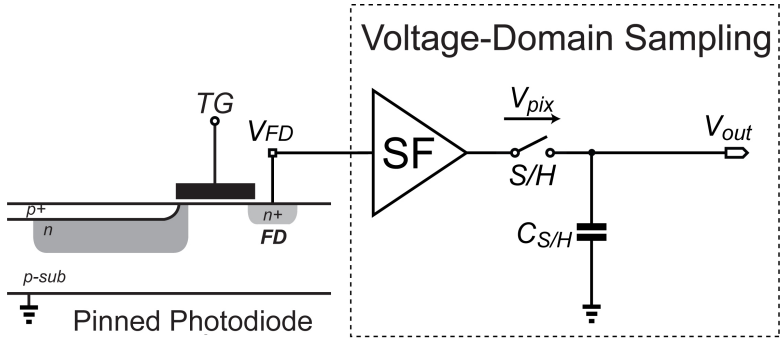


Figure 5.1: Signal readout mechanism: SF-based pixel with voltage-domain sampling

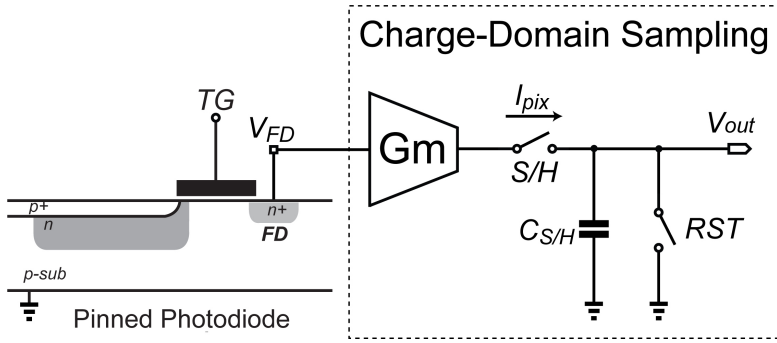


Figure 5.2: Signal readout mechanism: Gm-cell-based pixel with charge-domain sampling

5.2.1. Concept of Gm-Cell-Based Pixel

Figure 5.3 shows the operating principle of the Gm-cell-based pixel. The pixel is composed of a pinned-photodiode (PPD) followed by a Gm-cell. Combined with the S/H capacitors, the read-out chain acts as a Gm-C integrator. Unlike the conventional SF-based pixel, which samples the signal with an exponential settling process in voltage domain, the proposed architecture first converts the FD node voltage V_{FD} into a current I_{pix}. Afterwards, this current starts charging the S/H capacitors with capacitance value of $C_{S/H}$ within a programmable time window T_{ch}. Upon completion of the charging process (at the end of T_{ch}), the resulting voltage on the S/H capacitors is readout. To ensure that there is no relation between two adjacent sampling operations, the S/H capacitor is discharged by switching on RST before the next new sample. This process is often referred to as charge-domain sampling, which is also known as boxcar sampling [16].

Neglecting non-ideal effects of the circuit, the time-domain output voltage of the sampler can be written as:

$$\begin{aligned} V_{out}(t) &= \frac{1}{C_{S/H}} q[t] = \frac{1}{C_{S/H}} \int_{nT_s}^{nT_s+T_{ch}} I_{pix} dt \\ &= \frac{g_m}{C_{S/H}} \int_{nT_s}^{nT_s+T_{ch}} V_{FD} dt \end{aligned} \tag{5.1}$$

where g_m is the trans-conductance value of the Gm-cell, $C_{S/H}$ is the S/H capacitance, n is an integer, T_{ch} is the charging period, and T_s is the sampling period.

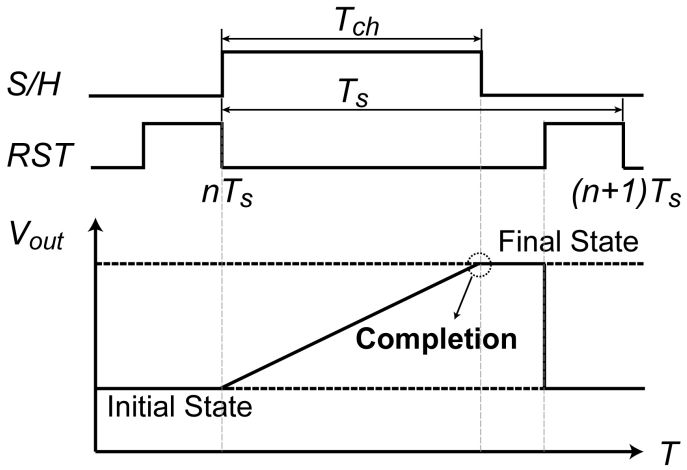


Figure 5.3: Basic timing diagram and conceptual output waveform of a Gm-cell-based pixel

5.2.2. Periodic Filtering Model of the Charge Domain Sampling

The described charging process in Equation (5.1) behaves as the convolution integral of an input signal and a rectangular window whose height is $g_m/C_{S/H}$ and width is T_{ch}. Thus, it forms a continuous-time (CT) first-order *sinc*-type low-pass filter prior to sampling at discrete-time (DT) intervals (Figure 5.4) [17]. The transfer function of this filter in the

s-domain [18] is given by:

$$H(s) = \frac{g_m T_{ch}}{C_{S/H}} \cdot \frac{1 - e^{-sT_{ch}}}{sT_{ch}} \tag{5.2}$$

and the ideal magnitude transfer function can be expressed as:

$$|H_{WI}(f)| = \frac{g_m T_{ch}}{C_{S/H}} \cdot \left| \frac{sin(\pi f T_{ch})}{\pi f T_{ch}} \right| = \frac{g_m T_{ch}}{C_{S/H}} \cdot |sinc(\pi f T_{ch})| \tag{5.3}$$

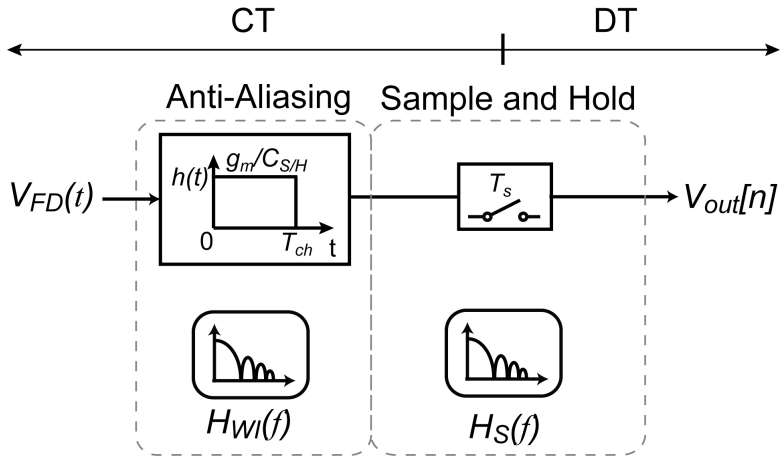


Figure 5.4: Block diagram model of charge-domain sampling

Figure 5.5 shows the curve of $|H_{WI}(f)|$ (without ZOH process). From the envelope of the curve, the roll-off of the transfer function side-lobe is found as -20 dB/dec, which is the same as a first-order low-pass filter. In addition, the notches of this *sinc*-type filter land at integer multiples of kf_{ch}, where $f_{ch} = 1/T_{ch}$ and k is an integer. Accordingly, the aliasing interference at kf_{ch} is theoretically infinite attenuated by the notches before they are aliased on top of the desired signal. As the notches only appear at discrete frequencies, the suppressed amount of high frequency components at other frequency ranges is decided by the skirts of sidelobe adjacent to a notch. If the aliasing component appears at an offset frequency Δf from the *k*-th notch kf_{ch}, it will be suppressed by:

$$|A(kf_{ch} + \Delta f)| = |\frac{sin(\pi + \pi \Delta f T_{ch})}{\pi + \pi \Delta f T_{ch}}| \approx |\frac{\Delta f}{f_{ch}}| \tag{5.4}$$

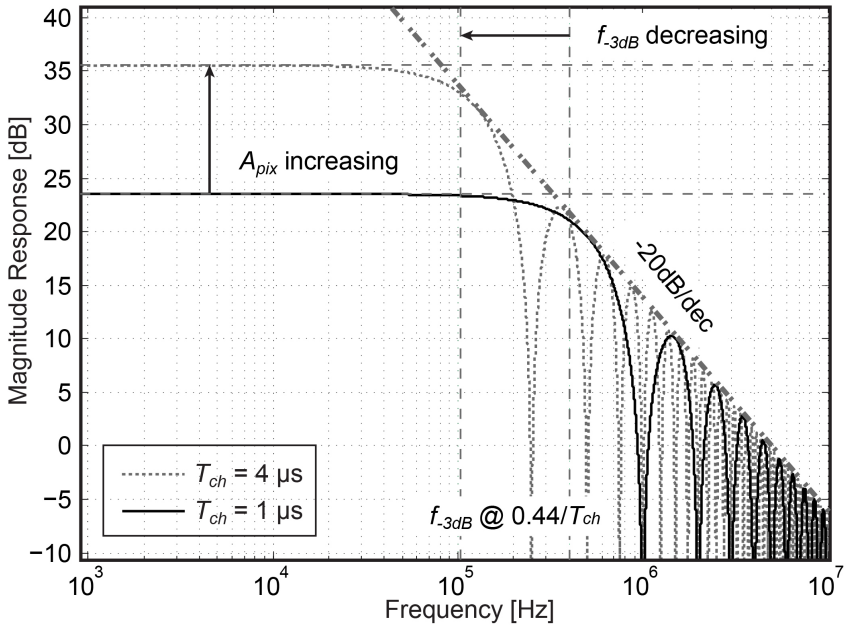


Figure 5.5: Transfer function of the charge sampling *sinc*-type low-pass filter

where $\Delta f \ll f_{ch}$. It can be shown that for a given signal bandwidth and a particular attenuation requirement in the aliasing bands, Equation(5.4) sets the required charging clock frequency to ensure a sufficiently wide $sinc$ notches. Our simulation in MATLAB shows that, with the aid of the $sinc$ notch attenuation, the charge-domain sampling reduces more than 20% thermal noise, in comparison with the voltage-domain sampling which features a first-order low-pass transfer function.

The transfer function also shows that the -3 dB bandwidth of the $sinc$ filter is around $f_{-3dB} \approx 0.44/T_{ch} = 0.44 f_{ch}$ [20]. Meanwhile, the ideal DC voltage gain is found as:

$$A_{pix} = \frac{V_{out}}{V_{FD}} = \frac{g_m T_{ch}}{C_{S/H}} = g_m \frac{1}{C_{S/H} f_{ch}} \tag{5.5}$$

where $1/C_{S/H} f_{ch}$ can be regarded as the equivalent discrete time output impedance of the Gm-cell. Given the fact that both the gain of the voltage amplification A_{pix} and -3 dB bandwidth f_{-3dB} are determined by T_{ch}, a programmable A_{pix} and f_{-3dB} can be obtained by tuning the time window

T_{ch} without using any other changes at circuit-level implementation. Figure 5.5 also shows the charge-domain sampler transfer function with a different T_{ch} applied. Note that increasing T_{ch} not only helps in boosting the DC gain, but also reducing the bandwidth of the charge-domain sampler. This result is used in the operation of the CIS with proposed Gm-cell-based pixel to reduce the input-referred noise, which will be described in next section.

5.2.3. Periodic Filtering Model of the Charge Domain CDS

CDS is a well-known noise reduction technique in CIS. By subtracting the reset level and signal level, which are sampled at T_{rst} and T_{sig}, the effectiveness of the CDS noise canceller can be characterized as a DT high-pass filtering operation, as analyzed in [21]. The CDS transfer function $H_{CDS}(f)$ and voltage domain CDS transfer function, including the low pass filter (LPF) are given by:

$$|H_{CDS}(f)| = |2sin(\pi f T_0)| \tag{5.6}$$

$$|H_{CDS_v}(f)| = \frac{|2sin(\pi f T_0)|}{\sqrt{(1+(f/f_{-3dB})^2)}} \tag{5.7}$$

where T_0 is the sampling interval between T_{rst} and T_{sig}. A behavioral model of the Gm-cell-based pixel with charge domain CDS is depicted in Figure 5.6. As two distinct filtering functions, namely, a CT *sinc* low-pass filter $H_{WI}(f)$ and a DT high-pass filter $H_{CDS}(f)$ are realized simultaneously, the overall transfer function of the charge-domain CDS without zero-order hold effect [22] can be written as:

$$\begin{aligned} |H_{CD}(f)| &= |H_{WI}(f)| \cdot |H_{CDS}(f)| \\ &= |2\frac{g_m T_{ch}}{C_{S/H}} sinc(\pi f T_{ch}) \cdot sin(\pi f T_0)| \end{aligned} \tag{5.8}$$

Compared to a corresponding voltage-domain CDS transfer function, which has an equal -3 dB bandwidth, the charge-domain CDS introduces two groups of notches. As shown by simulations in Figure 5.7, one group of notch frequencies is located at T_{ch}/k, owing to the charge-sampling

$sinc$-type filter $sinc(\pi f T_{ch})$, while the other group is placed at T_0/k, owing to the $sinc$ function effect $(sin(\pi f T_0))$ of the CDS operation [22]. The joint effect of $sinc(\pi f T_{ch})$ and $sin(\pi f T_{ch})$ increases the depth of the notches and thus further improves the attenuation in the stopband. As such, compared with the voltage-domain CDS response, the charge-domain CDS provides a greater extent attenuation on high-frequency noise components than the first-order low-pass filtering of the voltage-sampling circuits.

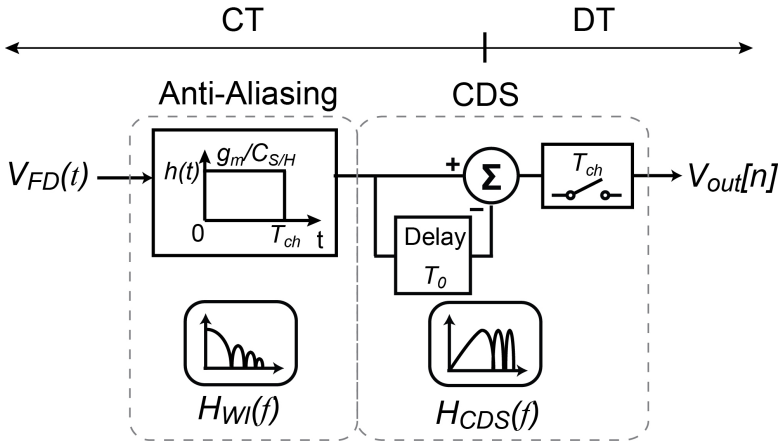


Figure 5.6: Block diagram model of charge-domain CDS

5.3. Noise Analysis of a Gm-Cell-Based Pixel

While the operational principle and periodic filtering model of the charge domain sampling of the Gm-cell-based pixel have been described in Section 5.2, this section 5.3 focuses on its noise characteristic. Compared to its counterpart based on source followers, a Gm-cell-based pixel operates in a non-stationary large-signal manner, i.e., its bias condition changes as a function of the operating time. Therefore, the traditional temporal noise analysis method on steady-state small-signal models does not readily apply to a Gm-cell-based pixel. In view of the above issues, we propose an exact temporal noise model to guide the analysis and design of a Gm-cell-based pixel.

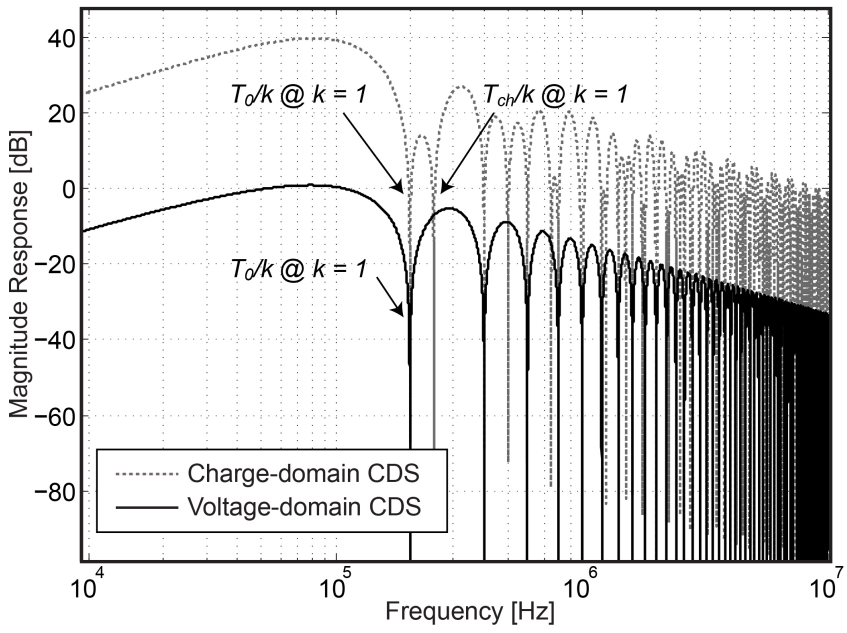


Figure 5.7: Transfer function of the charge-domain CDS versus voltage domain CDS

5.3.1. Nonstationary Noise Theory Analysis

Temporal noise analysis on conventional CIS readout circuits is established based on the fact that the pixel-level SF operates in the steady-state. As shown in Figure 5.8, in the process of the voltage-domain sampling with an exponential settling behavior, the statistics properties of the temporal noise do not vary as a function of time and can be well represented by its time-averaged root-mean-square (rms) value. However, this prerequisite is not valid for Gm-cell-based pixels. A time-domain plot of the voltage on the S/H capacitor with superimposed random noise is conceptually shown in Figure 5.9. As explained in Section 5.2, the final output signal on the S/H capacitor is obtained through a charging process. Given the fact that the proposed readout topology works with a large signal behavior throughout its operation, the standard deviation of the voltage distribution and hence the rms value of the noise is no longer static with time. Therefore, the conventional noise analysis method based on steady-state models is not appropriate for Gm-cell-based pixels along with its read-out

path. To quantitatively analyze the nonstationary noise, a time-domain linear analysis approach, based on the autocorrelation of a nonstationary random process, has been described in [14, 22]. Here, we apply a similar approach to evaluate the temporal noise characteristic of Gm-cell-based pixels.

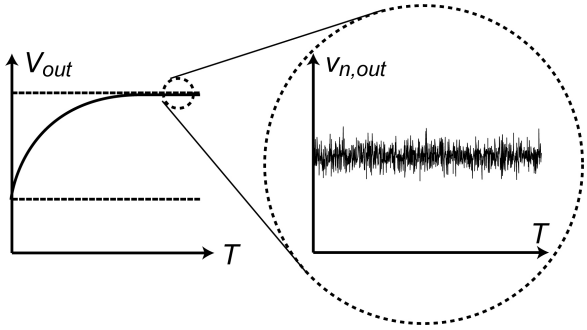


Figure 5.8: Steady-state noise waveform for SF-based pixel

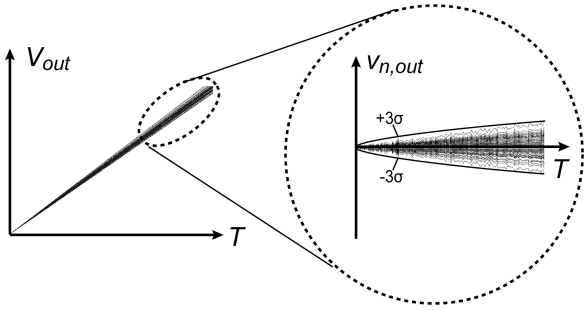


Figure 5.9: Non-steady-state noise waveform for Gm-cell-based pixel

Noise in the time-domain represents the variance of a random process, which can be derived from its autocorrelation as a function of time [23]. Suppose that the time-domain representatives of the input and output noise are $X(t)$ and $Y(t)$ respectively, the autocorrelation of the input noise between two time points (t_1 and t_2) is $R_{xx}(t_1, t_2)$ and the time-domain impulse response of the pixel readout circuit is $h_p(t)$. Thus, the autocorrelation of the output noise can be derived from time-domain convolutions:

$$R_{YY}(t_1, t_2) = h_P(t_1) * R_{XX}(t_1, t_2) * h_P(t_2) \tag{5.9}$$

The variance of $Y(t)$ as a function of the autocorrelation is:

$$\sigma_Y^2(t) = E[Y(t)Y(t)] = R_{YY}(t_1, t_2)|_{t_1=t_2=t} \tag{5.10}$$

where E is the expected value operator. Equations (5.9) and (5.10) serve as the fundamental for the time-domain analysis of Gm-cell-based pixels. As can be seen, in order to investigate the output noise in the time-domain, all that is required is the input noise autocorrelation functions of different noise sources, as well as the impulse response from the pixel input voltage (V_{FD}) to its output. During the charging phase of a Gm-cell-based pixel, both the thermal noise and flicker noise of the Gm-cell contribute to the overall output noise. In addition, the kTC noise caused by the column-level switch also contributes to a part of noise in the reset phase. Therefore, in the following discussions their contributions will be investigated separately.

5.3.2. Equivalent Noise Model and Noise Gain

Although a Gm–C integrator works in a large-signal behavior throughout its charging phase, its small-signal model at the completion moment of the sampling response can still be utilized for a first-order noise analysis, due to the fact that only the noise power at that point has impacts on the final decision. Figure 5.10 shows the noise model and the equivalent small signal model of the readout path of a Gm-cell-based pixel.

In order to facilitate the noise optimization, the mentioned output noise power needs to be referred to the FD node. For this purpose, the noise gain of the Gm-cell-based pixel must be first calculated. According to [14], the noise gain $|A_N|$ of an integrator-like Gm-cell can be determined by the ratio of voltage slopes at the output and input ports:

$$|A_N| = \left(\frac{dV_{out}(t)}{dt}\Big|_{t=T_{ch}}\right) \Big/ \left(\frac{dV_{FD}(t)}{dt}\Big|_{t=T_{ch}}\right) \tag{5.11}$$

The input signal V_{FD} of the Gm-cell during the charging phase can be assumed as a step input and is given by:

$$V_{FD}(t) = Mu(t) \tag{5.12}$$

where M is the input voltage magnitude. The time-domain response of a Gm-cell to a step input is given by:

$$V_{out}(t) = A_0 M(1 - e^{-t/\tau})u(t) \tag{5.13}$$

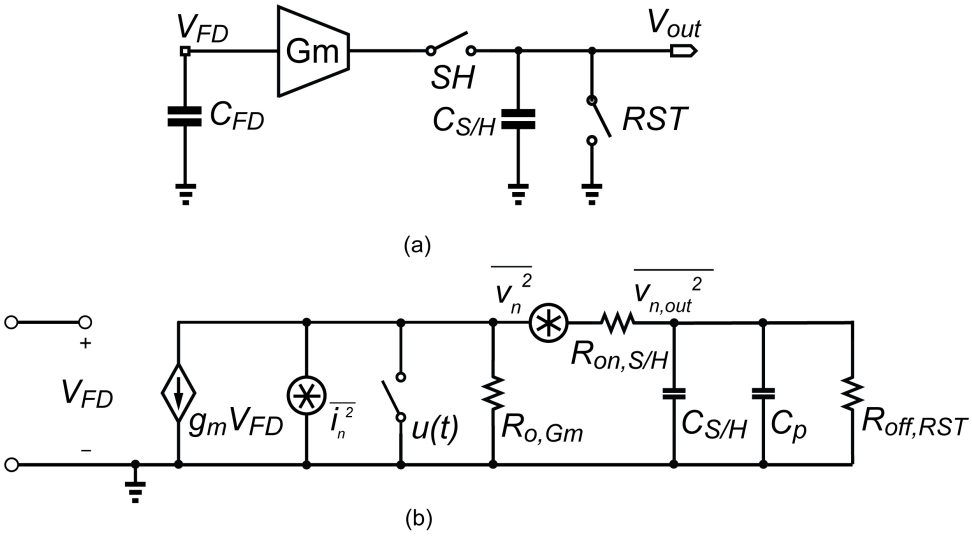


Figure 5.10: (a) Schematic of a Gm-cell-based pixel. (b) Equivalent noise model of a Gm-cell-based pixel.

and

$$A_0 = g_m R_{out} \tag{5.14}$$

$$\tau = R_{out} C_L = R_{out}(C_{S/H} + C_P) \tag{5.15}$$

$$R_{out} = R_{o,Gm} || (R_{off,RST} + R_{on,S/H})) \tag{5.16}$$

where A_0 is the DC gain of the Gm-cell at the steady-state, τ is the time constant of the Gm-C integrator, $R_{o,Gm}$ is the output impedance of the Gm-cell, $R_{on,S/H}$ is the on-resistance of switch SH, the value of which is much smaller than $R_{o,Gm}$, $R_{off,RST}$ is the off-resistance of switch RST, C_L is the total loading capacitance, $C_{S/H}$ is the sample and hold capacitance, C_p is the parasitic capacitance of the column bus. Thus, the final noise gain of the Gm-cell can be described by the following expression:

$$|A_N||_{t=T_{ch}} = A_0(1 - e^{-T_{ch}/\tau}) \tag{5.17}$$

Note that this result can be simplified into two special cases:

$$|A_N| = \begin{cases} G_m R_{out}, & \text{for } T_{ch} \gg \tau \quad \text{(a)} \\ G_m T_{ch}/C_L, & \text{for } T_{ch} \ll \tau \quad \text{(b)} \end{cases} \tag{5.18}$$

To be more precise, Figure 5.11 and Figure 5.12 showing the variation of the noise gain factor as a function of charging period T_{ch} with a wide range

of the time constant τ. As revealed in Figure 5.11 and Equation (5.18)(a), with a constant T_{ch} and the time-boundary $T_{ch} \gg \tau$, the noise gain increases as τ and R_{OUT} are increasing, showing the steady-state noise gain characteristic of a broadband amplifier. Figure 5.12 and Equation (5.18)(b) show an integrator-like noise gain with the time-boundary $T_{ch} \ll \tau$ resulting from the charge-sampling process as explained in [2], which is inversely proportional to τ and C_L with a constant T_{ch}.

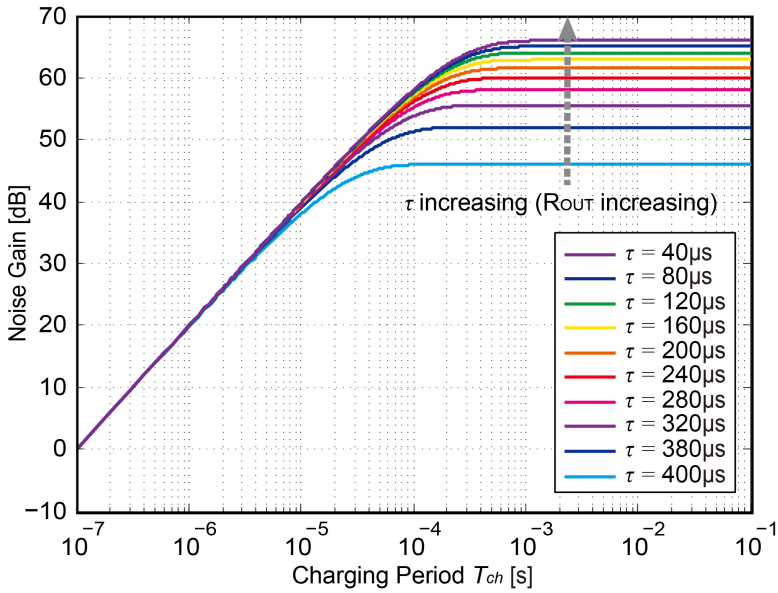


Figure 5.11: Noise gain factor as a function of charging period T_{ch} with τ and R_{OUT} increasing.

As charge-domain sampling is performed with the time-boundary $T_{ch} \ll \tau$, a dedicated Gm-cell structure with sufficient τ is called for. To realize a high output impedance, so as to enable a large τ, a cascode common-source amplifier is employed as the internal Gm-cell for this proposed pixel architecture. Figure 5.13(a) depicts the schematic of the Gm-cell used in Figure 5.10. In this structure, G_m is mainly determined by the input transistor M_1 ($G_m \approx g_{m1}$), and the output impedance $R_{o,Gm}$ is approximately equal to $R_{o,Gm} \approx g_{m2}r_{o2}r_{o1} \| g_{m3}r_{o3}r_{o4}$, where g_{m2} and g_{m3} are the trans-conductance of pMOS cascode M2 and nMOS cascode M3, r_{o1} to r_{o4} are the output resistance of transistor M1 to M4.

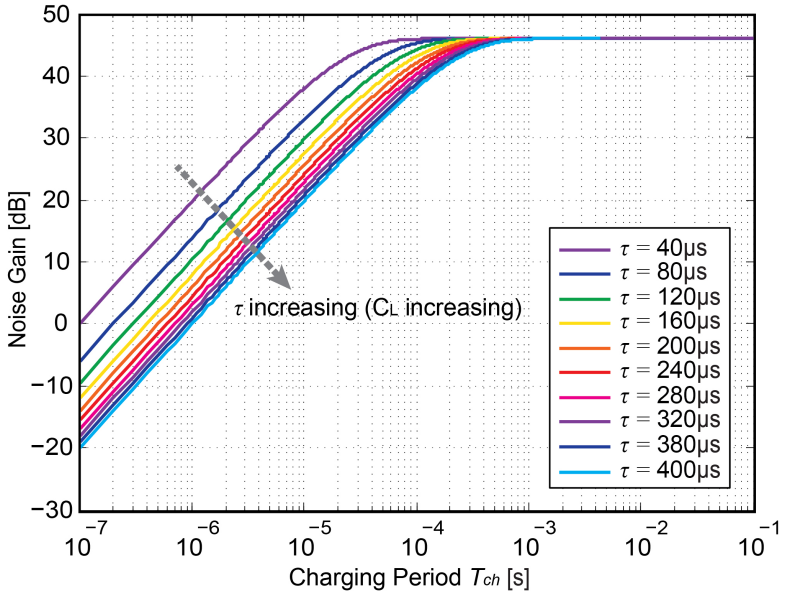


Figure 5.12: Noise gain factor as a function of charging period T_{ch} with τ and C_L increasing.

Coupled with the S/H stage, the overall Gm-C integrator equivalent circuit for noise calculation is shown in Figure 5.13(b). In such a case, Equation(5.18) can be re-written as:

$$|A_N| = \begin{cases} g_{m1}R_{out}, & \text{for } T_{ch} \gg \tau \quad \text{(a)} \\ g_{m1}T_{ch}/C_L, & \text{for } T_{ch} \ll \tau \quad \text{(b)} \end{cases} \tag{5.19}$$

where

$$R_{out} = g_{m2}r_{o1}r_{o2} \| g_{m3}r_{o3}r_{o4} \| (R_{off,RST} + R_{on,S/H}) \tag{5.20}$$

and

$$\tau = [g_{m2}r_{o1}r_{o2} \| g_{m3}r_{o3}r_{o4} \| (R_{off,RST} + R_{on,S/H})] \cdot (C_{S/H} + C_p) \tag{5.21}$$

5.3.3. Noise Model of Charging Phase

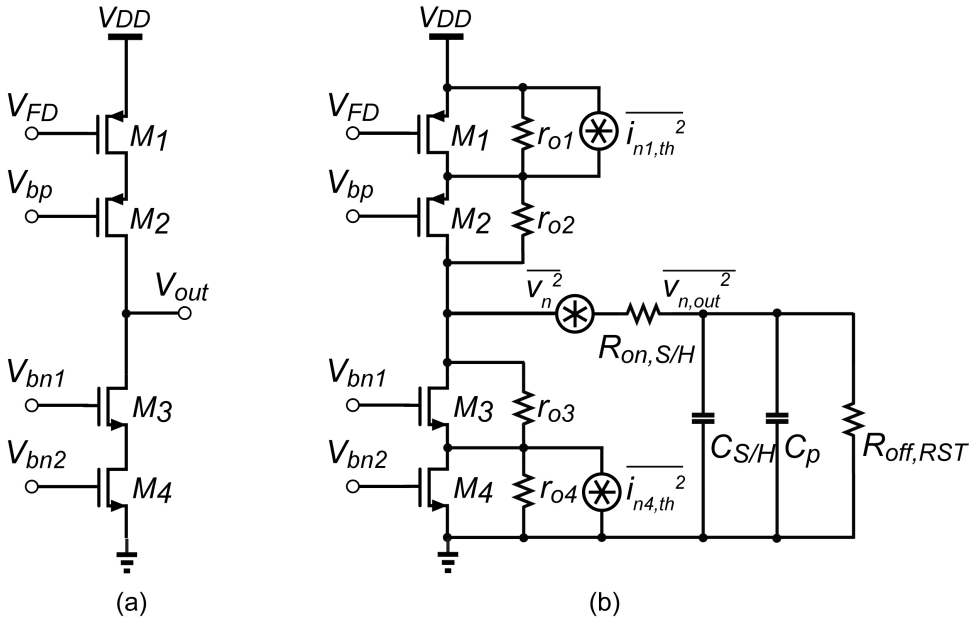


Figure 5.13: (a) Schematic of cascode common-source amplifier for Gm-cell. (b) Equivalent circuit of Gm-C integrator for noise calculation.

5

Thermal Noise

In a Gm-cell small signal model, the impulse response from the noise current source to the output voltage V_{out}, is given by:

$$h_p(t) = \frac{1}{C_L} e^{-t/\tau} u(t) = \frac{1}{C_{S/H} + C_p} e^{-t/\tau} u(t) \tag{5.22}$$

where $u(t)$ is the noise current unit step input.

Consider a white noise unit step input $u_n(t)$, the autocorrelation function of the thermal noise source is a dirac delta function $\delta(t)$ with an amplitude equal to its double-sided power spectral density (PSD):

$$R_{XX,th}(t_1, t_2) = \frac{S_{th,n}}{2} \delta(t_2 - t_1) \tag{5.23}$$

where $S_{th,n}$ is the equivalent single-sided thermal noise PSD. According to Figure 5.10, the noise sources include the equivalent current noise source i_n from the pixel-level Gm-cell, and the equivalent voltage noise source v_n

from the column-level sample-and-hold switch S/H. Thus, $S_{th,n}$ can be modeled as:

$$S_{th,n} = 4kTG_n + \frac{4kTR_{on,S/H}}{R_{out}^2} \approx \frac{8}{3}kT(g_{m1} + g_{m4}) \tag{5.24}$$

where $G_n = 2(g_{m1} + g_{m4})/3$ is the equivalent noise trans-conductance of i_n, $k = 1.3807 \times 10^{-23} J/K$ is the Boltzmann constant and T is absolute temperature in Kelvin.

By substituting Equation (5.9) and Equation (5.10) into Equation (5.23), we obtain the variance of the output voltage due to the time-variant thermal noise, as given by:

$$\sigma_{Y,th}^2(t) = \frac{S_{th,n}}{2}\int_0^t |h(\alpha)|^2 \, d\alpha \tag{5.25}$$

With the aid of Equation (5.24), the above integral can be solved as:

$$\sigma_{Y,th}^2(t) = \frac{2}{3}\cdot\frac{kT}{C_{S/H}+C_p}(g_{m1}+g_{m4})R_{out}\left[1-e^{-2t/\tau}\right]u(t) \tag{5.26}$$

In a charge sampling circuit, only the noise at the instant of the sampling completion (T_{ch}) has impact on the final readout noise. Accordingly, the concerned output thermal noise power of a Gm-cell based pixel can be evaluated as:

$$\begin{aligned}\overline{v_{n,th}^2} &= \sigma_{Y,th}^2(t)\Big|_{t=T_{ch}} \\ &= \frac{2}{3}\cdot\frac{kT}{C_{S/H}+C_p}(g_{m1}+g_{m4})R_{out}\left[1-e^{-2T_{ch}/\tau}\right]\end{aligned} \tag{5.27}$$

On the basis of Equation (5.17) and Equation (5.27), the input thermal noise power can be derived by:

$$\begin{aligned}\overline{v_{in,th}^2} &= \sigma_{Y,th}^2(t)\Big|_{t=T_{ch}} / |A_N|\,|_{t=T_{ch}}^2 \\ &= \frac{2}{3}\cdot\frac{kT}{\tau}\cdot\left(\frac{1}{g_{m1}}+\frac{g_{m4}}{g_{m1}^2}\right)\cdot\coth\left(\frac{T_{ch}}{2\tau}\right)\end{aligned} \tag{5.28}$$

As Equation (5.28) contains a hyperbolic function of the ratio of the charging time T_{ch} and time constant τ, the time limits $T_{ch} \gg t$ and $T_{ch} \ll t$ are thus

of interest. Hence, (5.28) can be re-written as:

$$\overline{v_{in,th}^2} = \begin{cases} 4kT \cdot \frac{2}{3}\left(\frac{1}{g_{m1}} + \frac{g_{m4}}{g_{m1}^2}\right) \cdot \frac{1}{4\tau}, & \text{for } T_{ch} \gg 2\tau \\ 4kT \cdot \frac{2}{3}\left(\frac{1}{g_{m1}} + \frac{g_{m4}}{g_{m1}^2}\right) \cdot \frac{1}{2T_{ch}}, & \text{for } T_{ch} \ll 2\tau \end{cases} \tag{5.29}$$

Figure 5.14 shows the variation of the input thermal noise power with a wide range of time constant τ. With a fixed T_{ch}, the input-referred thermal noise decreases as τ increases at the time-boundary of $T_{ch} \ll t$. Its noise behavior is identical with the input-referred thermal noise power in common single-pole steady-state systems. On the other hand, if $T_{ch} \ll t$, the input-referred thermal noise linearly reduces as T_{ch} gets longer for a given τ. Within this region, the thermal noise becomes T_{ch}-dependent and behaves as an integrator-like noise. As such, this interesting characteristic offers an orientation to the thermal noise estimation in the specific design of Gm-cell-based pixels.

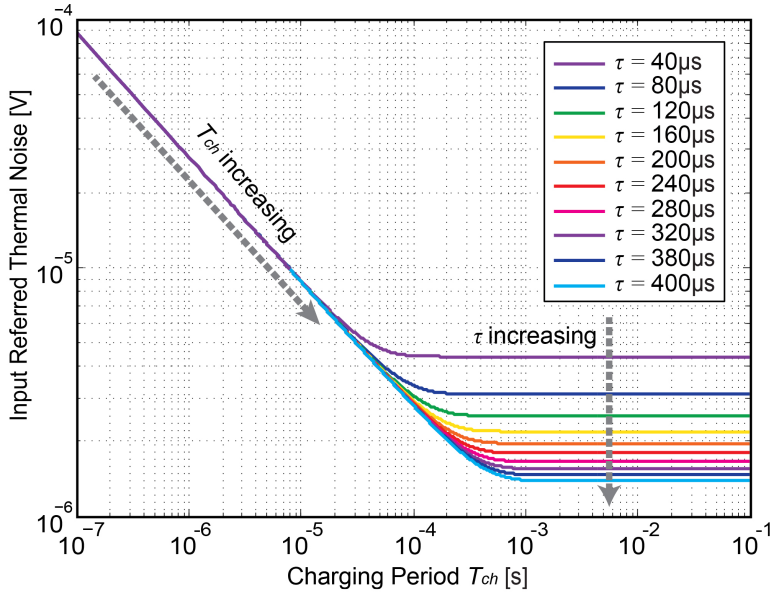


Figure 5.14: Input referred thermal noise a a function of charging period T_{ch}.

Flicker Noise

Flicker noise in CIS refers to those noise sources whose PSD is inversely proportional to the frequency. The flicker noise PSD sourced from the input MOS transistor of the Gm-cell can be modeled as:

$$S_{1/f,n} = \frac{K}{C_{ox} \cdot A} \cdot \frac{1}{f} \cdot (g_{m1} + g_{m4})^2 \tag{5.30}$$

where K is a process-dependent constant, C_{ox} is the unit oxide capacitance of the MOS gate, A is the channel area, f is the frequency. In contrast to thermal noise, the time-domain response of flicker noise is a non-stationary process. Its autocorrelation can be modeled as the output of a $1/f$ noise-shaping filter driven by the autocorrelation function of the thermal noise:

$$R_{XX,1/f}(t_1, t_2) = h_{1/f}(t_1) * R_{XX,th}(t_1, t_2) * h_{1/f}(t_2) \tag{5.31}$$

where $h_{1/f}(t)$ is the impulse response of an ideal $1/f$ noise-shaping filter:

$$h_{1/f}(t) = \left(\frac{2f_c}{t}\right)^{1/2} u(t) \tag{5.32}$$

here, f_c is the corner frequency of the flicker noise, which is relevant to the process and transistor parameter:

$$f_c = \frac{K}{C_{ox} \cdot A \cdot S_{th,n}} \cdot (g_{m1} + g_{m4})^2 \tag{5.33}$$

Based on Equation (5.32) to (5.33), the autocorrelation of flicker noise can be expressed as:

$$\begin{aligned} &R_{XX,1/f}(t_1, t_2) \\ &= \frac{2K(g_{m1} + g_{m4})^2}{C_{ox}A} \int_0^\infty \frac{1}{|\mu^2 + t_2 - t_1|^{1/2}} d\mu \end{aligned} \tag{5.34}$$

Equation (5.34) appears as a divergent integral function of time [24-26] and does not have a finite limit. To address this issue, characterization of the flicker noise is often reasonably limited to a finite length of observation time window [24] (or a limited bandwidth in the frequency domain [23]). The minimum of this time window is defined by the reciprocal of the upper limit of the concerned frequency range, i.e. the flicker corner frequency

(f_c), while the total operation time of the readout circuit (t_{op}) determines the maximum. Based on this approximation, the autocorrelation of flicker noise can be written as [25]:

$$R_{XX,1/f}\left(t_{op}, t_1, t_2\right) \cong \frac{2K(g_{m1}+g_{m4})^2}{C_{ox}A} \ln \frac{4t_{op}}{|t_2 - t_1|} \tag{5.35}$$

where $\frac{1}{f_c} \ll |t_2 - t_1| \ll t_{op}$. By substituting Equation (5.22) and Equation (5.34) into Equation (5.9) and Equation (5.10), the variance of the pixel output voltage owing to flicker noise can be expressed as:

$$\sigma^2_{Y,1/f}(t) = \frac{(g_{m1}+g_{m4})^2 R_{OUT} K}{2\left(C_{S/H}+C_p\right)C_{ox}A} \int_0^t \left(\ln \frac{4t_{op}}{\alpha}\right)\left[1 - e^{-2(t+\alpha)/\tau}\right] u(\alpha) d\alpha \tag{5.36}$$

Similarly, the output flicker noise at the sampling instant is evaluated at T_{ch}:

$$\overline{v^2_{n,1/f}} = \sigma^2_{Y,1/f}(t)\Big|_{t=T_{ch}} \tag{5.37}$$

However, the integral in Equation (5.36) does not have an analytic solution. Therefore, Equations (5.36) and Equation (5.37) must be numerically computed in MATLAB to get a quantitative evaluation of the flicker noise power. Note that t_{op} should be assigned with a sufficiently large value to ensure the accuracy of approximation (typically around one hour [22]). Take the CDS effect into consideration, the impulse response of the ideal $1/f$ noise-shaping filter are assumed as $h_{1/f}(T_{ch})$ and $h_{1/f}(T_0 + 2T_{ch})$. Therefore, the autocorrelation of the flicker noise with CDS is given as:

$$R_{XX,1/f}(T_{ch}, T_0 + 2T_{ch}) = h_{1/f}(T_{ch}) * R_{XX,th}(T_{ch}, T_0 + 2T_{ch}) * h_{1/f}(T_0 + 2T_{ch}) \tag{5.38}$$

where T_0 is the interval period between two samples (reset level and signal level) which is assumed as $T_0 = 1\mu s$. Consequently, the output flicker noise

power after CDS can be defined by:

$$\sigma^2_{Y,1/f}(t) = \frac{(g_{m1}+g_{m4})^2 R_{out} K}{2\left(C_{S/H}+C_p\right) C_{ox} A} \int_0^t \left(\ln \frac{4t_{op}}{\alpha}\right) \left[1 - e^{-2(2T_{ch}+T_0+\alpha)/\tau}\right] u(\alpha) d\alpha \tag{5.39}$$

As a brief proof, Figure 5.15 numerically plots the flicker noise output power as a function of charging time T_{ch}. In contrast to input-referred thermal noise power whose value reaches steady-state until $T_{ch} \approx 2\tau$,the flicker noise is continuously increased with an increasing T_{ch}, which agrees with the theoretical analysis of the flicker noise in frequency domain.

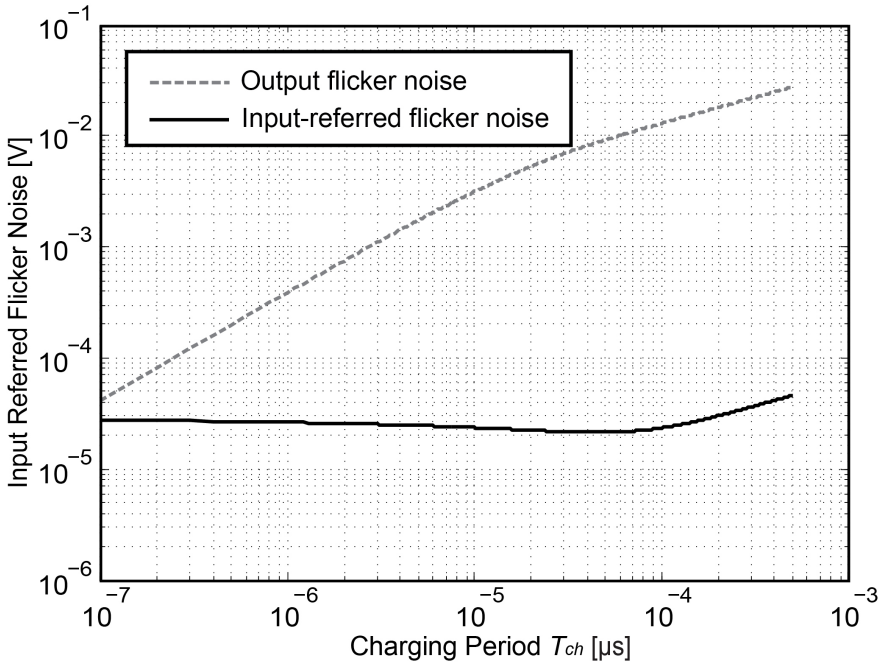


Figure 5.15: Input referred flicker noise a a function of charging period T_{ch}.

According to our circuit level simulations, the corner frequency f_c is around 500kHz, which is higher than the equivalent noise bandwidth of the proposed circuit, and thus the flicker noise obviously appears even beyond the noise bandwidth. As a result, the input-referred flicker noise is highly

dependent on T_{ch} and it is effectively reduced through increasing T_{ch}. On the contrary, as the Gm-cell enters into the steady-state region when T_{ch} gets longer. The input-referred flicker begins to increase due to a constant noise gain and noise bandwidth.

5.3.4. Noise Model of Discharging Phase

In order to segregate the sampling operations between two adjacent frames, the S/H capacitor is discharged by switching on RST before the next new frame. As the switch operation during this process is considered to have reached stationary levels with an exponential settling behavior, the noise is therefore analyzed based on steady-state models. By using the first-order low-pass filter transfer function, the thermal noise power caused by switch RST is calculated as:

$$\overline{v_{n1,kTC}^2} = \int_0^\infty 4kTR_{on,RST}\frac{1}{1+(2\pi f R_{on,RST}C_L)^2} = \frac{kT}{C_L} \tag{5.40}$$

where $R_{on,RST}$ is the on-resistance of switch RST. Different from the voltage-domain sampling circuit, the charging phase follows by the switch off operation of RST. As a consequence, part of the noise charge on C_L is discharged in the charging phase with a non-stationary random process and thus the resulting noise power from RST is given as:

$$\begin{aligned}\overline{v_{n,kTC}^2} &= \sigma_{Y,kTC}^2(t)\Big|_{t=T_{ch}} = \frac{kT}{C_L} - \sigma_{n1,kTC}^2(t)\Big|_{t=T_{ch}} \\ &= \frac{kT}{C_L} - \frac{kT}{C_L}\int_0^t |h(\alpha)|^2 \, d\alpha = \frac{kT}{C_L}e^{-2T_{ch}/\tau}\end{aligned} \tag{5.41}$$

where the term $e^{-2T_{ch}/\tau}$ represents the amplitude degrading during the charging phase. The value of the kTC noise from the discharging phase is also numerically investigated, with results presented in Figure 5.16 and Figure 5.17.

5.3.5. Overall Input-Referred Noise

Consequently, the overall input-referred temporal noise power of a Gm-cell-based pixel can be calculated by:

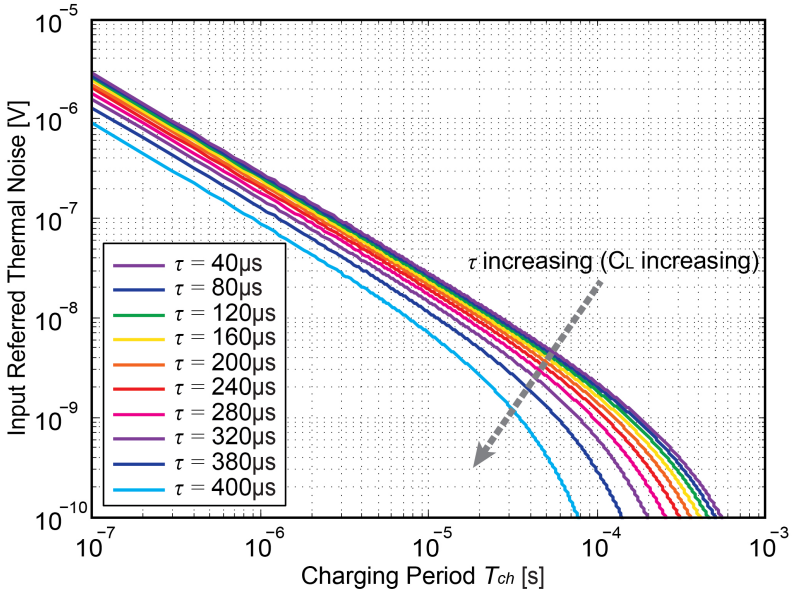


Figure 5.16: Input referred kTC noise a a function of charging period T_{ch} during discharging phase with τ and C_L increasing.

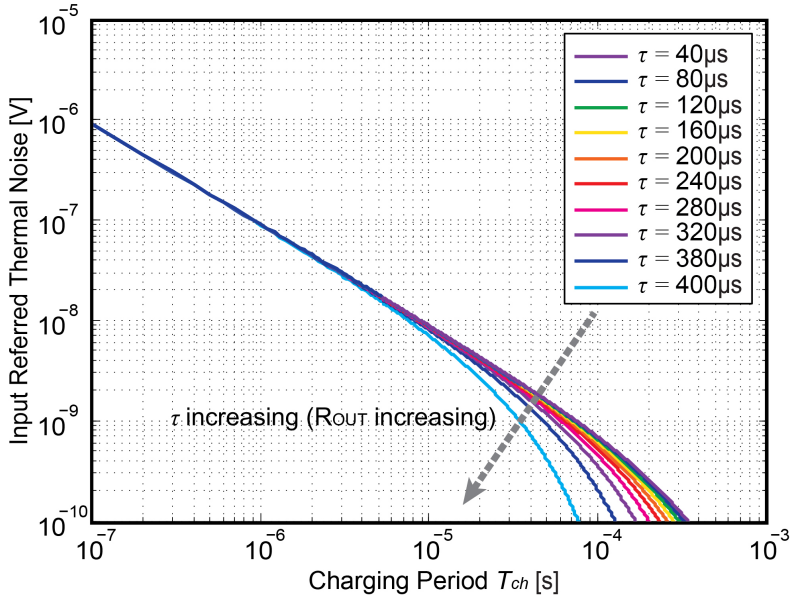


Figure 5.17: Input referred kTC noise a a function of charging period T_{ch} during discharging phase with τ and R_{OUT} increasing.

$$\begin{aligned}\overline{v_{n,in}^2} &= \frac{\sigma_{Y,th}^2(t)\Big|_{t=T_{ch}} + \sigma_{Y,1/f}^2(t)\Big|_{t=T_{ch}} + \sigma_{Y,kTC}^2(t)\Big|_{t=T_{ch}}}{|A_N|^2} \\ &= \frac{\sigma_{Y,th}^2(t)\Big|_{t=T_{ch}} + \sigma_{Y,1/f}^2(t)\Big|_{t=T_{ch}} + \sigma_{Y,kTC}^2(t)\Big|_{t=T_{ch}}}{[g_{m1}T_{ch}/(C_{S/H}+C_p)]^2}\end{aligned} \tag{5.42}$$

where $T_{ch} \ll \tau$. The combination of Equation (5.28), (5.39) and (5.41) provides an effective way to predict and calculate the temporal noise power of Gm-cell-based pixels in the time domain. Given the fact that the proposed circuit operates as a Gm–C integrator, T_{ch} should be settled with the range of $T_{ch} \ll \tau$. Applying the device parameters used for the design of the CIS chip as listed in 5.1, the noise components of the readout circuits and the resulting total noise are calculated in MATLAB, which is shown in Section 4 as a comparison of measurement result.

Table 5.1: Device parameter used for the noise simulation

Parameter	Value	Parameter	Value
g_{m1}	30 µS	A	3 µm (W) × 0.5 µm (L)
C_p	2pF	K	1×10^{-26} $F^2V^2m^{-2}$
$R_{o,Gm}$	20 MΩ	C_{ox}	4.3 fF/µ m^2
k	1.38×10^{-23}	f_c	500 kHz
T	300 K		

5.4. Circuit and Sensor Implementation

5.4.1. Pixel and Auxiliary Circuits Design

Figure 5.18 shows the implementation details and timing diagram of the proposed Gm-cell-based pixel in a CIS. It consists of a Gm-cell in each pixel and a CDS S/H capacitor bank at column-level. As the choice of the Gm-cell topology is dictated by the fill factor limitation, the proposed architecture adopts a single-ended cascode common-source topology as a pixel-level Gm-cell, where gm is set by the pMOS transistor M_{cs}. A

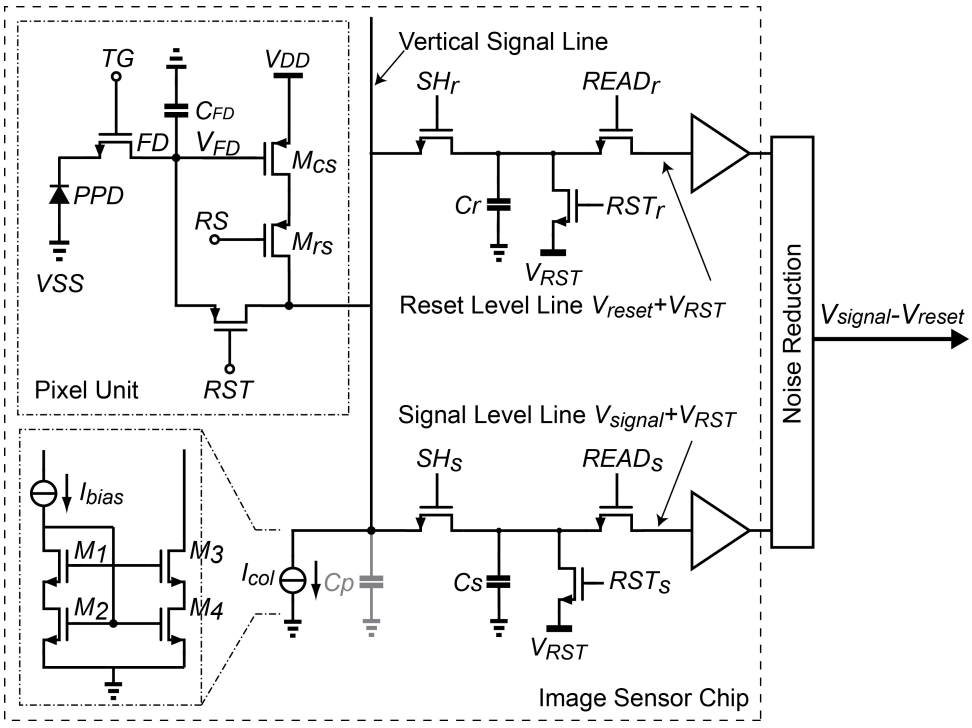


Figure 5.18: Schematic of the CIS with Gm-cell-based pixels

relatively large size of $M_{cs}(W/L = 3/0.5)$, needed for providing a sufficient g_m at the pixel-level, also helps to provide a sufficiently high self-biased reset voltage (around 2.3 V) at the FD node during the reset phase. A conceptual pixel layout is shown in Figure 5.19.

The $sinc$-type filter analysis above assumes that the output resistance of the trans-conductor is infinite for the case when the trans-conductor and the capacitor form an integrator. Although such an assumption is not possible, as long as the time constant of the integrator is prominently longer than T_{ch}, the finite output resistance will not affect the performance significantly. Therefore, the Gm-C integrator's time constant τ should be designed in the following way:

$$\tau = R_{o,Gm} \cdot (C_{S/H} + C_p) \gg T_{ch}/2\pi \tag{5.43}$$

where $R_{o,Gm}$ is the output impedance of the Gm-cell, $C_{S/H}$ is the capacitance of the S/H capacitors, and C_p is the parasitic capacitance of the column net. In order to boost $R_{o,Gm}$ as well as to mitigate the Miller effect

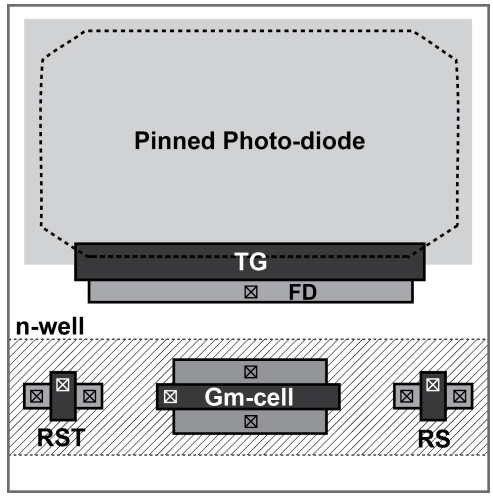


Figure 5.19: Conceptual pixel layout of the Gm-cell-based pixel.

[23], an adequate gate voltage V_{cas} is applied to the row select state of the pixel, allowing M_{rs} to operate as a cascode transistor, rather than to work in the triode region as a switch. Meanwhile, a high-impedance cascode current-source I_{col}, which is implemented by long channel transistors $M1$ to $M4$, is chosen as the load of the common-source stage to define the biasing current. What is more, the capacitor in each column is carefully sized to meet the time constant and gain requirement, while also ensure that the associated kT/C noise is not dominant. In this case, the values of C_r and C_s are both 2 pF, which in total occupy around 80% of the column area. Compared to other column- level architectures with similar readout gain, bandwidth and process [24], which paid the majority of the column area for additional amplifiers, the S/H capacitors used in this paper do not introduce a significant area overhead.

The uniformity of the CG across the pixel array is determined by the consistency of the T_{ch} pulsewidth, which in turn is affected by the rising/falling transition time of the clock pulse. To minimize the transition time, logic repeaters have been inserted to the clock distribution network. According to our simulations, the maximum clock delay from the clock input pad to the end of the repeater chain is less than 1 ns, while the variation of the T_{ch} pulse width is within 55 ps, which has negligible impact on the accuracy of the CG.

For the purpose of maximizing the output swing and improving the

linearity performance, the supply voltage of the prototype chip is set to 3.8 V. According to simulations, g_m of M_{cs} is around 30 μS, and $R_{o,Gm}$ is larger than 200 MΩ with a 4 μA bias in each pixel. With $C_r = C_s$ = 2 pF, T_{ch} can be digitally programmed between 100 ns to 4 μs, resulting in a tuneable pixel-level voltage gain ranging from ×1 to ×32.

5.4.2. Pixel Operating and Timing Diagram

The timing diagram of the proposed Gm-cell-based pixel in a CIS is shown in Figure 5.20. During the reset phase of each RS operating sequence, the Gm-cell is configured as a negative feedback scheme by switching on the reset transistor M_{rst}. As such, the Gm-cell is auto-zeroed, and the settled bias voltage of the common-source transistor M_{cs} as well as the reset level of the pixel is stored at the FD node capacitor.

After switching off M_{rst}, the Gm-cell is connected as an open-loop configuration, operating at the "memorized" bias condition stored on the parasitic capacitors of the FD node. With the help of switching on SH_r, a current I_r, which is proportional to the reset level V_r , is firstly produced by the Gm-cell and charges on the S/H capacitor C_r during a period T_{ch} from the initial state level V_{RST}. Then, at the end of the charge transfer from the PPD to the FD, the corresponding video signal current I_s is generated. Within the same period length T_{ch}, by switching on SH_s, this current is windowed charging into C_s from the same initial level V_{RST}. By performing these double charging processes, the resulting voltage level V_{reset} and V_{signal} are held on C_r and C_s, respectively, and are sequentially readout from the CIS chip via multiplexers and output buffers. An off-chip 16-b analog-to-digital converter (ADC) with an LSB of 30 μV has been implemented on the printed circuit board (PCB) to convert the analog output voltage levels into digital signal. The voltage subtraction of the reset level and the signal level (V_{signal}—V_{reset}) is then performed in the digital domain with the aid of a National Instruments vision acquisition system (NI-IMAQ & LabVIEW). In this way, we realize the CDS in digital domain and obtain the period-controlled amplified video signal V_{signal}–V_{reset} with the charge-domain CDS.

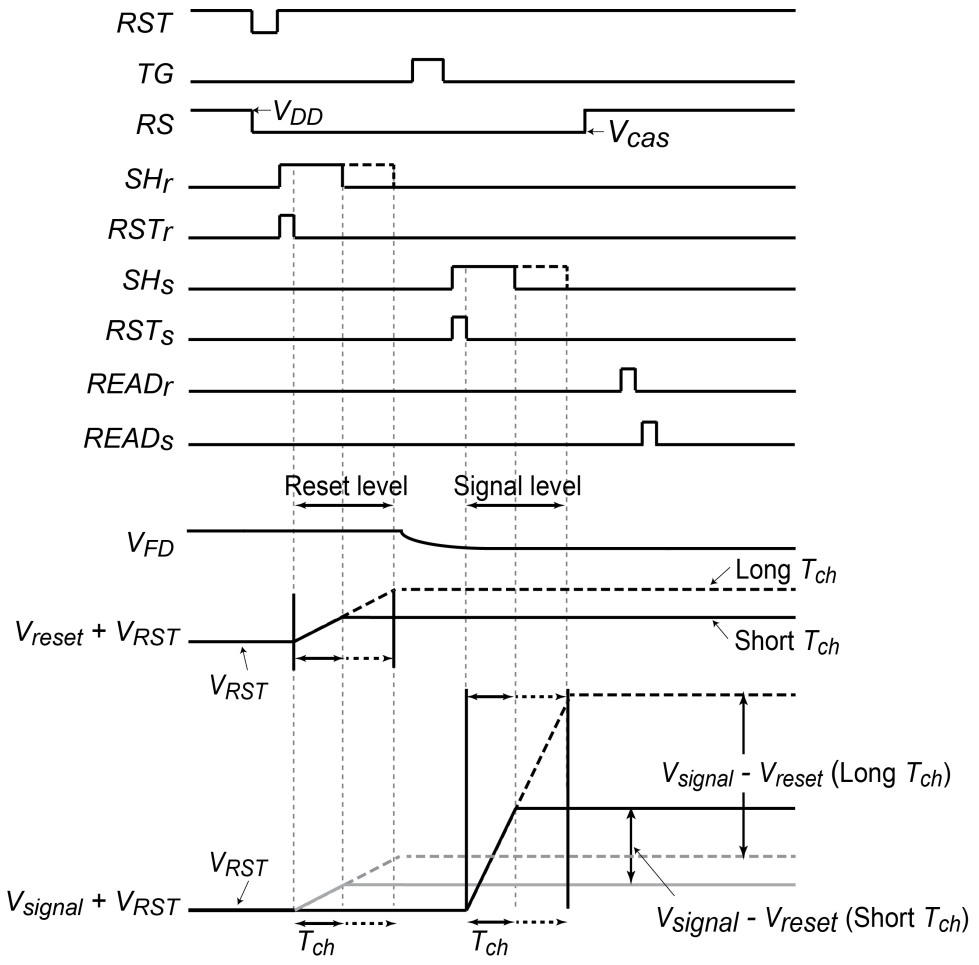


Figure 5.20: Timing diagram of the CIS with Gm-cell-based pixels

5.4.3. Silicon Realization

The test sensor with the proposed pixel architecture has been fabricated in a 0.18 μm 1P4M standard CIS process technology. Figure 5.21 presents a microphotograph of the prototype chip with the main functional blocks highlighted. The test pixels has been divided into six subgroups, each of which includes 20(H) × 32(V) pixels and features the same pixel pitch of 11 μm. For flexibility, the digital logic, which implements the charging clocks T_{ch} and other operating clocks are realized off-chip.

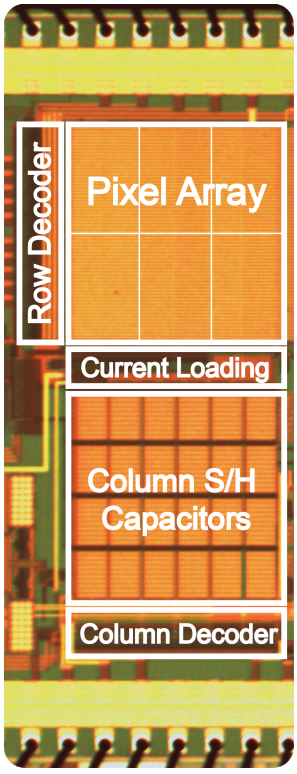


Figure 5.21: Die microphotograph

5.5. Experiment Results

5.5.1. Conversion Gain and Dynamic Range

The pixel-level conversion gain (CG_{tot}) associated with the period controlled function has been measured by using the photon transfer curve (PTC) measurement technique. Figure 5.23 shows the measured $CG_{tot} = CG_{FD} \times A_{pix}$ of the fabricated Gm-cell based pixel as a function of the charging period T_{ch}, where CG_{FD} is the CG at FD node. The plot shows a good linear behavior between CG_{tot} and T_{ch}, which agrees with the theoretical analysis Equation (5.7). To separately investigate the gain factor A_{pix} of the charge-sampling pixel, we also measure the CG_{FD} of an unity-gain pMOS SF-based reference 4T-pixel [24] as a comparison, in which the FD node is laid out with the same area as the proposed pixel. Note that the CG_{FD} of the SF-based pixel is measured as 55 μV/e$^-$, which indicates that the nominal value A_{pix} of the

charge sampling pixel is around ×30. The measurement results show that CG_{tot} can be programmable from 50 μV/e⁻ to 1.6 mV/e⁻ when a charging period from 100 ns to 4 μs applied. Four sample images captured by the test array at 0.5 lux at room temperature are shown in Figure 5.22 with T_{ch} programmable from 0.5 μs to 4 μs.

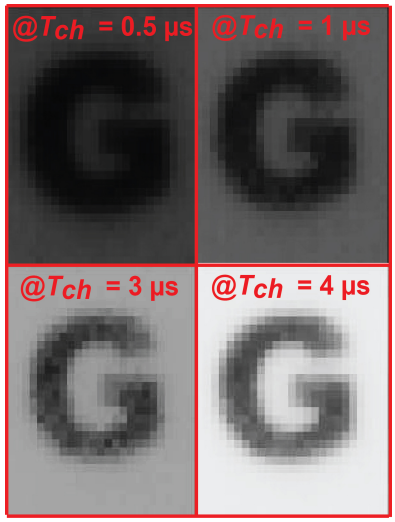


Figure 5.22: Sample images of the prototype sensor ($T_{ch} = 0.5 - 4\mu s$).

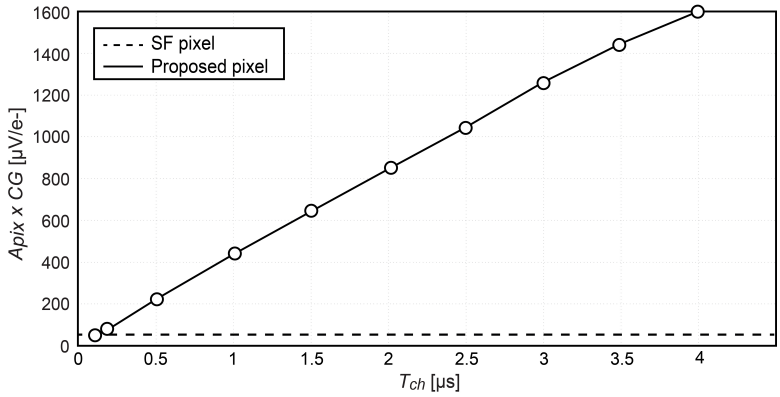


Figure 5.23: Measured CG ($CG_{FD} \times A_{pix}$) as a function of the charging period T_{ch}

Figure 5.24 shows the DR as a function of T_{ch}. The highest DR exceeds 68 dB at T_{ch} = 100 ns, and remains above 60 dB at T_{ch} = 4 μs. In addition to the single exposure DR, the proposed pixel provides a

calculated potential DR of 89 dB using typical multiple exposure methods thanks to the embedding of an adjustable-gain function.

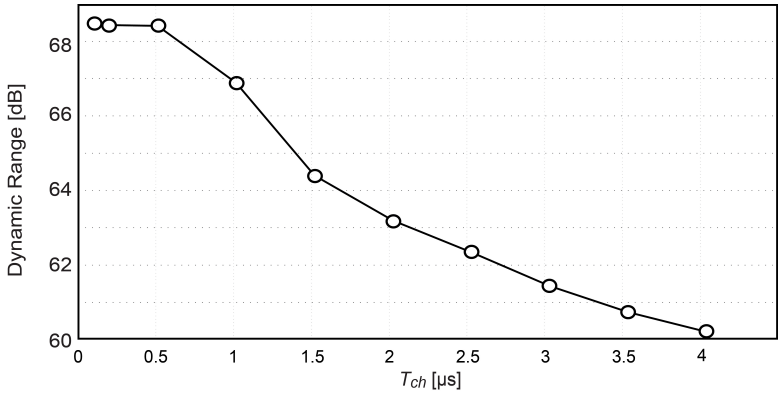


Figure 5.24: Measured DR as a function of the charging period T_{ch}.

5.5.2. Temporal Noise

The temporal noise characterization has been done in dark and implemented by keeping the transfer gate TG off during the measurement period. The rms temporal noise is first measured by a board-level 16-b ADC and then referred to the electron domain by dividing its corresponding measured CG. Figure 5.25 and Figure 5.26 shows the measured input-referred noise of the proposed pixel as a function of T_{ch}. The noise-reduction tendency initially is proportional to $1/T_{ch}$ and later becomes proportional to $1/\sqrt{T_{ch}}$. This result indicates that the Gm-cell-based pixel not only reduces the noise originating from the exceeding circuits connected at the back of the pixel as a result of the signal amplification of the charge-sampling technique, but also suppresses the thermal noise generated by the pixel level circuit as a result of noise-bandwidth reduction. At T_{ch} = 4 µs, the pixel achieves an input-referred noise of 0.51 e^-_{rms}. The inset of Figure 5.26 shows the corresponding noise histogram. This result is obtained from 320 pixels after performing 1000 readouts with a CDS period of 5 µs and a row read-out time of 10 µs. In addition, when referred the noise back to the input of the signal chain in the voltage domain by dividing its corresponding gain factor A_{pix}, the lowest measured input-referred noise level is found around 27 µV, which is shown and compared with other

state-of-the-art low-noise CIS in Figure 5.28. Figure 5.28 presents that an improvement in figure-of-merit regarding the read-out noise reduction was successfully obtained by using the proposed Gm-cell-based pixel and charge-domain CDS technique.

For verification of the time-domain noise analysis model, Figure 5.27 shows the measured input-referred noise with a comparison to the simulation results in voltage domain. In the calculation results described above, noise due to the clock jitter effect and sample and hold process, as well as the noise generated from the board-level succeeding readout circuits are ignored. As a result, there is a noise value deviation between the calculation and measurement results. Moreover, because of the trans-conductance is V_{FD}-dependent and the Gm-cell is open loop, the g_m variation degrades the pixel output linearity, leading to a noise reduction factor deviation between two results. As Figure 5.27 indicates, the noise reduction tendency obtained from the calculation model shows a steeper slope than the measurement results. However, the measured and calculated results show a reasonable agreement on the noise reduction tendency, demonstrating the validity of the noise calculation by using the time-domain noise analysis model.

5.5.3. Linearity and Fixed Pattern Noise

Figure 5.29 shows the measured pixel output signal as a function of the exposure time, as well the corresponding linearity error. The peak linearity error of the proposed pixel architecture is measured as 2.5 % with an output voltage range ranging from 0 to 0.5 V. Because the trans-conductance is V_{FD}-dependence and the Gm-cell is open loop, the g_m variation across the whole array is relatively large compared with an SF-based pixel array. This degrades the pixel output linearity, and decreases the effectiveness of CDS. The latter results in a worse fixed pattern noise (FPN), which is measured as 3.8 % at T_{ch} = 4 μs. For this sake, digital calibration has to be done after the acquisition of the raw image from the sensor to improve the linearity and FPN. Besides the common approach of performing digital image processing, a trans-conductance linearization technique, such as source-degeneration [23], can also be applied to each Gm-cell to compensate for the nonlinearity, with the cost of a slightly elevated input referred noise.

To further improve the linearity and provide enough robustness against

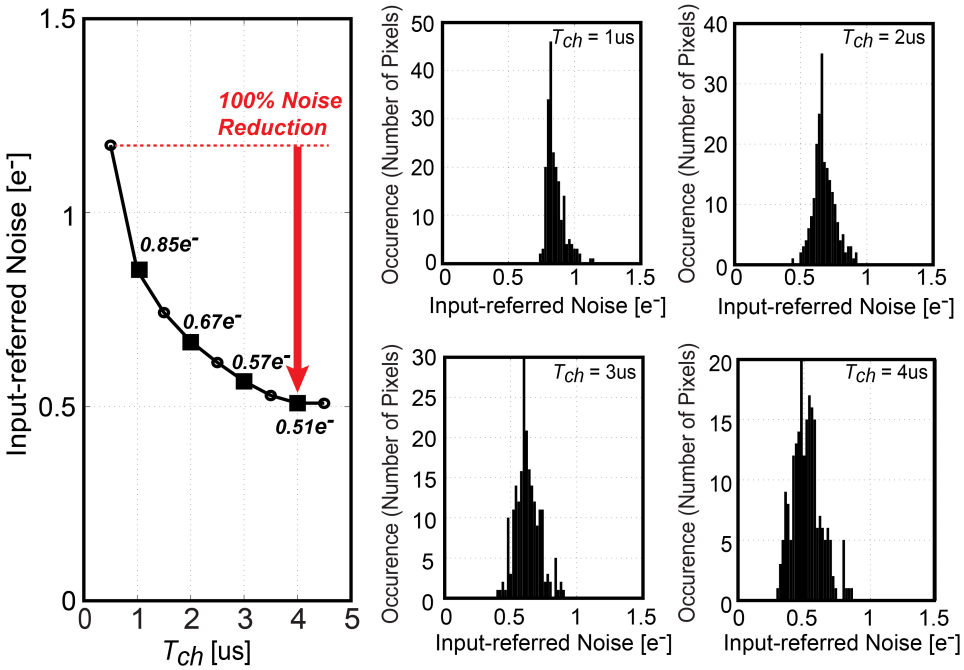


Figure 5.25: Input-referred noise in voltage domain as a function of T_{ch} for measured and simulated results.

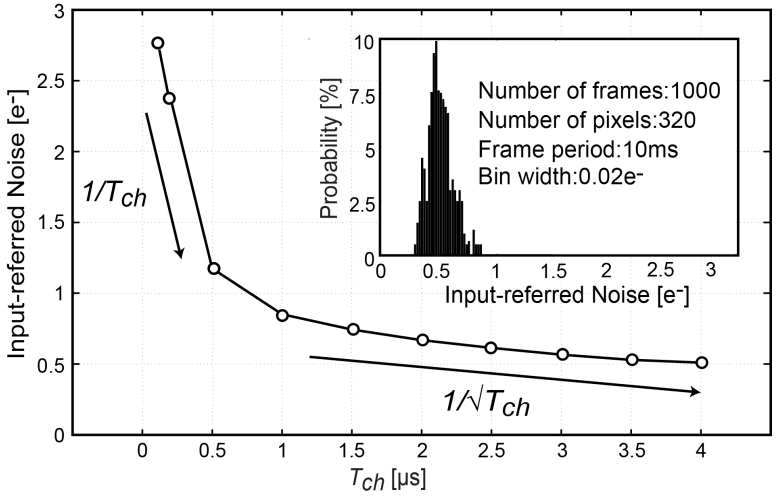


Figure 5.26: Measured input-referred noise as a function of the charging period T_{ch} and noise histogram at T_{ch} = 4 µs.

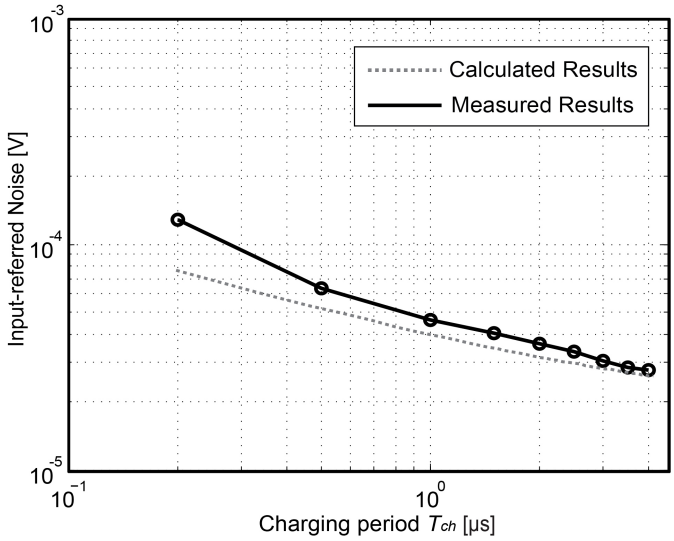


Figure 5.27: Input-referred noise in voltage domain as a function of T_{ch} for measured and simulated results.

variation, several circuit techniques based on continuous-time filters have been proposed in prior works. In [28], digital calibration of the feedback DAC can be used to match the non-linear Gm cell transfer function, thus to improve the linearity of the Gm-cell. Another approach [29] is to place the Gm-cell within the $\Delta\Sigma$-loop by using the input of the Gm-cell and feedback DAC. An additional impedance boosting circuit to achieve high impedance for CDAC [30] and feedback-assisted Gm linearization technique [31] have also been described to provide more solutions.

5.5.4. Results Summary

Table 5.2 and Table 5.3 summarize the performance of the proposed Gm-cell-based pixel in comparison with prior work on low noise CIS. Compared to pixel-level open-loop amplification [1], this work has the same pixel pitch and process node, while achieving 1.7× lower input-referred noise. Although the pixel pitch is large due to an extra n-well introduced by the pMOS transistors, it can be potentially reduced (e.g., $\sim$ 7μm pixel pitch with a 50% fill factor) with the help of an optimized layout approach [4] and a smaller size pixel transistor. By utilizing the charge-sampling approach, the low noise performance of our prototype is

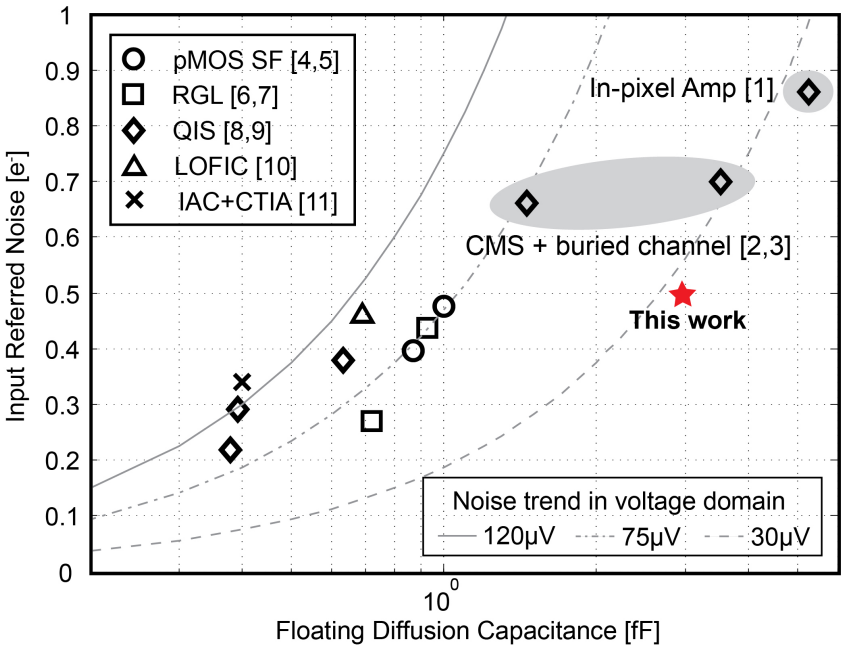


Figure 5.28: Comparison of input-referred noise in the electron domain vs. FD capacitance, and noise trend in the voltage domain with reported image sensors [25]. The values are based on the best guess with the known values of CG_{FD} in reported publications.

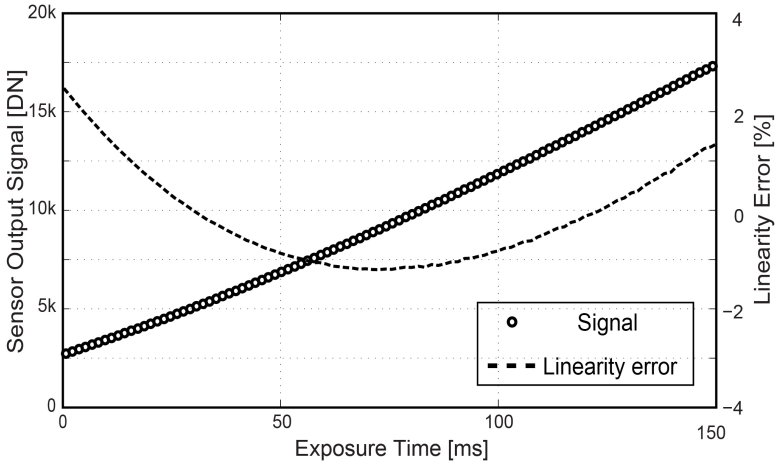


Figure 5.29: Measured pixel output as a function of the exposure time.

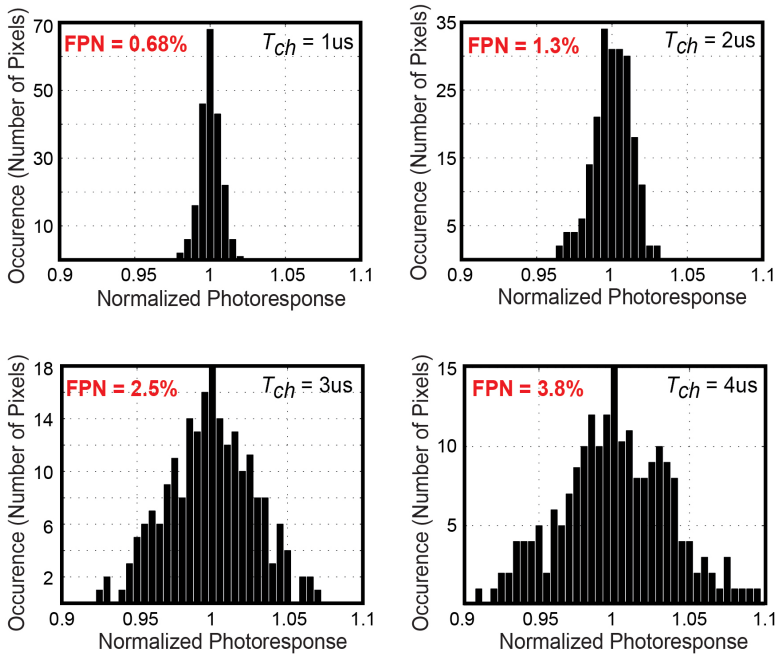


Figure 5.30: FPN as a function of T_{ch} for measured results.

achieved with a 10 µs row read-out time. It is worth noting that this row read-out speed would not significantly degrade even if the pixel array is extended to a larger size, thanks to the adoption of the charge sampling approach.

5.6. Conclusions

In this chapter, a prototype CIS with Gm-cell-based pixels has been presented. The proposed structure realizes tunable CG with period-controlled method. This enables the CG and the noise-equivalent number of electrons to be programmable according to the application without any change in hardware. In contrast to conventional CIS pixel architectures, a Gm-cell-based pixel operates in a large-signal manner, and its noise behaves as a function of sampling period. To allow a precise and predictive noise performance optimization for such type of pixels and their readout circuits, a non-stationary thermal and flicker noise analysis model based on time-domain approach is presented and discussed in this chapter. A proof-of-concept test chip has been built. The obtained noise

Table 5.2: Performance Summary

Parameter	Value
Process	180nm CIS 1P4M
Pixel pitch	11 µm
Number of pixels	60 (H) × 64 (V)
Fill factor	50%
Readout noise	0.5 e^-_{rms}
CG	90 µV/e^- ∼ 1600 µV/e^-
Row time	10 µs
Non-linearity	2.5%
FPN	3.8%

Table 5.3: Comparison to Previous Works

	This work	**ISSCC'11 [1]**	**ISSCC'12 [2]**	**JSSC'16 [4]**	**EDL'15 [8]**	**VLSI'15 [10]**
Process	180nm CIS	180nm CIS	180nm CIS	180nm CIS	65nm CIS	180nm CIS
Pixel pitch [µm]	11	11	10	6.5	1.4	5.5
Fill factor [%]	50	50	33	40	—	—
Readout noise [e^-_{rms}]	0.5	0.86	0.7	0.48	0.29	0.5
CG [µV/e^-]	90 ∼ 1600	300	45	160	413	240
Row readout time [µs]	10	15	1600	25	—	143

performance is comparable to the state-of-the-art low-noise CIS, while this work employs a simpler circuit, without suffering from DR limitations, and is fabricated in a low cost, standard CIS process.

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6

Conclusions and Future Work

This thesis focuses on temporal noise reduction for CMOS image sensors. In this final chapter, the general conclusions of this thesis are summarized. A vision for future possible research directions is discussed.

6.1. Conclusions

In this section, the general conclusions of four designs described in this thesis are summarized.

Temporal noise reduction using pMOS unity-gain source follower and optimized column amplifier (Chapter 2)

- In modern CMOS processes, the pMOS transistors are naturally buried-channel devices, featuring a lower oxide trap density than the nMOS transistors. Therefore, an in-pixel pMOS-based source follower (SF) helps in achieving a lower noise floor. However, this approach suffers from a severe voltage gain degradation due to the higher body effect trans-conductance of pMOS transistors.

- An effective solution to eliminate the impact of this body effect is to employ a separated n-well for the SF transistor instead of sharing the common n-well with other in-pixel transistors. Due to this separation, the contribution of the body effect trans-conductance to the overall output trans-conductance of the SF could be ignored. As such, the voltage gain of a pMOS SF without body effect approaches unity.

- A conventional single-ended common-source cascode amplifier suffers from poor immunity to circuit non-idealities and environmental interference. To address this problem, a column-level low-dropout (LDO) regulator with local ground rail for each column amplifier is proposed to reject interference from the common ground.

- The proposed SF structure improves the conversion gain (CG) after the in-pixel SF by 42% compared to the reference pixel. By adopting the proposed pixel structure and amplifier configuration, the prototype CIS features an input-referred noise of 1.1 e^-_{rms} with a column-level ×16 analog gain.

Temporal noise analysis and measurement for n-type and p-type pixels with CMS technique (Chapter 3)

- A hole-based p-type pixel shows several advantages over its n-type counterparts. However, one of the weak points for the p-type pixel is a relatively higher thermal noise due to its lower trans-conductance. Hence, the doubled thermal noise power after correlated double sampling (CDS), together with the residual 1/f noise power, is considered as one of the most significant factors that limits the p-type pixels noise performance.

- The effectiveness of the correlated multiple sampling (CMS) noise canceller can be characterized as a pass-band narrowing operation due to the differentiation and averaging procedures in the CMS configuration. Therefore, this technique has been considered as an effective approach to not only reduce $1/f$ noise, but also to decrease thermal noise.

- The post-CMS noise behavior for both n-type and p-type pixels are modeled by calculating their output noise power spectrum (PSD) density as well as the noise transfer function. The calculation results show that when the sampling number M increases, the high frequency region noise is lowered while the low frequency region noise becomes slightly higher. In total, the final noise reduction factor is 31% for the n-type pixel and 50% for the p-type.

- The measurement result shows a noise reduction tendency as the sampling number of CMS increases. The n-type pixel shows a saturation of the noise improvement tendency from 8-times CMS, while the p-type pixel elevates this saturation level up to 64-times due to a lower $1/f$ noise coefficient. Comparing the input-referred noise with digital-only CDS, the CMS noise reduction factor is around 24% for n-type pixels and 45% for p-type pixels with 64-times CMS applied. With M = 16 and 64, the residual $1/f$ noise in nMOS SF constraints further a noise reduction and the noise level of the p-type pixel becomes lower than that of the n-type one. With M = 64, the n-type pixel features an input-referred noise of 1.1 e^-_{rms} and the p-type pixel shows a lower noise level at 0.88 h^+_{rms}.

Temporal noise reduction with programmable-gain AFE and digital CMS technique (Chapter 4)

- In pursuit of achieving a low noise performance, dedicated low-noise signal process solutions with effective CMS feature for CIS is called for, which are supposed to be realized by optimizing the trade-off between noise, speed and power consumption of the entire readout circuit, as well as combining with a highly-compact layout.

- In respect of the noise performance, a thinner oxide layer MOSFET typically shows a lower 1/f noise than the thicker one. Therefore, using thin oxide devices for analog signal processing circuit would offer a fundamental advantage for noise reduction in a CIS.

- An OTA based on a gain-boosted cascoded inverter is employed in this analog-front end (AFE) design with the concern of maximizing the current-efficiency and minimizing the noise. To address the issue of poor immunity against process, supply voltage, and temperature (PVT) variations, a dynamic biasing scheme has been used to assist the DC biasing to the main core inverter. This scheme also inherently includes an auto-zeroing process.

- A column-wise reference-adaptive incremental $\Delta\Sigma$ ADC is proposed to further shorten the conversion time. The adaptive reference-control method splits the $\Delta\Sigma$ data conversion into the coarse pre-determined phase and the fine conversion phase. In the coarse phase, a comparator is first operated to determine the DAC reference that will be later used for fine conversion. In the following fine phase, the pre-determined corresponding reference is adopted by the $\Delta\Sigma$ ADC to complete the fine conversion.

- The proposed column-parallel read-out circuit suppresses the readout noise with a gain stage and a band-pass (CDS & CMS) filtering characteristic, achieving a 107 μV input-referred noise, which is equivalent to 0.55 e $^{-}_{rms}$. By optimizing the trade-off between noise, power consumption and frame-rate, the figure-of-merit (FoM) of 1.76 e-·nJ is comparable to the state-of-the-art low-noise CIS.

Temporal noise reduction using Gm-cell-based pixel and period-controlled variable conversion gain (Chapter 5)

- In order to address the trade-off between the low input-referred noise and high dynamic range, a Gm-cell-based pixel together with a charge-domain correlated-double sampling (CDS) technique has been proposed to provide a way to efficiently embed a tunable conversion gain along the read-out path.

- Periodical filtering model of the Gm-cell-based pixel shows that a programmable gain and a programmable bandwidth can be obtained by tuning the time window (T_{ch}) without using any other changes at circuit-level implementation. The increasing time window not only helps in boosting the DC gain, but also reducing the bandwidth of the charge-domain sampler.

- Simulation proves that the charge-domain CDS provides a greater extent attenuation on high-frequency noise components with the aid of the notch attenuation, than the first-order low-pass filtering of the voltage-sampling circuits.

- An analysis model for both thermal noise and flicker noise in Gm-cell-based pixels has been developed by employing the time-domain linear analysis approach and the non-stationary noise analysis theory, which help to quantitatively evaluate the temporal noise characteristic of Gm-cell-based pixels.

- Measurement result shows a good linear behavior between conversion gain and T_{ch}, which agrees with the theoretical analysis. From the noise measurement data, it can be observed that the noise-reduction tendency initially is proportional to $1/T_{ch}$ and later becomes proportional to $1/\sqrt{T_{ch}}$. This result indicates that the Gm-cell-based pixel not only reduces the noise originating from the exceeding circuits connected at the back of the pixel, but also suppresses the thermal noise generated by the pixel level circuit. At T_{ch} = 4 μs, the pixel achieves an input-referred noise of 0.51 e^-_{rms}.

6.2. Future Work

To further obtain a lower noise level and better performance for photon-starved imaging, especially for single-photon imaging, a vision for future possible research topics is discussed in this section.

Further optimization of the hole-based p-type pixel

As the prototype described in Chapter 3 focuses solely on noise behavior, it is a necessity to address further investigation and optimization regarding the overall image quality for a p-type pixel.

In this chapter, Figure 3.12 shows that the CG of the p-type pixel is obviously smaller than the CG of the n-type pixel (110 μV/h$^+$ vs. 153 μV/e$^-$). However, the floating diffusion (FD) node active area showing in the pixel layout for both type of pixels have exactly the same dimensions. To further reduce the input-referred noise, following the approach proposed in [1], it is worthwhile to investigate which components of the FD capacitance contribute more parasitic capacitance than its counterpart.

Besides, low dark current is also essential to the dark image quality, especially for the scenario of single-photon imaging. Therefore, the dark current performance for the prototype p-type pixel with different temperatures should be characterized and investigated.

Further optimization of the digital CMS technique

As discussed in Chapter 4, to ensure that the AFE output V_{in} always is in the middle of the input range of the fine $\Delta\Sigma$ modulator, we reserve a redundancy for the reference voltage of the $\Delta\Sigma$ ADC by extending the fine conversion range equal to 1.2 LSB instead of 1 LSB of the coarse conversion. However, if the ADC operates in this way, the conversion should involve an extra step to compare the V_{in} to $(k + 0.1) \cdot V_{LSB}$ at the end of the coarse conversion. This additional comparison step can be implemented on-chip by adding an extra look-ahead circuit.

What's more, as the second stage is a fine ADC with a reduced conversion range, the non-idealities of the digital-to-analog converter (DAC) introduce extra errors that worsen the overall accuracy and linearity. In order to mitigate this, a dynamic reference adjustment approach associated with residue computation is called for [2].

Further optimization of the Gm-cell-based pixel

As described in Chapter 5, the proposed Gm-cell-based pixel enables a tunable conversion gain in a period-controlled manner. However, this is at the expense of a higher fixed pattern noise (FPN), and a limited linear voltage swing.

To correct the Gm-cell open-loop-gain induced gain-FPN, a gain map or a look-up table is needed for gain correction during the background calibration phase, whose results are stored in digital memories. To perform the calibration across the overall pixel array, a global calibration solution is called for. This solution addresses the challenge of measuring and recording the gain error on a pixel-to-pixel basis, with the consideration of minimizing the associated area overhead.

To extend the pixel output swing, one possible approach is to increase the loading capacitance for the Gm-cell-based pixel. When the capacitance increases, the gain of the pixel decreases. Thus, a larger capacitance could attenuate the voltage swing and widen the linear region at the output of the pixel. In addition, instead of using a fixed stand-alone capacitor, a sample-and-hold switched-capacitor array can be used to add the flexibility of switching the gain step.

To further reduce the noise, one effective solution is to further decrease the floating diffusion (FD) node capacitance. From the measured CG data, it can be derived that the FD capacitance determined CG of the prototype pixel is just 50 μV/e$^-$. Hence, there is a large potential to enhance the CG by shrinking the active area of FD and process optimization.

Apart from that, circuit-level optimizations and novel techniques are called for to further minimize the noise originating from both the Gm-cell-based pixel and the readout circuits. To serve this purpose, an evolved Gm-cell-based pixel prototype has been designed and implemented [4]. This newly developed prototype incorporates several design improvement including optimized pixel-level Gm-cell structure, low-noise current source, finite impulse response (FIR) and infinite impulse response (IIR) filter, etc.. The prototype noise performance has been characterized with photon-counting histogram valley-to-peak modulation (PCH-VPM) method [5]. The PCH result of the best pixel is depicted in Figure 6.1. The histogram clearly shows a quantization effect and indicates a 0.31 e^-_{rms} noise level of the pixel.

Furthermore, the above mentioned solutions for Gm-cell-based pixel can

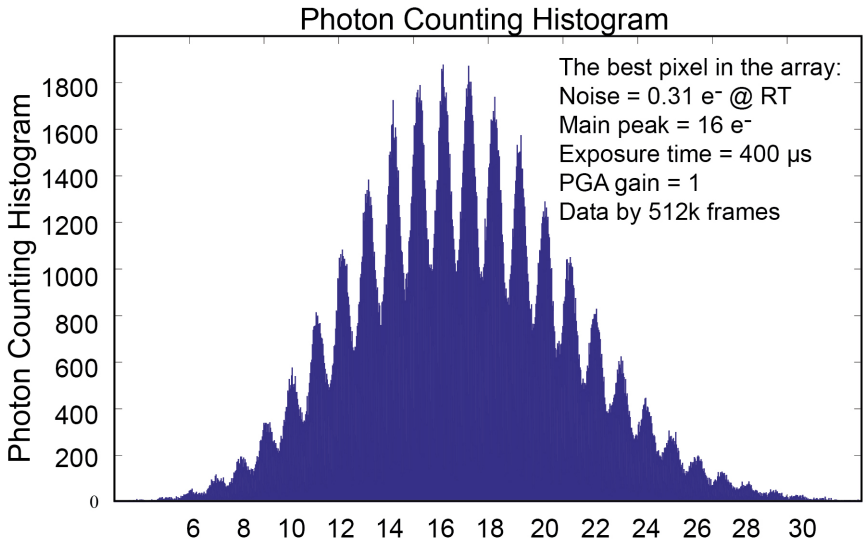


Figure 6.1: Photon counting histogram of the best pixel

be addressed even with recent and future advances in CIS manufacturing and integration process. For example, the FD node capacitance shrinking can be benefit from a more advanced process node and a FD capacitance reduction process. Furthermore, as the 3-D CIS stacking process is getting mature [3], the second ASIC wafer can be utilized to address the required space for extra gain-FPN calibration circuits, digital memories and additional loading capacitances.

Acknowledgement

Figure 6.1 is taken from the newly developed prototype dark noise measurement conducted by Liqiang Han. The author would like to thank him for his valuable contribution to this chapter.

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Summary

In pursuit of achieving the noise condition of single-photon imaging, system-level and circuit-level innovations and optimizations for CMOS image sensor (CIS) noise reduction are called for. Stimulated by this motivation, this thesis focuses on reducing the temporal noise generated in the pixels and the readout electronics.

In Chapter 2, a CIS with in-pixel nearly unity-gain pMOS transistor based source followers and optimized column-parallel amplifiers has been presented. By eliminating the body effect of the pMOS transistor based source follower, the voltage gain for the pixel level readout circuitry approaches unity. To realize a better performance in terms of noise, a single-ended common source cascode amplifier with ground rail regulation has been adopted to enhance the power-supply rejection ratio of the column-parallel analog front-end circuitry. The proposed techniques have been implemented in a prototype and fabricated in a standard 0.18 μm CIS process. Electrical characterization results show that the proposed pixel improves the conversion gain after the in-pixel source follower by 42 % compared to that of the conventional structure. The prototype sensor with proposed readout architecture reaches a 1.1 e^-_{rms} input-referred temporal noise with a column-level $\times$16 gain.

In Chapter 3, a noise analysis and noise measurements of n-type and p-type pixels with correlated multiple sampling (CMS) technique have been described. The output noise power spectral density of both pixel types with different CMS noise reduction factors have been simulated and calculated in the spectral domain. For validation, two groups of test pixels have been fabricated with a n-type and p-type 65/90 nm CIS technology. The calculated and the measured noise results with CMS show a good agreement. Measurement results also show that the n-type and p-type pixels reach a 1.1 e^-_{rms} and 0.88 h^+_{rms} input-referred temporal noise respectively with a board-level 64-times digital CMS and $\times$6 analog gain.

In Chapter 4, an inverter-based programmable-gain amplifier and a digital CMS reference-adaptive ADC has been presented and verified with a VGA format prototype fabricated in a 65/90 nm CIS process. The

proposed column-parallel read-out circuits suppress the readout noise with a gain stage and a band-pass filtering characteristic, achieving a 98 μV input-referred noise, which is equivalent to 0.55 e^-_{rms}. In contrast to conventional digital CMS architectures, the proposed ADC architecture operates with a reference-adaptive mechanism, which shortens the conversion time and speeds up the frame-rate. By optimizing the trade-off between noise, power consumption and frame-rate, the figure-of-merit (FoM) of 1.88 e^-·nJ is comparable to the state-of-the-art low-noise CIS.

In Chapter 5, a deep sub-electron temporal noise CIS with a Gm-cell based pixel and a correlated-double charge-domain sampling technique has been described. With the proposed technique, the CIS, which is implemented in a standard 0.18 μm CIS process, features pixel-level amplification and achieves an input-referred noise of 0.5 e^-_{rms} with a correlated double sampling period of 5 μs and a row read-out time of 10 μs. The proposed structure also realizes a variable conversion gain with a period-controlled method. This enables the read-out path conversion gain and the noise-equivalent number of electrons to be programmable according to the application without any change in hardware. The experiments show that the measured CG can be tuned from 50 μV/e^- to 1.6 mV/e^- with a charging period from 100 ns to 4 μs. The measured characteristics of the prototype CIS are in a good agreement with calculation results, demonstrating the effectiveness of the proposed techniques.

Samenvatting

Om het noodzakelijke ruisniveau voor single-foton beeldvorming te behalen zijn er voor de ruisvermindering van CMOS beeldsensoren (CIS) vernieuwingen en optimalisaties op systeem- en schakelingsniveau nodig. Met deze drijfveer focust dit proefschrift erop om de temporele ruis gegenereerd in de pixel en uitleeselectronica te verminderen.

In hoofdstuk 2 wordt er een CIS met in-pixel bijna eenheidsversterking pMOS transistor gebaseerde bronvolger en geoptimaliseerde kolom-parallelle versterkers gepresenteerd. Door het elimineren van het body effect van de pMOS transistor gebaseerde bronvolger benadert de spanningsversterking voor het pixel niveau uitleesschakeling eenheid. Om een betere prestatie op gebied van ruis te bekomen wordt er gebruik gemaakt van een enkelzijdige schakeling met gemeenschappelijke bron cascadeversterker met ground rail regulation om de power-supply rejection ratio van de kolom-parallelle analoge front-end schakeling te verbeteren. De voorgestelde technieken zijn geïmplementeerd in een prototype en gefabriceerd in een standaard 0.18 µm CIS proces. Elektrische karakterisatie resultaten tonen dat de voorgestelde pixel de conversieversterking na de in-pixel bronvolger verbetert met 42 % in vergelijking met een conventionele structuur. Het prototype met de voorgestelde uitleesarchitectuur haalt 1.1 e^-_{rms} ingang gerefereerde temporele ruis met een kolomniveau x16 versterking.

In hoofdstuk 3 zijn een ruisanalyse en ruismetingen van een n-type en p-type pixel met gecorreleerde meerdere bemonstering (CMS) beschreven. De uitgaande spectrale ruisvermogendichtheid van beide pixel types met verschillende CMS ruis verminderingsfactoren zijn gesimuleerd en berekend in het spectrale domein. Voor validatie zijn twee groepen van test pixels gefabriceerd met een n-type en p-type 65/90 nm CIS technologie. De berekende en gemeten ruisresultaten met CMS tonen een goede overeenkomst. De meetresultaten tonen ook dat de n-type en p-type pixels respectievelijk 1.1 e^-_{rms} en 0.88 h^+_{rms} ingang gerefereerde temporele ruis halen met een board-level 64-voudige digitale CMS en $\times 6$ analoge versterking.

In hoofdstuk 4 wordt een inverter gebaseerde programmeerbare versterker en een digitale CMS referentie-adaptieve ADC gepresenteerd en geverifieerd met een VGA formaat prototype gefabriceerd in een 65/90 nm CIS proces. De voorgestelde kolom-parallelle uitleesschakelingen onderdrukken de uitleesruis met een trapversterking en een banddoorlaat filter karakteristiek, en behaalt 98 μV ingang gerefereerde ruis, wat overeenkomt met 0.55 e^-_{rms}. In contrast met conventionele digitale CMS architectuur werkt de voorgestelde ADC architectuur met een referentie-adaptief mechanisme, wat de omzettingstijd vermindert en de beeldfrequentie verhoogt. Door het compromis tussen ruis, vermogenverbruik en beeldfrequentie te optimaliseren is de maat van verdienste (FoM) van 1.88 e^-·nJ vergelijkbaar met de meest recente lage ruis CIS.

In hoofdstuk 5 is een diepe sub-elektron temporele ruis CIS met een Gm-cel gebaseerde pixel en een gecorreleerde dubbele ladingsdomein bemonsteringstechniek beschreven. Met de voorgestelde techniek haalt de CIS, die geïmplementeerd is in een standaard 0.18 μm CIS proces en pixelniveau versterking heeft een ingang gerefereerde ruis van 0.5 e^-_{rms} met een gecorreleerde dubbele bemonsteringsperiode van 5 μs en een rij uitleestijd van 10 μs. De voorgestelde structuur realiseert ook een variabele conversieversterking met een periode gecontroleerde methode. Dit staat toe de uitleespadconversieversterking en de ruis equivalente hoeveelheid elektronen te programmeren naargelang de toepassing zonder enige noodzakelijke verandering in hardware. De experimenten tonen dat de gemeten conversieversterking kan aangepast worden van 50 μV/e^- tot 1.6 mV/e^- met een laadperiode van 100 ns tot 4 μs. De gemeten karakteristieken van het prototype CIS komen goed overeen met de berekende resultaten, en tonen de effectiviteit van de voorgestelde technieken.

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List of Publications

Journal Articles

- **Xiaoliang Ge** and Albert J. P. Theuwissen, "Temporal Noise Analysis of Charge-Domain Sampling Readout Circuits for CMOS Image Sensors," Sensors, vol. 18, no. 3, p. 707, Feb. 2018.

- **Xiaoliang Ge** and Albert J. P. Theuwissen, "A 0.5 e^-_{rms} Temporal Noise CMOS Image Sensor With Gm-Cell-Based Pixel and Period-Controlled Variable Conversion Gain," IEEE Transactions on Electron Devices, vol. 64, no. 12, pp. 5019-5026, Dec. 2017, doi: 10.1109/TED.2017.2759787.

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- **Xiaoliang Ge** and Albert J. P. Theuwissen, "A 0.5 e- Temporal Noise CMOS Image Sensor with Charge-Domain CDS and Period-Controlled Variable Conversion Gain," 2017 International Image Sensor Workshop, 30 May - 2 June, 2017, Hiroshima, Japan.

- **Xiaoliang Ge** and Albert J. P. Theuwissen, "A CMOS image sensor with nearly unity-gain source follower and optimized column amplifier," 2016 IEEE SENSORS, 30 Oct.-3 Nov., 2016, Orlando, USA, pp. 1-3, doi: 10.1109/ICSENS.2016.7808589.

- **Xiaoliang Ge**, Bastien Mamdy and Albert J. P. Theuwissen, "A comparative noise analysis and measurement for n-type and p-type pixels with CMS technique," 2016 Electronic Imaging, 14-18 Feb., 2016, San Francisco, USA.

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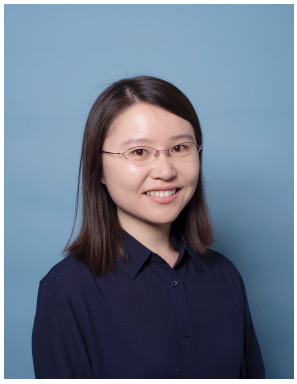
- Shuang Xie, Accel Abarca, Jules Markenhof, **Xiaoliang Ge** and Albert J. P. Theuwissen, ”Analysis and calibration of process variations for an array of temperature sensors,” 2017 IEEE SENSORS, 30 Oct.-1 Nov., 2017, Glasgow, United Kingdom, pp. 1-3, doi: 10.1109/ICSENS.2017.8233959.

- Yang Xu, **Xiaoliang Ge** and Albert J. P. Theuwissen, ”Investigating Transfer Gate Potential Barrier by Fee-Forward Effect Measurement,” 2015 International Image Sensor Workshop, 8-11 June, 2015, Vaals, the Netherlands.

Workshop Contributions

- **Xiaoliang Ge** and Albert J. P. Theuwissen, ”A 0.5 e- Temporal Noise CMOS Image Sensor with Charge-Domain CDS and Period-Controlled Variable Conversion Gain,” 2017 ISSCC Student Research Preview Session.

About the Author



Xiaoliang Ge was born in Beijing, China, on March 19th, 1988. She received her B.Sc degree from South China University of Technology, Guangzhou, China, in 2010, and her M.Sc degree from Delft University of Technology, Delft, the Netherlands, in 2012, both in microelectronics. Since September 2013, she has been working toward her Ph.D degree at the Electronic Instrumentation Laboratory, Delft University of Technology. Her Ph.D research mainly concentrated on reducing dark temporal noise for CMOS image sensor both at circuit level and system level.

Since March 2018, she has been working as a pixel designer at ams AG in Antwerp, Belgium. Her main research interest includes the design and optimization of CMOS image sensor pixels and their process development.